

μA26LS32 **Quad Differential** **Line Receiver**

Linear Division Interface Products

Description

The μA26LS32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The device features an input sensitivity of 200 mV over the input range of ± 7.0 V. The μA26LS32 provides an enable function common to all four receivers and three-state outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The μA26LS32 offers optimum performance when used with the μA26LS31 Quad Differential Line Driver.

- **Input Voltage Range Of ± 7.0 V (Differential Or Common Mode) ± 0.2 V Sensitivity Over The Input Voltage Range**
- **Meets All The Requirements Of EIA Standards RS-422 And RS-423**
- **Input Impedance (15K Typical)**
- **30 mV Input Hysteresis**
- **Operation From Single +5.0 V Supply**
- **Fail-Safe Input/Output Relationship. Output Always High When Inputs Are Open.**
- **Three-State Drive, With Choice Of Complementary Output Enables, For Receiving Directly Onto A Data Bus.**
- **Propagation Delay 17 ns Typical**
- **Advanced Low Power Schottky processing**
- **100% Reliability Assurance Screening To MIL-STD-883 Requirements.**

Absolute Maximum Ratings

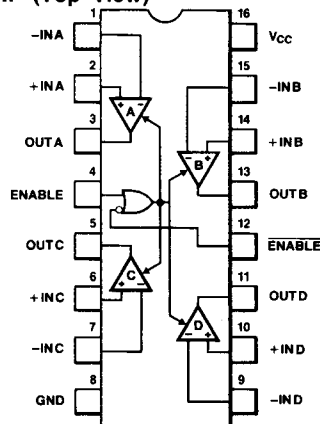
Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
0°C to +70°C	
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation ^{1, 2}	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage ³	
7.0 V	
Common Mode Voltage Range	
± 25 V	
Differential Input Voltage	
± 25 V	
Enable Voltage	
7.0 V	
Output Sink Current	
50 mA	

Notes

1. T_J Max = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Connection Diagram

16-Lead DIP (Top View)



CD02181F

Order Information

Device Code	Package Code	Package Description
μA26LS32DC	7B	Ceramic DIP
μA26LS32PC	9B	Molded DIP

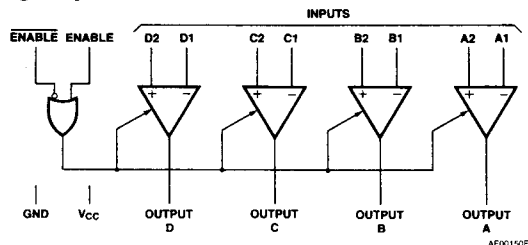
Function Table (Each Receiver)

Differential Inputs	Enables		Outputs
A - B	E	$\bar{E}$	V
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
? = Indeterminate

X = Immaterial
X = High Impedance (off)

Logic Symbol



AF00150F

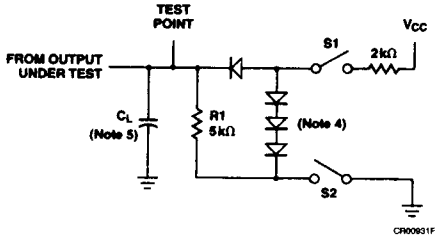
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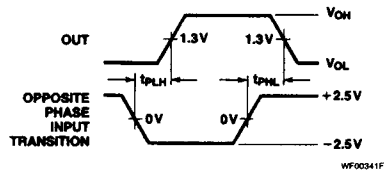
Electrical Characteristics $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$, unless otherwise specified.

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$-7.0\text{ V} \leq V_{CM} \leq +7.0\text{ V}$, $V_O = V_{OL}$ or V_{OH}	-0.2	± 0.06	+0.2	V
R_i	Input Resistance	$-15\text{ V} \leq V_{CM} \leq +15\text{ V}$, One Input AC Ground	6.0	15		kΩ
I_i	Input Current (Under Test)	$V_i = +15\text{ V}$, Other Input $-15\text{ V} \leq V_i \leq +15\text{ V}$			2.3	mA
I_i	Input Current (Under Test)	$V_i = -15\text{ V}$, Other Input $-15\text{ V} \leq V_i \leq +15\text{ V}$			-2.8	mA
V_{OH}	Output Voltage HIGH	$V_{CC} = \text{Min}$, $\Delta V_i = +1.0\text{ V}$, $V_{ENABLE} = 0.8\text{ V}$, $I_{OH} = -440\text{ }\mu\text{A}$	2.7	3.4		V
V_{OL}	Output Voltage LOW	$V_{CC} = \text{Min}$, $\Delta V_i = -1.0\text{ V}$, $V_{ENABLE} = 0.8\text{ V}$	$I_{OL} = 4.0\text{ mA}$		0.4	V
			$I_{OL} = 8.0\text{ mA}$		0.45	
V_{iL}	Enable Voltage LOW				0.8	V
V_{iH}	Enable Voltage HIGH				2.0	
V_{iC}	Enable Clamp Voltage	$V_{CC} = \text{Min}$, $I_i = -18\text{ mA}$			-1.5	V
I_{OZ}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max}$	$V_O = 2.4\text{ V}$		20	μA
			$V_O = 0.4\text{ V}$		-20	
I_{iL}	Enable Current LOW	$V_i = 0.4\text{ V}$		-0.2	-0.36	mA
I_{iH}	Enable Current HIGH	$V_i = 2.7\text{ V}$		0.5	20	μA
I_i	Enable Input High Current	$V_i = 5.5\text{ V}$		1.0	100	μA
I_{OS}	Output Short Circuit Current	$V_O = 0\text{ V}$, $V_{CC} = \text{Max}$, $\Delta V_i = +1.0\text{ V}$	-15	-50	-85	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$, All $V_i = \text{GND}$, Outputs Disabled		52	70	mA
V_{HYST}	Input Hysteresis	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $V_{CM} = 0\text{ V}$		30		mV
t_{PLH}	Input to Output	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, see test circuit		17	25	ns
t_{PHL}	Input to Output	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, see test circuit		17	25	ns
t_{LZ}	Enable to Output	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, see test circuit		20	30	ns
t_{HZ}	Enable to Output	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, see test circuit		15	22	ns
t_{ZL}	Enable to Output	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, see test circuit		15	22	ns
t_{ZH}	Enable to Output	$T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, see test circuit		15	22	ns

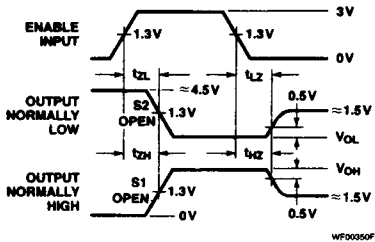
Load Test Circuit for Three-State Outputs



Propagation Delay (Notes 1 and 3)



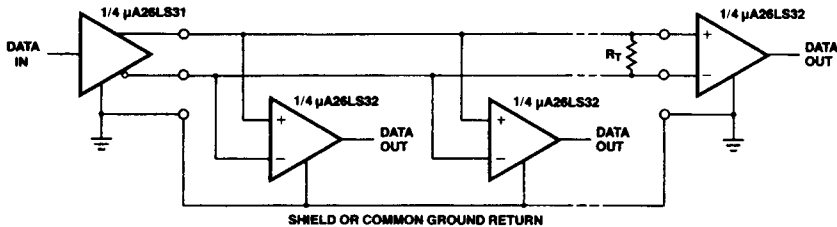
Enable and Disable Times (Notes 2 and 3)



Notes

1. Diagram shown for Enable Low.
2. $S1$ and $S2$ of Load Circuit are closed except where shown.
3. Pulse Generator for all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50 \Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.
4. All diodes are IN916 or IN3064.
5. C_L includes probe and jig capacitance.

Typical Application



AF00141F