

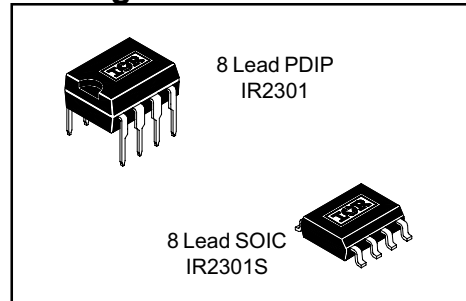
IR2301(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 5 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- Also available LEAD-FREE (PbF)

Packages



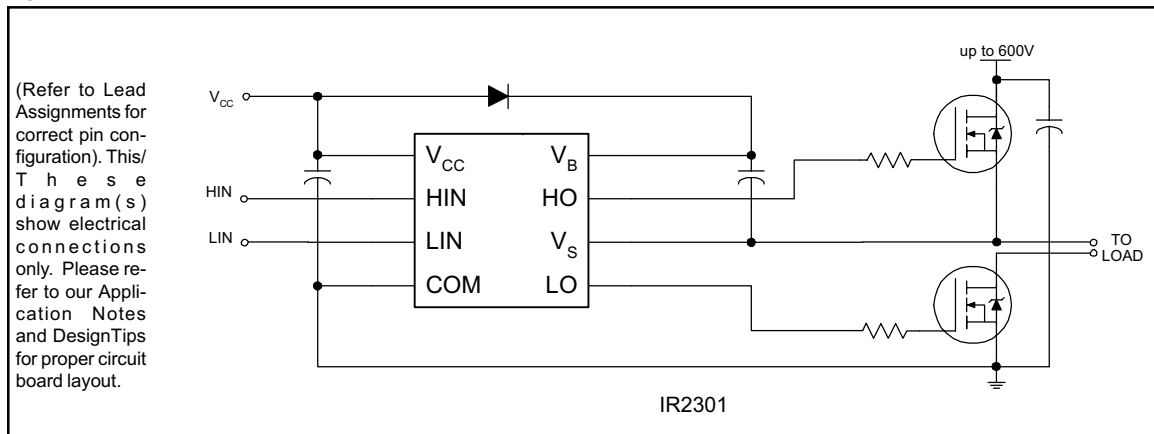
Description

The IR2301(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

2106/2301//2108//2109/2302/2304 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106/2301	HIN/LIN	no	none	COM
21064				VSS/COM
2108	HIN/LIN	yes	Internal 540ns Programmable 0.54~5µs	COM
21084				VSS/COM
2109/2302	IN/SD	yes	Internal 540ns Programmable 0.54~5µs	COM
21094				VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage	COM - 0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R _{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 5	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	5	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage	COM	V _{CC}	
T _A	Ambient temperature	-40	150	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 \text{ pF}, T_A = 25^\circ\text{C}.$

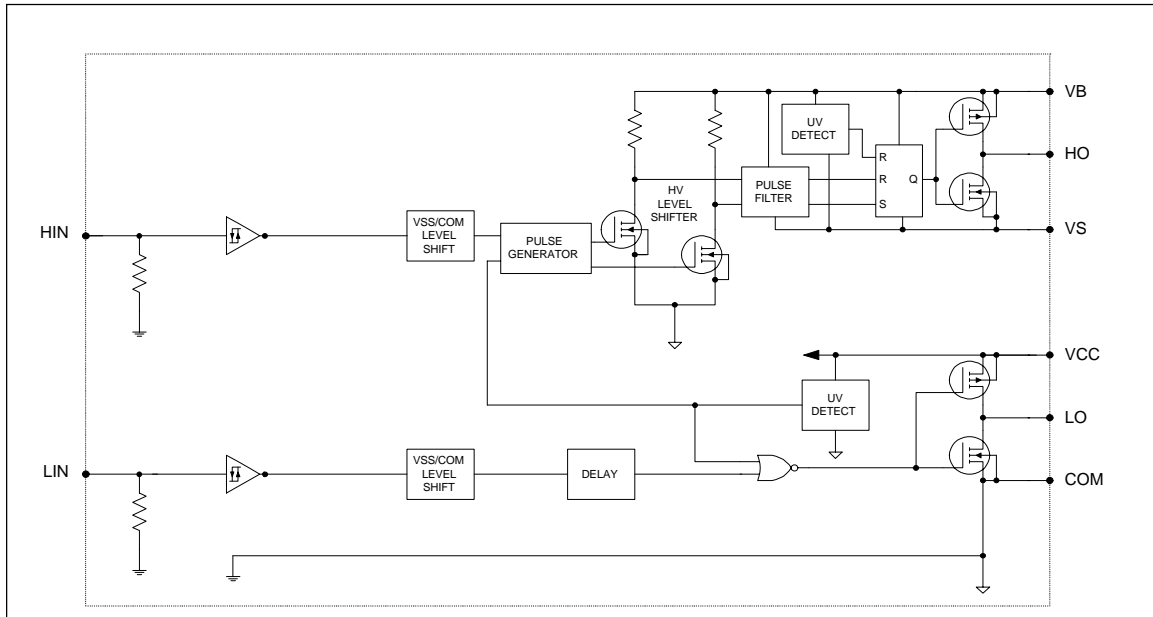
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	200	280		$V_S = 0V \text{ or } 600V$
MT	Delay matching, HS & LS turn-on/off	—	0	50		
t_r	Turn-on rise time	—	130	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$

Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V,$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads. The V_O, I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.9	—	—	V	$V_{CC} = 10V \text{ to } 20V$
V_{IL}	Logic "0" input voltage	—	—	0.8		$V_{CC} = 10V \text{ to } 20V$
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20 \text{ mA}$
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20 \text{ mA}$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	100		$V_{IN} = 0V \text{ or } 5V$
I_{QCC}	Quiescent V_{CC} supply current	50	120	190		$V_{IN} = 0V \text{ or } 5V$
I_{IN+}	Logic "1" input bias current	—	5	20		$V_{IN} = 5V$
I_{IN-}	Logic "0" input bias current	—	—	2		$V_{IN} = 0V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	3.3	4.1	5	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	3	3.8	4.7		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.1	0.3	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V,$ $PW \leq 10 \mu\text{s}$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V,$ $PW \leq 10 \mu\text{s}$

Functional Block Diagrams



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

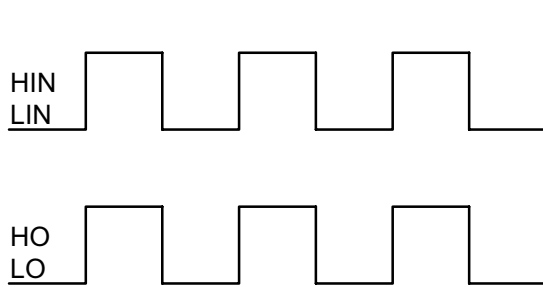
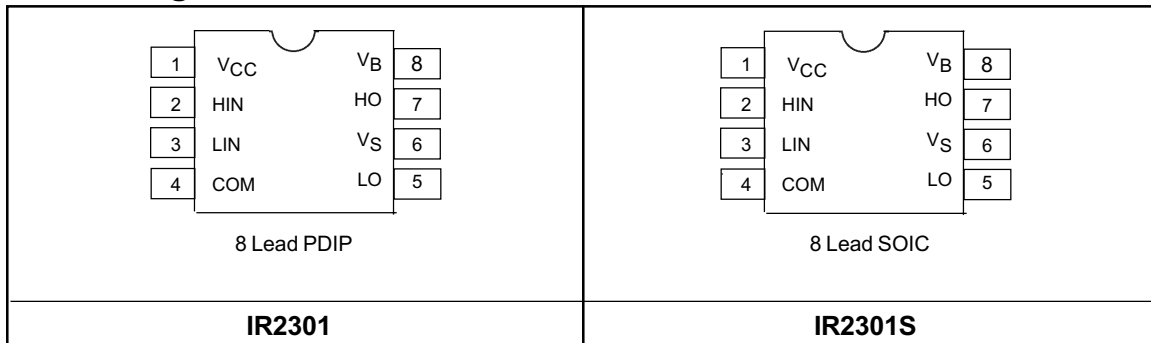


Figure 1. Input/Output Timing Diagram

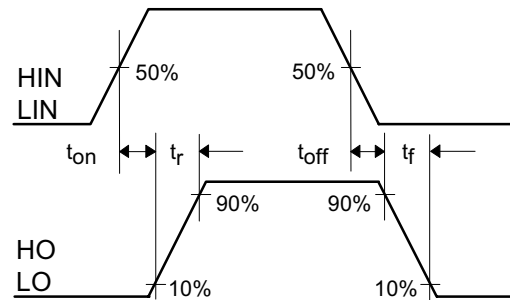


Figure 2. Switching Time Waveform Definitions

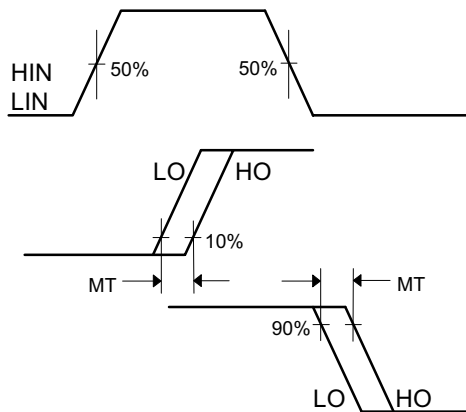


Figure 3. Delay Matching Waveform Definitions

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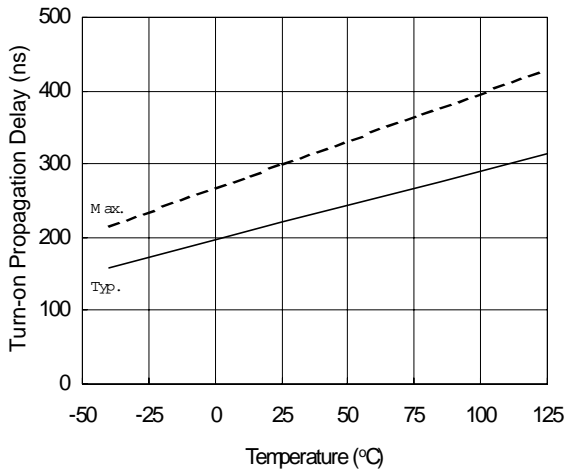


Figure 4A. Turn-on Propagation Delay vs. Temperature

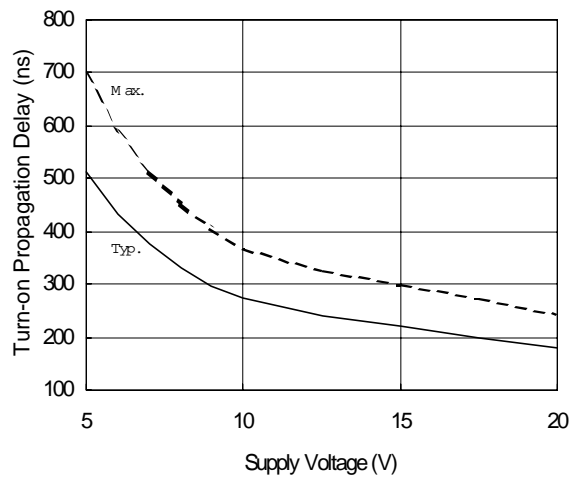


Figure 4B. Turn-on Propagation Delay vs. Supply Voltage

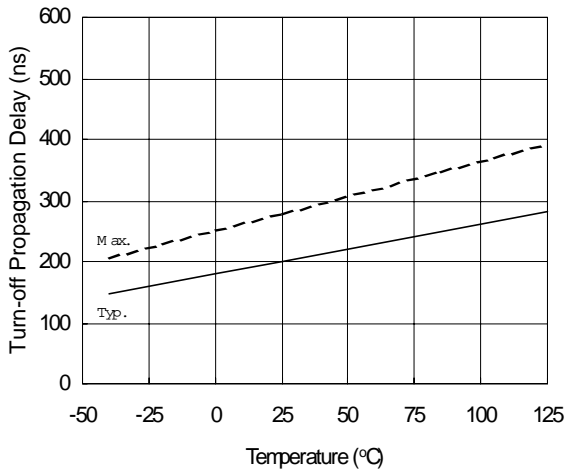


Figure 5A. Turn-off Propagation Delay vs. Temperature

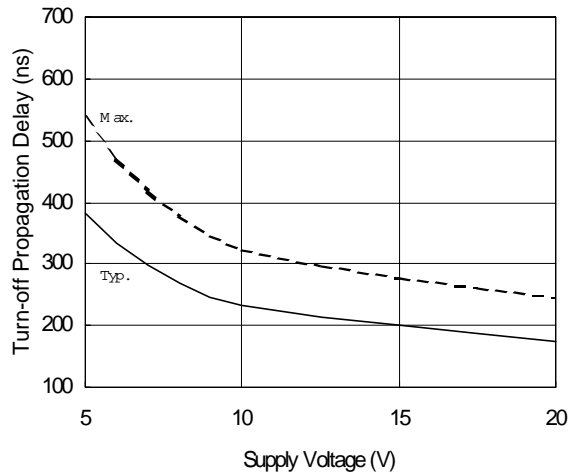


Figure 5B. Turn-off Propagation Delay vs. Supply Voltage

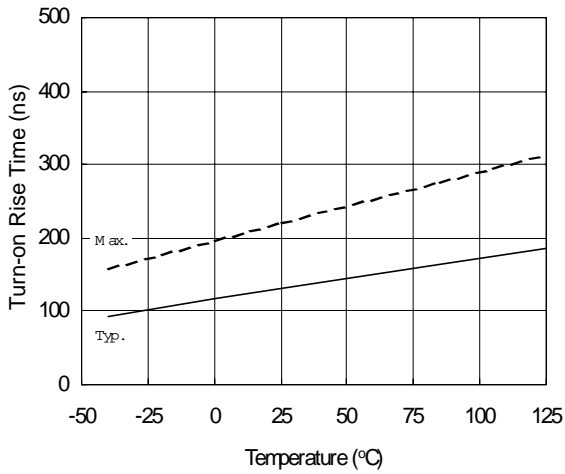


Figure 6A. Turn-on Rise Time vs. Temperature

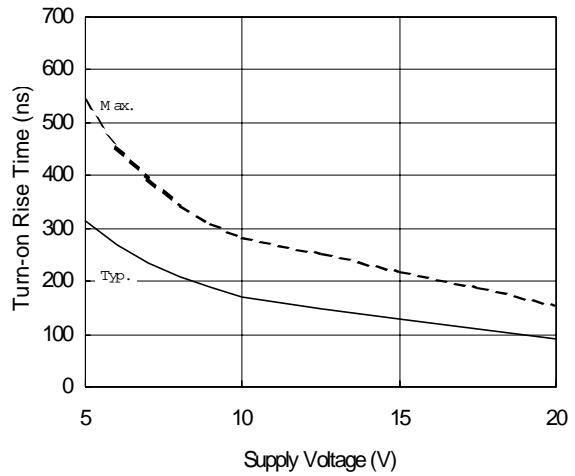


Figure 6B. Turn-on Rise Time vs. Supply Voltage

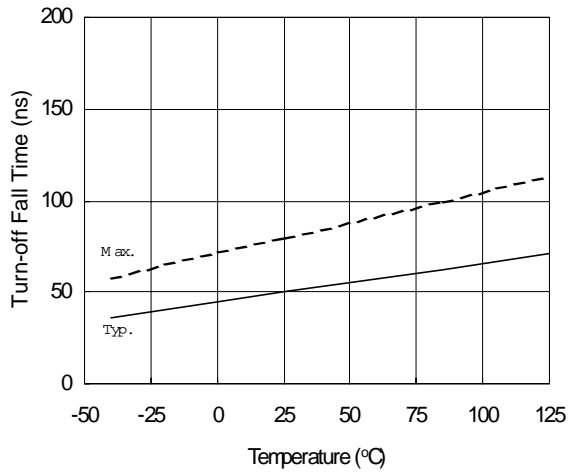


Figure 7A. Turn-off Fall Time vs. Temperature

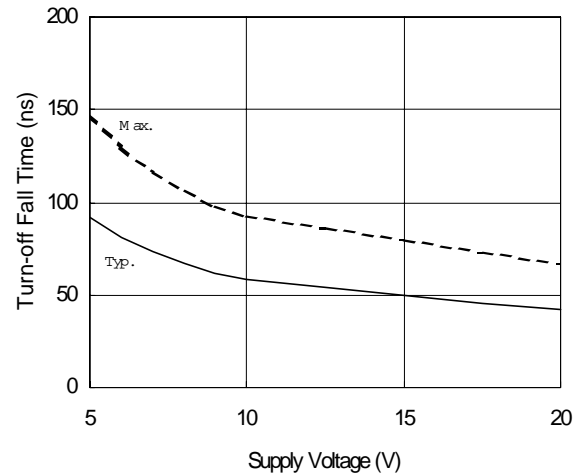


Figure 7B. Turn-off Fall Time vs. Supply Voltage

IR2301(S) & (PbF)

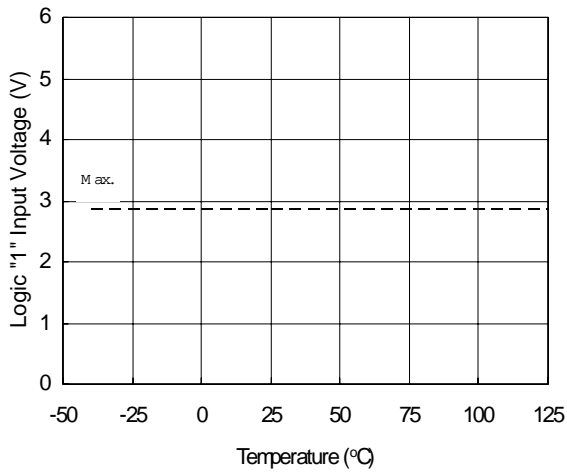


Figure 8A. Logic "1" Input Voltage vs. Temperature

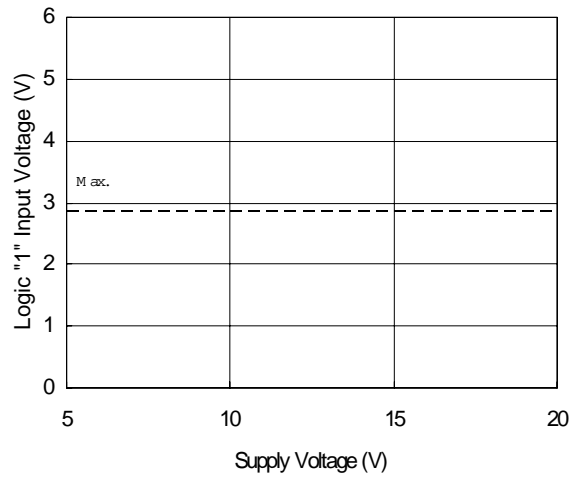


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

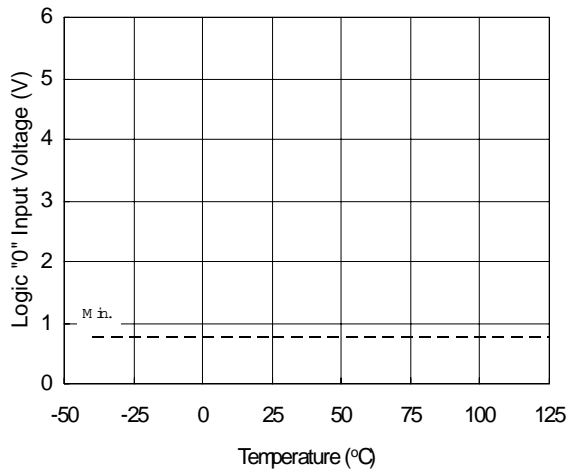


Figure 9A. Logic "0" Input Voltage vs. Temperature

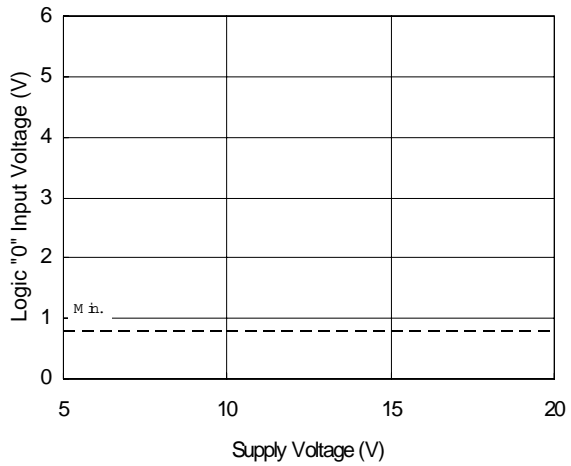


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

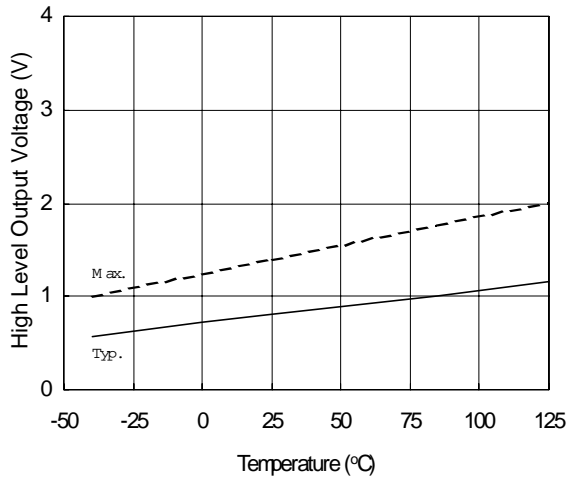


Figure 10A. High Level Output Voltage vs. Temperature

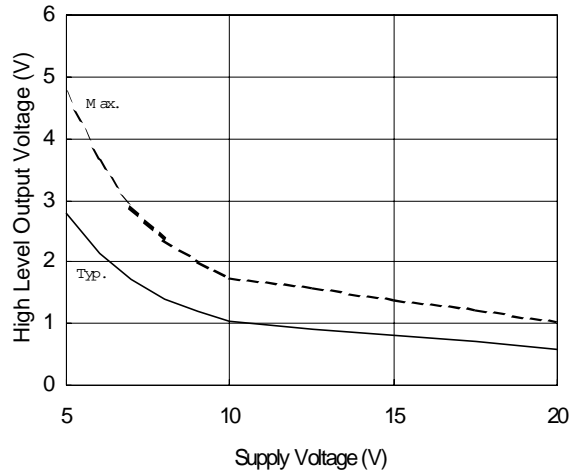


Figure 10B. High Level Output Voltage vs. Supply Voltage

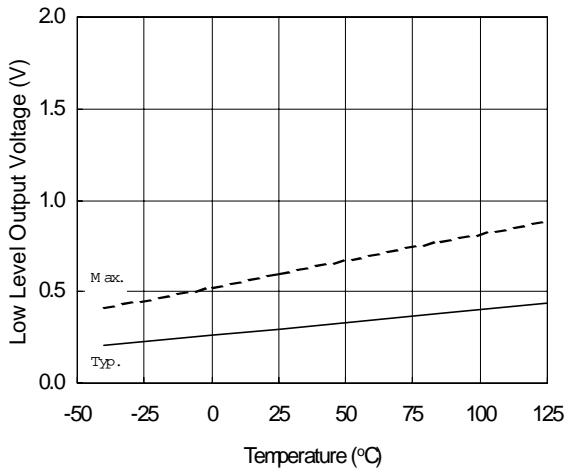


Figure 11A. Low Level Output Voltage vs. Temperature

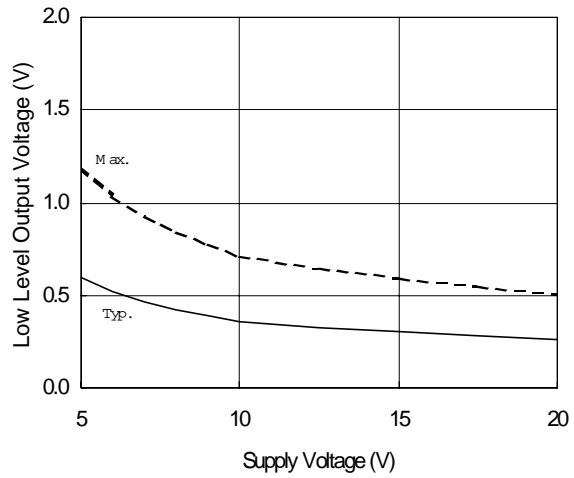


Figure 11B. Low Level Output Voltage vs. Supply Voltage

IR2301(S) & (PbF)

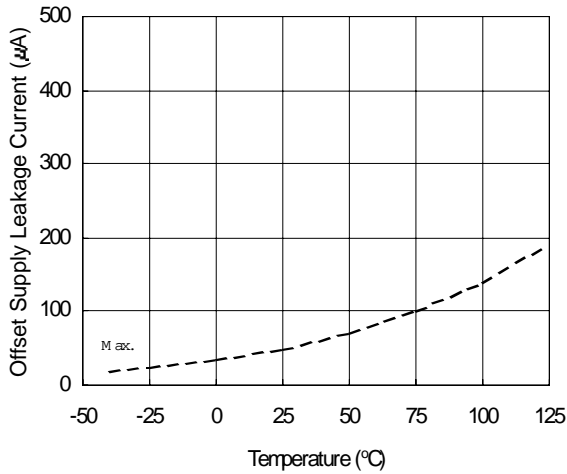


Figure 12A. Offset Supply Leakage Current vs. Temperature

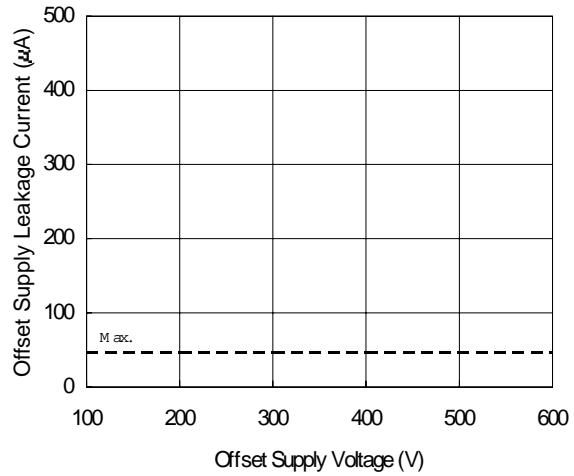


Figure 12B. Offset Supply Leakage Current vs. Supply Voltage

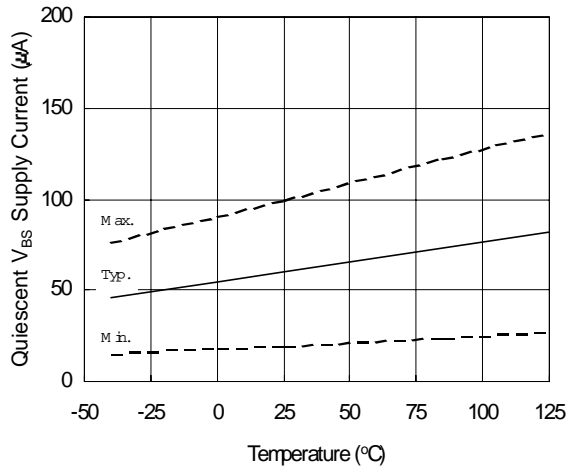


Figure 13A. Quiescent VBS Supply Current vs. Temperature

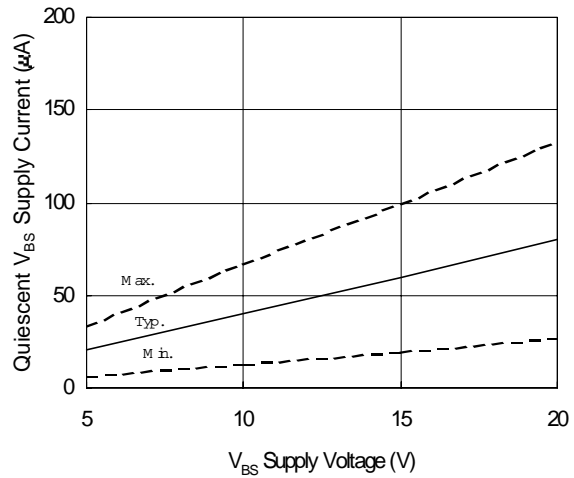


Figure 13B. Quiescent VBS Supply Current vs. Supply Voltage

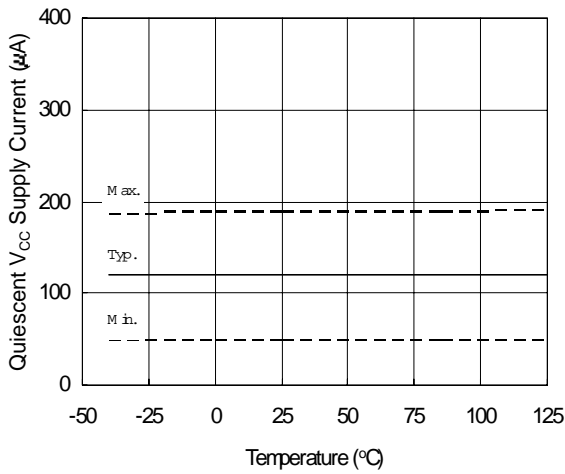


Figure 14A. Quiescent V_{CC} Supply Current vs. Temperature

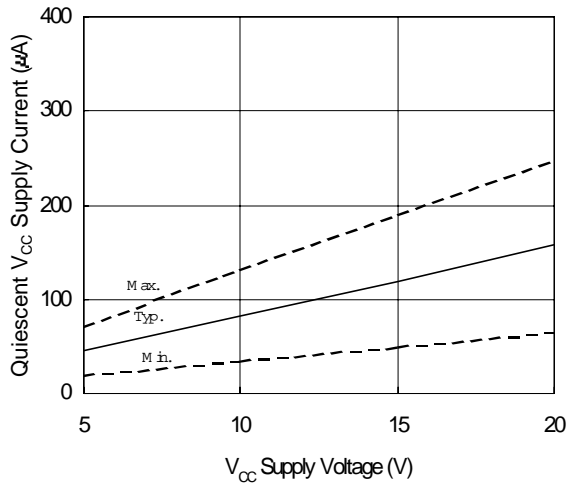


Figure 14B. Quiescent V_{CC} Supply Current vs. V_{CC} Supply Voltage

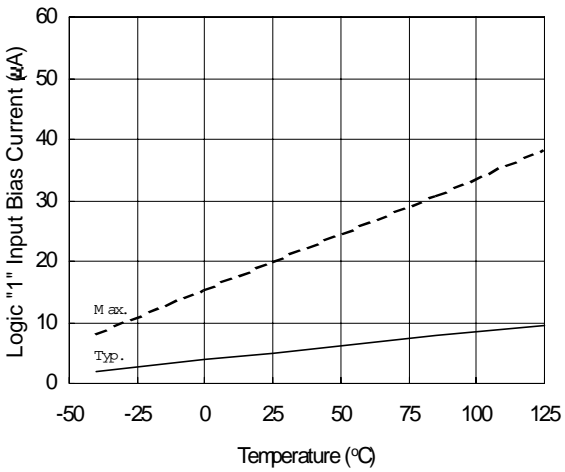


Figure 15A. Logic "1" Input Bias Current vs. Temperature

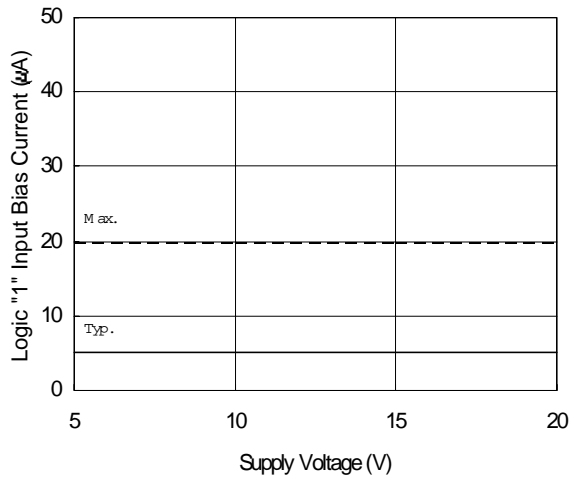


Figure 15B. Logic "1" Input Bias Current vs. Supply Voltage

IR2301(S) & (PbF)

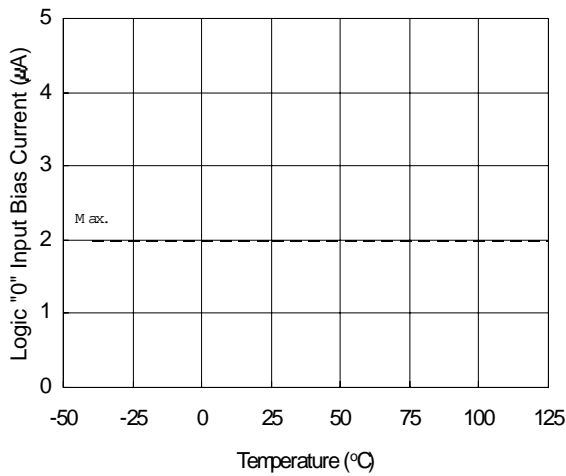


Figure 16A. Logic "0" Input Bias Current vs. Temperature

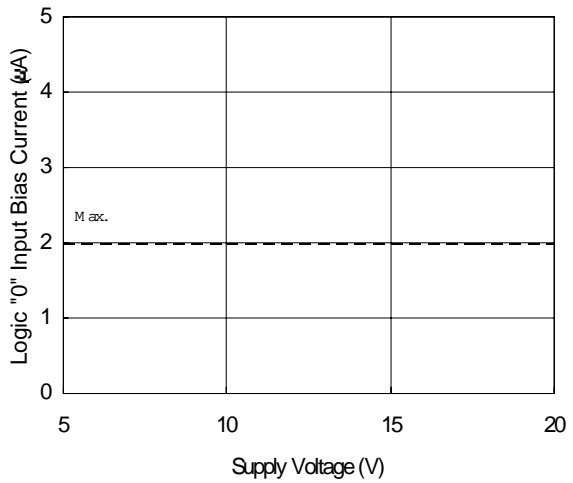


Figure 16B. Logic "0" Input Bias Current vs. Supply Voltage

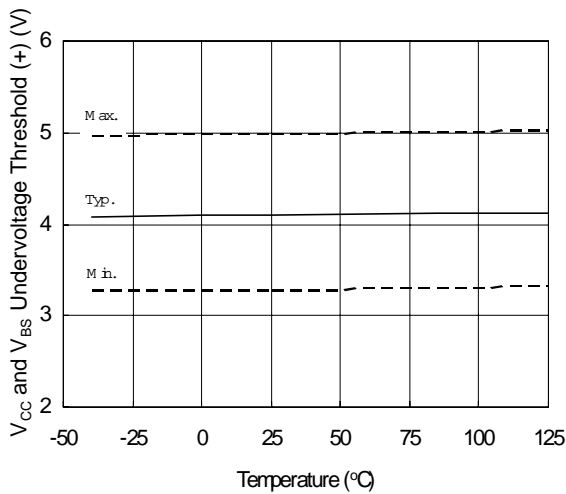


Figure 17. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

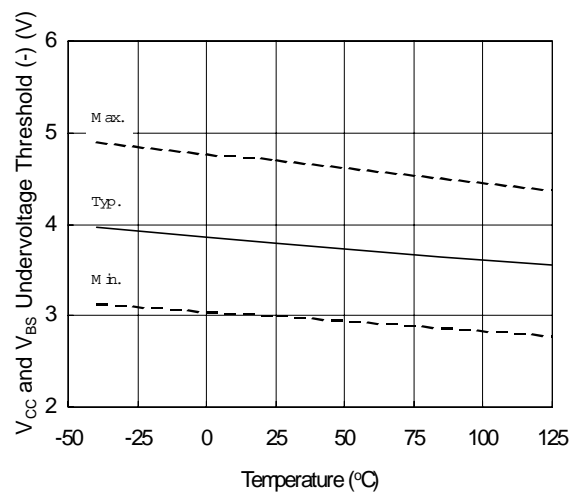


Figure 18. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

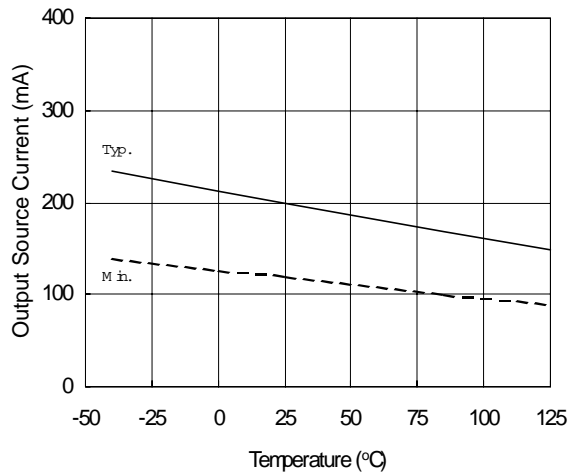


Figure 19A. Output Source Current vs. Temperature

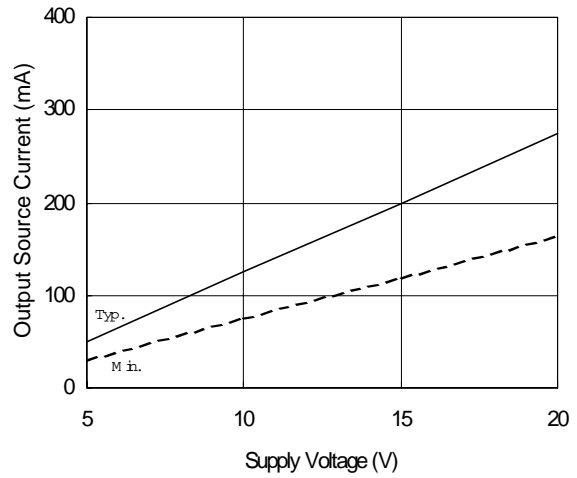


Figure 19B. Output Source Current vs. Supply Voltage

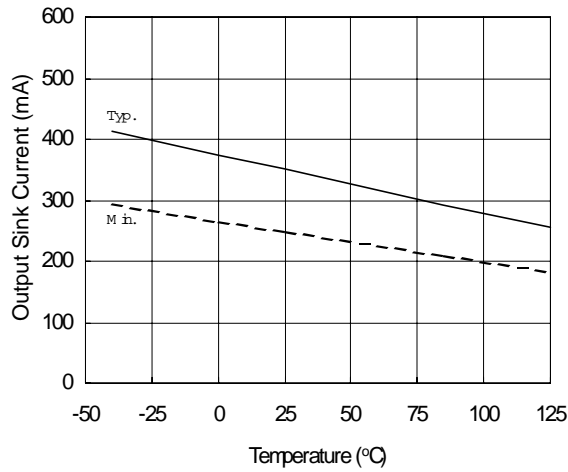


Figure 20A. Output Sink Current vs. Temperature

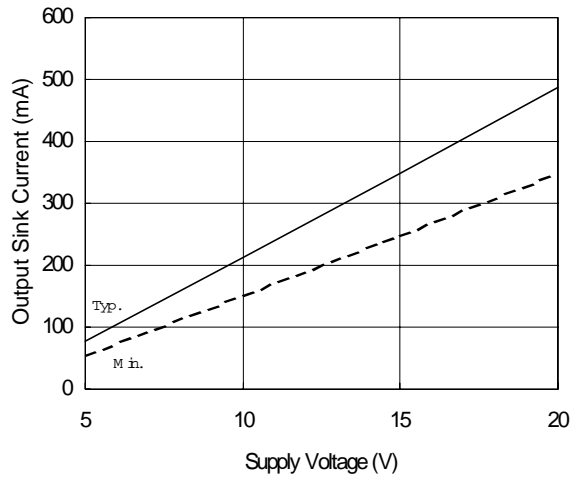


Figure 20B. Output Sink Current vs. Supply Voltage

IR2301(S) & (PbF)

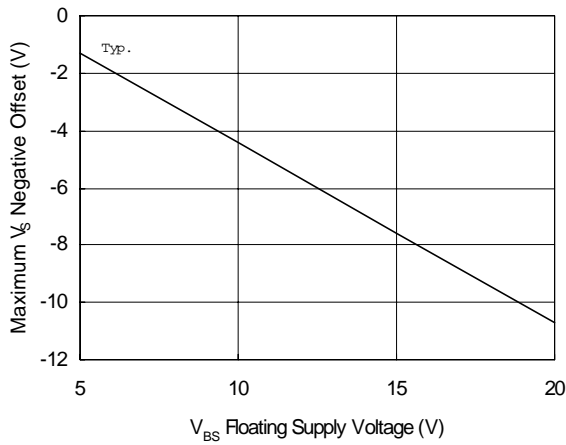


Figure 21. Maximum V_S Negative Offset vs. V_{BS} Floating Supply Voltage

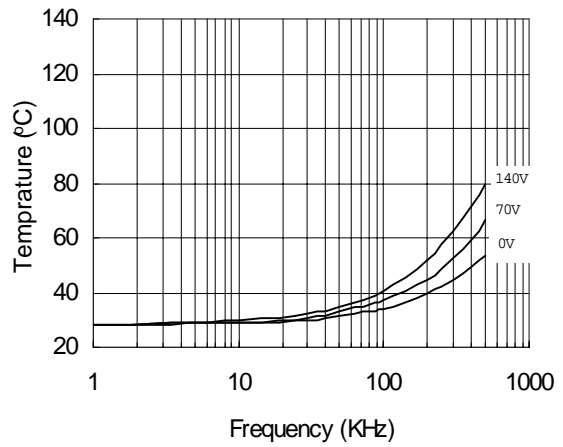


Figure 22. IR2301 vs. Frequency (IRFBC20), $R_{gate}=33\Omega$, $V_{CC}=15V$

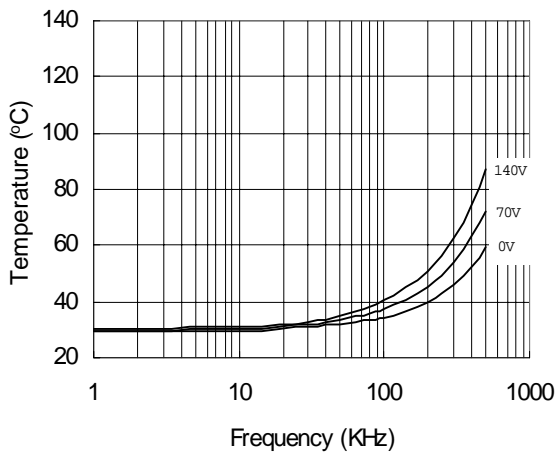


Figure 23. IR2301 vs. Frequency (IRFBC30), $R_{gate}=22\Omega$, $V_{CC}=15V$

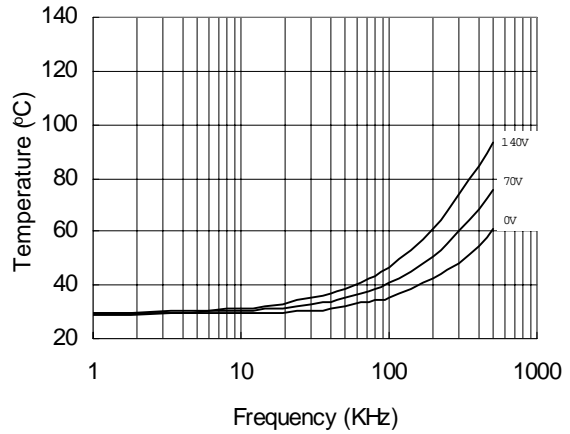
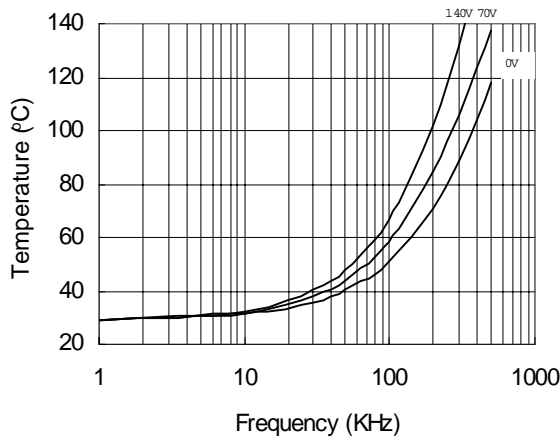
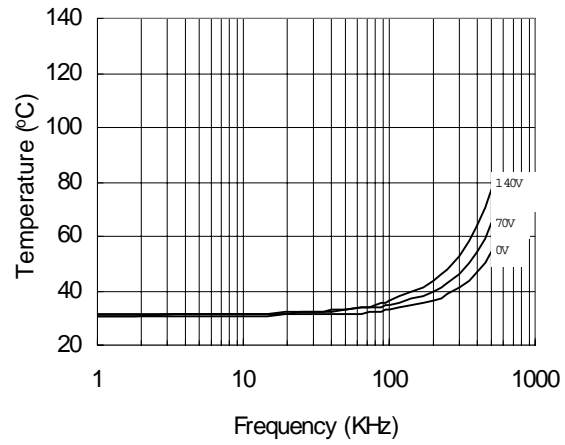


Figure 24. IR2301 vs. Frequency (IRFBC40), $R_{gate}=15\Omega$, $V_{CC}=15V$

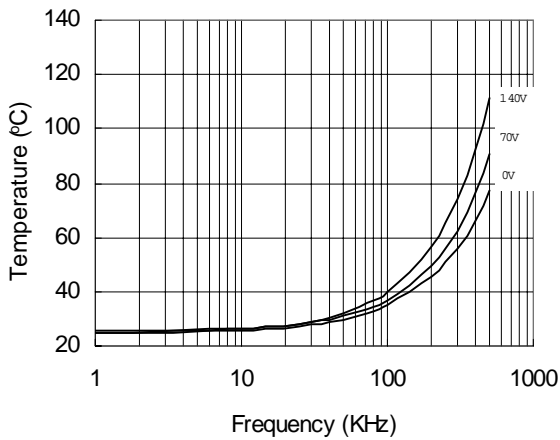
IR2301(S) & (PbF)



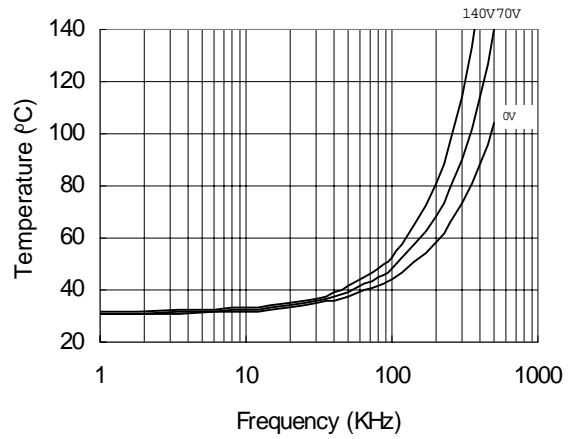
**Figure 25. IR2301 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{CC}=15V$**



**Figure 26. IR2301S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$**



**Figure 27. IR2301S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$**



**Figure 28. IR2301S vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$**

IR2301(S) & (PbF)

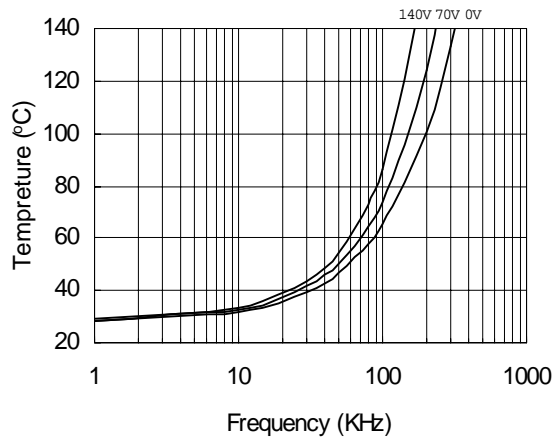
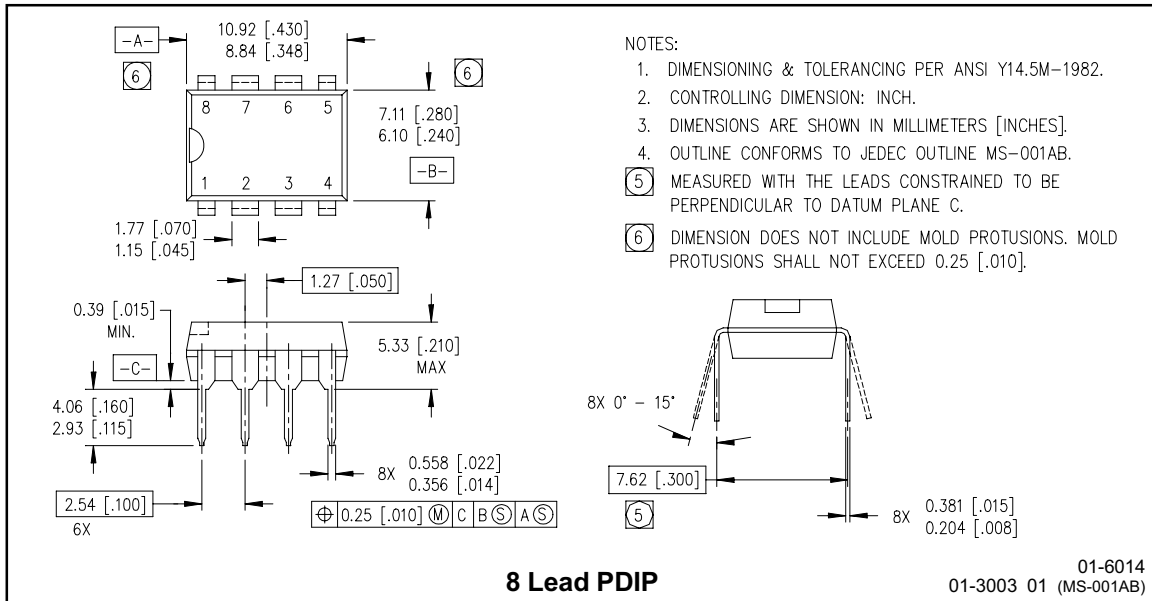


Figure 29. IR2301S vs. Frequency
(IRFPE50), $R_{gate}=10\Omega$, $V_{CC}=15V$

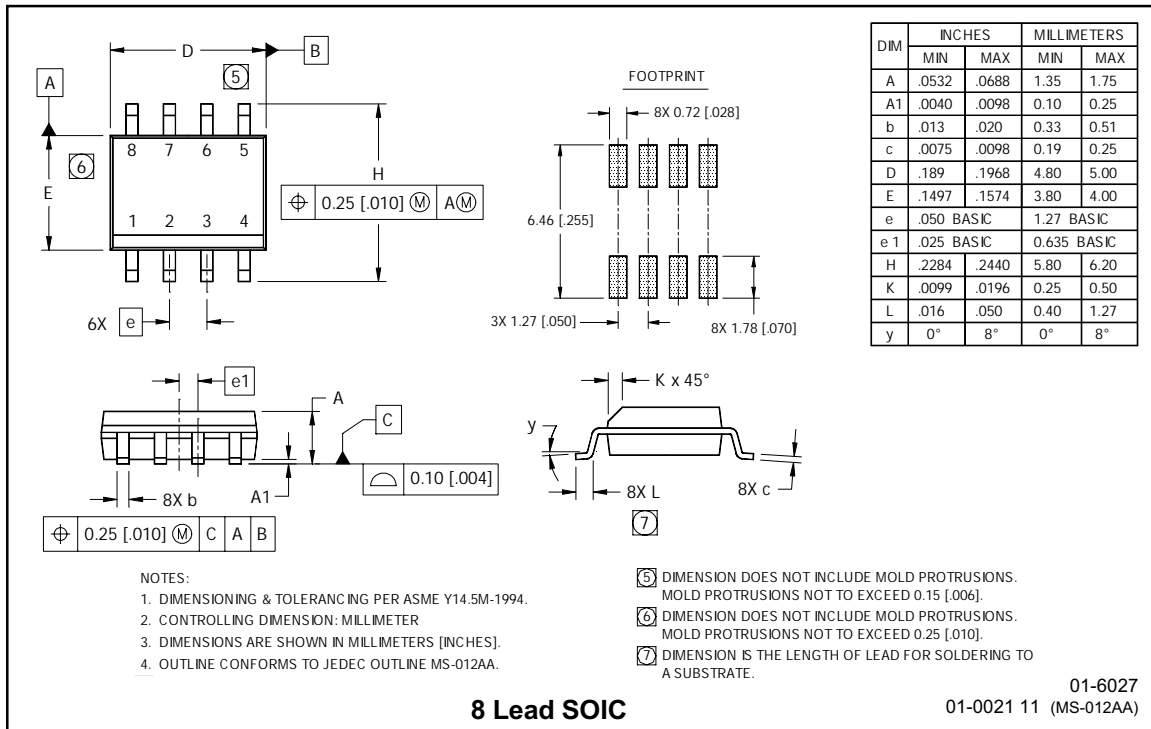
Case Outlines



NOTES:

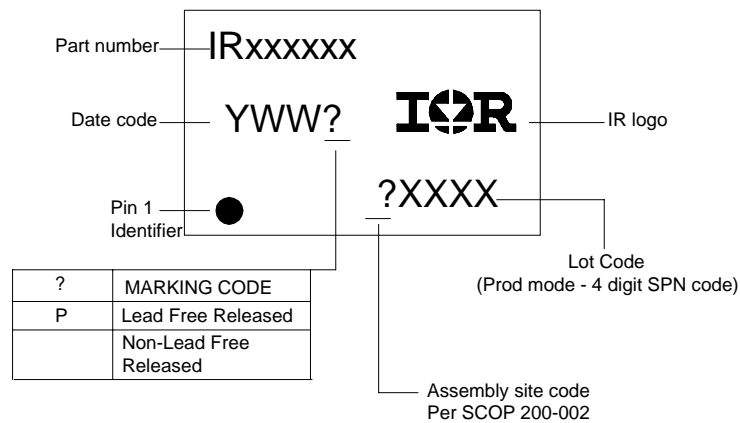
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

IR2301(S) & (PbF)



IR2301(S) & (PbF)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2301 order IR2301
8-Lead SOIC IR2301S order IR2301S

Leadfree Part

8-Lead PDIP R2301 order IR2301PbF
8-Lead SOIC IR2301S order IR2301SPbF