

# Primary side startup controller

## General description

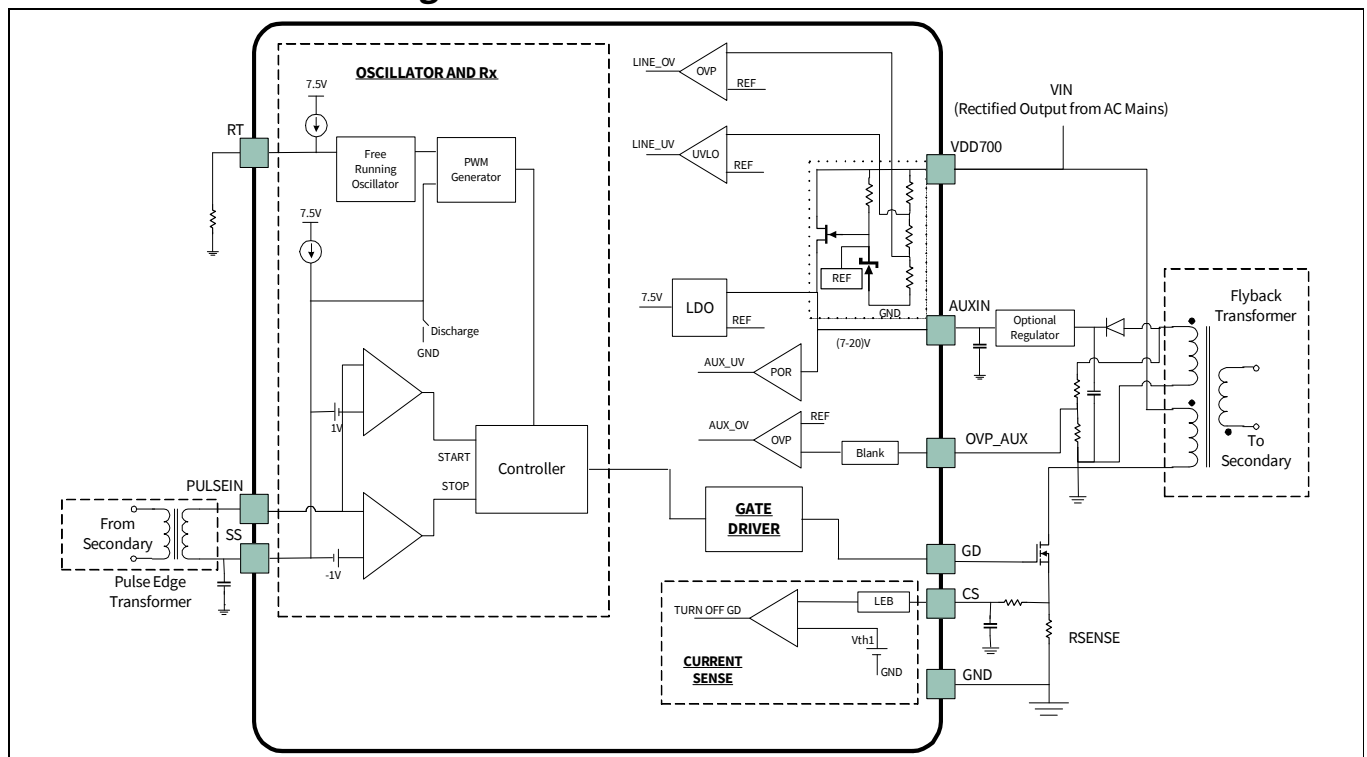
EZ-PD™ PAG1P (**P**ower **A**dapter **G**eneration **1** **P**imary) is Infineon's primary-side start-up controller for AC/DC applications targeting the mobile power adapter segment. EZ-PD™ PAG1P interfaces directly with either the AC mains in an X-cap discharge mode or the DC output of a bridge rectifier. EZ-PD™ PAG1P is available in a 10-pin SOIC package.

EZ-PD™ PAG1P is designed for a secondary controlled AC/DC flyback converter topology. In this topology, voltage and current regulation is performed by the secondary controller. EZ-PD™ PAG1P is responsible for providing the start-up function, driving the primary side FET as well as responding to fault conditions.

## Features

- Works across universal AC mains input 85 VAC to 265 VAC
- Low-side gate driver to drive primary side FET
- Line undervoltage protection (UVP) and line overvoltage protection
- Overcurrent protection (OCP)
- Overvoltage protection (OVP) during soft-start
- Programmable soft-start configurable with external capacitor
- Fixed auto-restart timer for fault recovery
- Supports X-cap discharge mode to obtain better efficiency
- Integrated high-voltage start-up and shunt regulator
- Synchronizes to PWM from secondary side using a pulse edge Transformer

## Functional block diagram

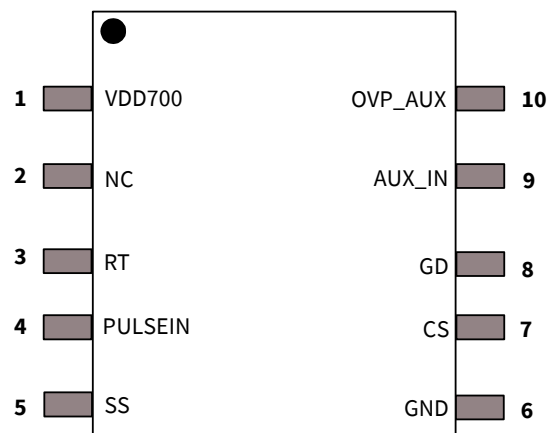


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## Pinout

# 1 Pinout



**Figure 1** Pin map

**Table 1** EZ-PD™ PAG1P pin description

| Pin number | Pin name | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | VDD700   | Start-up power supply input. VDD700 is the power supply source during the start-up phase. This pin can be connected to either the bridge rectifier output as shown in <a href="#">Figure 2</a> , or directly to the AC mains through a diode as shown in <a href="#">Figure 3</a> . This pin has a maximum voltage rating of 500 V.                                                                              |
| 2          | NC       | No connect                                                                                                                                                                                                                                                                                                                                                                                                       |
| 3          | RT       | Timing resistor. The RT pin is used to connect to an external timing resistor of 499 kΩ which determines the free running oscillator frequency Fosc. Oscillator frequency is typically 30 kHz.                                                                                                                                                                                                                   |
| 4          | PULSEIN  | Pulse Edge Transformer (PET) input. Once the start-up phase is successfully complete, EZ-PD™ PAG1P synchronizes to the secondary side pulses received at the PULSEIN input. The secondary controller provides PWM control information to the primary using a PET. The pulse amplitude shall not exceed V_PULSEINNEGAMP and V_PULSEINPOSAMP and the pulse width shall be in the T_PULSEINPW range.                |
| 5          | SS       | Soft-start pin. Connect a 0.1-μF capacitor to GND. The soft-start time is provided in the specification section ( <a href="#">Table 13</a> ). This pin also connects to the other end of the pulse transformer. The external capacitor connected to the SS pin determines the soft-start time. The duty cycle of the gate drive gradually increases to provide a smooth transfer of power to the secondary side. |
| 6          | GND      | Ground                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7          | CS       | Primary side current sense input. Current sense input is used to monitor the overcurrent fault scenario. Overcurrent fault is detected with the voltage between this input and ground exceeds V_CSTH1 threshold.                                                                                                                                                                                                 |
| 8          | GD       | Primary FET gate driver. EZ-PD™ PAG1P integrates a low side gate driver to drive the gate of an external FET.                                                                                                                                                                                                                                                                                                    |

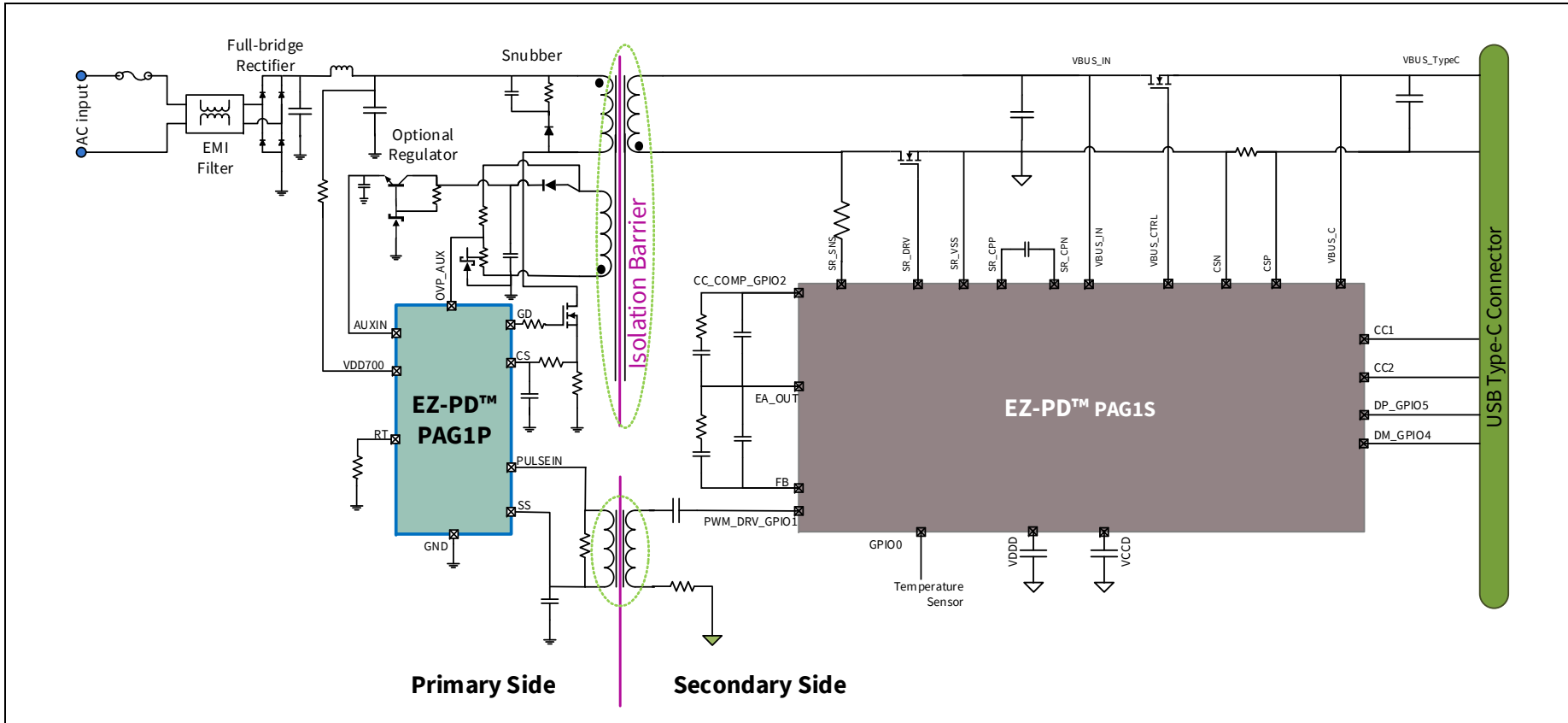
## Pinout

**Table 1** EZ-PD™ PAG1P pin description (continued)

| Pin number | Pin name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9          | AUX_IN   | Auxiliary supply input. AUX_IN serves as the power supply source after the start-up phase. This pin should be connected to the output of auxiliary winding through a rectifier or a regulator depending on whether the maximum voltage on the output of the auxiliary winding exceeds 22 V. EZ-PD™ PAG1P switches its power supply source to AUX_IN once the secondary side provides power.                                                      |
| 10         | OVP_AUX  | Auxiliary winding overvoltage detection. EZ-PD™ PAG1P monitors this pin for overvoltage condition on the secondary side, using an external resistor divider. Any voltage exceeding V_OVPAUXRISE on this pin is treated as an overvoltage fault condition. The overvoltage condition is monitored only during open loop operation. A Schottky diode to GND should be connected to ensure negative voltage is not seen when the gate driver is ON. |

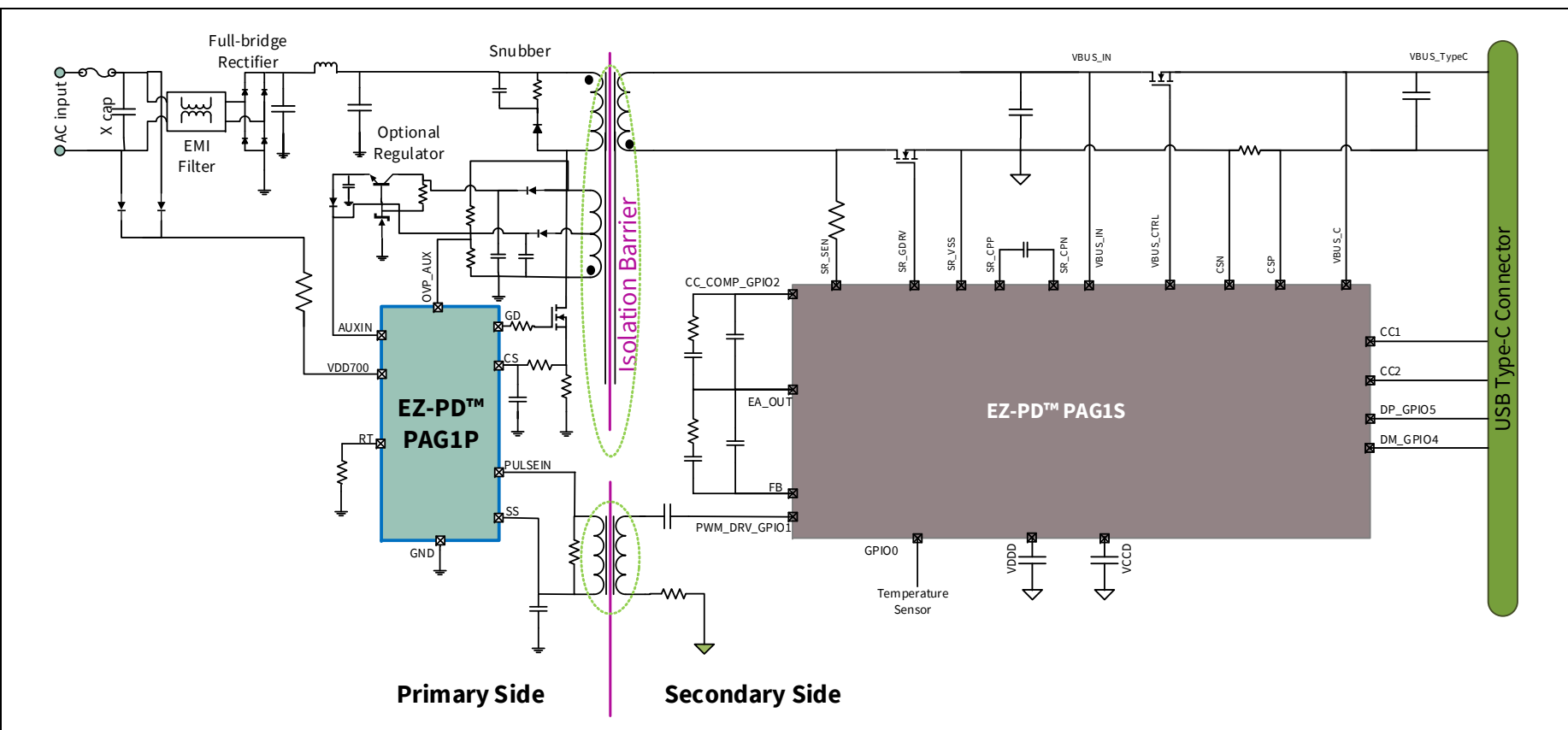
## 2 Application overview

EZ-PD™ PAG1P works with Infineon's secondary side controller EZ-PD™ PAG1S. **Figure 2** shows the application diagram of a USB Power Delivery power adapter solution with 'EZ-PD™ PAG1P + EZ-PD™ PAG1S'. In this system, once the start-up phase is complete, the primary FET control is completely synchronized to the PWM pulses received from the secondary side. The PWM pulses are transmitted over an isolation barrier using a PET. EZ-PD™ PAG1P takes over control of the primary FET only during power-up and system fault scenarios.



**Figure 2** Type-C based mobile phone power adapter with EZ-PD™ PAG1P (CYPAP111xx) and EZ-PD™ PAG1S in a secondary controlled flyback topology configuration

**Figure 3** shows the application diagram for a power adapter where EZ-PD™ PAG1P is powered directly from the AC mains before the full bridge rectifier. This topology enables discharging the X cap using EZ-PD™ PAG1P instead of using a passive resistor thereby improving efficiency.



**Figure 3** Type-C based mobile phone power adapter with EZ-PD™ PAG1P (CYPAP112xx) used in X-cap discharge configuration

### 3 Functional description

#### 3.1 Soft-start

The Soft-start feature allows EZ-PD™ PAG1P to gradually increase the output voltage of the flyback converter till the secondary side takes control of the regulation. Soft-start is used during initial start-up sequence and fault condition. The duration of the soft-start is controlled by an external capacitor connected to the SS pin and the frequency of the soft-start is determined by an external resistor connected to the RT pin. An internal current source of 5  $\mu$ A charges the external capacitor and the maximum amplitude for the soft-start ramp is 3.75 V. 3.75 V dictates the maximum duty cycle. Under Soft-start, the maximum ON time of the primary FET is limited to 19  $\mu$ s which is equivalent to 70% duty cycle at 30 kHz. When the secondary side takes control, the maximum ON time is limited to 25  $\mu$ s.

#### 3.2 X-cap mode

In EZ-PD™ PAG1P X-cap part, X-cap mode is detected when 3 V\_VDD700UVRise transitions occur within 64 ms. A flag is set indicating the part is operating in X-cap mode. When 3 V\_VDD700UVRise transitions are not detected within 64 ms after the flag is set, a line disconnect is detected and an internal discharge path is turned ON to discharge the X-capacitor.

#### 3.3 Secondary synchronization

During the start-up phase, if EZ-PD™ PAG1P sees appropriate input pulses at the PULSEIN pin, then it synchronizes the primary FET control to the secondary pulses. The PWM control signal from the secondary side is coupled to the primary side using a Pulse Edge Transformer (PET). The PET is an important component to ensure proper frequency response and should have just an adequate Q-factor to avoid excessive overshoot. The positive pulse from the PET is treated as primary FET turn-on signal and the negative pulse from the PET is treated as primary FET turn-off signal. The pulse amplitude shall not exceed V\_PULSEINNEGAMP and V\_PULSEINPOSAMP and the pulse width shall be within T\_PULSEINPW range.

The synchronization path between the secondary and primary through the PET is also used for communication of shutdown condition. Three consecutive negative pulses from the secondary side is treated as a shutdown signal. On receiving such three consecutive negative pulses, EZ-PD™ PAG1P will shutdown after 200 ms.

#### 3.4 Power circuit

EZ-PD™ PAG1P integrates a high voltage start-up regulator. During power-up, EZ-PD™ PAG1P shall be powered from the line input via the VDD700 pin. Once voltage on the auxiliary winding is available from the secondary side, EZ-PD™ PAG1P switches its power supply input to AUX\_IN pin and no power will be sourced from the VDD700 pin.

#### 3.5 Overcurrent and overvoltage fault protection

EZ-PD™ PAG1P implements overcurrent protection. When the CS pin voltage exceeds V\_CSTH1, EZ-PD™ PAG1P limits the primary current by turning OFF the primary FET.

EZ-PD™ PAG1P provides three types of voltage protection – protection against line undervoltage/overvoltage and secondary overvoltage. The line undervoltage/overvoltage monitoring is via VDD700 pin and the respective thresholds are V\_VDDUVRise and V\_VDDOVRise. Gate pulses are turned off until fault is removed. Once the voltage on VDD700 is within operating range, EZ-PD™ PAG1P does an auto-restart.

In addition, EZ-PD™ PAG1P monitors the voltage on OVP\_AUX pin for detecting overvoltage condition on the secondary side. The voltage on the OVP\_AUX pin is a scaled-down version of the secondary side voltage. When voltage on OVP\_AUX exceeds V\_OVPAUXRise, the gate driver is turned off. Once the voltage on OVP\_AUX goes below the fault range, EZ-PD™ PAG1P does an auto-restart. EZ-PD™ PAG1P monitors secondary overvoltage only during start-up phase or during fault condition after auto-restart.

The flow chart in [Figure 4](#) and the [Functional block diagram](#) show the operation of the chip.

### 3.6 Auto-restart timer

A fixed timer of TAR sec is available for various fault conditions. The timer is operated from a free running oscillator inside EZ-PD™ PAG1P. Free running oscillator will be running at Fosc.

### 3.7 Protection and fault condition

Primarily there are four types of protection actions used in various fault conditions.

1. Autorestart: In this mode, EZ-PD™ PAG1P will wait TAR sec before doing a soft start. This sequence is repeated continuously (see [Figure 5](#)).
2. Latch or shutdown: No auto-restart timer or soft start is implemented. Shuts the IC immediately and power to the IC needs to be removed to unlatch.
3. Gate OFF: This only turns OFF the gate drive pulse and waits for the fault condition to pass before the IC functions normally.
4. Max duty cycle: Gate driver will be ON for 19  $\mu$ s (maximum) during soft-start. When secondary is in control, gate drive will be ON for 25  $\mu$ s (maximum).

## Functional description

**Table 2** provides the fault conditions and protection action.

**Table 2**      **Faults conditions and protection action**

| Sl# | Fault                                                                   | Action                                                                                                                                                                            |
|-----|-------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | VDD700 pin is under threshold voltage<br>V_VDD700UVRise                 | Gate driver output is low. When VDD700 exceeds V_VDD700UVRise, do a soft-start followed by Autorestart.                                                                           |
| 2   | VDD700 pin exceeds threshold voltage<br>V_VDD700OVRise                  | Gate driver output is low during fault condition followed by Autorestart.                                                                                                         |
| 3   | OVP_AUX pin exceeds threshold voltage<br>V_OVPAUXRise                   | Gate driver output is low during fault condition followed by Autorestart. This is valid only when EZ-PD™ PAG1P is operating in open loop.                                         |
| 4   | CS pin exceeds threshold voltage V_CSTH1                                | Gate driver output is low during fault condition. In open loop, do the Autorestart after fault condition is removed. In closed loop, wait for the next pulse from secondary side. |
| 6   | Stop command from Secondary side                                        | Shutdown after 200 ms.                                                                                                                                                            |
| 7   | Receive no pulses from Secondary side for TAR sec after last stop pulse | Autorestart                                                                                                                                                                       |
| 8   | Start pulse and no Stop pulse from Secondary side                       | Keep gate driver ON for 25 $\mu$ s. EZ-PD™ PAG1P will wait for TAR sec before doing Autorestart.                                                                                  |

Functional description

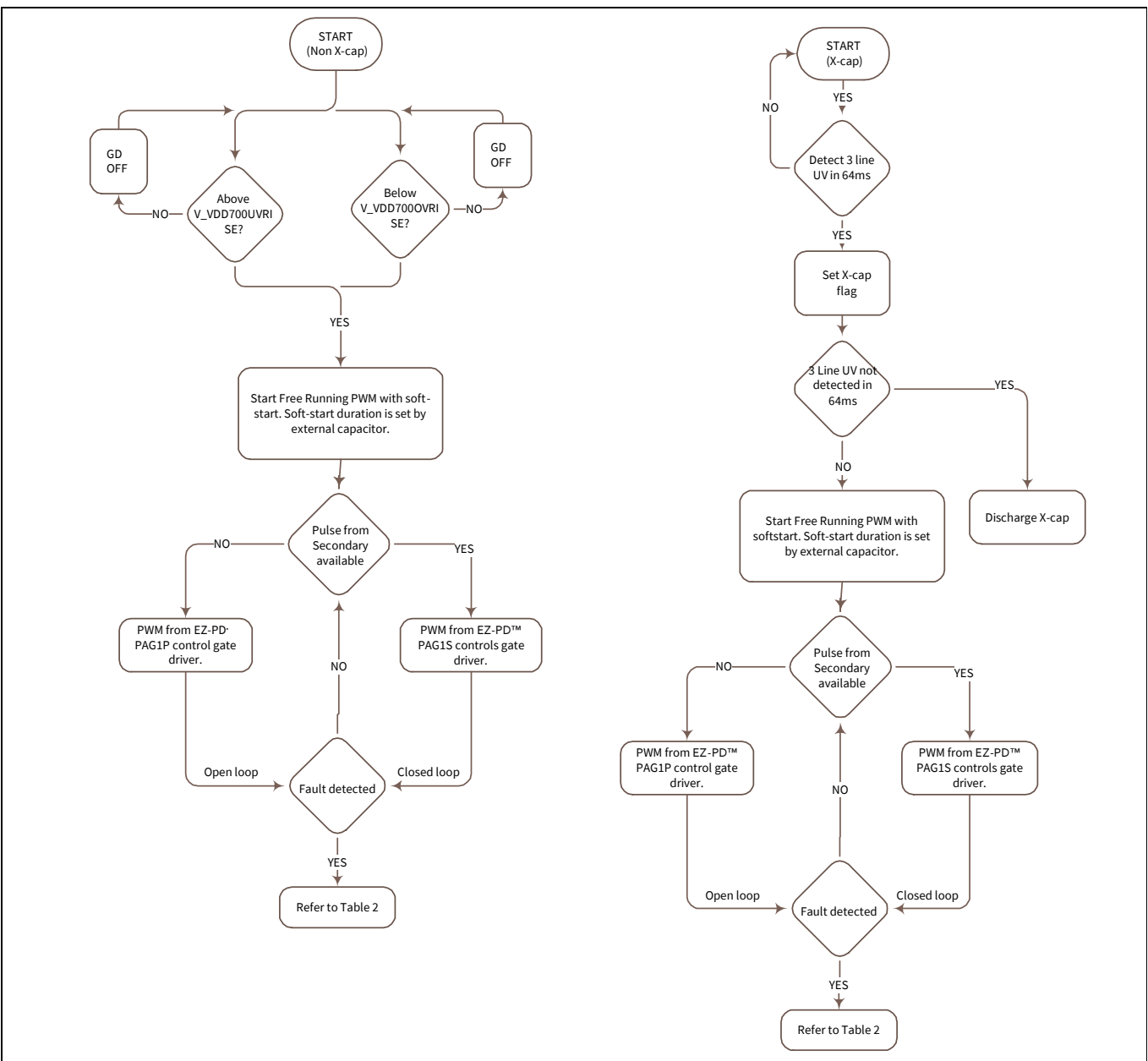


Figure 4 EZ-PD™ PAG1P operation flow chart

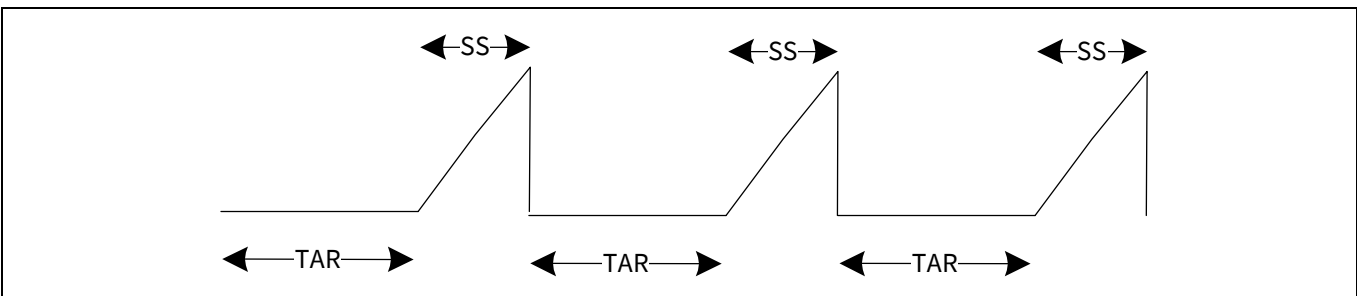


Figure 5 Auto-restart

## Electrical specifications

## 4 Electrical specifications

**Table 3 Absolute maximum ratings**

| Description                                  | Min  | Typ | Max  | Unit | Details/conditions                                                                                        |
|----------------------------------------------|------|-----|------|------|-----------------------------------------------------------------------------------------------------------|
| Voltage on VDD700                            | 0    | —   | 500  | V    | —                                                                                                         |
| Output current on GD                         | −1   | —   | 1    | A    | —                                                                                                         |
| Voltage on AUX_IN                            | 0    | —   | 22   | V    | —                                                                                                         |
| Voltage on CS, SS, OVP_AUX                   | −0.3 | —   | 8.25 |      | —                                                                                                         |
| Voltage on RT                                | 0    | —   | 8.25 |      | —                                                                                                         |
| Voltage on PULSEIN                           | −5   | —   | 8.25 |      | —                                                                                                         |
| Operating junction temperature               | −40  | —   | 125  | °C   | —                                                                                                         |
| Storage temperature                          | −55  | —   | 150  |      | —                                                                                                         |
| Ambient temperature                          | −40  | —   | 105  |      | —                                                                                                         |
| Electrostatic discharge human body model     | 2000 | —   | —    | V    | —                                                                                                         |
| Electrostatic discharge charged device model | 500  | —   | —    |      | —                                                                                                         |
| Pin current for latch-up                     | −100 | —   | 100  | mA   | Except for SS and OVP_AUX. For SS and OVP_AUX, use −0.5 V. For RT, negative injection is not recommended. |

**Table 4 Silicon power specifications**

| Spec ID      | Parameter        | Description                                 | Min  | Typ | Max | Unit | Details/conditions                                                       |
|--------------|------------------|---------------------------------------------|------|-----|-----|------|--------------------------------------------------------------------------|
| SID.VDD700.1 | VDD700           | High voltage supply                         | 120  | —   | 380 | V    | —                                                                        |
| SID.AUXIN.1  | V_AUXIN          | Auxiliary supply                            | 13   | —   | 20  |      | —                                                                        |
| SID.PWR.1    | I_VDD700_LATCH   | Current from VDD700 (VDD700 = 325 V)        | —    | 50  | —   | μA   | EZ-PD™ PAG1P is in shutdown.                                             |
| SID.PWR.2    | I_VDD700_NOGD    | Current from VDD700 (VDD700 = 325 V)        | —    | 350 | —   |      | All circuits active except gate driver not toggling                      |
| SID.PWR.3    | I_VDD700_ACTIVE  | Current from VDD700 (VDD700 = 325 V)        | —    | 800 | —   |      | All circuits active including gate driver toggling at 30 kHz; CL = 1 nF. |
| SID.PWR.4    | I_AUXIN_NOGD     | Current from AUXIN (AUXIN = 12 V)           | —    | 350 | —   |      | All circuits active except gate driver not toggling                      |
| SID.PWR.5    | I_AUXIN_ACTIVE   | Current from AUXIN (AUXIN = 12 V)           | —    | 800 | —   |      | All circuits active including gate driver toggling at 30 kHz; CL = 1 nF. |
| SID.PWR.6    | I_VDD700_STARTUP | Current from VDD700 when starting up        | —    | 10  | —   | mA   | VDD700 = 325 V; AUXIN = 0 V                                              |
| SID.PWR.7    | I_XCAP_DISCHARGE | Current from VDD700 while discharging X-cap | 0.48 | 1.7 | 2   |      | —                                                                        |

## Electrical specifications

**Table 5 Undervoltage and overvoltage on VDD700**

| Spec ID      | Parameter      | Description                        | Min | Typ | Max | Unit | Details/conditions |
|--------------|----------------|------------------------------------|-----|-----|-----|------|--------------------|
| SID.VDD700.2 | V_VDD700UVRISE | Undervoltage rising threshold      | 90  | 100 | 115 | V    | —                  |
| SID.VDD700.3 | V_VDD700UVFALL | Undervoltage falling threshold     | 81  | 90  | 110 |      | —                  |
| SID.VDD700.4 | V_VDD700OVRISE | Overvoltage rising threshold       | 400 | 430 | 490 |      | —                  |
| SID.VDD700.5 | V_VDD700OVFALL | Overvoltage falling threshold      | 395 | 420 | 480 |      | —                  |
| SID.VDD700.6 | T_VDD700UVDB   | Debounce time undervoltage falling | —   | 30  | —   | ms   | —                  |

**Table 6 Overvoltage on AUXIN**

| Spec ID      | Parameter    | Description                                              | Min | Typ | Max  | Unit | Details/conditions |
|--------------|--------------|----------------------------------------------------------|-----|-----|------|------|--------------------|
| SID.OVPAUX.1 | V_OVPAUXRISE | Overvoltage threshold on OVP_AUX                         | 1.1 | 1.2 | 1.26 | V    | —                  |
| SID.OVPAUX.3 | T_OVPAUXBLK  | Blanking time on OVP_AUX when GD output goes high to low | 0.9 | 1.1 | 1.3  | μs   | —                  |

**Table 7 Gate driver**

| Spec ID  | Parameter | Description                                 | Min | Typ | Max | Unit | Details/conditions              |
|----------|-----------|---------------------------------------------|-----|-----|-----|------|---------------------------------|
| SID.GD.1 | V_GDVOL   | GD Low Level Output voltage                 | —   | 1   | 2   | V    | AUXIN = 12 V and sinking 200 mA |
| SID.GD.2 | V_GDVOH   | GD High Level Output voltage                | 8   | 10  | —   |      |                                 |
| SID.GD.3 | T_GDTR    | Rise time                                   | —   | 25  | 60  | ns   | CL = 1 nF, AUXIN = 12 V         |
| SID.GD.4 | T_GDTF    | Fall time                                   | —   | 20  | 37  |      |                                 |
| SID.GD.5 | T_GDPDR   | Delay time from PULSEIN to GD, rising edge  | —   | 90  | 125 |      |                                 |
| SID.GD.6 | T_GDPDF   | Delay time from PULSEIN to GD, falling edge | —   | 70  | 100 |      |                                 |

**Table 8 Current sense fault protection**

| Spec ID  | Parameter | Description                      | Min | Typ | Max | Unit | Details/conditions |
|----------|-----------|----------------------------------|-----|-----|-----|------|--------------------|
| SID.CS.1 | V_CSTH1   | Threshold voltage pulse-by-pulse | 430 | 500 | 550 | mV   | —                  |
| SID.CS.3 | T_CSPD    | Delay time from CS to GD         | —   | —   | 160 | ns   | CL = 1 nF          |
| SID.CS.4 | T_CSLEB   | Leading edge blanking time       | 150 | 250 | 300 |      | —                  |

## Electrical specifications

**Table 9 PULSEIN**

| Spec ID       | Parameter       | Description                            | Min | Typ | Max | Unit | Details/conditions |
|---------------|-----------------|----------------------------------------|-----|-----|-----|------|--------------------|
| SID.PULSEIN.1 | V_PULSEINNEGAMP | Minimum negative going pulse amplitude | −4  | −2  | −   | V    | −                  |
| SID.PULSEIN.2 | V_PULSEINPOSAMP | Maximum positive going pulse amplitude | −   | 2   | 4   |      | −                  |
| SID.PULSEIN.3 | T_PULSEINPW     | Pulse Width                            | 25  | −   | 200 | ns   | −                  |

**Table 10 Free running oscillator**

| Spec ID   | Parameter | Description        | Min | Typ | Max | Unit | Details/conditions                                                             |
|-----------|-----------|--------------------|-----|-----|-----|------|--------------------------------------------------------------------------------|
| SID.OSC.1 | FOSC      | Frequency          | 27  | 30  | 38  | kHz  | $F_{OSC} = (I_{RTCURR}) * (1/5 \text{ pF}) * (1/4 \text{ V}) = 30 \text{ kHz}$ |
| SID.OSC.2 | DCMIN     | Minimum duty cycle | 3   | −   | −   | %    | −                                                                              |
| SID.OSC.3 | DCMAX     | Maximum duty cycle | −   | −   | 70  |      | −                                                                              |

**Table 11 Timing resistor**

| Spec ID  | Parameter | Description        | Min | Typ           | Max | Unit          | Details/conditions |
|----------|-----------|--------------------|-----|---------------|-----|---------------|--------------------|
| SID.RT.1 | RT        | Timing resistor    | −   | $499 \pm 1\%$ | −   | k $\Omega$    | −                  |
| SID.RT.2 | I_RTCURR  | Current through RT | −   | $2.4 \pm 5\%$ | −   | $\mu\text{A}$ | −                  |

**Table 12 Auto-restart time**

| Spec ID  | Parameter | Description       | Min | Typ | Max | Unit        | Details/conditions |
|----------|-----------|-------------------|-----|-----|-----|-------------|--------------------|
| SID.AR.1 | TAR       | Auto-restart time | −   | 2   | −   | Seco<br>nds | −                  |

**Table 13 Soft-start capacitor charging current**

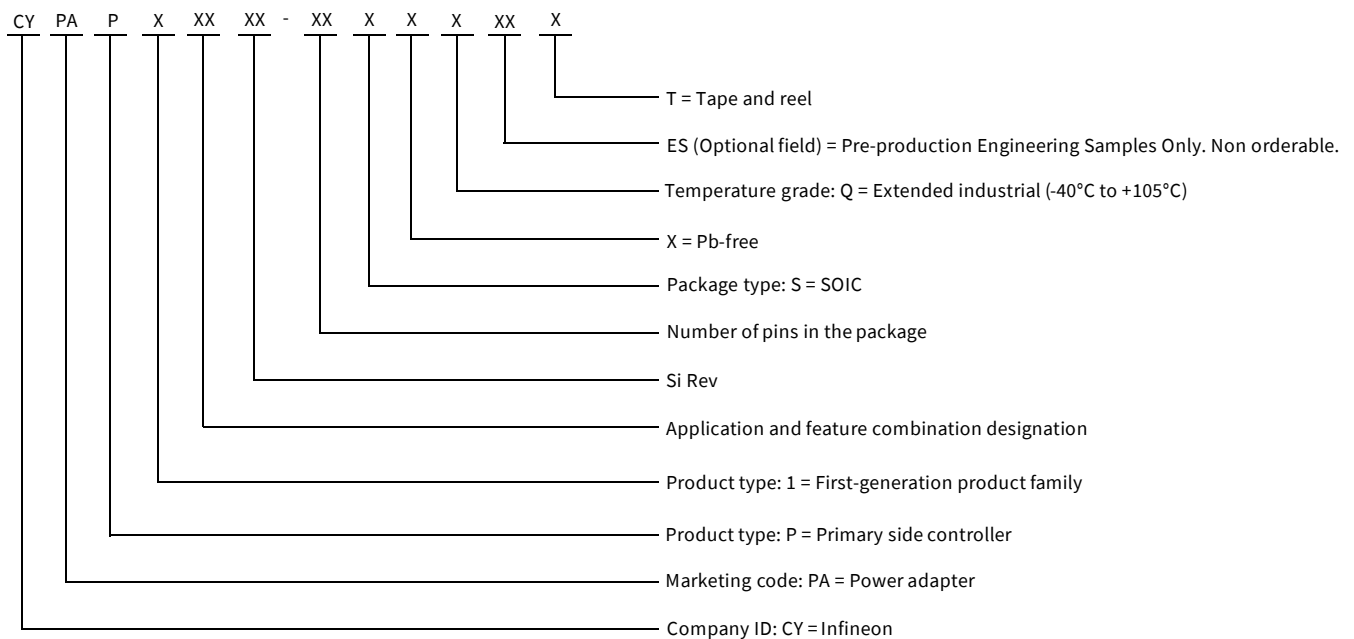
| Spec ID  | Parameter | Description                               | Min | Typ | Max | Unit          | Details/conditions                                                                                         |
|----------|-----------|-------------------------------------------|-----|-----|-----|---------------|------------------------------------------------------------------------------------------------------------|
| SID.SS.1 | I_SSCURR  | Current for charging soft-start capacitor | −   | 4.8 | 6   | $\mu\text{A}$ | Soft-start time = $I/C \text{ V/s}$ ; Maximum soft-start voltage is 3.75 V and start of soft-start is 1 V. |

## 5 Ordering information

**Table 14** Ordering part number

| MPN               | Mode      | Package type | Silicon revision |
|-------------------|-----------|--------------|------------------|
| CYPAP111A3-10SXQ  | Non X-cap | 10-pin SOIC  | A3               |
| CYPAP111A3-10SXQT |           |              |                  |
| CYPAP112A3-10SXQ  | X-cap     |              |                  |
| CYPAP112A3-10SXQT |           |              |                  |

### 5.1 Ordering code definitions



6 Packaging

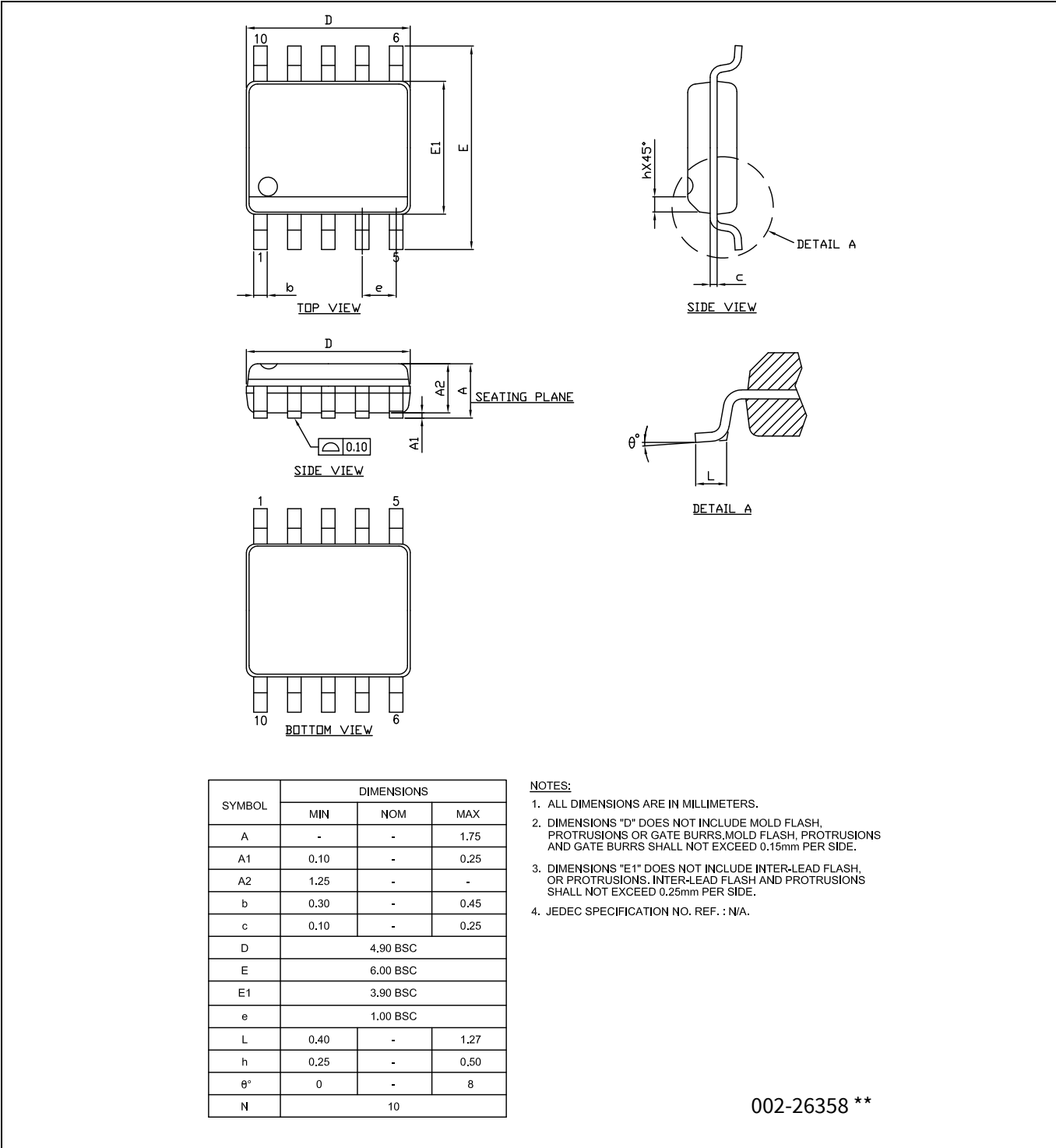


Figure 6 10-pin SOIC package outline

## Revision history

| Document version | Date of release | Description of changes                                                                                                                                                                     |
|------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *D               | 2019-12-10      | Changed datasheet status to final                                                                                                                                                          |
| *E               | 2020-06-18      | Updated SID.OSC.1 parameter min value from 24 to 27 and max value from 36 to 38 in <b>Table 10</b>                                                                                         |
| *F               | 2022-05-18      | Updated to Infineon template<br>Changed part numbers from CYPAP111A3-10SXQES and CYPAP112A3-10SXQES to CYPAP111A3-10SXQT and CYPAP112A3-10SXQT in <b>“Ordering information”</b> on page 14 |

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