

Off-Line Current Mode PWM Control Circuit with Very Low Start Up Current

Description

The CS-384XB provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components. The family has been optimized for very low start up current (300 μ A, typ).

The CS-384XB family incorporates a precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clamp eliminates the need for an external oscillator when a 50% duty-cycle is used. Duty-cycles of almost 100% are

possible. On board logic ensures that V_{REF} is stabilized before the output stage is enabled. Ion-implant resistors provide tighter control of undervoltage lockout.

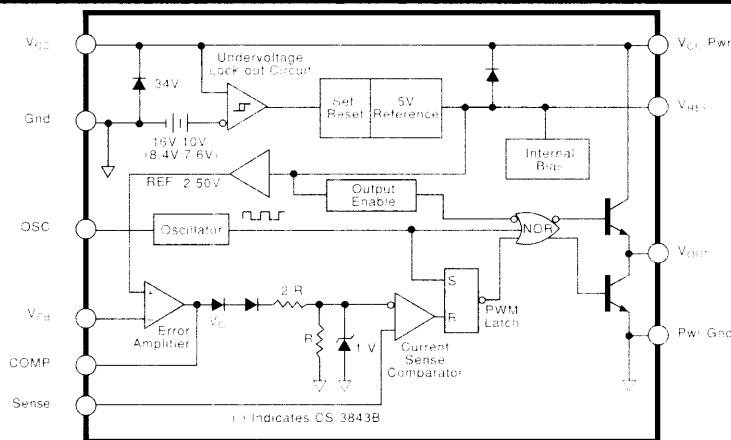
Other features include pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as the gate of a power MOSFET. The output is LOW in the off state, consistent with N-channel devices.

These ICs are available in 8 and 14 lead surface mount (SO) and 8 lead PDIP packages.

Absolute Maximum Ratings

Supply Voltage ($I_{CC} < 30$ mA)	Self Limiting
Supply Voltage (Low Impedance Source)	30V
Output Current	± 1 A
Output Energy (Capacitive Load)	5 μ J
Analog Inputs (V_{FB} , Sense)	-0.3V to 5.5V
Error Amp Output Sink Current	10mA
Lead Temperature Soldering	
Wave Solder (through hole styles only)	10 sec. max, 260°C peak
Reflow (SMD styles only)	60 sec. max above 183°C, 230°C peak

Block Diagram

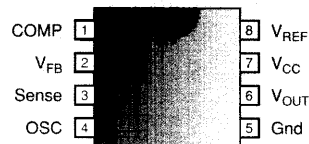


Features

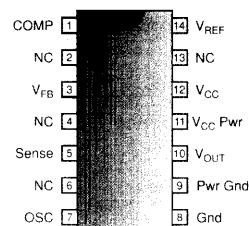
- Very low Start Up Current (300 μ A typ)
- Optimized Off-line Control
- Internally Trimmed, Temperature Compensated Oscillator
- Maximum Duty-cycle Clamp
- V_{REF} stabilization before Output Enable
- Pulse-by-pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1% Trimmed Bandgap Reference
- High Current Totem Pole Output

Package Options

8 Lead PDIP & SO Narrow



14L SO Narrow



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■ Reference Section

Output Voltage	$T_J=25^{\circ}\text{C}$, $I_{\text{OUT}}=1\text{mA}$	4.90	5.00	5.10	V
Load Regulation	$1\leq I_{\text{OUT}}\leq 20\text{mA}$		6	25	mV
Total Output Variation	Line, Load, Temperature (Note 2)	4.82		5.18	V
Long Term Stability	$T_A=125^{\circ}\text{C}$, 1kHrs. (Note 2)		5	25	mV

■ Oscillator Section

Initial Accuracy	Sawtooth Mode (see Fig. 3), $T_J=25^{\circ}\text{C}$	47	52	57	kHz
	Triangular Mode (see Fig. 3), $T_J=25^{\circ}\text{C}$	44	52	60	kHz
Temp. Stability	Sawtooth Mode $T_{\text{MIN}}\leq T_A\leq T_{\text{MAX}}$ (Note 2)		5		%
	Triangular Mode $T_{\text{MIN}}\leq T_A\leq T_{\text{MAX}}$ (Note 2)		8		%
	Discharge Current		12		V
Discharge Current	$T_J=25^{\circ}\text{C}$	7.5	8.3	9.3	mA
	$T_{\text{MIN}}\leq T_A\leq T_{\text{MAX}}$	7.2		9.5	mA

■ Error Amp Section

Input Voltage	$V_{\text{COMP}}=2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current			-13	-20	nA
A_{VOL}	$2\leq V_{\text{OUT}}\leq 4\text{V}$	65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1.0		MHz
PSRR	$12\leq V_{\text{CC}}\leq 25\text{V}$	60	70		dB
Output Sink Current	$V_{\text{FB}}=2.7\text{V}$, $R_L=15\text{k}\Omega$ to V_{REF}	2	4		mA
Output Source Current	$V_{\text{FB}}=2.3\text{V}$, $V_{\text{OSC}}=5\text{V}$	-0.5	-0.8		mA
$V_{\text{OUT High}}$	$V_{\text{FB}}=2.3\text{V}$, $R_L=15\text{k}\Omega$ to ground	5	6		V
$V_{\text{OUT Low}}$	$V_{\text{FB}}=2.7\text{V}$, $R_L=15\text{k}\Omega$ to V_{REF}		0.7	1.1	V

■ Current Sense Section

Gain	(Notes 3 & 4)	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_{\text{OUT}}=5\text{V}$ (Note 3)	0.9	1.0	1.1	V
PSRR	$12\leq V_{\text{CC}}\leq 25\text{V}$ (Note 3)		70		dB
Input Bias Current			-2	-10	nA
Delay to Output	$T_J=25^{\circ}\text{C}$ (Note 2)		150	300	ns

■ Output Section

Output Low Level	$I_{\text{SINK}}=20\text{mA}$		0.1	0.4	V
	$I_{\text{SINK}}=200\text{mA}$		1.5	2.2	V
Output High Level	$I_{\text{SINK}}=20\text{mA}$	13.0	13.5		V
	$I_{\text{SINK}}=200\text{mA}$	12.0	12.5		V

■ Output Section: continued

Rise Time	$T_j=25^{\circ}\text{C}$, $C_L=1\text{nF}$ (Note 2)	50	150	ns
Fall Time	$T_j=25^{\circ}\text{C}$, $C_L=1\text{nF}$ (Note 2)	50	150	ns
Output Leakage	UVLO Active, $V_{OUT}=0$	-0.01	-10.00	μA

■ Total Standby Current

Start-Up Current		0.3	0.5	mA
Operating Supply Current	$V_{FB}=V_{sense}=0\text{V}$, $R_T=10\text{k}\Omega$, $C_T=3.3\mu\text{F}$	11	17	mA
V_{CC} Zener Voltage	$I_{CC}=25\text{mA}$	34		V

■ Under-Voltage Lockout Section

Start Threshold		14.5	16.0	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	8.5	10.0	11.5	7.0	7.6	8.2	V

Notes: 1. Adjust V_{CC} above the start threshold before setting at 15V.

2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with $V_{FB}=0$.

4. Gain defined as:

$$A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}}; 0 \leq V_{Sense} \leq 0.8V.$$

PACKAGE PIN		PIN SYMBOL	FUNCTION
8L PDIP/SO	14L SO Narrow		
1	1	COMP	Error amp output, used to compensate error amplifier
2	3	V_{FB}	Error amp inverting input
3	5	Sense	Noninverting input to Current Sense Comparator
4	7	COMP	Output of the current sense comparator, connected to V_{FB}
5	8	Gnd	Ground
	9	Pwr Gnd	Output driver Ground
6	10	V_{OUT}	Output drive pin
	11	V_{CC} Pwr	Output driver positive supply
7	12	V_{CC}	Positive power supply
8	14	V_{REF}	Output of 5V internal reference
	2,4,6,13	NC	No Connection

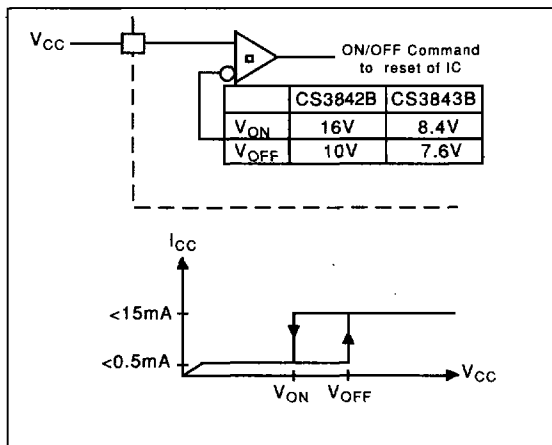
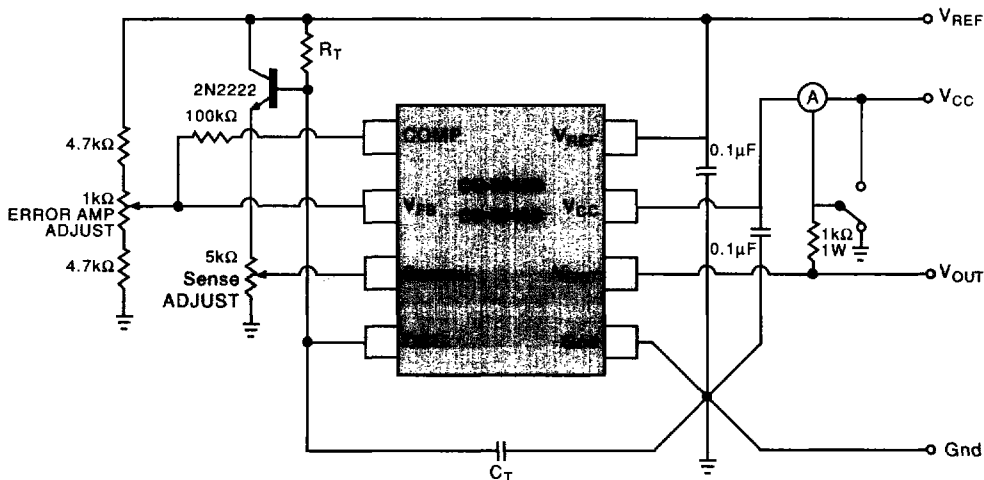
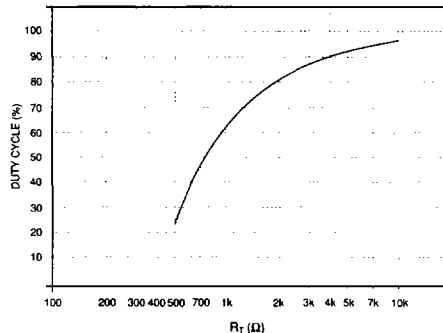
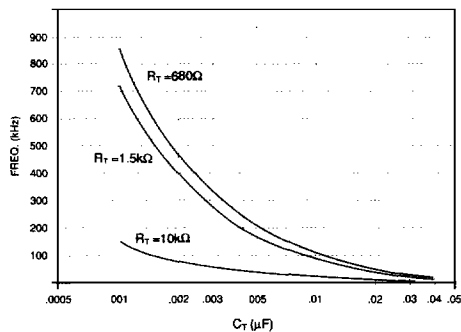


Figure 1: Typical Undervoltage Characteristics

Undervoltage Lockout

During Undervoltage Lockout (Figure 1), the output driver is biased to a high impedance state. V_{OUT} should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 2). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty

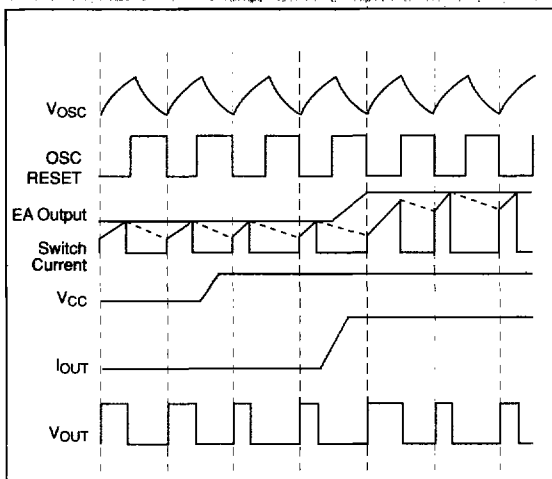


Figure 2: Timing Diagram for key CS-384XB parameters

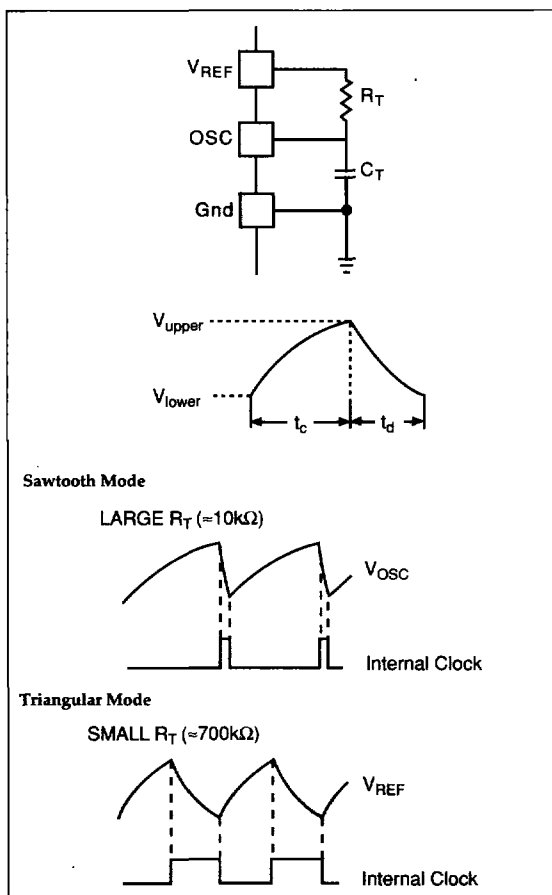


Figure 3: Oscillator Timing Network and parameters

cycle tends to exceed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of oscillator timing components.

Setting the Oscillator

The oscillator timing capacitor, C_T , is charged by V_{REF} through R_T and discharged by an internal current source (Figure 3). During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp.

Charge and discharge times are determined by the general formulas:

$$t_c = R_T C_T \ln \left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}} \right)$$

$$t_d = R_T C_T \ln \left(\frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}} \right)$$

Substituting in typical values for the parameters in the above formulas:

$V_{REF} = 5.0V$, $V_{upper} = 2.7V$, $V_{lower} = 1.0V$, $I_d = 8.3A$, then

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln \left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

The frequency and maximum duty cycle can be determined from the Typical Performance Characteristics graphs.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to ground in a single point ground.

The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

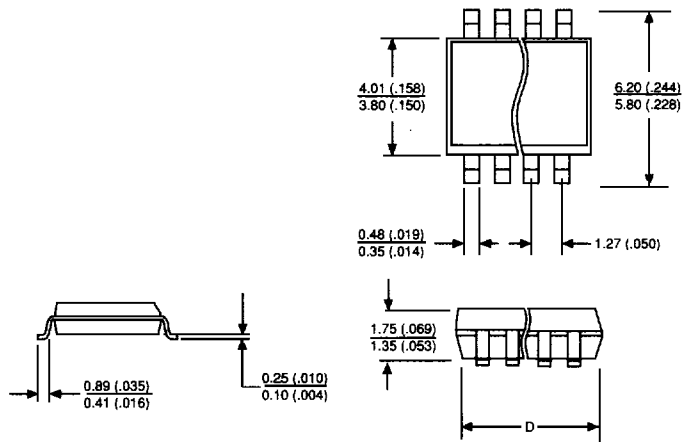
PACKAGE DIMENSIONS (CONTINUATION)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead PDIP	9.40	9.14	.370	.360
8 Lead SO Narrow	5.00	4.80	.197	.188
14L SO Narrow	8.74	8.53	.344	.336

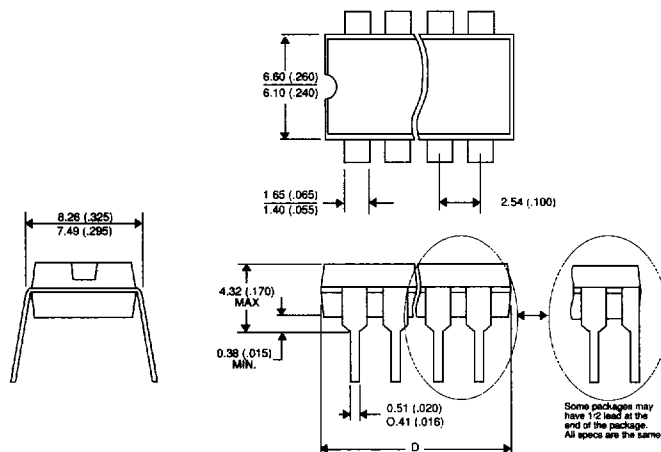
PACKAGE THERMAL DATA

Thermal Data		8 Lead PDIP	8L SO Narrow	14 L SO Narrow	
$R\theta_{JC}$	typ	52	45	30	°C/W
$R\theta_{JA}$	typ	100	165	125	°C/W

8L SO Narrow



8 Lead PDIP



Ordering Information

Part Number	Description
CS-3842BN8	8L PDIP
CS-3842BD8	8L SO Narrow
CS-3842BD14	14L SO Narrow
CS-3843BN8	8L PDIP
CS-3843BD8	8L SO Narrow
CS-3843BD14	14L SO Narrow

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.