

DS1776 PI-Bus Transceiver

General Description

The DS1776 is an octal PI-bus Transceiver. The A to B path is latched. B outputs are open collector with series Schottky diode, ensuring minimum B output loading. B outputs also have ramped rise and fall times (2.5 ns typical), ensuring minimum PI-bus ringing. B inputs have glitch rejection circuitry, 4 ns typical.

Designed using National's Bi-CMOS process for both low operating and disabled power. AC performance is optimized for the PI-Bus inter-operability requirements.

The DS1776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. This bus has a loaded characteristic impedance range of 20Ω to 50Ω and is terminated on each end with a 30Ω to 40Ω resistor.

The DS1776 is an octal bidirectional transceiver with open collector B and TRI-STATE® A port output drivers. A latch function is provided for the A port signals. The B port output

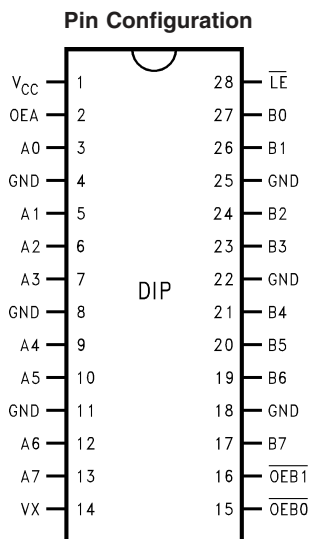
driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

A separate high level control voltage (V_X) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, V_X is tied to V_{CC} .

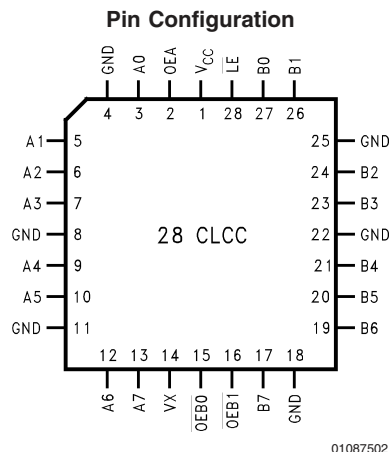
Features

- Mil-Std-883C qualified
- Similar to BTL
- Low power $I_{CCL} = 41$ mA max
- B output controlled ramp rate
- B input noise immunity, typically 4 ns
- Available in 28-pin DIP, Flatpak and CLCC
- Pin and function compatible with Signetics 54F776

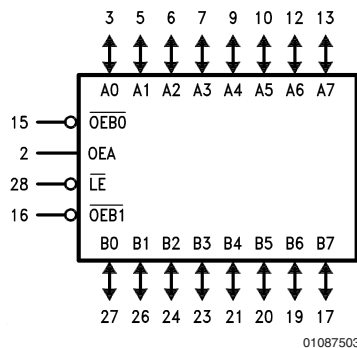
Pin Configurations



Order Number DS1776E/883 or DS1776J/883
See NS Package E28A or J28B



Logic Symbol



MIL-STD-883C**Device Specifications****Absolute Maximum Ratings** (Note 1),

(Note 2)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage (V_{CC})	–0.5V to +7.0V
V_X , V_{OH} Output Level Control Voltage (A Outputs)	–0.5V to +7.0V
$\overline{OEB}$ n, $\overline{OEA}$, $\overline{LE}$ Input Voltage (V_I)	–0.5V to +7.0V
A0–A7, B0–B7 Input Voltage (V_I)	–0.5V to +5.5V
Input Current (I_I)	–40 mA to +5 mA
Voltage Applied to Output in	

High Output State (V_O)	–0.5V to + V_{CC} V
A0–A7 Current Applied to Output in Low Output State (I_O)	40 mA
B0–B7 Current Applied to Output in Low Output State (I_O)	200 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Lead Temperature (Soldering 10 Sec.)	260°C
ESD Tolerance: $C_{ZAP} = 120$ pF, $R_{ZAP} = 1500\Omega$	0.5 kV

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temp. Range (T_A)	–55	+125	°C
Input Rise or Fall Times (t_r , t_f)		50	ns

PI Bus Transceiver DS1776**DC Electrical Characteristics**

$V_{CC} = 5V \pm 10\%$ (Unless Otherwise Specified) DC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = –55°C

Symbol	Parameter		Conditions (Notes 3, 5)		Temp. Group	Min	Typ (Note 4)	Max	Units
V_{IH}	High Level Input Voltage	Except Bn Bn			1, 2, 3	2 1.6			V V
V_{IL}	Low Level Input Voltage	Except Bn Bn			1, 2, 3			0.8 1.45	V V
I_{OH}	High Level Output Current	An	$V_{IN} = V_{IH}$ $V_{OH} = V_{CC} - 2.0V$		1, 2, 3			–3	mA
		Bn	$V_{CC} = \text{Max}$, $\overline{OEA} = \overline{LE}$ $V_{IH} = 2.0V$, $V_{OH} = 2.1V$					100	μA
I_{OL}	Low Level Output Current	An	$V_{IN} = V_{IL}$ $V_{OL} = 0.5V$		1, 2, 3			20	mA
		Bn	$V_{OL} = 1.15V$					100	mA
I_{IK}	Input Clamp Current	Except An			1, 2, 3			–18	mA
		An						–40	mA
I_{OZ}	TRI-STATE Output Leakage Current	An Bn			1, 2, 3			± 70	μA
V_{OH}	High Level Output Voltage	An	$V_{CC} = \text{Min}$, $V_{IH} = 1.9V$	$I_{OH} = -3$ mA $V_X = V_{CC}$	1, 2, 3	2.5		V_{CC}	V
				$I_{OH} = -0.4$ mA $V_X = 3.13V$ to 3.47V		2.5		V_X	V
V_{OL}	Low Output Level Voltage	An	$V_{CC} = \text{Min}$, $V_{IL} = 1.2V$	$I_{OL} = 20$ mA, $V_X = V_{CC}$				0.5	V
		Bn	$V_{CC} = \text{Min}$, $V_{IL} = 0.8V$	$I_{OL} = 100$ mA $I_{OL} = 4$ mA	1, 2, 3		0.4	1.15	V
V_{IK}	Input Clamp Voltage	An	$V_{CC} = \text{Min}$, $I_I = -40$ mA		1, 2, 3			–0.5	V
		Except An	$V_{CC} = \text{Min}$, $I_I = -18$ mA					–1.2	V
I_{IH2}	Input Current	$\overline{OEBn}$, $\overline{OEA}$, $\overline{LE}$	$V_{CC} = \text{Min}$, $V_I = 7.0V$		1, 2, 3		1	100	μA

DC Electrical Characteristics (Continued)
 $V_{CC} = 5V \pm 10\%$ (Unless Otherwise Specified) DC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = -55°C

Symbol	Parameter		Conditions (Notes 3, 5)	Temp. Group	Min	Typ (Note 4)	Max	Units
	at Max Input Voltage	An	$V_{CC} = \text{Min}, V_I = 5.5V$			0.01	1	mA
		Bn	$V_{CC} = \text{Min}, V_I = 5.5V$			0.01	1	mA
I_{IH1}	Input Current at Max Input Voltage	$\overline{OE}B, OEA, \overline{LE}$ B0–B7	$V_{CC} = \text{Max}, V_I = 2.7V$ $V_{CC} = \text{Max}, V_I = 2.1V$				20 100	μA μA
I_{IL}	Low Level Input Current	$\overline{OE}B, OEA, \overline{LE}$	$V_{CC} = \text{Max}, V_I = 0.5V$	2, 3	-40			μA
				1	-20			μA
		Bn	$V_{CC} = \text{Max}, V_I = 0.3V$	1, 2, 3	-100			μA
I_{OZH} + I_{IH}	TRI-STATE Output Current, High Level Voltage Applied	An	$V_{CC} = \text{Max}, V_O = 2.7V$	1, 2, 3			70	μA
I_{OZH} + I_{IL}	TRI-STATE Output Current, Low Level Voltage Applied	An	$V_{CC} = \text{Max}, V_O = 0.5V$	1, 2, 3	-70			μA
I_X	High Level Control Current		$V_{CC} = \text{Max}, V_X = V_{CC},$ $\overline{LE} = OEA = \overline{OEBn} = 2.7V$ An=2.7V, Bn=2.0V	1, 2, 3	-100		100	μA
			$V_{CC} = \text{Max}, V_X = 3.14V \text{ \& } 3.47V,$ $\overline{LE} = OEA = \overline{OEBn} = 2.7V,$ An=2.7V, Bn=2.0V	1, 2, 3	-10		10	mA
I_{OS}	Short-Circuit Output Current (Note 6)	An	$V_{CC} = \text{Max}, Bn = 1.9V,$ $OEA = 2.0V, \overline{OEBn} = 2.7V$	1, 2, 3	-60	-75	-150	mA
I_{CC}	Supply Current	I_{CCH}	$V_{CC} = \text{Max}, V_{IH} (A) = 5.0V$	1, 2			37	mA
		I_{CCH}		3			41	mA
		I_{CCL}	$V_{CC} = \text{Max}, V_{IL} (A) = 0.3V$	1, 2, 3			38	mA
		I_{CCZ}	$V_{CC} = \text{Max}, V_{IL} (A) = 0.3V$	1, 2, 3			35	mA
I_{OFF}	Power Off Output Current		Bn=2.1V, $V_{CC} = 0.0V,$ $V_{IL} = \text{Max}$ or $V_{IH} = \text{Min}$	1, 2, 3			100	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.

Note 4: All typical values are at $V_{CC} = 5V, T_A = 25^\circ C$.

Note 5: Due to test equipment limitations, actual test conditions are for $V_{IH} = 1.9V$ and for $V_{IL} = 1.2V$, however the specified test limits and conditions are guaranteed.

Note 6: Not more than one output should be shorted at a time. For testing I_{OS} the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test I_{OS} test should be performed last.

Note 7: Not more than one output should be shorted at a time. For testing I_{OS} , the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC Electrical Characteristics

$V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) AC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = -55°C

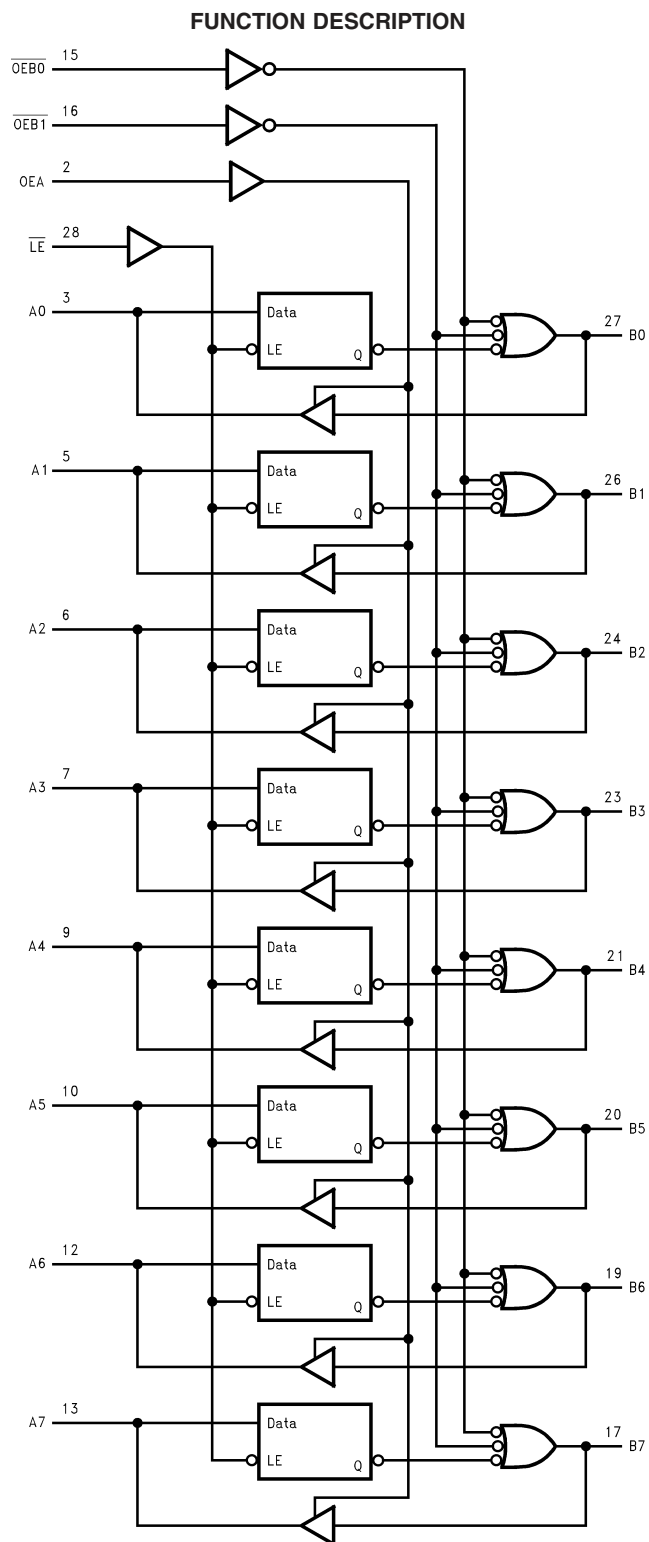
Path	Parameter	Conditions	Temp. Group	Min	Max	Units
B-TO-A PATH						
t _{PLH}	Propagation Delay B to A	Waveform 1, 2	1, 2, 3	4.5	17	ns
t _{PHL}				6	17	ns
t _{PZH}	Output Enable OEA to A	Waveform 3, 4	1, 2, 3	4	17	ns
t _{PZL}				4	17	ns
t _{PHZ}	Output Disable OEA to A	Waveform 3, 4	1, 2, 3	2	12	ns
t _{PLZ}				2	13	ns
A-TO-B PATH						
t _{PLH}	Propagation Delay A to B	Waveform 1, 2	1, 3	2	13	ns
			2	2	17	ns
t _{PHL}			1, 2, 3	2.5	13	ns
t _{PLH}	Propagation Delay $\overline{LE}$ to B	Waveform 1, 2	1, 3	2	16	ns
			2	2	22	ns
t _{PHL}			1, 2, 3	2	16	ns
t _{PLH}	Enable/Disable $\overline{OEBn}$ to B	Waveform 1, 2	1, 3	2	13	ns
			2	2	16	ns
t _{PHL}			1	3.5	14	ns
			2	3.5	13	ns
			3	3.5	16	ns
t _{TLH}			Transition Time, B Side	1.3V to 1.7V	1, 3	0.5
	2	0.5		10	ns	
t _{THL}	1.7V to 1.3V	1		0.5	5.5	ns
	2	0.5		7	ns	
	3	0.5		10	ns	
SETUP/HOLD/PULSE WIDTH SPECS						
t _S	A to $\overline{LE}$ Setup	Waveform 5	1, 2, 3	7		ns
t _H	A to $\overline{LE}$ Hold	Waveform 5	1, 2, 3	0		ns
t _W	$\overline{LE}$ Pulse Width Low	Waveform 5	1, 2, 3	12		ns

Descriptions

TABLE 1. Pin Description

Symbol	Pins	Type	Name and Function
A0	3	I/O	TTL Level, latched input/TRI-STATE output (with V_X control option)
A1	5	I/O	
A2	6	I/O	
A3	7	I/O	
A4	9	I/O	
A5	10	I/O	
A6	12	I/O	
A7	13	I/O	
B0	27	I/O	Data input with special threshold circuitry to reject noise/Open Collector output, High current drive
B1	26	I/O	
B2	24	I/O	
B3	23	I/O	
B4	21	I/O	
B5	20	I/O	
B6	19	I/O	
B7	17	I/O	
$\overline{OEB} 0$	15	I	Enables the B outputs when both pins are low
$\overline{OEB} 1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

Descriptions (Continued)



01087504

V_{CC} = Pin 1
 V_X = Pin 14
 GND = Pins 4, 8, 11, 18, 22, 25

FIGURE 1. Functional Logic Diagram

Descriptions (Continued)

TABLE 2. Function Table

Inputs						Latch State	Outputs		Mode
An	Bn (Note 8)	$\overline{LE}$	OEA	$\overline{OEB}$ 0	$\overline{OEB}$ 1		An	Bn	
H	X	L	L	L	L	H	Z	H	A TRI-STATE, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A TRI-STATE, Latched Data to B
—	—	L	H	L	L	(Note 10)	(Note 8)	(Note 8)	Feedback: A to B, B to A
—	H	H	H	L	L	H (Note 9)	H	off (Note 9)	Preconditioned Latch Enabling Data Transfer from B to A
—	L	H	H	L	L	H (Note 9)	L	off (Note 9)	
—	—	H	H	L	L	Qn	Qn	Qn	Latch State to A and B
H	X	L	L	H	X	H	Z	off	B off and A TRI-STATE
L	X	L	L	H	X	L	Z	off	
X	X	H	L	H	X	Qn	Z	off	
—	H	L	H	H	X	H	H	off	B off, Data from B to A
—	L	L	H	H	X	L	L	off	
—	H	H	H	H	X	Qn	H	off	
—	L	H	H	H	X	Qn	L	off	
H	X	L	L	X	H	H	Z	off	B off and A TRI-STATE
L	X	L	L	X	H	L	Z	off	
X	X	H	L	X	H	Qn	Z	off	
—	H	L	H	X	H	H	H	off	B off, Data from B to A
—	L	L	H	X	H	L	L	off	
—	H	H	H	X	H	Qn	H	off	
—	L	H	H	X	H	Qn	L	off	

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

— = Input not externally driven

Z = High Impedance (off) state

Qn = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition**Note 8:** Condition will cause a feedback loop path; A to B and B to A.**Note 9:** The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}$ 0 and $\overline{OEB}$ 1, are Low and $\overline{LE}$ is high.**Note 10:** Precaution should be taken to ensure that the B inputs do not float. If they do, they are equal to a Low state.**Note 11:** off = Applies to "B" (OC) outputs only. Indicates that the outputs are turned off.

CONTROLLER POWER SEQUENCING OPERATION

The DS1776 has a design feature which controls the output transitions during power up (or down). There are two possible conditions that occur.

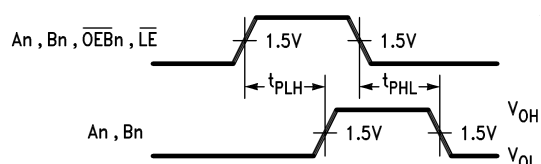
1. When $\overline{LE}$ = Low and $\overline{OEB}$ n = Low, the B outputs are disabled until the $\overline{LE}$ circuit can take control. This feature

ensures that the B outputs will follow the A inputs and allow only one transition during power up (or down).

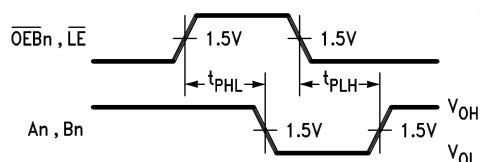
2. If $\overline{LE}$ = High or $\overline{OEB}$ n = High, then the B outputs still remain disabled during power up (or down).

Switching Characteristics

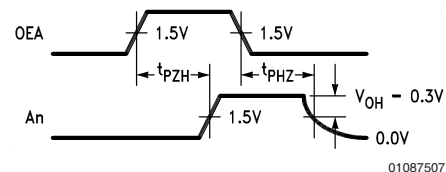
AC WAVEFORMS



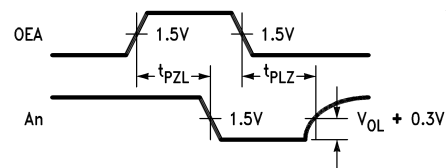
Waveform 1: Propagation Delay for Data to Output



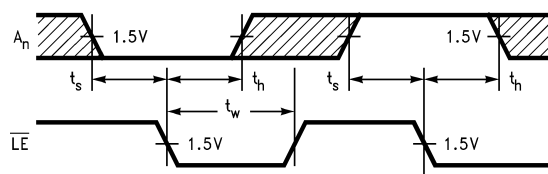
Waveform 2: Propagation Delay for Data to Output



Waveform 3: TRI-STATE Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4: TRI-STATE Output Enable Time to Low Level and Output Disable Time from Low Level

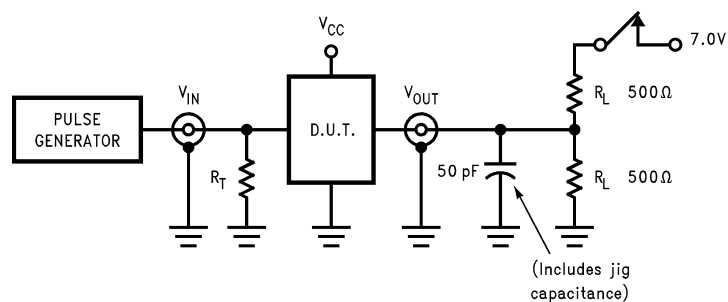


The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5: Data Setup and Hold Times and LE Pulse Widths

TEST CIRCUIT AND WAVEFORMS

Test Circuit for TRI-STATE Outputs on A Side



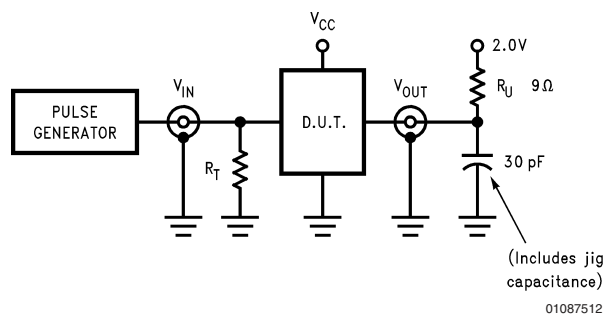
01087510

Switch Position

Test	Switch
t_{PLZ} , t_{PZL}	Closed
All Other	Open

Switching Characteristics (Continued)

Test Circuit for TRI-STATE Outputs on B Side



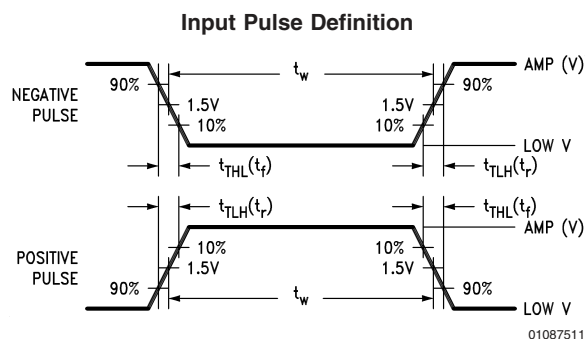
DEFINITIONS

R_L = Load resistor 500Ω

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

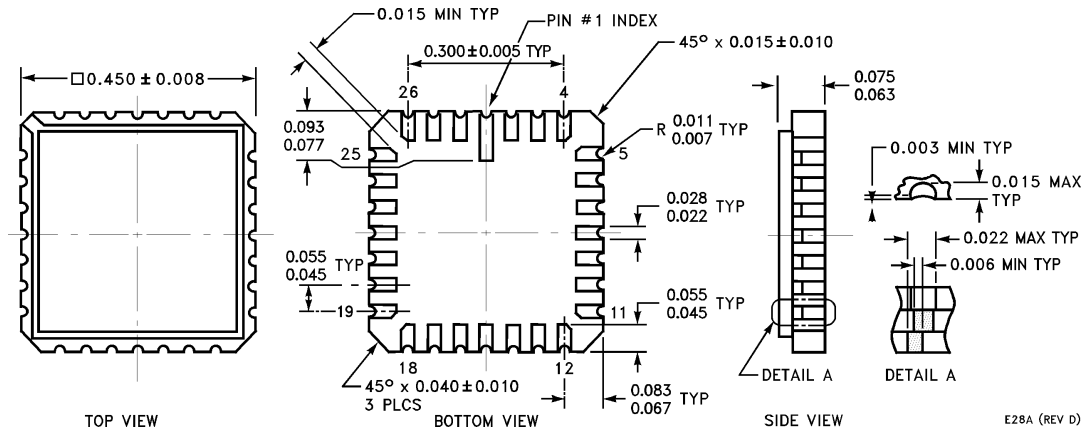
R_U = Pull up resistor



	Input Pulse Characteristics					
	Amplitude	Low V	Rep. Rate	t _w	t _{TLH}	t _{THL}
A Side	3.0V	0.0V	1 MHz	500 ns	2 ns	2 ns
B Side	2.0V	1.0V	1 MHz	500 ns	2 ns	2 ns

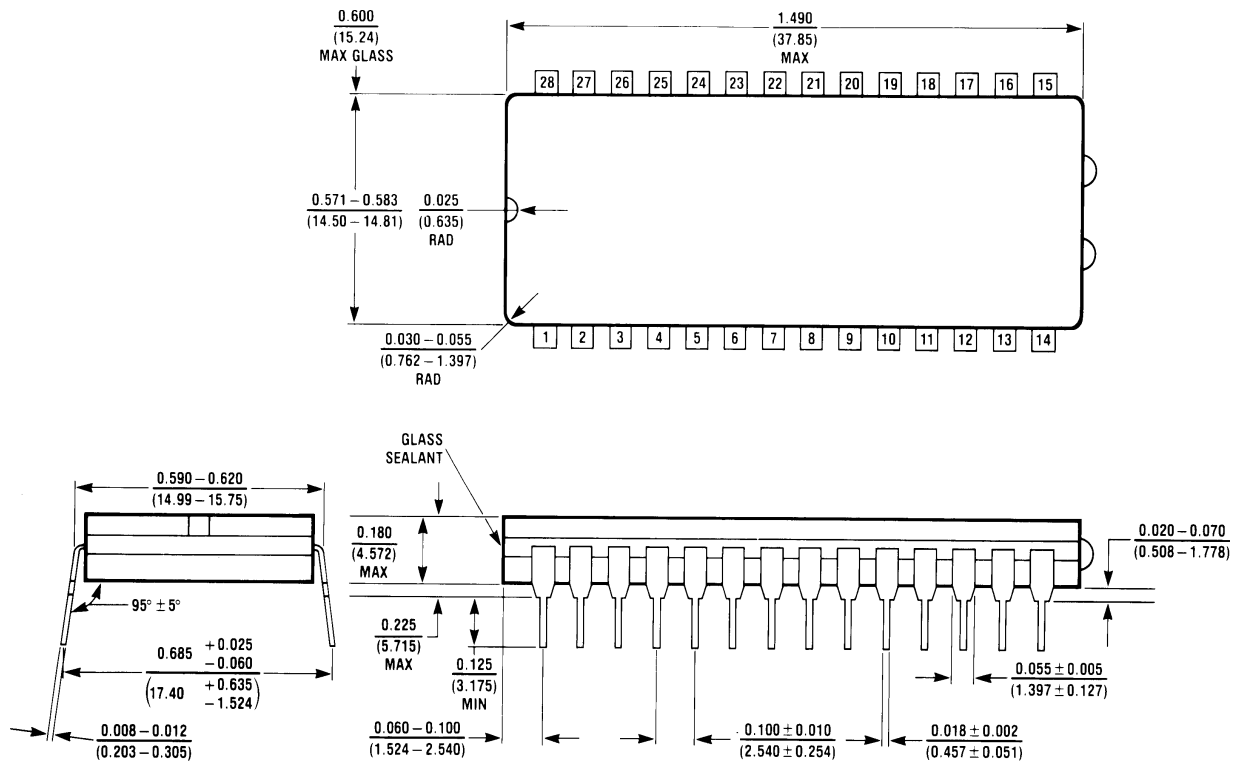
Physical Dimensions inches (millimeters)

unless otherwise noted



28-Lead Leadless Chip Carrier (E)
Order Number DS1776E/883
NS Package Number E28A

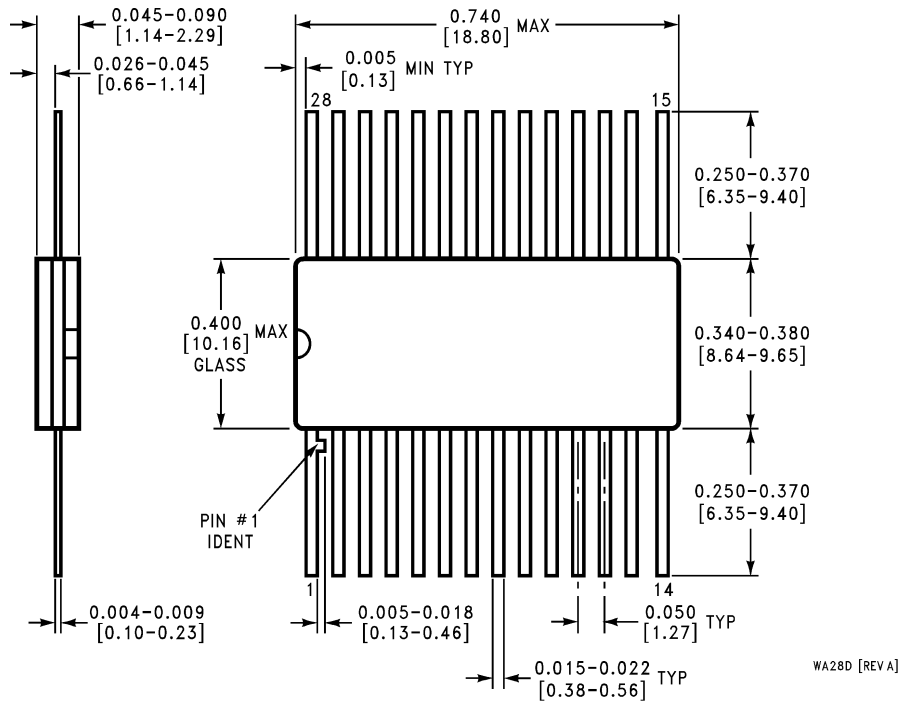
E28A (REV D)



28-Lead Ceramic Dual-In-Line Package (J)
Order Number DS1776J/883
NS Package Number J28B

J28B (REV C)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Ceramic Flatpak (F)
Order Number DS1776W/883
NS Package Number WA28D

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



National Semiconductor
Americas Customer
Support Center
 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
 Fax: +49 (0) 180-530 85 86
 Email: europa.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +44 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
 Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
 Fax: 81-3-5639-7507
 Email: jpn.feedback@nsc.com
 Tel: 81-3-5639-7560