

CONNECTION DIAGRAM
PINOUT A

54LS/74LS353 016167

DUAL 4-INPUT MULTIPLEXER

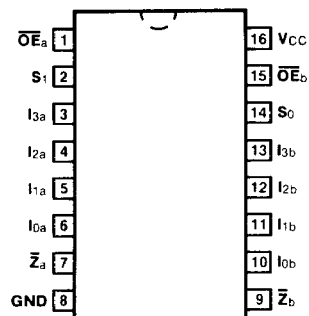
(With 3-State Outputs)

DESCRIPTION — The '353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **INVERTED VERSION OF 'LS253**
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**

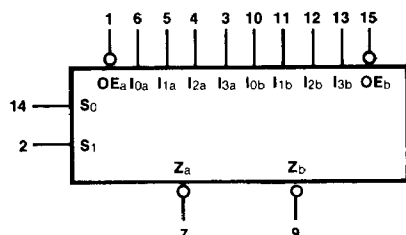
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS353PC		9B
Ceramic DIP (D)	A	74LS353DC	54LS353DM	6B
Flatpak (F)	A	74LS353FC	54LS353FM	4L



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$I_{0a} - I_{3a}$	Side A Data Inputs	0.5/0.25
$I_{0b} - I_{3b}$	Side B Data Inputs	0.5/0.25
S_0, S_1	Common Select Inputs	0.5/0.25
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.25
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.25
$\overline{Z}_a, \overline{Z}_b$	3-State Outputs (Inverted)	65/15 (25)/(7.5)

LOGIC SYMBOL


$V_{CC} = \text{Pin 16}$
 $GND = \text{Pin 8}$

FUNCTIONAL DESCRIPTION — The '353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.

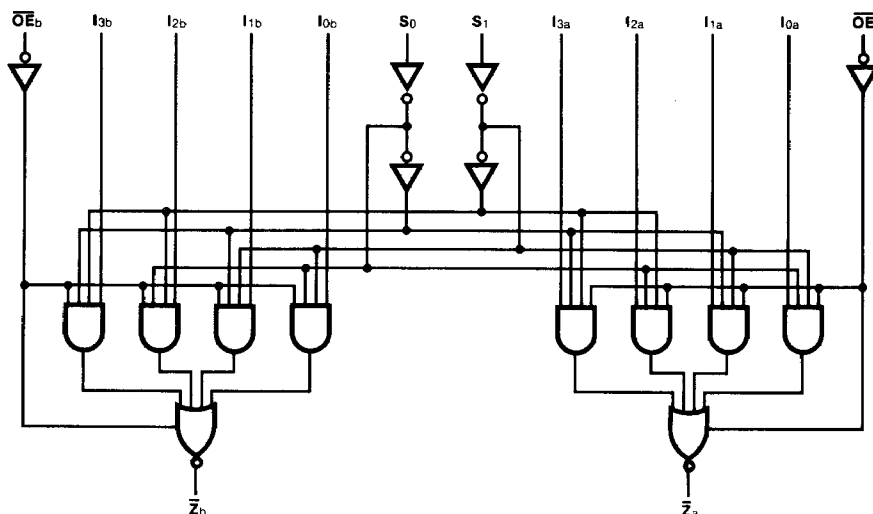
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

(Z) = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			Min	Max		
I _{CC}	Power Supply Current	Outputs HIGH		12	mA	V _{CC} = Max I _n , S _n , $\overline{O\bar{E}_n}$ = Gnd
		Outputs OFF		14		V _{CC} = Max, $\overline{O\bar{E}_n}$ = 4.5 V I _n , S _n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		CL = 45 pF			
		Min	Max		
tPLH tPHL	Propagation Delay Sn to Z̄n		24 32	ns	Figs. 3-1, 3-20
tPLH tPHL	Propagation Delay In to Z̄n		15 15	ns	Figs. 3-1, 3-4
tPZH tPZL	Output Enable Time		18 18	ns	Figs. 3-3, 3-11, 3-12 RL = 667Ω
tPHZ tPLZ	Output Disable Time		18 18	ns	Figs. 3-3, 3-11, 3-12 RL = 667Ω, CL = 5 pF