REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - ro	01-04-19	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

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DRAWING APPROVAL DATE
91-07-10

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, OPERATIONAL AMPLIFIER, LOW NOISE, PRECISION,

MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89627**

SHEET 1 OF 11

DSCC FORM 2233
APR 97

5962-E371-01

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Slew rate
01	HA-5127	Operational amplifier	7 V/µs minimum
02	HA-5137	Operational amplifier	14 V/µs minimum
03	HA-5147	Operational amplifier	28 V/µs minimum

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage between $+V_S$ and $-V_S$ terminals ..... 44 V dc
Differential input voltage ..... 0.7 V dc 1/
Voltage at either input terminal ..... $+V_S$ to $-V_S$
Input current ..... 25 mA
Differential output current ..... Short circuit protected
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +275°C
Junction temperature (T_J) ..... +175°C
Maximum power dissipation (P_D):
  Case G ..... 1.02 W 2/
  Case P ..... 1.22 W 2/
  Case 2 ..... 1.19 W 2/
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):
  Case G ..... 98°C/W
  Case P ..... 92°C/W
  Case 2 ..... 84°C/W

1/ For differential input voltages greater than 0.7 V, the input current must be limited to 25 mA to protect the back-to-back input diodes.

2/ Derate linearly above T_A = +75°C as follows: case G = 10.2 mW/°C, case P = 12.2 mW/°C, and case 2 = 11.9 mW/°C.

1.4 Recommended operating conditions.

Positive supply voltage range ($+V_S$) ..... +15 V dc
Negative supply voltage range ($-V_S$) ..... –15 V dc
Common mode input voltage (V_{CM}) ..... $\leq (+V_S - -V_S) / 2$
Load resistance (R_L) ..... 600 Ω
Ambient temperature range(T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	V_{CM} = 0.0 V	1	All		±100	µV
			2,3			±300	
Input bias current	I_B	V_{CM} = 0.0 V	1	All		±80	nA
			2,3			±150	
Input offset current	I_{IO}	V_{CM} = 0.0 V , $+R_S$ = 10 kΩ,	1	All		±75	nA
		$-R_S$ = 10 kΩ	2,3			±135	
Common mode range	+CMR	$+V_S$ = 4.7 V, $-V_S$ = -25.3 V	1,2,3	All	10.3		V
	-CMR	$+V_S$ = 25.3 V, $-V_S$ = -4.7 V			-10.3		
Large signal voltage gain	$+A_{VOL}$	V_{OUT} = 0.0 V and 10 V,	4	All	700		kV/V
		R_L = 2.0 kΩ	5,6		300		
	$-A_{VOL}$	V_{OUT} = 0.0 V and -10 V,	4		700		
		R_L = 2.0 kΩ	5,6		300		
Common mode rejection ratio	+CMRR	ΔV_{CM} = 11	1	All	100		dB
		ΔV_{CM} = 10	2,3		100		
	-CMRR	ΔV_{CM} = -11	1		100		
		ΔV_{CM} = -10	2,3		100		
Output voltage swing	$+V_{OUT1}$	R_L = 2.0 kΩ	4,5,6	All	11.5		V
	$-V_{OUT1}$	R_L = 10 kΩ			-11.5		
	$+V_{OUT2}$	R_L = 600 Ω	4		10		
	$-V_{OUT2}$	R_L = 600 Ω			-10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio	+PSRR	$\Delta\pm V_S$ = 14 V	1	All	86		dB
		$\Delta\pm V_S$ = 13.5 V	2,3		86		
	-PSRR	$\Delta\pm V_S$ = 14 V	1		86		
		$\Delta\pm V_S$ = 13.5 V	2,3		86		
Output current	$+I_{OUT}$	V_{OUT} = -10 V, T_A = +25°C	4	All	16.5		mA
	$-I_{OUT}$	V_{OUT} = 10 V, T_A = +25°C			-16.5		
Quiescent power supply current	$+I_{CC}$	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	All		4.0	mA
	$-I_{CC}$					-4.0	
Offset voltage adjustment	$+V_{IO}$ (adj)	2/	1,2,3	All	V_{IO} -1.0		mV
	$-V_{IO}$ (adj)				V_{IO} +1.0		
Slew rate 2/	+SR	V_{OUT} = -3.0 V to +3.0 V, R_L = 2.0 kΩ	7	01	7.0		V/µs
			8 3/		7.0		
		V_{OUT} = -4.0 V to +4.0 V, R_L = 2.0 kΩ	7	02	14		
			8 3/		14		
			7	03	28		
			8 3/		28		
	-SR	V_{OUT} = +3.0 V to -3.0 V, R_L = 2.0 kΩ	7	01	7.0		
			8 3/		7.0		
		V_{OUT} = +4.0 V to -4.0 V, R_L = 2.0 kΩ	7	02	14		
			8 3/		14		
			7	03	28		
			8 3/		28		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Rise time 4/	t_r	V_{OUT} = 0.0 mV to +200 mV, R_L = 2.0 kΩ, T_A = +25°C	7	01		150	ns
				02		100	
				03		50	
Fall time 4/	t_f	V_{OUT} = 0.0 mV to -200 mV, R_L = 2.0 kΩ, T_A = +25°C	7	01		150	ns
				02		100	
				03		50	
Overshoot 2/	+OS	V_{OUT} = 0.0 mV to 200 mV, R_L = 2.0 kΩ, T_A = +25°C	7	All		40	%
	-OS	V_{OUT} = 0.0 mV to –200 mV, R_L = 2.0 kΩ, T_A = +25°C				40	
Average offset voltage 3/ drift	$\Delta V_{IO}/\Delta t$	V_{CM} = 0.0 V	1,2,3	All		1.9	µV/°C
Differential input 3/ resistance	R_{IN}	V_{CM} = 0.0 V, R_L = 2.0 kΩ, T_A = +25°C	4	All	0.8		MΩ
Low frequency 3/ peak-to-peak noise	E_{np-p}	0.1 Hz to 10 Hz, R_L = 2.0 kΩ, T_A = +25°C	4	All		0.25	μV_{P-P}
Input noise voltage 3/ density	E_n	R_S = 20 Ω, f_O = 10 Hz, R_L = 2.0 kΩ, T_A = +25°C	4	All		8.0	nV / $\sqrt{Hz}$
		R_S = 20 Ω, f_O = 1.0 kHz, R_L = 2.0 kΩ, T_A = +25°C				6.5	
Input noise current 3/ density	I_n	R_S = 2.0 MΩ, f_O = 10 Hz, R_L = 2.0 kΩ, T_A = +25°C	4	All		5.0	pA / $\sqrt{Hz}$
		R_S = 2.0 MΩ, f_O = 1.0 kHz, R_L = 2.0 kΩ, T_A = +25°C				0.8	
Unity gain bandwidth 3/	UGBW	V_{OUT} = 100 mV, R_L = 2.0 kΩ, T_A = +25°C	4	01	5.0		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain bandwidth 3/ product	GBWP	V_{OUT} = 100 mV, R_L = 2.0 kΩ, f = 50 kHz, T_A = +25°C	4	02	60		MHz
				03	120		
		V_{OUT} = 100 mV, R_L = 2.0 kΩ, f = 1.0 MHz, T_A = +25°C		02	45		
				03	100		
Full power 3/ 5/ bandwidth	FPBW	V_{PK} = 10 V, R_L = 2.0 kΩ, T_A = +25°C	4	01	111		kHz
				02	220		
				03	445		
Settling time 3/	t_S	To 0.1 % for a 10 V step, R_L = 2.0 kΩ, T_A = +25°C	9	01		2.0	µs
				02		1.5	
				03		600	
Output resistance 3/	R_{OUT}	Open loop, T_A = +25°C	4	All		100	Ω
Quiescent power 6/ consumption	P_C	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	All		120	mW

1/ Unless otherwise specified, $+V_S$ = +15 V, $-V_S$ = -15 V, R_S = 50 Ω, R_L = 100 kΩ, C_L = 50 pF, and V_{OUT} = 0.0 V.

2/ Offset adjustment range is V_{IO} (measured) ±1.0 mV minimum referred to output. This test is for functionality only to assure adjustment through 0.0 V.

3/ If not tested, shall be guaranteed to the limits specified in table I herein.

4/ Measured between 10 % and 90 % points.

5/ Full power bandwidth = SR / ($2\pi \times V_{PK}$).

6/ Quiescent power consumption based on quiescent supply current test maximum (no load outputs).

Device types	01,02,03	
Case outlines	G and P	2
Terminal number	Terminal symbol	
1	BALANCE	NC
2	-INPUT	BALANCE
3	+INPUT	NC
4	$-V_S$	NC
5	NC	-INPUT
6	OUTPUT	NC
7	$+V_S$	+INPUT
8	BALANCE	NC
9	---	NC
10	---	$-V_S$
11	---	NC
12	---	NC
13	---	NC
14	---	NC
15	---	OUTPUT
16	---	NC
17	---	$+V_S$
18	---	NC
19	---	NC
20	---	BALANCE

NC = No connection

FIGURE 1. Terminal connections.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,4,5,6,7
Group A test requirements (method 5005)	1,2,3,4,5,6,7,8**,9**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 8 and 9, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 10 and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-04-19

Approved sources of supply for SMD 5962-89627 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8962701GC	3/	HA2-5127/883
5962-8962701PA	34371	HA7-5127/883
5962-89627012A	3/	HA4-5127/883
5962-8962702GC	3/	HA2-5137/883
5962-8962702PA	3/	HA7-5137/883
5962-89627022A	3/	HA4-5137/883
5962-8962703GC	34371	HA2-5147/883
5962-8962703PA	34371	HA7-5147/883
5962-89627032A	34371	HA4-5147/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation P.O. Box 883 Melbourne, FL 32902-0883