ecoSwitch™ Advanced Load Management

Controlled Load Switch with Reverse Current Protection and Low R_{ON}

NCP45760

The NCP45760 load management device provides a component and area−reducing solution for efficient power domain switching with inrush current limit via soft start. This device is designed to integrate control and driver functionality with back−to−back high performance low on−resistance power MOSFETs in a single package. This cost effective solution is ideal for reverse current applications and the specific power management and disconnect functions used in USB Type−C and Type−C Power Delivery ports.

Features

- Advanced Controller with Charge Pump
- Integrated N−Channel MOSFET with Low R_{ON}
- Soft−Start via Controlled Slew Rate
- Adjustable Slew Rate Control
- Fault Detection with Power Good Output
- Thermal Shutdown and Under Voltage Lockout
- Short−Circuit and Adjustable Over−Current Protections
- Reverse−current Protection
- Input Voltage Range 3 V to 24 V
- Extremely Low Standby Current
- This is a Pb−free, RoHS/REACH Compliant Device

Typical Applications

- USB Type C Power Delivery
- Reverse Current Load Switching Applications
- Servers, Set−Top Boxes and Gateways
- Notebook and Tablet Computers
- Telecom, Networking, Medical and Industrial Equipment
- Hot−Swap Devices and Peripheral Ports

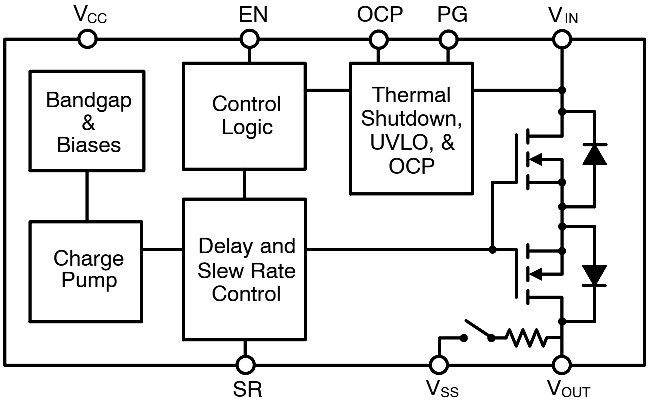

Figure 1. Block Diagram

ON Semiconductor®

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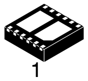
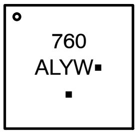
R_{ON} TYP	V_{IN}	*DC I_{MAX}
20 mΩ	3.0 V − 24 V	8.0 A

*I_{MAX} is defined as the maximum steady state current the load switch can pass at room ambient temperature without entering thermal lockout. See the SOA section for more information on transient current limitations.



DFN12, 3x3
CASE 506EN

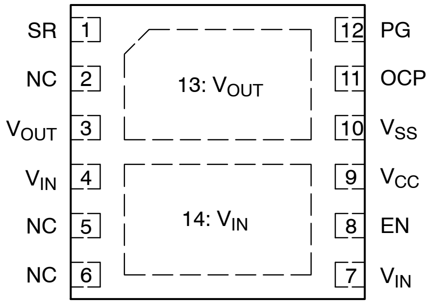
MARKING DIAGRAM



760 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP45760IMN24RTWG	DFN12	3000 / Tape & Reel

January, 2021 − Rev. 1

Publication Order Number:
NCP45760/D

Table 1. PIN DESCRIPTION

Pin	Name	Function
1	SR	Slew Rate control pin. Slew rate adjustment made with an external capacitor to GND; float if not used.
3,13	V_{OUT}	Source of MOSFET connected to load. – **Pin 13 should be used for high current (>0.5 A)**
4,7,14	V_{IN}	Input voltage (3 V – 24 V) – **Pin 14 should be used for high current (>0.5 A)**
8	EN	Active−high digital input used to turn on the MOSFET driver, pin has an internal pull down resistor to GND.
9	V_{CC}	Driver supply voltage (3.0 V – 5.5 V)
10	V_{SS}	Driver ground
11	OCP	Over−current protection trip point adjustment made with a voltage applied (0 V – 1.2 V), pin has an internal pull up resistor to EN; short to ground if over−current protection is not needed.
12	PG	Active−high, open−drain output that indicates when the gate of the MOSFET is fully charged, external pull up resistor ≥ 100 kΩ to an external voltage source required; tie to GND if not used.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 6	V
Input Voltage Range	V_{IN}	−0.3 to 30	V
Output Voltage Range	V_{OUT}	−0.3 to 30	V
EN Input Voltage Range	V_{EN}	GND−0.3 to (V_{CC} + 0.3)	V
PG Output Voltage Range (Note 1)	V_{PG}	−0.3 to 6	V
OCP Input Voltage Range	V_{OCP}	−0.3 to 6	V
Thermal Resistance, Junction−to−Ambient, Steady State (Note 2)	$R_{\theta JA}$	28.6	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)	$R_{\theta JC}$	1.7	°C/W
Continuous MOSFET Current @ T_A = 25°C (Note 2)	I_{MAX}	8	A
Total Power Dissipation @ T_A = 25°C (Note 2) Derate above T_A = 25°C	P_D	3.49 34.9	W mW/°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Notes 3 and 4)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Notes 3 and 4)	ESD_{CDM}	0.5	kV
Latch−up Current Immunity (Note 3)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. PG is an open drain output that requires an external pull−up resistor > 100 kΩ to an external voltage source.
2. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JS−001
   ESD Charged Device Model per ESD JS−002
   Latch−up Current tested per JESD78
   PG, OCP, and SR pins must be connected correctly for compliance.
4. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
VCC	V_{CC}	3	5.5	V
VIN	V_{IN}	3	24	V
OCP External Resistor to VSS	R_{OCP}	short	open	kΩ
OFF to ON Transition Energy Dissipation Limit (See application section)	E_{TRANS}		100	mJ
VSS	V_{SS}		0	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V − 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
On−Resistance	V_{CC} = 4.5 V, V_{IN} = 3 V	R_{ON}		20	23	mΩ
	V_{CC} = 3.3 V, V_{IN} = 4.5 V			20	23	
	V_{CC} = 3.3 V, V_{IN} = 15 V			20	23	
	V_{CC} = 3.3 V, V_{IN} = 24 V			20	23	
Leakage Current − V_{IN} to V_{OUT} (Note 5)	V_{EN} = 0 V, V_{IN} = 24 V, V_{CC} = 5.5 V	I_{LEAK}		21	100	nA
V_{IN} Control Current − V_{IN} to V_{SS}	V_{EN} = 0 V, V_{IN} = 24 V (for typical)	I_{INCTL}		0.83	2.0	μA
	V_{EN} = V_{CC}, V_{IN} = 24 V (for typical)	I_{INCTL_EN}		144	300	
Supply Standby Current (Note 6)	V_{EN} = 0 V, V_{IN} = 24 V (for typical)	I_{STBY}		1.55		μA
Supply Dynamic Current (Note 7)	V_{EN} = V_{CC}, V_{IN} = 24 V (for typical)	I_{DYN}		0.35	0.5	mA
EN Input High Voltage		V_{IH}	2			V
EN Input Low Voltage		V_{IL}			0.8	V
EN Input Leakage Current	V_{EN} = 0 V	I_{IL}	−1.0	0.01	1	μA
EN Pull Down Resistance		R_{PD}	76	100	124	kΩ
PG Output Low Voltage	I_{SINK} = 100 μA	V_{OL}		0.022	0.1	V
PG Output Leakage Current	V_{TERM} = 3.3 V	I_{OH}		3	100	nA
Slew Rate Control Constant (Note 8)		K_{SR}	70	100	130	μA

FAULT PROTECTIONS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Thermal Shutdown Threshold (Note 9)		T_{SDT}		145		°C
Thermal Shutdown Hysteresis (Note 9)		T_{HYS}		20		°C
V_{IN} Under Voltage Lockout Threshold	V_{IN} rising	V_{UVLO}		2		V
V_{IN} Under Voltage Lockout Hysteresis		V_{HYS}		200		mV
Over−Current Protection Trip	R_{OCP} = open	I_{TRIP}	0.55	0.853	1.15	A
	R_{OCP} = 100 kΩ			2.9		
	R_{OCP} = 32 kΩ			5.5		
	R_{OCP} = short to GND (Note 10)			8		
Over−Current Protection Blanking Time		t_{OCP}		2.25		ms
Short−Circuit Protection Trip Current	Soft & Hard Short (Note 11)	I_{SC}		12.5		A

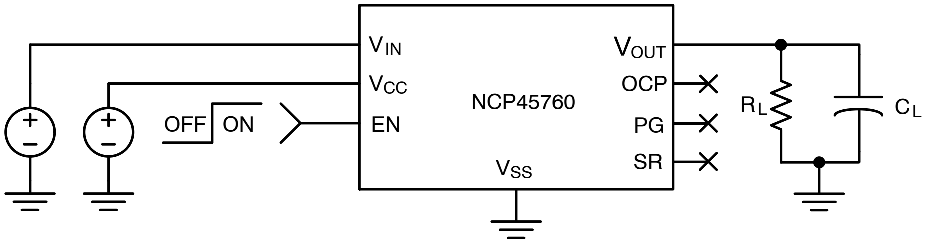
5. Average current from V_{IN} to V_{OUT} with MOSFET turned off.
6. Average current from V_{CC} to GND with MOSFET turned off.
7. Average current from V_{CC} to GND after charge up time of MOSFET.
8. See Applications Information section for details on how to adjust the gate slew rate.
9. Operation above T_J = 125°C is not guaranteed.
10. Transient currents exceeding the short−circuit protection trip current will cause the device to fault. For OCP setting less than 20 kΩ, high steady state current may cause an over temperature lockout before the OCP threshold is reached due to self−heating.
11. Short Circuit Protection protects the device against hard shorts ($R_{SHORT} \leq$ 250 mΩ V_{OUT} to Ground) for V_{IN} < 18 V, and against soft shorts (R_{SHORT} > 250 mΩ) for V_{IN} < 24V. Short circuit protection testing assumed a 100 W supply capability limit on V_{IN}.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Notes 12 and 13)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate – Default	V_{CC} = 4.5 V; V_{IN} = 3 V	SR	13	21.0	28	V/ms
	V_{CC} = 5.0 V; V_{IN} = 3 V		13	21.0	28	
	V_{CC} = 3.3 V; V_{IN} = 24 V		13	22.8	28	
	V_{CC} = 5.0 V; V_{IN} = 24 V		13	23.0	28	
Output Turn–on Delay	V_{CC} = 4.5 V; V_{IN} = 3 V	T_{ON}		175	700	μs
	V_{CC} = 5.0 V; V_{IN} = 3 V			165	700	
	V_{CC} = 3.3 V; V_{IN} = 24 V			185	700	
	V_{CC} = 5.0 V; V_{IN} = 24 V			175	700	
Output Turn–off Delay	V_{CC} = 4.5 V; V_{IN} = 3 V	T_{OFF}		60		μs
	V_{CC} = 5.0 V; V_{IN} = 3 V			60		
	V_{CC} = 3.3 V; V_{IN} = 24 V			40		
	V_{CC} = 5.0 V; V_{IN} = 24 V			40		
Power Good Turn–on Time	V_{CC} = 4.5 V; V_{IN} = 3 V	$T_{PG,ON}$	0.25	0.436	2.5	ms
	V_{CC} = 5.0 V; V_{IN} = 3 V		0.25	0.428	2.5	
	V_{CC} = 3.3 V; V_{IN} = 24 V		0.25	0.460	2.5	
	V_{CC} = 5.0 V; V_{IN} = 24 V		0.25	0.451	2.5	
Power Good Turn–off Time (Note 14)	V_{CC} = 4.5 V; V_{IN} = 3 V	$T_{PG,OFF}$			10	ns
	V_{CC} = 5.0 V; V_{IN} = 3 V				10	
	V_{CC} = 3.3 V; V_{IN} = 24 V				10	
	V_{CC} = 5.0 V; V_{IN} = 24 V				10	

12. See below figure for Test Circuit and Timing Diagram.
13. Tested with the following conditions: $V_{TERM} = V_{CC}$; R_{PG} = 100 kΩ; R_L = 10 Ω; C_L = 0.1 μF.
14. PG Turn–off time is dependent on external pull up resistor and capacitive loading. Tested with 100 kΩ pull up to 3.3 V.



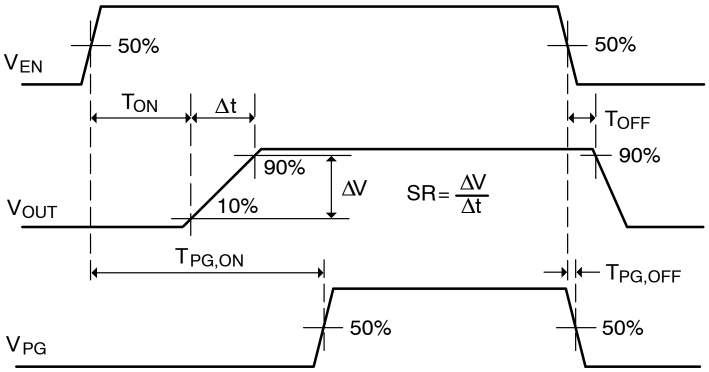


Figure 2. Switching Characteristics Test Circuit and Timing Diagrams

TYPICAL CHARACTERISTICS

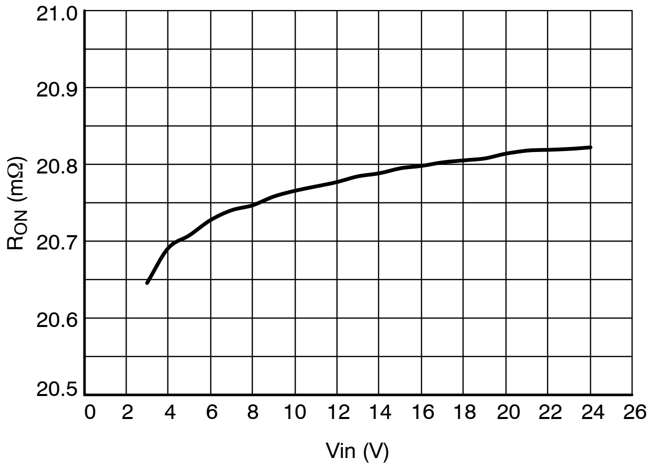


Figure 3. On−Resistance vs. Input Voltage

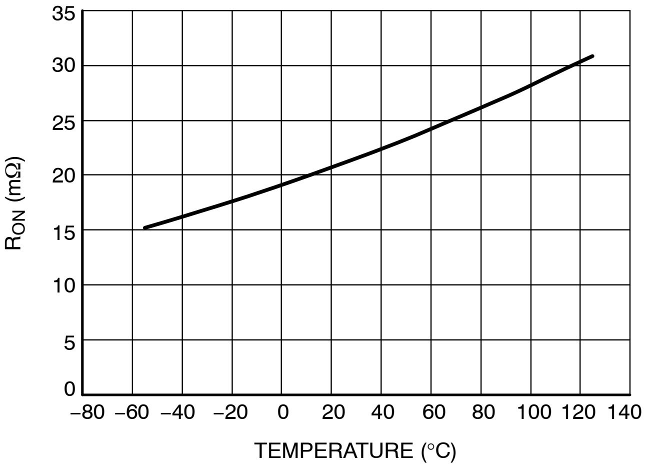


Figure 4. On−Resistance vs. Temperature

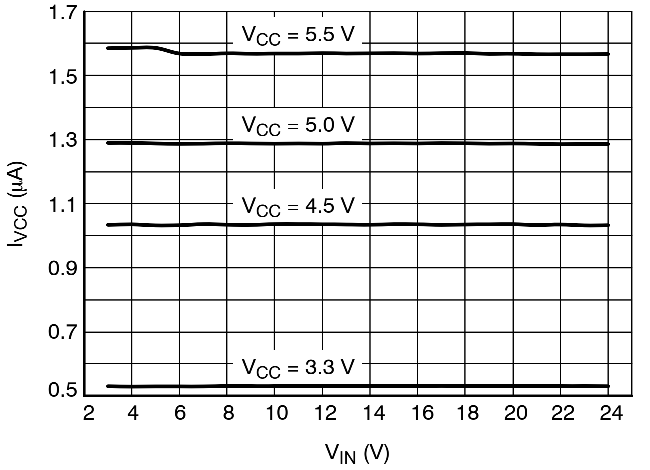


Figure 5. Supply Standby Current vs. V_{IN} Voltage

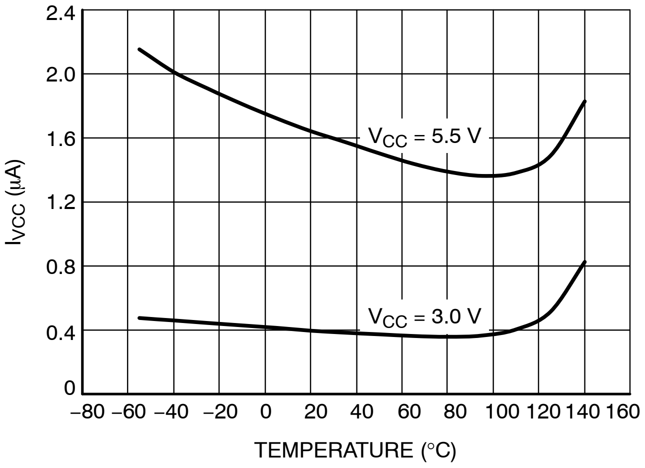


Figure 6. Supply Standby Current vs. Temperature

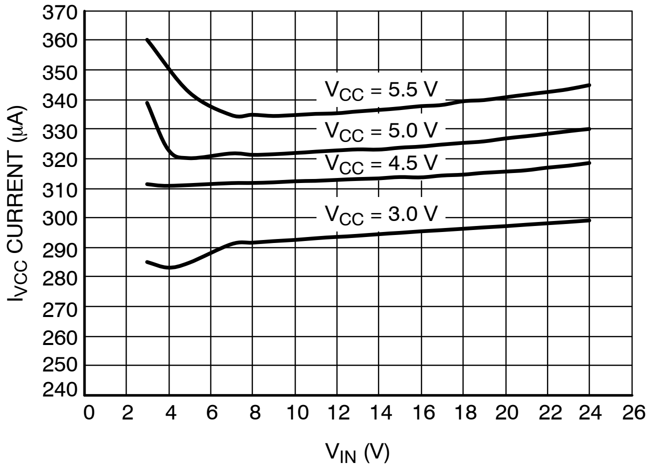


Figure 7. Dynamic Current vs. Input Voltage

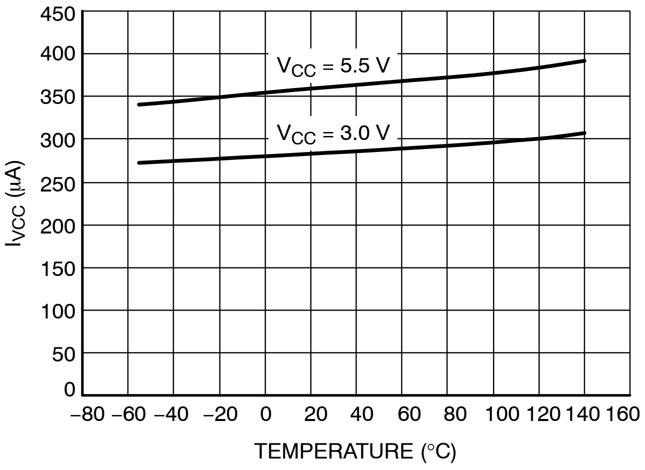


Figure 8. Supply Dynamic Current vs. Temperature

TYPICAL CHARACTERISTICS

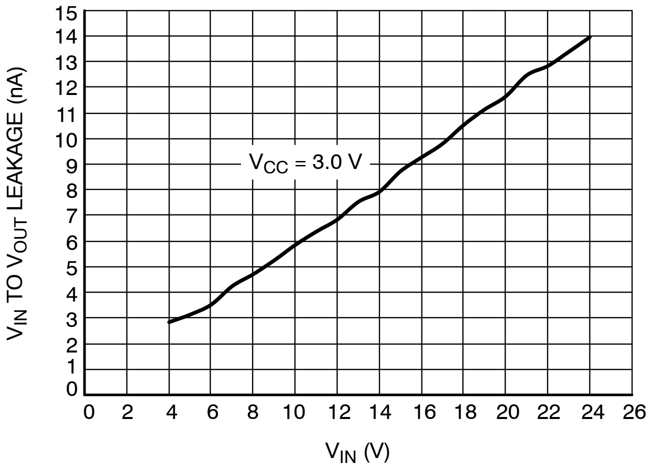


Figure 9. Input to Output Leakage vs. Input Voltage

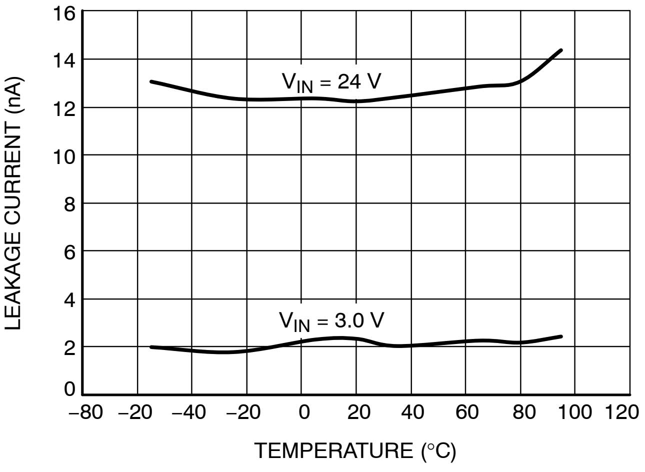


Figure 10. Input to Output Leakage vs. Temperature

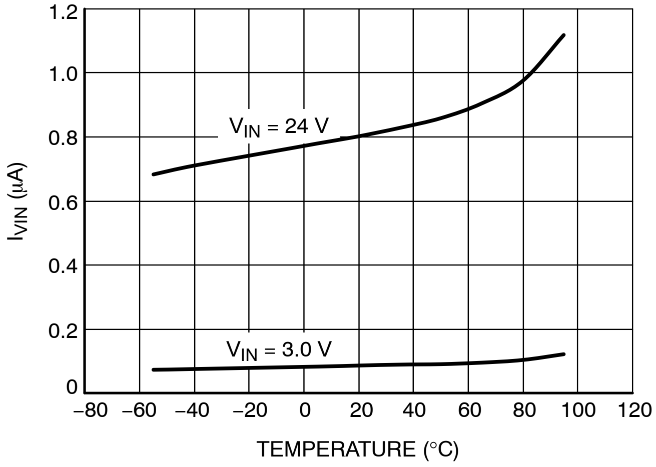


Figure 11. Vin Controller Current vs. Temperature (EN=0)

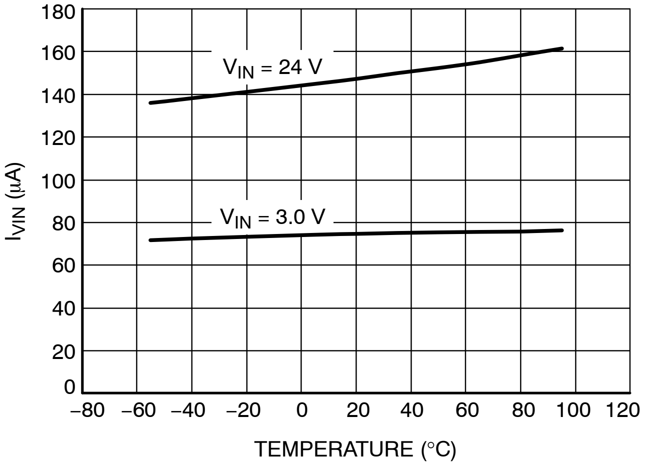


Figure 12. Vin Controller Current vs. Temperature (EN=HIGH)

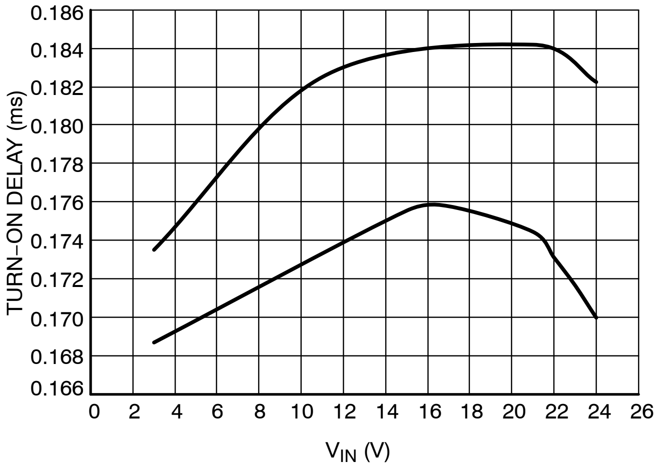


Figure 13. Output Turn−On Delay vs. Input Voltage

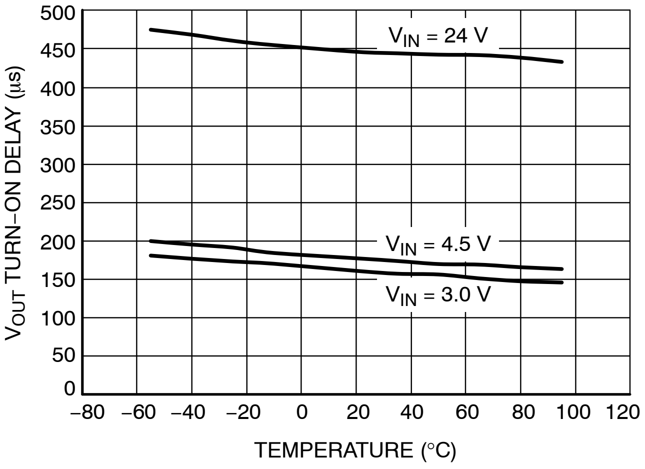


Figure 14. Output Turn−On Delay vs. Temperature

TYPICAL CHARACTERISTICS

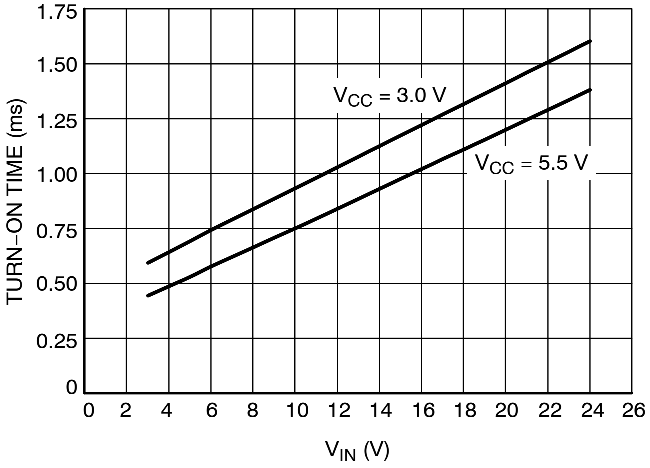


Figure 15. Power Good Turn−On Time vs. Input Voltage

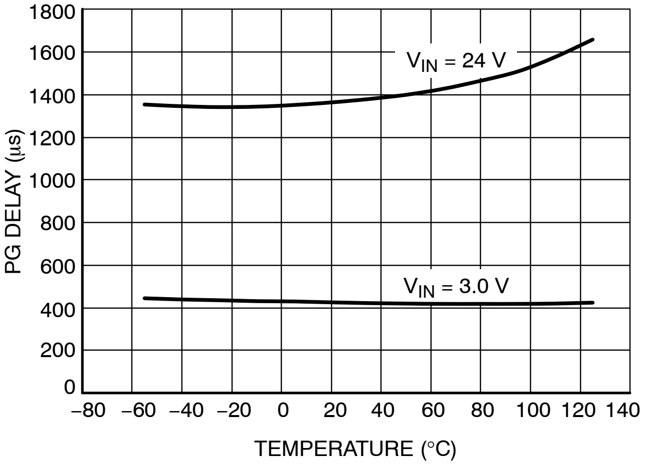


Figure 16. Power Good Turn−On vs. Temperature

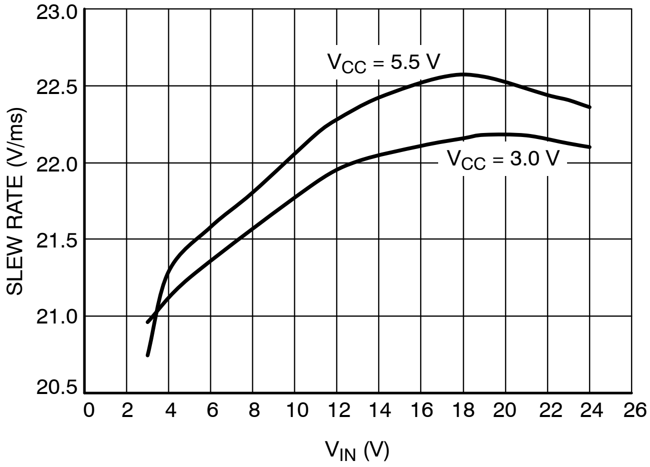


Figure 17. Default Slew Rate vs. Input Voltage

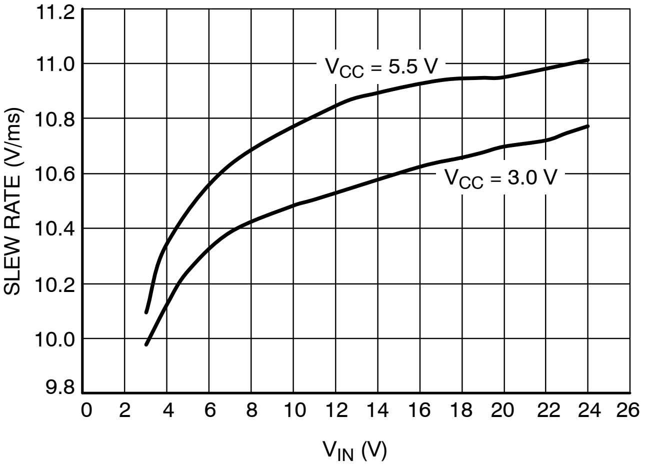


Figure 18. Slew Rate vs. Input Voltage (10 nF on SR pin to GND)

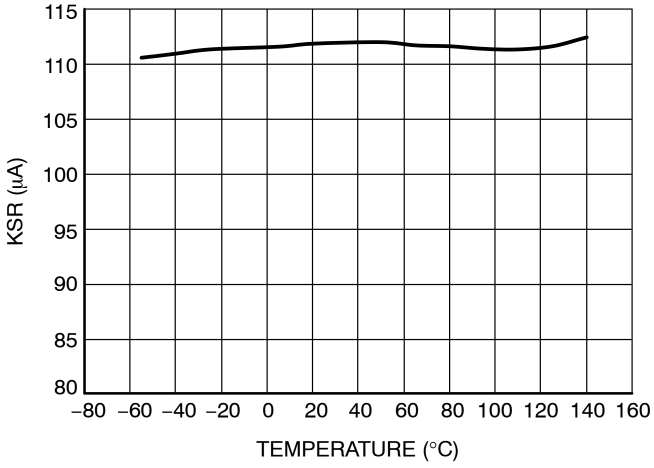


Figure 19. KSR vs. Temperature

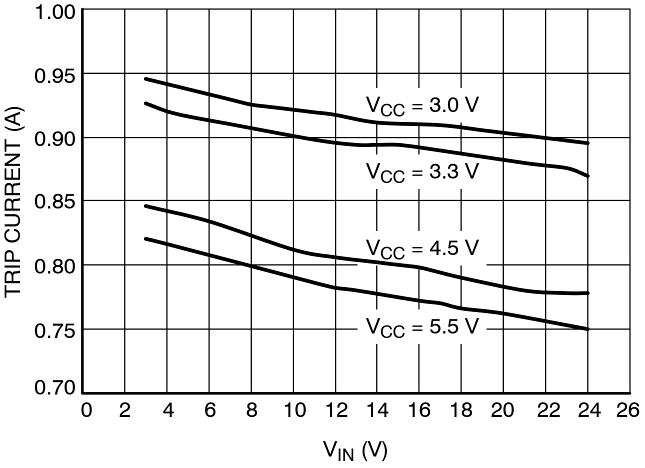


Figure 20. OCP Trip Current vs. Input Voltage

TYPICAL CHARACTERISTICS

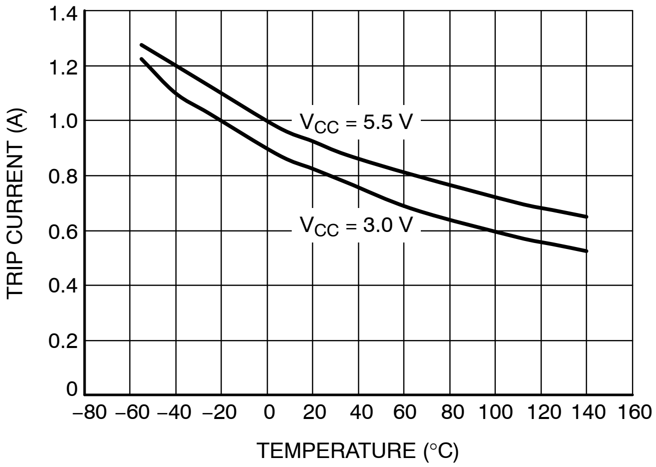


Figure 21. OCP Trip Current vs. Temperature

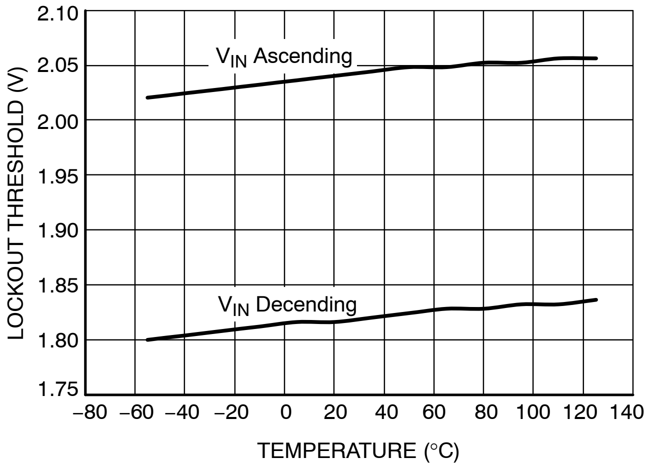


Figure 22. UVLO Trip Voltage vs. Temperature

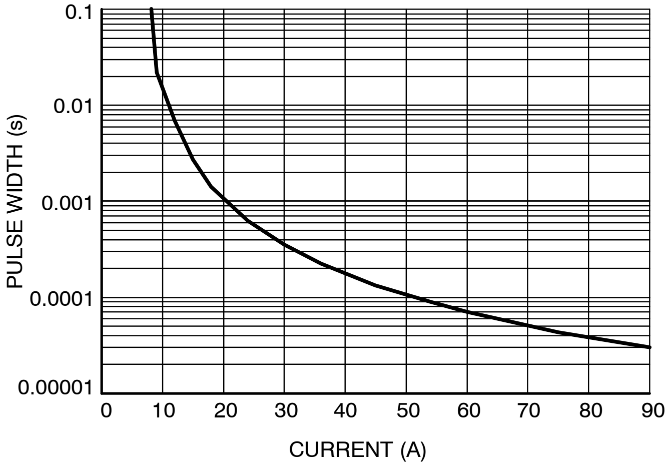


Figure 23. Safe Operating Area VIN to VOUT Transient

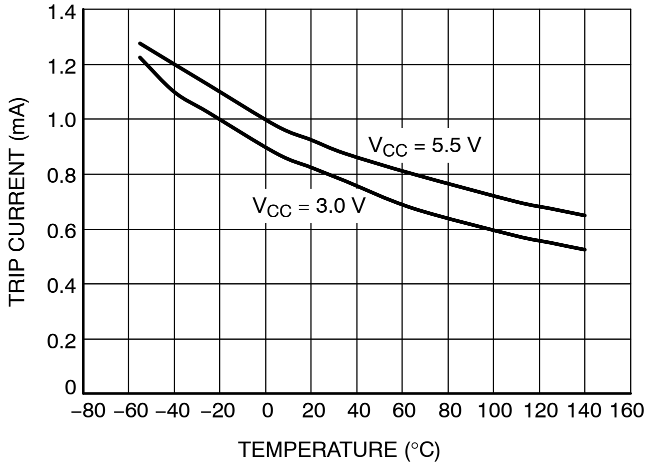


Figure 24. OCP Trip Current vs. Temperature (OCP = OPEN)

APPLICATIONS INFORMATION

Enable Control

The NCP45760 part enables the MOSFET in an active−high configuration. When the EN pin is at a logic high level and the V_{CC} supply pin has an adequate voltage applied, the MOSFET will be enabled. When the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not driven.

Short−Circuit Protection

The NCP45760 device is equipped with a short−circuit protection that helps protect the part and the system from a sudden high−current event, such as the output, V_{OUT}, being hard−shorted to ground.

Once active, the circuitry monitors the voltage difference between the V_{IN} pin and the V_{OUT} pin. When the difference is equal to the short−circuit protection threshold voltage, the MOSFET is turned off. The part remains off and is latched in the Fault state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

The short circuit protection feature protects the device from hard shorts (R_{SHORT} < 250 mΩ V_{OUT} to GND) for V_{IN} ≤ 18 V. Hard short circuit testing used a 10 mΩ short to ground for this scenario. The short circuit protection circuitry remains active regardless of the EN state to protect against enabling into a short circuit.

Over−Current Protection

The NCP45760 device is equipped with an over−current protection (OCP) that helps protect the part and the system from a high current event which exceeds the expected operational current (e.g., a soft short).

In the event that the current from the V_{IN} pin to the V_{OUT} pin exceeds the OCP threshold for longer than the blanking time, the MOSFET will shut down and the PG pin is driven low. Like the short−circuit protection, the part remains latched in the Fault state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

The over−current trip point is determined by the resistance between the OCP pin and ground. If no over−current protection is needed, then the OCP pin should be tied to GND; if the OCP protection is disabled in this way, the short−circuit protection will still remain active.

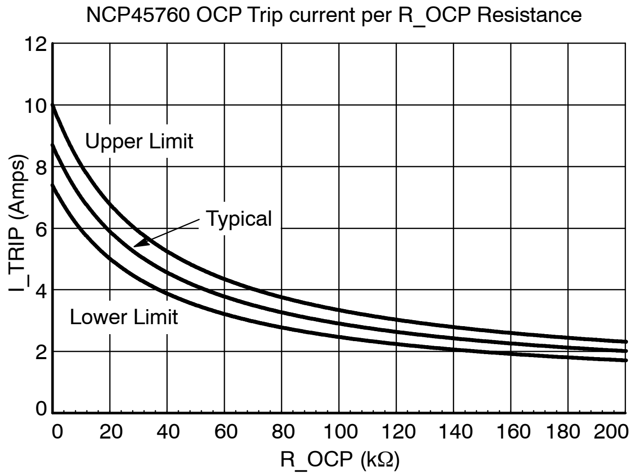


Figure 25. OCP Trip Current Setting

Thermal Shutdown

The thermal shutdown of the NCP45760 device protects the part from internally or externally generated excessive temperatures. This circuitry is disabled when EN is not active to reduce standby current. When an over−temperature condition is detected, the MOSFET is turned off.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Under Voltage Lockout

The under voltage lockout of the NCP45760 device turns the MOSFET off and activates the load bleed when the input voltage, V_{IN}, drops below the under voltage lockout threshold. This circuitry is disabled when EN is not active to reduce standby current.

If the V_{IN} voltage rises above the under voltage lockout threshold, and EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Power Good

The NCP45760 device has a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active−high, open−drain output that requires an external pull up resistor, RPG, greater than or equal to 100 kΩ to an external voltage.

The power good output can be used as the enable signal for other active−high devices in the system. This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

Slew Rate Control

The NCP45760 device is equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}} \ [V/s] \qquad \text{(eq. 1)}$$

where K_{SR} is the specified slew rate control constant, found on page 3, and C_{SR} is the capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

Capacitive Load

The peak in−rush current associated with the initial charging of the application load capacitance needs to stay below the specified I_{max}. C_L (capacitive load) should be less then C_{max} as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \qquad \text{(eq. 2)}$$

Where I_{max} is the maximum load current, and SR_{typ} is the typical default slew rate when no external load capacitor is added to the SR pin.

OFF to ON Transition Energy Dissipation

The energy dissipation due to load current traveling from V_{IN} to V_{OUT} is very low during steady state operation due to the low R_{ON}. When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from V_{IN} to V_{OUT} transitions from high impedance to R_{ON}, and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN} \cdot \left(I_{INRUSH} + 0.8 \cdot I_{LOAD}\right) \cdot dt \qquad \text{(eq. 3)}$$

Where V_{IN} is the voltage on the V_{IN} pin, I_{INRUSH} is the inrush current caused by capacitive loading on V_{OUT}, and dt is the time it takes V_{OUT} to rise from 0 V to V_{IN}. I_{INRUSH} can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \qquad \text{(eq. 4)}$$

Where dv/dt is the programmed slew rate, and C_L is the capacitive loading on V_{OUT}. To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to E_{TRANS} listed in operating ranges table.

ecoSWITCH LAYOUT GUIDELINES

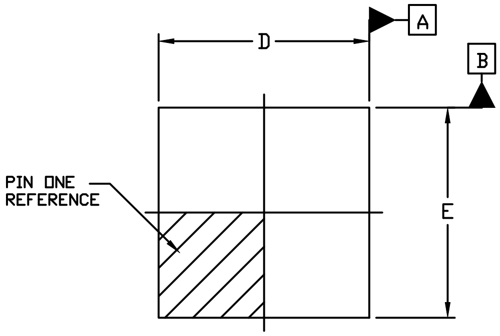
Electrical Layout Considerations

Correct physical PCB layout is important for proper low noise accurate operation of all ecoSWITCH products.

Power Planes: The ecoSWITCH is optimized for extremely low Ron resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the VIN and VOUT pins of the ecoSWITCH to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSWITCH requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. Direct coupling of VIN to VOUT should be avoided, as this will adversely affect slew rates.

DFN12 3x3, 0.5P
CASE 506EN
ISSUE O

DATE 27 SEP 2018

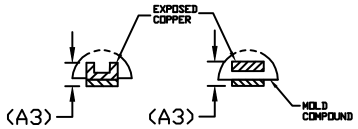


TOP VIEW

NOTES:

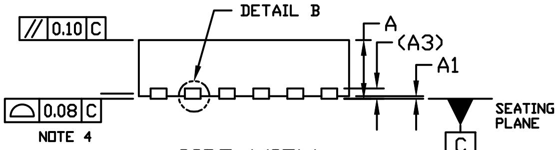
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	—	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.03	1.13	1.23
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
e	0.50 BSC		
k	0.20	—	—
L	0.20	0.30	0.40
L1	—	—	0.15

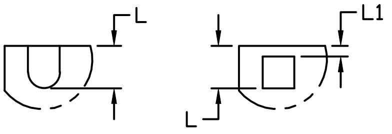


DETAIL B

ALTERNATE CONSTRUCTIONS

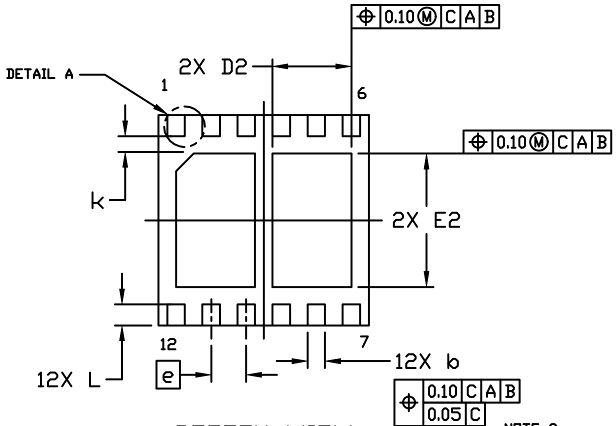


SIDE VIEW

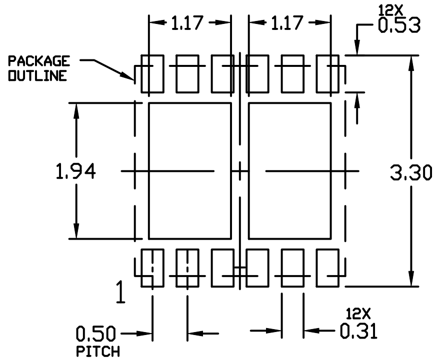


DETAIL A

ALTERNATE TERMINAL CONSTRUCTIONS

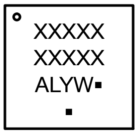


BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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