

# PROFET™ Load Guard

## Smart high-side power switch

## Features

- High-side switch with diagnosis and embedded protection
- Part of PROFET™ Load Guard family
- Switch ON capability while inverse current condition (InverseON)
- Capacitive load switching mode
- Green product (RoHS compliant)

## Potential applications

- Replaces electromechanical relays, fuses and discrete circuits
- Protection of system supply
- Main switch for ECU power supply
- Suitable for driving resistive, inductive and capacitive loads
- Suitable for driving heating elements
- Suitable for driving ADAS & AD modules, e.g. cameras, radar, ultrasonic, and LIDAR modules
- Suitable for driving sub modules, e.g. displays

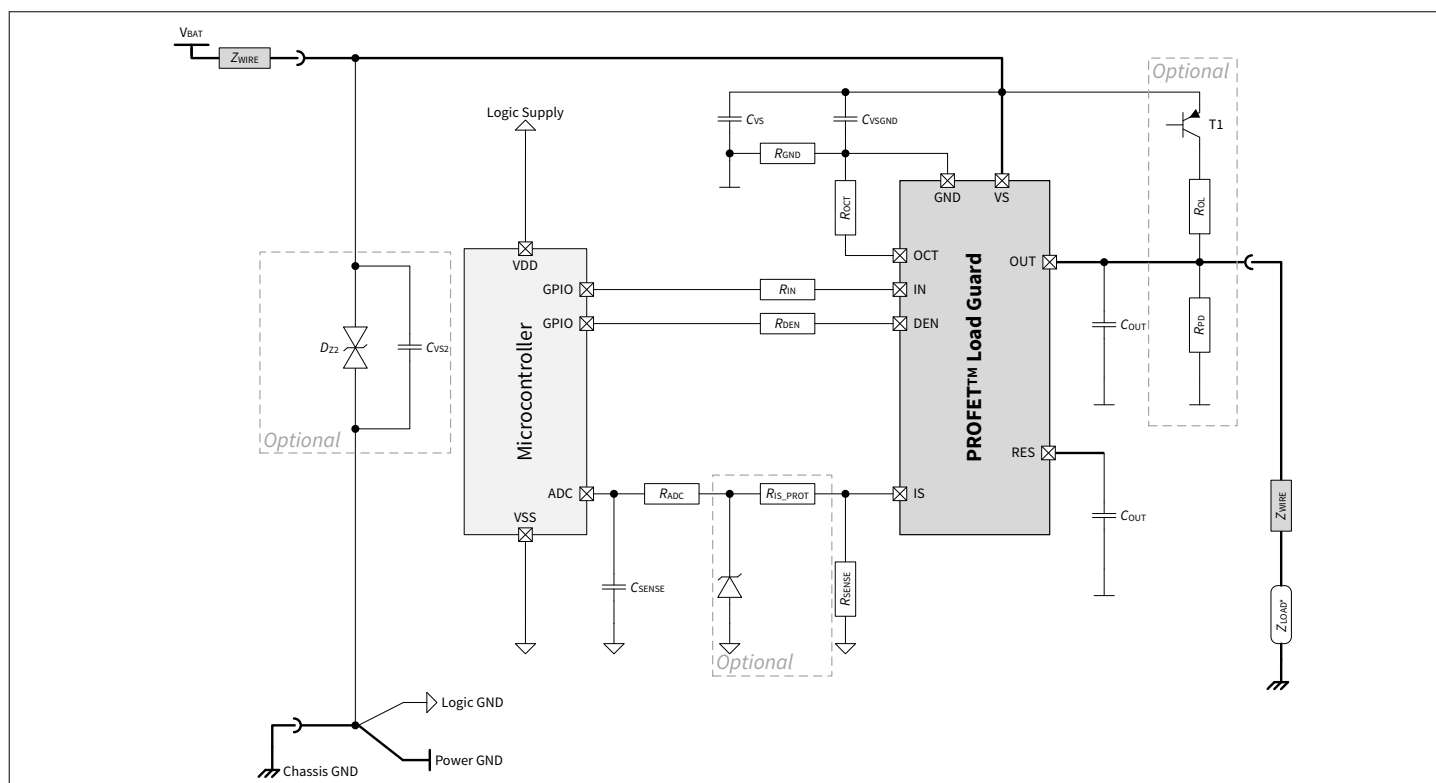
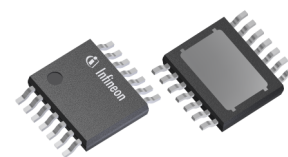
## Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100, Grade 1.

### Description

The PROFET™ Load Guard is a Smart High Side Switch, providing protection functions and enhanced diagnosis capabilities. The device offers an adjustable current limitation to offer higher reliability for protecting the system. In case of a short circuit to ground the PCB traces, connectors, as well as loads, can be protected. Furthermore, the PROFET™ Load Guard has a capacitive load switching mode implemented to charge capacitors.



Further information in [Chapter 9](#)

## Description

| Parameter                                                      | Symbol             | Values            |
|----------------------------------------------------------------|--------------------|-------------------|
| Minimum operating voltage                                      | $V_{S(OP)}$        | 3 V               |
| Minimum operating voltage (cranking)                           | $V_{S(UV)}$        | 2.7 V             |
| Maximum operating voltage                                      | $V_S$              | 28 V              |
| Minimum overvoltage protection ( $T_J \geq 25^\circ\text{C}$ ) | $V_{DS(CLAMP)_25}$ | 35 V              |
| Maximum current in sleep mode ( $T_J \leq 85^\circ\text{C}$ )  | $I_{VS(SLEEP)_85}$ | 0.5 $\mu\text{A}$ |
| Maximum operative current                                      | $I_{GND(ACTIVE)}$  | 4.5 mA            |
| Typical ON-state resistance ( $T_J = 25^\circ\text{C}$ )       | $R_{DS(ON)_25}$    | 50 m $\Omega$     |
| Maximum ON-state resistance ( $T_J = 150^\circ\text{C}$ )      | $R_{DS(ON)_150}$   | 100 m $\Omega$    |
| Nominal load current ( $T_A = 85^\circ\text{C}$ )              | $I_{L(NOM)}$       | 3 A               |
| Typical current sense ratio at $I_L = I_{L(NOM)}$              | $k_{ILIS}$         | 2030              |
| Adjustable overcurrent limitation                              | $I_{LIM}$          | 0.79 A - 8.86 A   |

**Diagnostic features**

- Proportional load current sense
- Open load in ON and OFF state
- Short circuit to ground and battery

**Protection features**

- Absolute and dynamic temperature protection with restart control
- Adjustable overcurrent limitation
- Overvoltage protection

| Type         | Package     | Marking |
|--------------|-------------|---------|
| BTG7050-1EPL | PG-TSDSO-14 | 7050-1L |

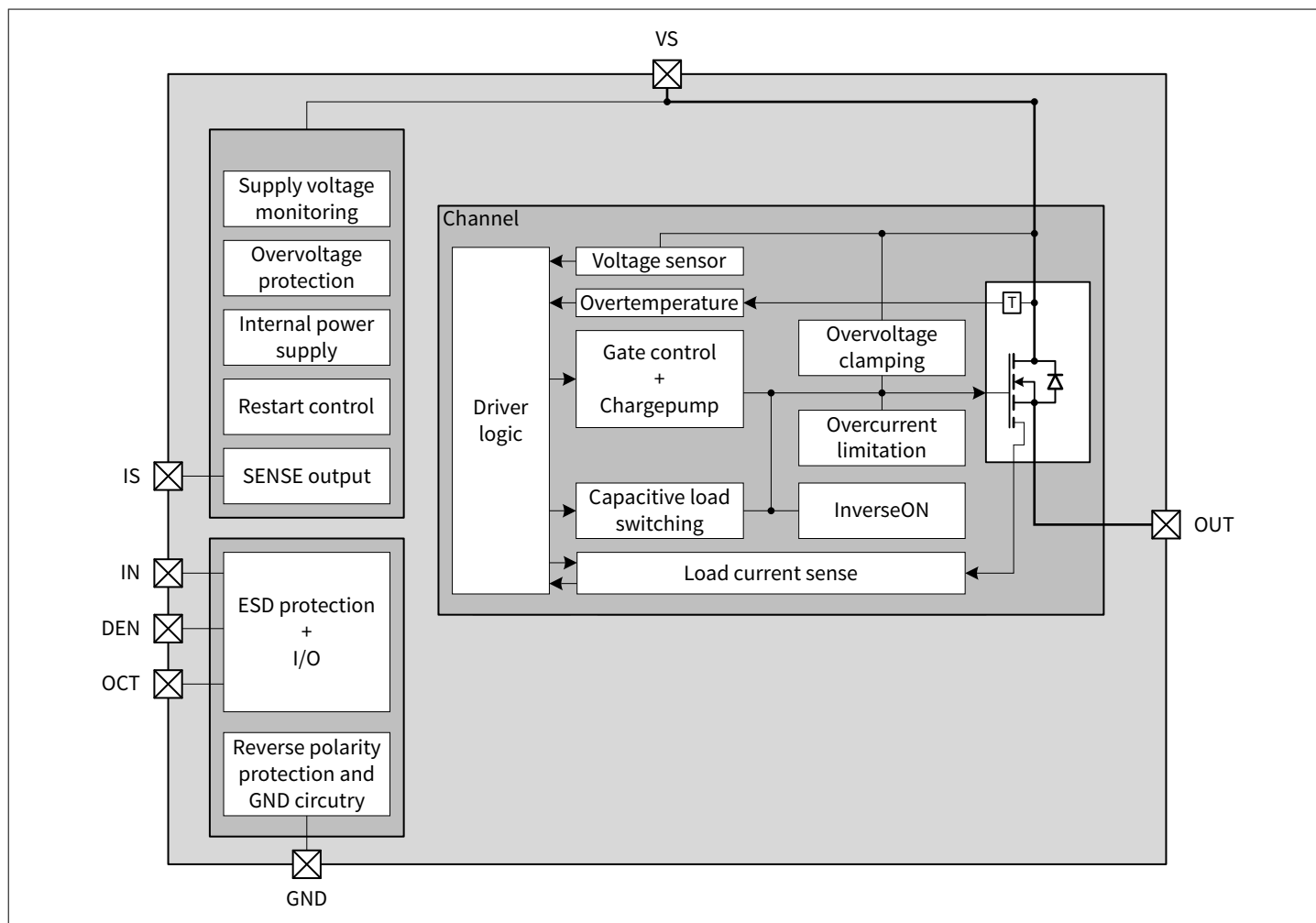
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## 1 Block diagram and terms

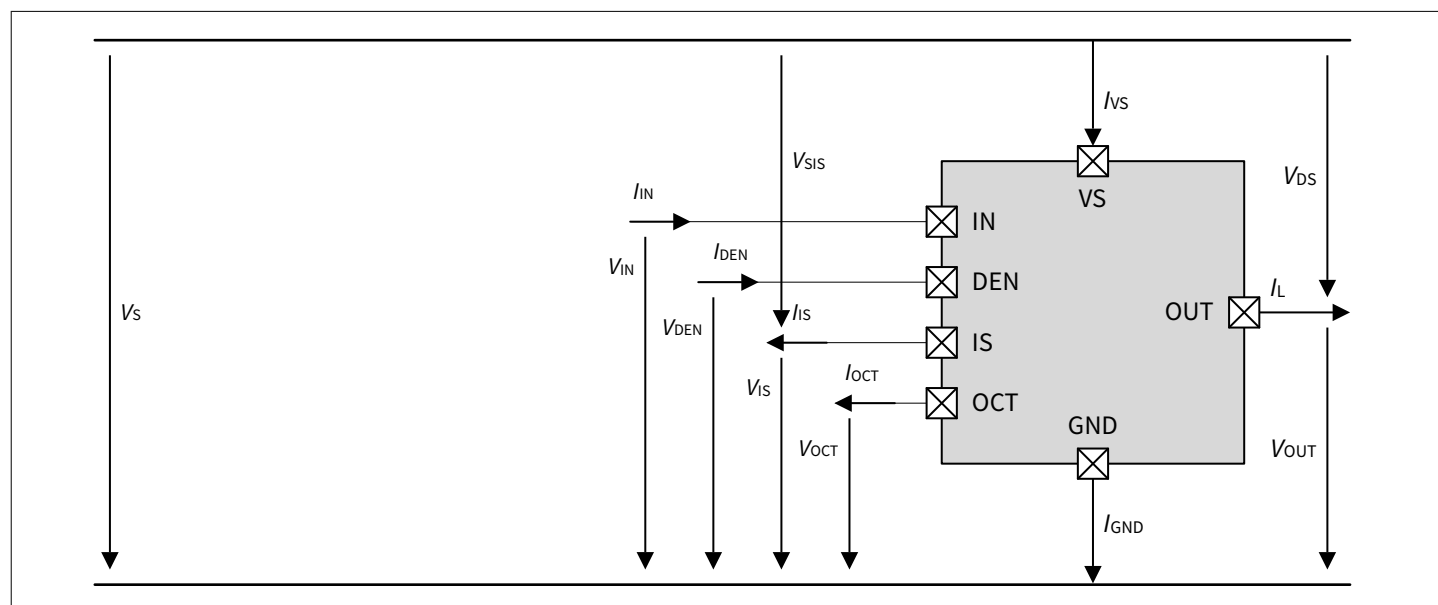
### 1.1 Block diagram



**Figure 2** Block diagram of BTG7050-1EPL

## 1.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.



**Figure 3** Voltage and current convention

## 2 Pin configuration

### 2.1 Pin assignment

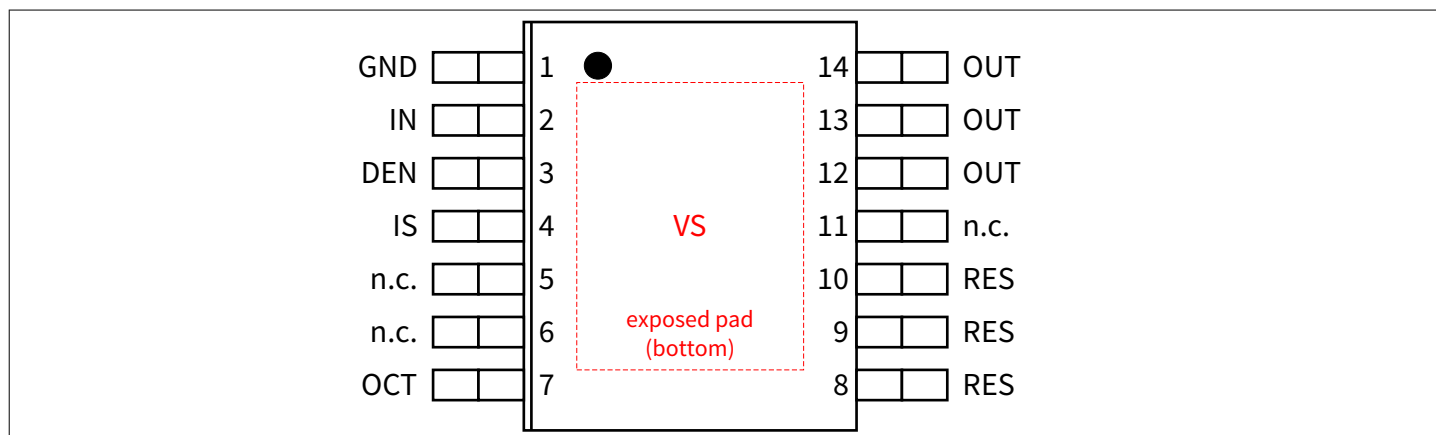


Figure 4 Pin configuration

### 2.2 Pin definitions and functions

Table 1 Pin definition

| Pin      | Symbol           | Function                                                                                                                                                                                                                                |
|----------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EP       | VS (exposed pad) | <b>Supply Voltage</b><br>Battery voltage                                                                                                                                                                                                |
| 1        | GND              | <b>Ground</b><br>Ground connection for the internal logic                                                                                                                                                                               |
| 2        | IN               | <b>Input Channel</b><br>Digital signal to switch ON the channel ("high" active)<br>If not used: Connect with a 10kΩ resistor either to GND pin or to module ground                                                                      |
| 3        | DEN              | <b>Diagnostic Enable</b><br>Digital signal to enable device diagnosis ("high" active) and to clear the protection counter<br>If not used: Connect with a 10kΩ resistor either to GND pin or to module ground                            |
| 4        | IS               | <b>SENSE current output</b><br>Analog/digital signal for diagnosis<br>If not used: Left open                                                                                                                                            |
| 7        | OCT              | <b>Adjustable overcurrent threshold</b><br>A resistor $R_{OCT}$ needs to be connected between OCT pin and GND pin to adjust the overcurrent threshold<br>If not used: Threshold selection as described in <a href="#">Chapter 7.1.1</a> |
| 5, 6, 11 | n.c.             | Not connected, internally not bonded                                                                                                                                                                                                    |
| 12-14    | OUT              | <b>Output</b><br>Protected high-side power output channel <sup>1)</sup>                                                                                                                                                                 |

(table continues...)

**Table 1** (continued) Pin definition

| Pin  | Symbol | Function                                                                                              |
|------|--------|-------------------------------------------------------------------------------------------------------|
| 8-10 | RES    | <b>RESERVED</b><br>It is recommended to connect these pins to VS or with a capacitor $C_{OUT}$ to GND |

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

$T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

**Table 2 Absolute maximum ratings**

| Parameter                                      | Symbol          | Values |      |      | Unit | Note or condition                                                                                                          | P-<br>Number |
|------------------------------------------------|-----------------|--------|------|------|------|----------------------------------------------------------------------------------------------------------------------------|--------------|
|                                                |                 | Min.   | Typ. | Max. |      |                                                                                                                            |              |
| Supply pins                                    |                 |        |      |      |      |                                                                                                                            |              |
| Power supply voltage                           | $V_S$           | -0.3   | –    | 28   | V    | <sup>2)</sup><br>–                                                                                                         | PRQ-34       |
| Load dump voltage                              | $V_{BAT(LD)}$   | –      | –    | 35   | V    | <sup>2)</sup><br>suppressed load dump<br>acc. to ISO16750-2<br>(2010). $R_I = 2\ \Omega$                                   | PRQ-36       |
| Supply voltage for<br>short circuit protection | $V_{BAT(SC)}$   | 0      | –    | 24   | V    | <sup>2)</sup><br>Setup acc. to AEC-<br>Q100-012                                                                            | PRQ-38       |
| Reverse polarity<br>voltage                    | $-V_{BAT(REV)}$ | –      | –    | 16   | V    | <sup>2)</sup><br>$t \leq 2\text{min}$<br>$T_A = +25^{\circ}\text{C}$<br>Setup as described<br>in <a href="#">Chapter 9</a> | PRQ-40       |
| Current through GND<br>pin                     | $I_{GND}$       | -50    | –    | 50   | mA   | <sup>2)</sup><br>$R_{GND}$ according<br>to <a href="#">Chapter 9</a>                                                       | PRQ-44       |

#### Logic & control pins (Digital Input = DI)

##### DI = IN, DEN

|                                                          |               |    |   |    |    |                                                      |        |
|----------------------------------------------------------|---------------|----|---|----|----|------------------------------------------------------|--------|
| Current through DI pin                                   | $I_{DI}$      | -1 | – | 2  | mA | <sup>2)</sup> <sup>1)</sup>                          | PRQ-47 |
| Current through DI<br>pin - Reverse battery<br>condition | $I_{DI(REV)}$ | -1 | – | 10 | mA | <sup>2)</sup> <sup>1)</sup><br>$t \leq 2\text{ min}$ | PRQ-48 |

#### Analog & control pin (Analog Input = AI)

##### AI = OCT

|                                                          |               |    |   |    |    |                                                      |        |
|----------------------------------------------------------|---------------|----|---|----|----|------------------------------------------------------|--------|
| Current through AI pin                                   | $I_{AI}$      | -1 | – | 2  | mA | <sup>2)</sup> <sup>1)</sup>                          | PRQ-60 |
| Current through AI<br>pin - Reverse battery<br>condition | $I_{AI(REV)}$ | -1 | – | 10 | mA | <sup>2)</sup> <sup>1)</sup><br>$t \leq 2\text{ min}$ | PRQ-61 |

(table continues...)

**Table 2** (continued) Absolute maximum ratings

| Parameter                                                 | Symbol                    | Values |      |                          | Unit | Note or condition                                                                                                         | P-Number |
|-----------------------------------------------------------|---------------------------|--------|------|--------------------------|------|---------------------------------------------------------------------------------------------------------------------------|----------|
|                                                           |                           | Min.   | Typ. | Max.                     |      |                                                                                                                           |          |
| IS pin                                                    |                           |        |      |                          |      |                                                                                                                           |          |
| Voltage at IS pin                                         | V <sub>IS</sub>           | -1.5   | –    | V <sub>S</sub>           | V    | <sup>2)</sup><br>I <sub>IS</sub> = 10 μA                                                                                  | PRQ-50   |
| Current through IS Pin                                    | I <sub>IS</sub>           | -25    | –    | I <sub>IS(SAT),MAX</sub> | mA   | <sup>2)</sup><br>–                                                                                                        | PRQ-52   |
| Temperatures                                              |                           |        |      |                          |      |                                                                                                                           |          |
| Junction temperature                                      | T <sub>J</sub>            | -40    | –    | +150                     | °C   | <sup>2)</sup><br>–                                                                                                        | PRQ-53   |
| Storage temperature                                       | T <sub>STG</sub>          | -55    | –    | +150                     | °C   | <sup>2)</sup><br>–                                                                                                        | PRQ-54   |
| ESD susceptibility                                        |                           |        |      |                          |      |                                                                                                                           |          |
| ESD Susceptibility all pins (HBM)                         | V <sub>ESD(HBM)</sub>     | -2     | –    | 2                        | kV   | <sup>2)</sup><br>HBM <sup>3)</sup>                                                                                        | PRQ-55   |
| ESD Susceptibility OUTn vs GND and VS connected (HBM)     | V <sub>ESD(HBM)_OUT</sub> | -4     | –    | 4                        | kV   | <sup>2)</sup><br>HBM <sup>3)</sup>                                                                                        | PRQ-56   |
| ESD Susceptibility all pins (CDM)                         | V <sub>ESD(CDM)</sub>     | -500   | –    | 500                      | V    | <sup>2)</sup><br>CDM <sup>4)</sup>                                                                                        | PRQ-57   |
| ESD Susceptibility corner pins (CDM) - (pins 1, 7, 8, 14) | V <sub>ESD(CDM)_CRN</sub> | -750   | –    | 750                      | V    | <sup>2)</sup><br>CDM <sup>4)</sup>                                                                                        | PRQ-58   |
| Power stage                                               |                           |        |      |                          |      |                                                                                                                           |          |
| Maximum energy dissipation - single pulse                 | E <sub>AS</sub>           | –      | –    | 12                       | mJ   | <sup>2)</sup><br>I <sub>L</sub> = 2·I <sub>L(NOM)</sub><br>T <sub>J(0)</sub> = 150°C<br>V <sub>S</sub> = 28 V             | PRQ-766  |
| Maximum energy dissipation - repetitive pulse             | E <sub>AR</sub>           | –      | –    | 2.5                      | mJ   | <sup>2)</sup><br>I <sub>L</sub> = I <sub>L(NOM)</sub><br>T <sub>J(0)</sub> = 85°C<br>V <sub>S</sub> = 13.5 V<br>1M cycles | PRQ-767  |
| Load current                                              | I <sub>L</sub>            | –      | –    | I <sub>LIM,MAX</sub>     | A    | <sup>2)</sup><br>–                                                                                                        | PRQ-768  |

1) Maximum  $V_{DI}$  to be considered for Latch-Up tests: 5.5 V

2) Not subject to production test - specified by design

3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002

4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011

## Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

### 3.2 Functional range

Table 3 Functional range

| Parameter                                                  | Symbol           | Values |      |      | Unit | Note or condition                                                                  | P-Number |
|------------------------------------------------------------|------------------|--------|------|------|------|------------------------------------------------------------------------------------|----------|
|                                                            |                  | Min.   | Typ. | Max. |      |                                                                                    |          |
| Supply voltage range for normal operation                  | $V_{S(NOR)}$     | 4      | 13.5 | 20   | V    | <sup>1)</sup><br>–                                                                 | PRQ-66   |
| Lower extended supply voltage range for operation (normal) | $V_{S(EXT,LOW)}$ | 2.7    | –    | 4    | V    | <sup>1)</sup><br><sup>2)</sup><br><sup>3)</sup><br>(parameter deviations possible) | PRQ-67   |
| Upper extended supply voltage range for operation          | $V_{S(EXT,UP)}$  | 20     | –    | 28   | V    | <sup>1)</sup><br><sup>3)</sup><br>(parameter deviations possible)                  | PRQ-68   |
| Junction temperature                                       | $T_J$            | –40    | –    | +150 | °C   | <sup>1)</sup><br>–                                                                 | PRQ-69   |

1) Not subject to production test - specified by design

2) In case of  $V_S$  voltage decreasing refer to the maximum voltage of  $V_{S(UV)}$ , in case of  $V_S$  voltage increasing refer to the maximum voltage of  $V_{S(OP)}$

3) Protection functions still operative

## Note

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified by the conditions given in the Electrical Characteristics tables.

### 3.3 Thermal resistance

Table 4 Thermal resistance

| Parameter                                       | Symbol        | Values |      |      | Unit | Note or condition              | P-Number |
|-------------------------------------------------|---------------|--------|------|------|------|--------------------------------|----------|
|                                                 |               | Min.   | Typ. | Max. |      |                                |          |
| Thermal characterization parameter junction-top | $\Psi_{JTOP}$ | –      | 4.4  | 7.5  | K/W  | <sup>1)</sup><br><sup>2)</sup> | PRQ-623  |

(table continues...)

**Table 4** (continued) Thermal resistance

| Parameter                              | Symbol     | Values |      |      | Unit | Note or condition                    | P-Number |
|----------------------------------------|------------|--------|------|------|------|--------------------------------------|----------|
|                                        |            | Min.   | Typ. | Max. |      |                                      |          |
| Thermal resistance junction-to-case    | $R_{thJC}$ | –      | 5.1  | 8.6  | K/W  | 1)<br>2)<br>simulated at exposed pad | PRQ-624  |
| Thermal resistance junction-to-ambient | $R_{thJA}$ | –      | 33.5 | –    | K/W  | 1)<br>2)                             | PRQ-625  |

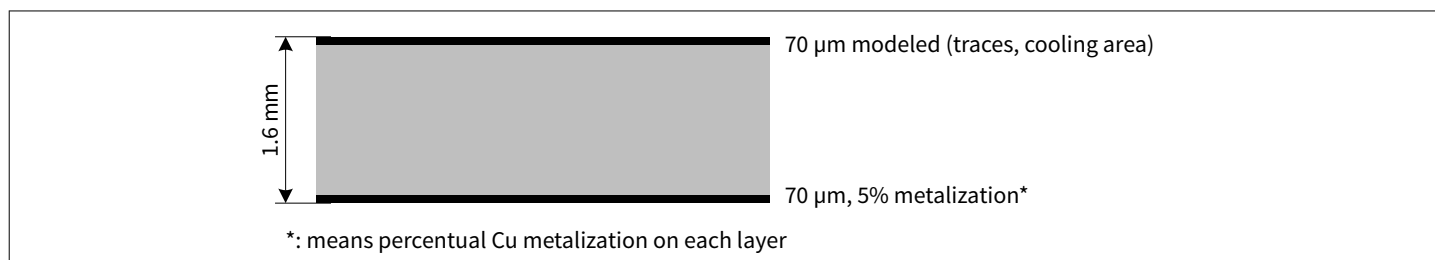
1) Not subject to production test - specified by design

2) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at  $T_A = 105^\circ\text{C}$ ,  $P_{DISSIPATION} = 1\text{ W}$

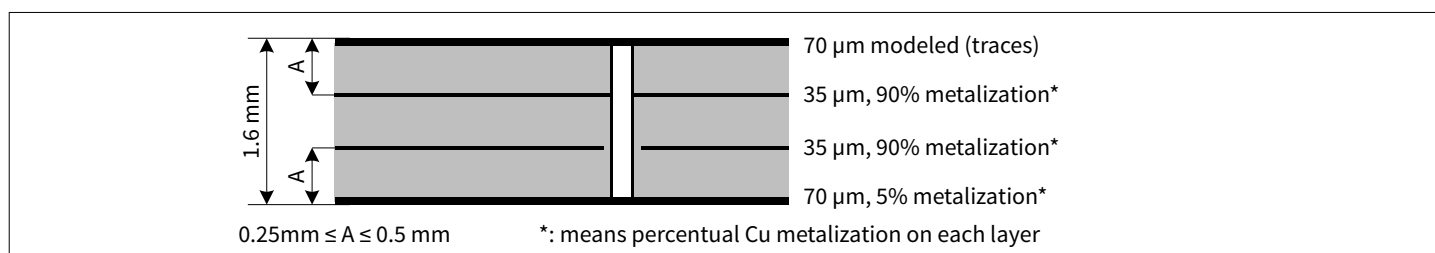
**Note**

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

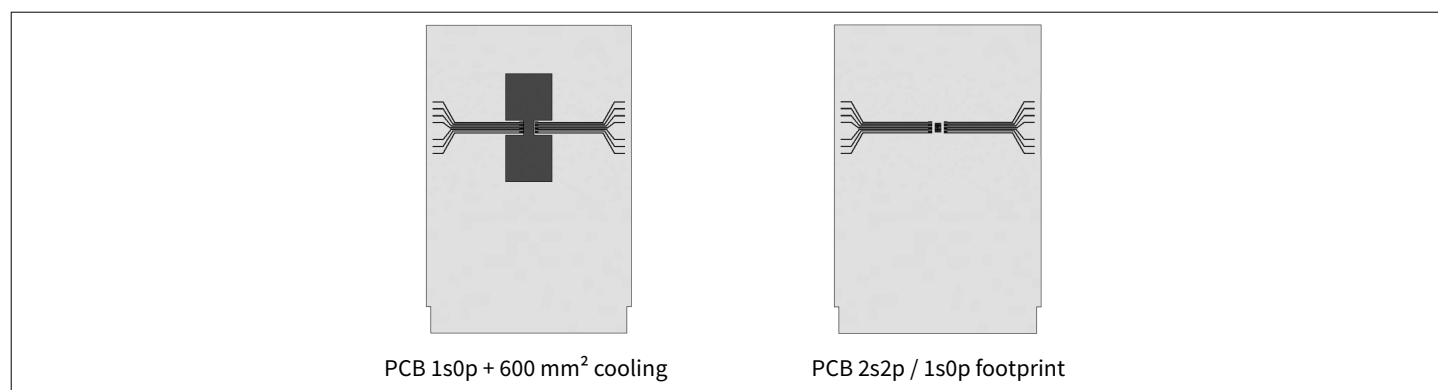
### 3.3.1 PCB setup



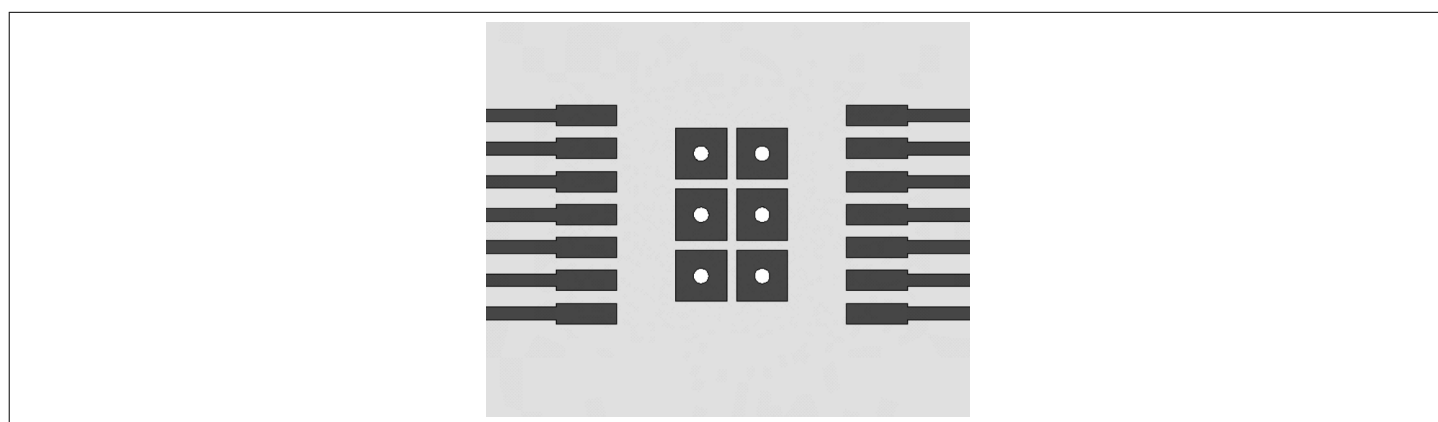
**Figure 5** 1s0p PCB cross section



**Figure 6** 2s2p PCB cross section



**Figure 7** PCB setup for thermal simulations



**Figure 8** Thermal vias on PCB for 2s2p PCB setup

3.3.2 Thermal impedance

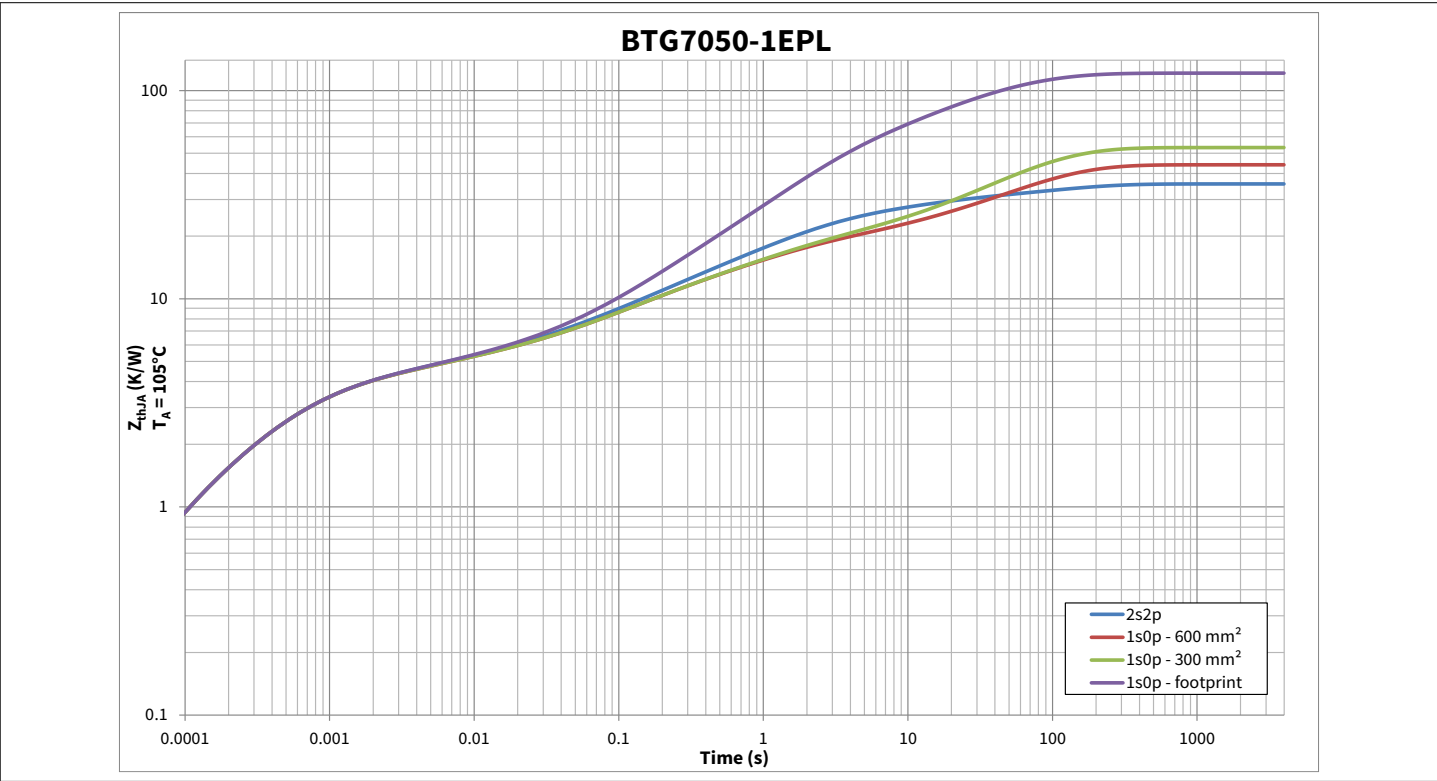


Figure 9 Typical thermal impedance. PCB setup according to PCB setup

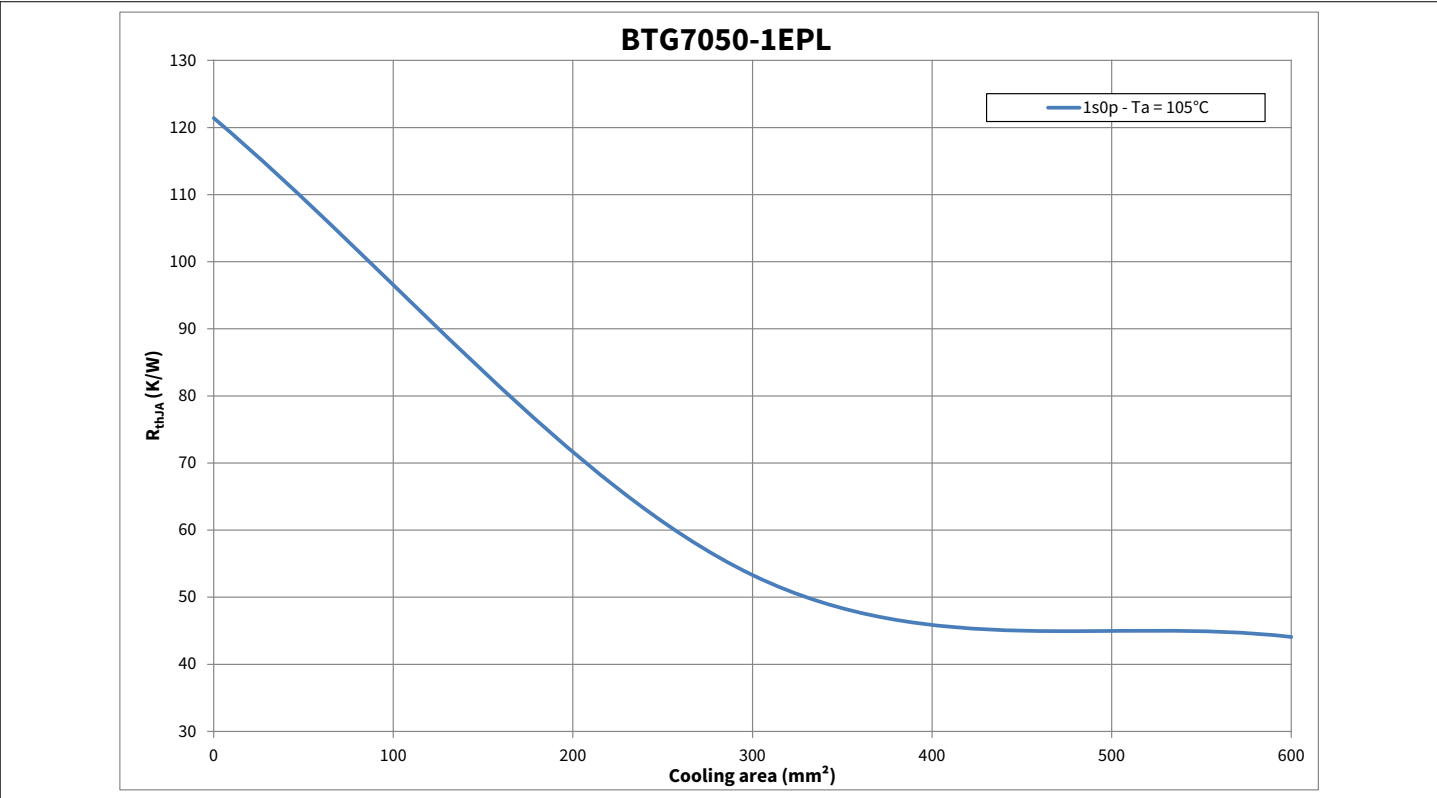


Figure 10 Thermal resistance on 1s0p PCB with various cooling surfaces

4 I/O pins

The device has two digital pins for direct control.

4.1 Digital I/O pins

Digital input (DI) pins = IN, DEN

4.1.1 Input pins

The input pin IN activates the output channel. The input circuitry is compatible with a 3.3 V and a 5 V microcontroller. The electrical equivalent of the input circuitry is shown in Figure 11. In case the pin is not used, it must be connected by a 10 kΩ resistor either to GND pin or to module ground.

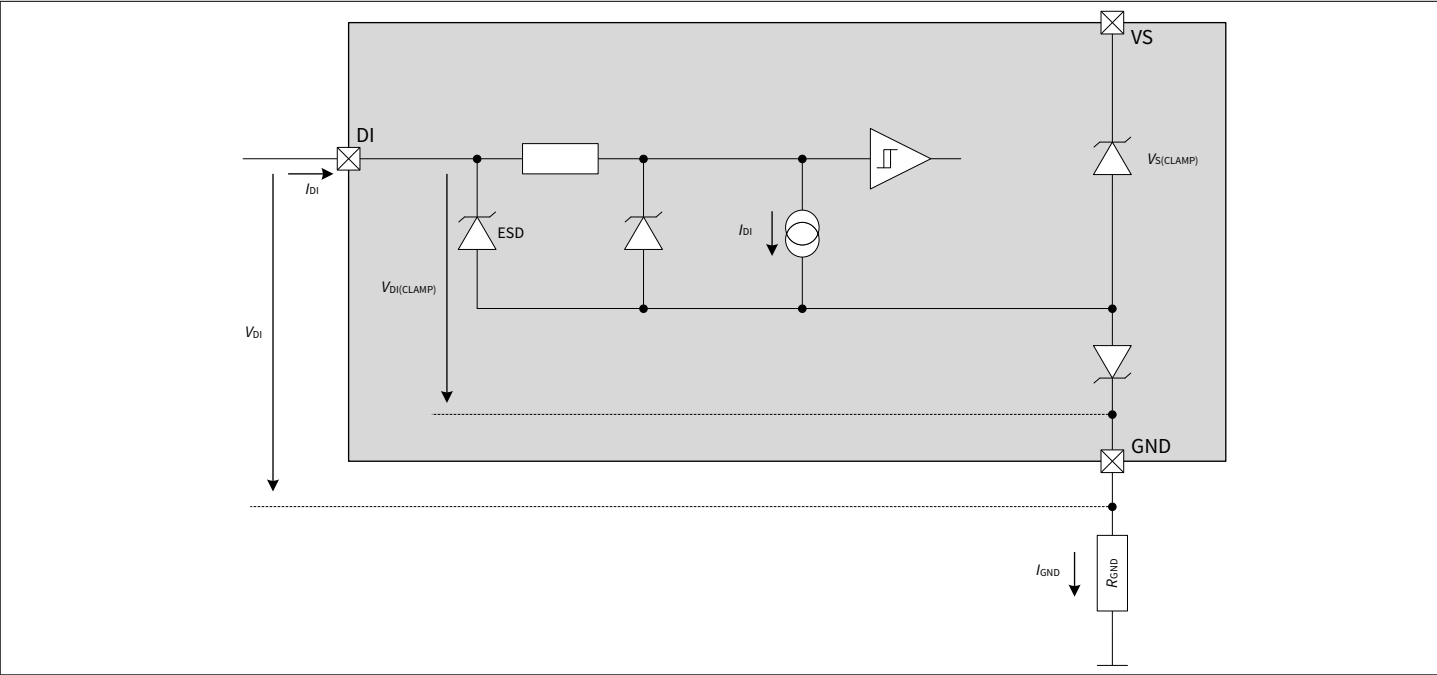


Figure 11 Input circuitry

The logic thresholds for “low” and “high” states are defined by parameters  $V_{DI(TH)}$  and  $V_{DI(HYS)}$ . The relationship between these two values is shown in Figure 12.

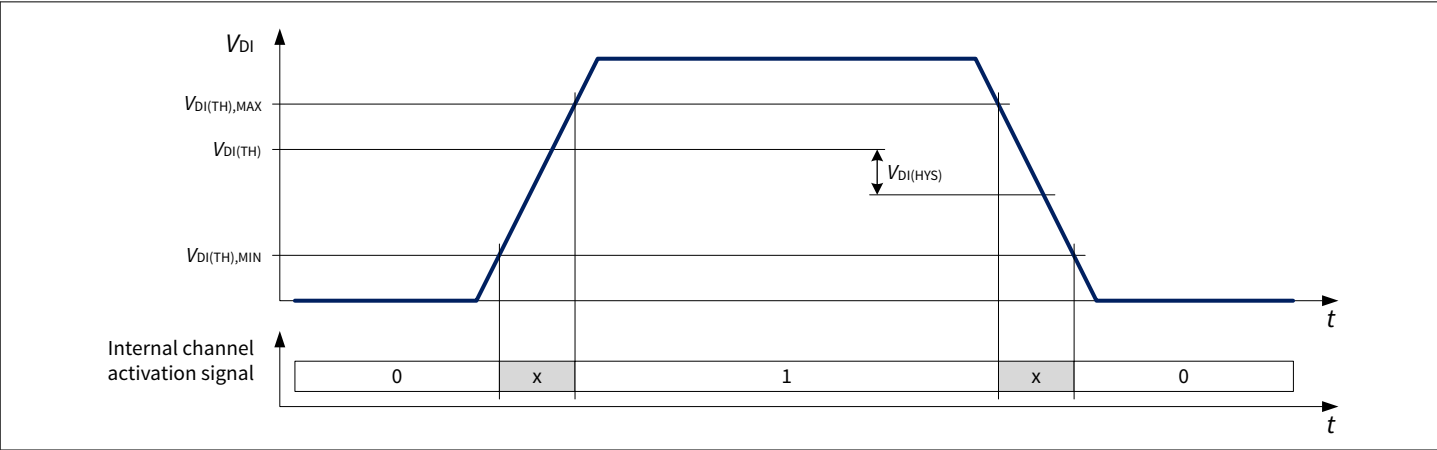


Figure 12 Input threshold voltages and hysteresis

### 4.1.2 Diagnosis pins

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and the protection circuitry. When DEN pin is set to “high”, the diagnosis is enabled (see [Chapter 8.2](#) for more details). When it is set to “low”, the diagnosis is disabled (IS pin is set to high impedance). See [Figure 12](#) for more details.

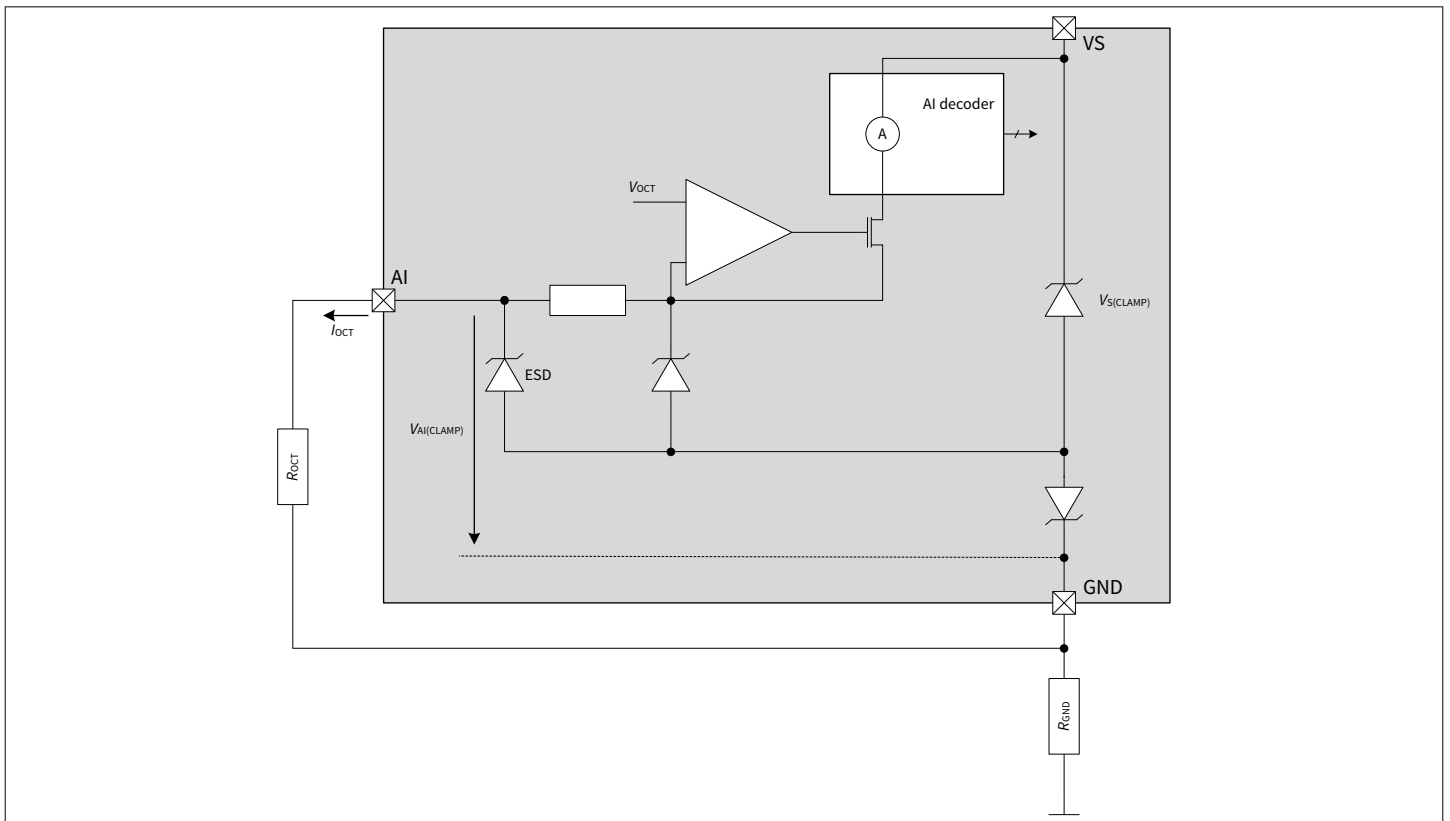
The transition from “high” to “low” of DEN pin clears the protection latch of the channel depending on the logic state of IN pin and DEN pulse length (see [Chapter 7.3](#) for more details).

## 4.2 Analog I/O pins

Analog input (AI) pins = OCT

### 4.2.1 Adjustable overcurrent threshold pin

To be able to adjust the overcurrent limitation for the OUT pin, the device offers an OCT pin. The pin needs to be connected to device ground via an external resistor  $R_{OCT}$ . The adjustable current limit allows the flexibility to adjust the overcurrent limitation as defined in [Table 10](#). This improves the reliability of the system by limiting the inrush or overload current. The electrical equivalent of the overcurrent pin circuit circuitry is shown in [Figure 13](#).



**Figure 13** Adjustable overcurrent threshold pin circuitry

## 4.3 Electrical characteristics I/O pins

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Digital input (DI) pins = IN, DEN

Analog input (AI) pins = OCT

**Table 5**                      **Electrical characteristics I/O pins**

| Parameter                                    | Symbol               | Values |      |      | Unit | Note or condition                                                                                       | P-Number |
|----------------------------------------------|----------------------|--------|------|------|------|---------------------------------------------------------------------------------------------------------|----------|
|                                              |                      | Min.   | Typ. | Max. |      |                                                                                                         |          |
| DI pins                                      |                      |        |      |      |      |                                                                                                         |          |
| Digital input voltage threshold              | $V_{DI(TH)}$         | 0.8    | 1.3  | 2    | V    | See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>                                             | PRQ-76   |
| Digital input clamping voltage               | $V_{DI(CLAMP1)}$     | –      | 7    | –    | V    | <sup>1)</sup><br>$I_{DI} = 1 \text{ mA}$<br>See <a href="#">Figure 11</a> and <a href="#">Figure 12</a> | PRQ-77   |
| Digital input clamping voltage               | $V_{DI(CLAMP2)}$     | 6.5    | 7.5  | 8.5  | V    | $I_{DI} = 2 \text{ mA}$<br>See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>                  | PRQ-78   |
| Digital input hysteresis                     | $V_{DI(HYS)}$        | –      | 0.25 | –    | V    | <sup>1)</sup><br>See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>                            | PRQ-80   |
| Digital input current ("high")               | $I_{DI(H)}$          | 2      | 10   | 25   | μA   | $V_{DI} = 2 \text{ V}$<br>See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>                   | PRQ-81   |
| Digital input current ("low")                | $I_{DI(L)}$          | 2      | 10   | 25   | μA   | $V_{DI} = 0.8 \text{ V}$<br>See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>                 | PRQ-82   |
| AI pins                                      |                      |        |      |      |      |                                                                                                         |          |
| Analog input clamping voltage                | $V_{AI(CLAMP1)}$     | –      | 7    | –    | V    | <sup>1)</sup><br>$I_{OCT} = 1 \text{ mA}$<br>See <a href="#">Figure 13</a>                              | PRQ-88   |
| Analog input clamping voltage                | $V_{AI(CLAMP2)}$     | 6.5    | 7.5  | 8.5  | V    | $I_{OCT} = 2 \text{ mA}$<br>See <a href="#">Figure 13</a>                                               | PRQ-630  |
| Analog overcurrent voltage threshold         | $V_{OCT}$            | 0.44   | 0.5  | 0.56 | V    | <sup>1)</sup><br>$I_{OCT,MIN} \leq I_{OCT} \leq I_{OCT,MAX}$<br>INn = "high" or DEN = "high"            | PRQ-628  |
| Analog linear overcurrent range              | $I_{OCT}$            | 20     | –    | 228  | μA   | <sup>1)</sup><br>INn = "high" or DEN = "high"                                                           | PRQ-89   |
| OCT short to device ground detection current | $I_{OCT(SHORT2GND)}$ | 320    | –    | –    | μA   | <sup>2)</sup><br>DEN = "high"<br>INn = "low"                                                            | PRQ-91   |

**(table continues...)**

**Table 5** (continued) Electrical characteristics I/O pins

| Parameter                  | Symbol                 | Values |      |      | Unit          | Note or condition                            | P-<br>Number |
|----------------------------|------------------------|--------|------|------|---------------|----------------------------------------------|--------------|
|                            |                        | Min.   | Typ. | Max. |               |                                              |              |
| OCT open detection current | $I_{\text{OCT(OPEN)}}$ | –      | –    | 5    | $\mu\text{A}$ | <sup>2)</sup><br>DEN = "high"<br>INn = "low" | PRQ-619      |

1) Not subject to production test - specified by design

2) Functional test only

## 5 Power Supply

The device is supplied by  $V_S$ , which is used to supply the internal logic as well as to supply the power output stages. In case of an undervoltage condition, the device has an detection circuit, which prevents the activation of the power output stage as well as the diagnosis.

### 5.1 Operation modes and transitions

#### 5.1.1 Operation modes

The device has the following operation modes:

- Sleep
- Inactive with diagnosis
- Active with diagnosis
- Active without diagnosis
- Capacitive load switching mode with diagnosis
- Capacitive load switching mode without diagnosis

The transition between operation modes is determined according to these variables:

- Logic level at IN pin
- PWM signal at IN pin
- Logic level at DEN pin

The state diagram including the possible transitions is shown in Figure 14. The behavior of the device as well as some parameters may change independent from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors  $V_S$  supply voltage, some changes within the same operation mode can be seen accordingly.

Table 6 shows the correlation between operation modes,  $V_S$  supply voltage, and the state of the most important functions (channel status).

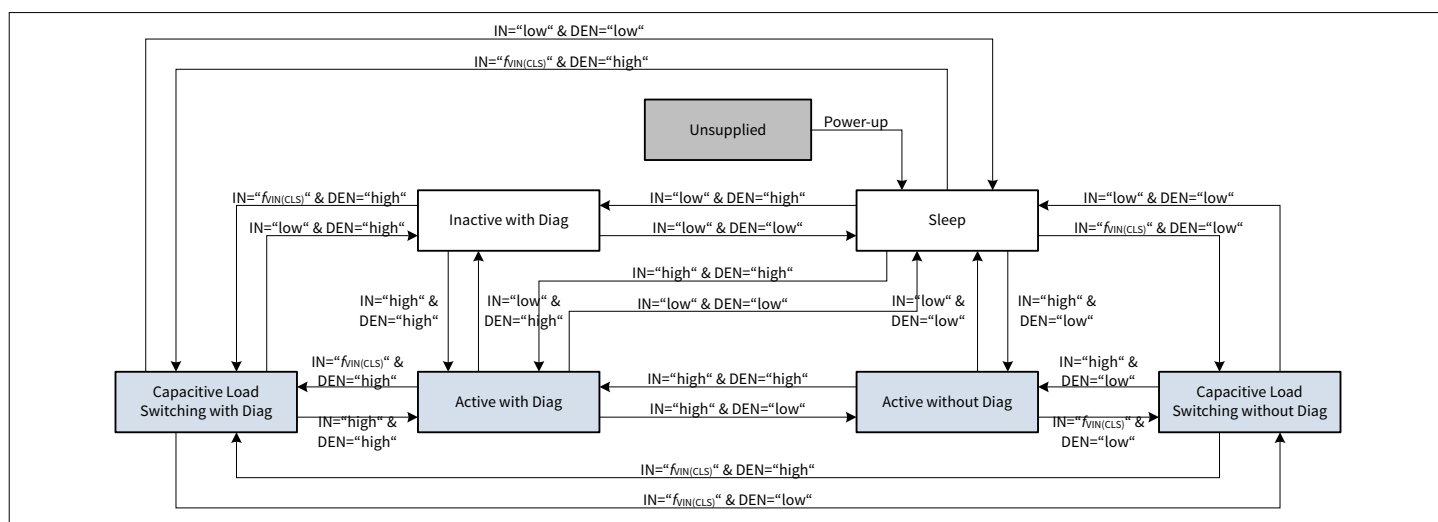


Figure 14 Operation mode state diagram

Table 6 Operation mode, device function and  $V_S$  voltage

| Operation mode | Function  | $V_S > V_{S(OP)}$ | $V_S < V_{S(OP)}$ |
|----------------|-----------|-------------------|-------------------|
| Sleep          | Channels  | OFF               | OFF               |
|                | Diagnosis | OFF               | OFF               |

(table continues...)

**Table 6** (continued) Operation mode, device function and  $V_S$  voltage

| Operation mode                                   | Function  | $V_S > V_{S(OP)}$ | $V_S < V_{S(OP)}$ |
|--------------------------------------------------|-----------|-------------------|-------------------|
| Inactive with diagnosis                          | Channels  | OFF               | OFF               |
|                                                  | Diagnosis | ON                | OFF               |
| Active with diagnosis                            | Channels  | ON                | OFF               |
|                                                  | Diagnosis | ON                | OFF               |
| Active without diagnosis                         | Channels  | ON                | OFF               |
|                                                  | Diagnosis | OFF               | OFF               |
| Capacitive load switching mode with diagnosis    | Channels  | ON                | OFF               |
|                                                  | Diagnosis | ON                | OFF               |
| Capacitive load switching mode without diagnosis | Channels  | ON                | OFF               |
|                                                  | Diagnosis | OFF               | OFF               |

#### 5.1.1.1 Unsupplied

In this state the device supply voltage is below the undervoltage threshold  $V_{S(UV)}$ .

#### 5.1.1.2 Power-up

The power-up transition is entered when the supply voltage ( $V_S$ ) is applied to the device. The supply rises until it exceeds the undervoltage threshold  $V_{S(OP)}$ .

#### 5.1.1.3 Sleep

The device is in sleep mode when digital input (DI) pins are set to "low". While in sleep mode the current consumption is at  $I_{VS(SLEEP)}$ . Overtemperature, overload protection and undervoltage mechanism are disabled. The device can go in sleep mode only if the protection is not active ( $n_{RESTART(CR)} = 0$ ,  $T_J < T_{J(ABS)}$  and  $(T_J - T_{J(REF)}) < T_{J(DYN)}$  (including hysteresis)), see [Chapter 7.3](#).

#### 5.1.1.4 Inactive with diagnosis

The device is in inactive with diagnosis mode while DEN pin is set to "high" and input pins are set to "low". The channels are OFF, therefore open load in OFF diagnosis is possible. Depending on the load condition, either a fault current  $I_{S(FAULT)}$  or an open load in OFF current  $I_{S(OLOFF)}$  may be present at IS pin. During such condition, the current consumption of the device is increased.

#### 5.1.1.5 Active with diagnosis

Active with diagnosis mode is the normal operation mode of the device. The device enters active with diagnosis mode for the channel when IN = "high" and DEN = "high", in this condition the output is switched ON with diagnosis. Device current consumption is specified by parameter  $I_{GND(ACTIVE)}$ .

#### 5.1.1.6 Active without diagnosis

The device is in active without diagnosis mode when IN = "high" and DEN = "low", in this condition the output is switched ON without diagnosis.

#### 5.1.1.7 Capacitive load switching mode with diagnosis

The device has a capacitive load switching mode implemented to drive capacitive loads. The capacitive load switching mode with diagnosis can be activated with IN = " $f_{VIN(CLS)}$ " and DEN = "high", in this condition the output is switched ON with diagnosis. Device current consumption is specified by parameter  $I_{GND(ACTIVE)}$ .

### 5.1.1.8 Capacitive load switching mode without diagnosis

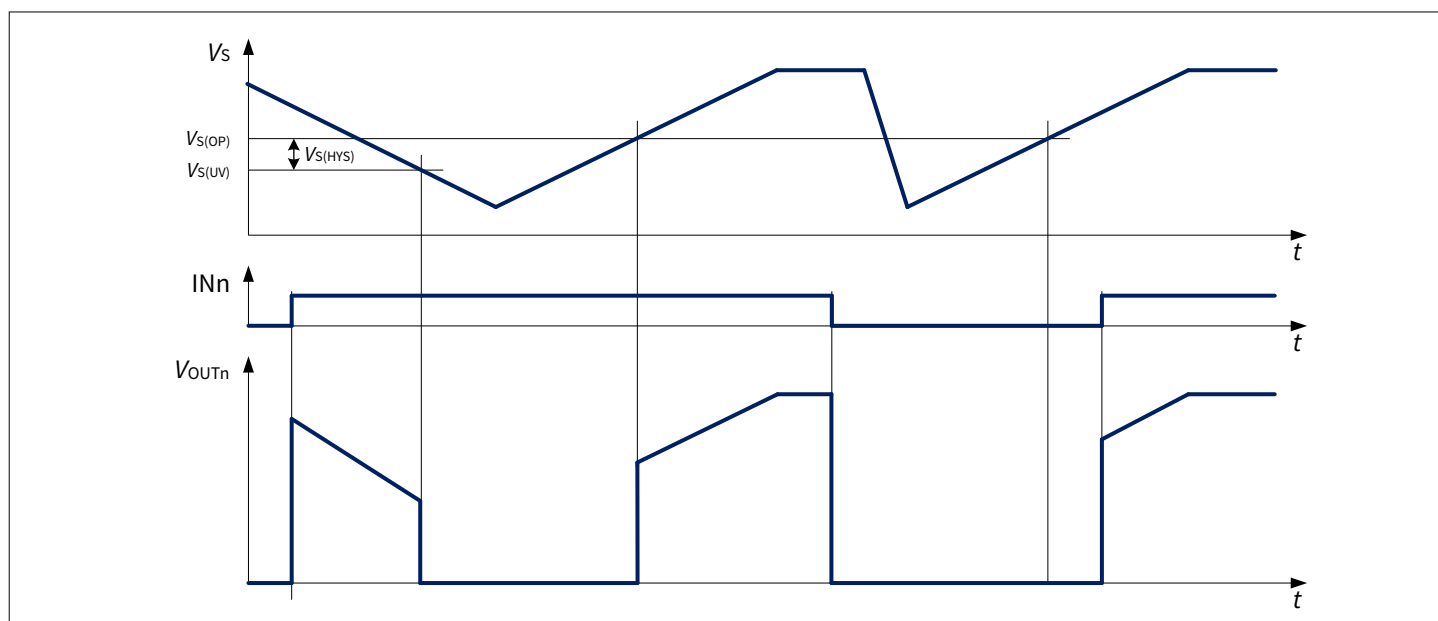
The device is in capacitive load switching mode without diagnosis when  $IN = "f_{VIN(CLS)}"$  and  $DEN = "low"$ , in this condition the output is switched ON without diagnosis.

## 5.2 Undervoltage on $V_S$

Between  $V_{S(OP)}$  and  $V_{S(UV)}$  the undervoltage mechanism is triggered.

The power output stage follows the input logic as long as  $V_S > V_{S(OP)}$ .

If the device is Active or in Capacitive Load Switching Mode, with or without Diagnosis and the supply voltage  $V_S$  drops below the undervoltage threshold  $V_{S(UV)}$ , the internal logic switches OFF the output channel.



**Figure 15**  $V_S$  undervoltage behavior

## 5.3 Electrical characteristics power supply

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTG7050-1EPL:  $R_L = 4.7\ \Omega$

**Table 7** Electrical characteristics power supply

| Parameter                          | Symbol             | Values |      |      | Unit | Note or condition                                                                                                                                     | P-Number |
|------------------------------------|--------------------|--------|------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
|                                    |                    | Min.   | Typ. | Max. |      |                                                                                                                                                       |          |
| VS pin                             |                    |        |      |      |      |                                                                                                                                                       |          |
| Power supply undervoltage shutdown | V <sub>S(UV)</sub> | 1.8    | 2.2  | 2.7  | V    | V <sub>S</sub> decreasing<br>INn = “high”<br>From 0 ≤ V <sub>DS</sub> ≤ 0.5 V to<br>V <sub>DS</sub> ~ V <sub>S</sub><br>See <a href="#">Figure 15</a> | PRQ-98   |

(table continues...)

**Table 7** (continued) Electrical characteristics power supply

| Parameter                                                                                | Symbol              | Values |      |      | Unit          | Note or condition                                                                                                            | P-Number |
|------------------------------------------------------------------------------------------|---------------------|--------|------|------|---------------|------------------------------------------------------------------------------------------------------------------------------|----------|
|                                                                                          |                     | Min.   | Typ. | Max. |               |                                                                                                                              |          |
| Power supply minimum operating voltage                                                   | $V_{S(OP)}$         | 2.1    | 2.5  | 3    | V             | $V_S$ increasing<br>INn = "high"<br>From $V_{DS} \sim V_S$ to<br>$0 \leq V_{DS} \leq 0.5$ V<br>See <a href="#">Figure 15</a> | PRQ-99   |
| Power supply undervoltage shutdown hysteresis                                            | $V_{S(HYS)}$        | –      | 0.3  | –    | V             | <sup>1)</sup><br>$V_{S(OP)} - V_{S(UV)}$<br>See <a href="#">Figure 15</a>                                                    | PRQ-100  |
| Breakdown voltage between GND and VS pins in reverse battery                             | $-V_{S(REV)}$       | 16     | –    | 30   | V             | <sup>1)</sup><br>$I_{GND(REV)} = 7$ mA<br>$T_J = 150^\circ\text{C}$                                                          | PRQ-101  |
| Power supply current consumption in sleep mode with loads at $T_J \leq 85^\circ\text{C}$ | $I_{VS(SLEEP)_85}$  | –      | 0.03 | 0.5  | $\mu\text{A}$ | <sup>1)</sup><br>$V_S = 20$ V<br>$V_{OUT} = 0$ V<br>IN = DEN = "low"<br>$T_J \leq 85^\circ\text{C}$                          | PRQ-776  |
| Power supply current consumption in sleep mode with loads at $T_J = 150^\circ\text{C}$   | $I_{VS(SLEEP)_150}$ | –      | 3.5  | 14   | $\mu\text{A}$ | $V_S = 20$ V<br>$V_{OUT} = 0$ V<br>IN = DEN = "low"<br>$T_J = 150^\circ\text{C}$                                             | PRQ-777  |
| Operating current in active with diagnosis mode                                          | $I_{GND(ACTIVE)}$   | –      | 3.7  | 4.5  | mA            | $V_S = 20$ V<br>IN = DEN = "high"                                                                                            | PRQ-778  |
| Operating current in inactive with diagnosis mode                                        | $I_{GND(INACTIVE)}$ | –      | 1.8  | 2.2  | mA            | $V_S = 20$ V<br>INn = "low"<br>DEN = "high"<br>$I_{OCT} = I_{OCT,MAX}$                                                       | PRQ-779  |

<sup>1)</sup> Not subject to production test - specified by design

## 6 Power Stage

The high-side power stages are built using a N-channel vertical power MOSFET with charge pump.

### 6.1 Output ON-state resistance

The ON-state resistance  $R_{DS(ON)}$  depends mainly on junction temperature  $T_J$ . Figure 16, shows the variation of  $R_{DS(ON)}$  across the whole  $T_J$  range. The value “2” on the y-axis corresponds to the maximum  $R_{DS(ON)}$  measured at  $T_J = 150^\circ\text{C}$ .

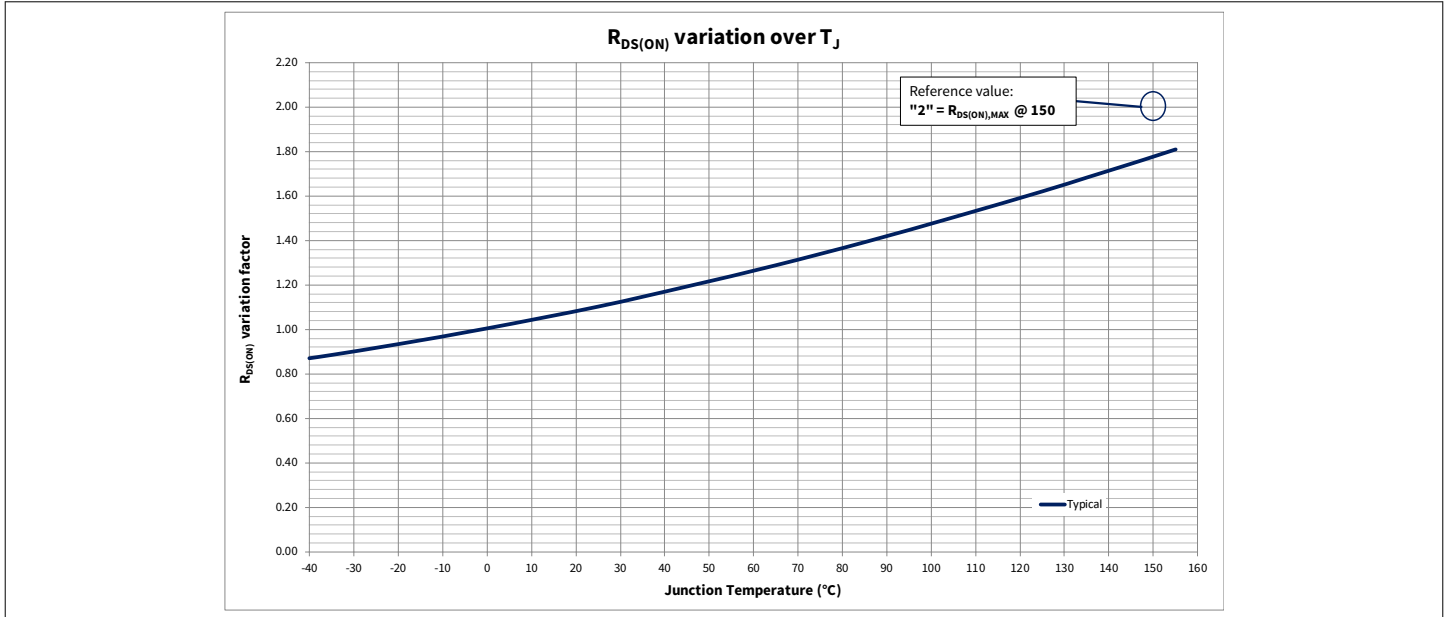


Figure 16  $R_{DS(ON)}$  variation factor

The behavior in reverse polarity is described in Chapter 7.4.1.

## 6.2 Switching loads

### 6.2.1 Switching resistive loads

When switching resistive loads, the switching times and slew rates shown in Figure 17 can be considered. The switching energy values  $E_{ON}$  and  $E_{OFF}$  are proportional to load resistance and times  $t_{ON}$  and  $t_{OFF}$ .

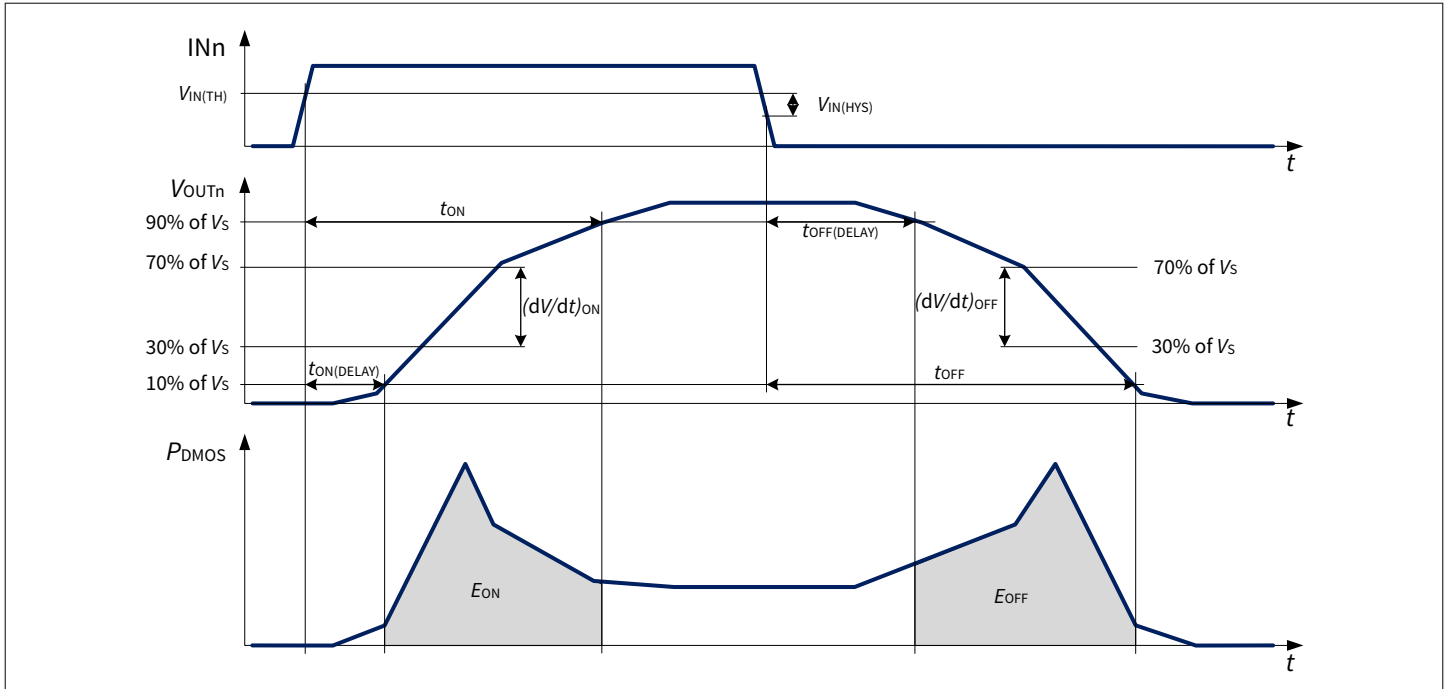


Figure 17 Switching a resistive load

## 6.2.2 Switching inductive loads

When switching OFF inductive loads with high-side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the output voltage so that  $V_{DS} \leq V_{DS(CLAMP)}$ . Chapter 6.2.2 shows a concept drawing of the implementation.

The clamping structure is active in all operation modes listed in Chapter 5.1.

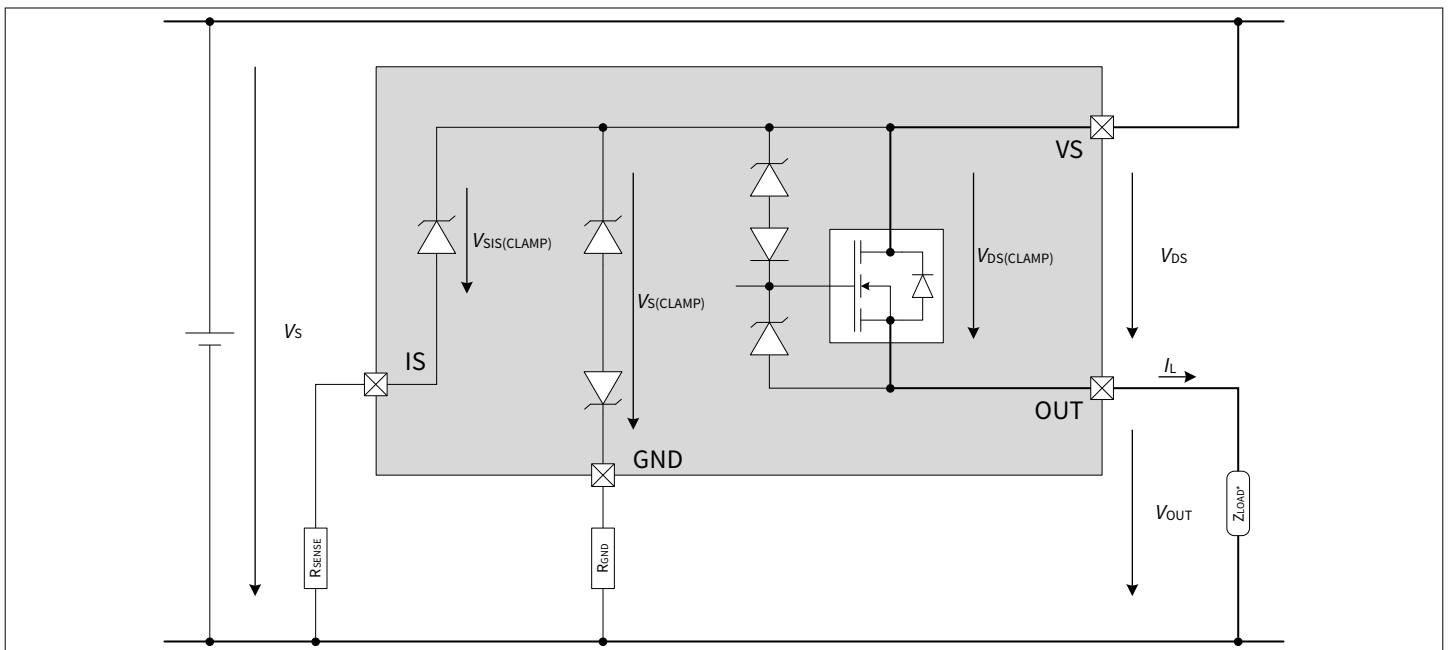


Figure 18 Output clamping concept

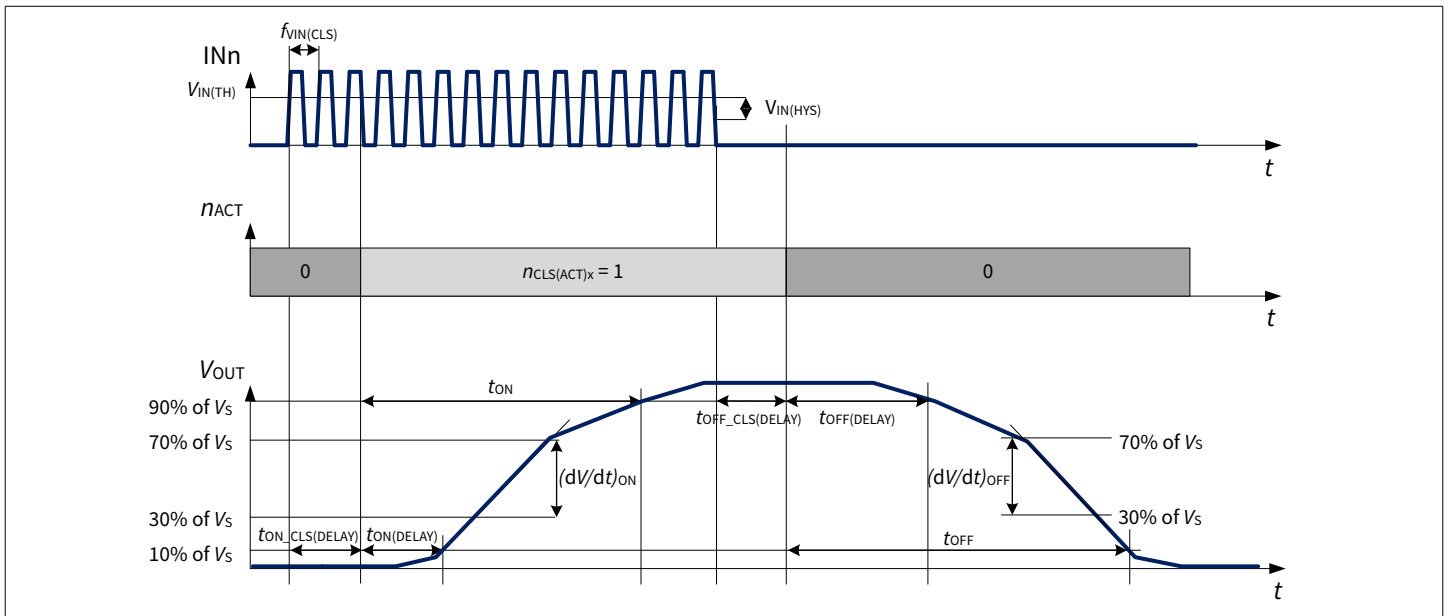
During demagnetization of inductive loads, energy has to be dissipated in the device. The energy can be calculated with:

$$E = V_{DS(CLAMP)} \cdot \left[ \frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

The maximum energy the device can sustain is limited by the thermal design. Please refer to [Table 2](#) for the maximum allowed values of  $E_{AS}$  (single pulse energy) and  $E_{AR}$  (repetitive energy).

### 6.2.3 Switching capacitive loads

When  $f_{VIN(CLS)}$  is applied the device enters CLS mode after  $t_{ON\_CLS(DELAY)}$  as shown in [Figure 19](#). A pumping mode is applied to charge the capacitor while the overcurrent limitation is active using the overcurrent limitation setting as set by the OCT pin, as shown in [Figure 20](#). During CLS mode, protection and diagnosis functions are active.



**Figure 19** Switching a capacitive load

When the device is in CLS mode, the dynamic overtemperature protection is reduced to  $T_{J(DYN)\_CLS}$  with continuous restart.

A transition from CLS mode to Active mode is performed automatically when  $V_{DS} \leq V_{DS(OLOFF)}$ .

On the contrary, when  $V_{DS} > V_{DS(OLOFF)}$ , the CLS mode has to be left after a maximum time of  $t_{CLSx}$  by setting input to "low" or "high".

A transition from capacitive load switching mode to active mode shall be performed only if there is no short circuit at the output. To distinguish between short circuit and normal load, a current sense measurement must be performed before leaving. If the current measurement delivers an expected value, the transition from CLS mode to active mode may be performed. If the current measurement delivers an open load value (no output current), it has to be assumed that there is either an open load or a short circuit at the output. Additionally, a short circuit condition could be excluded by an external voltage measurement at the output.

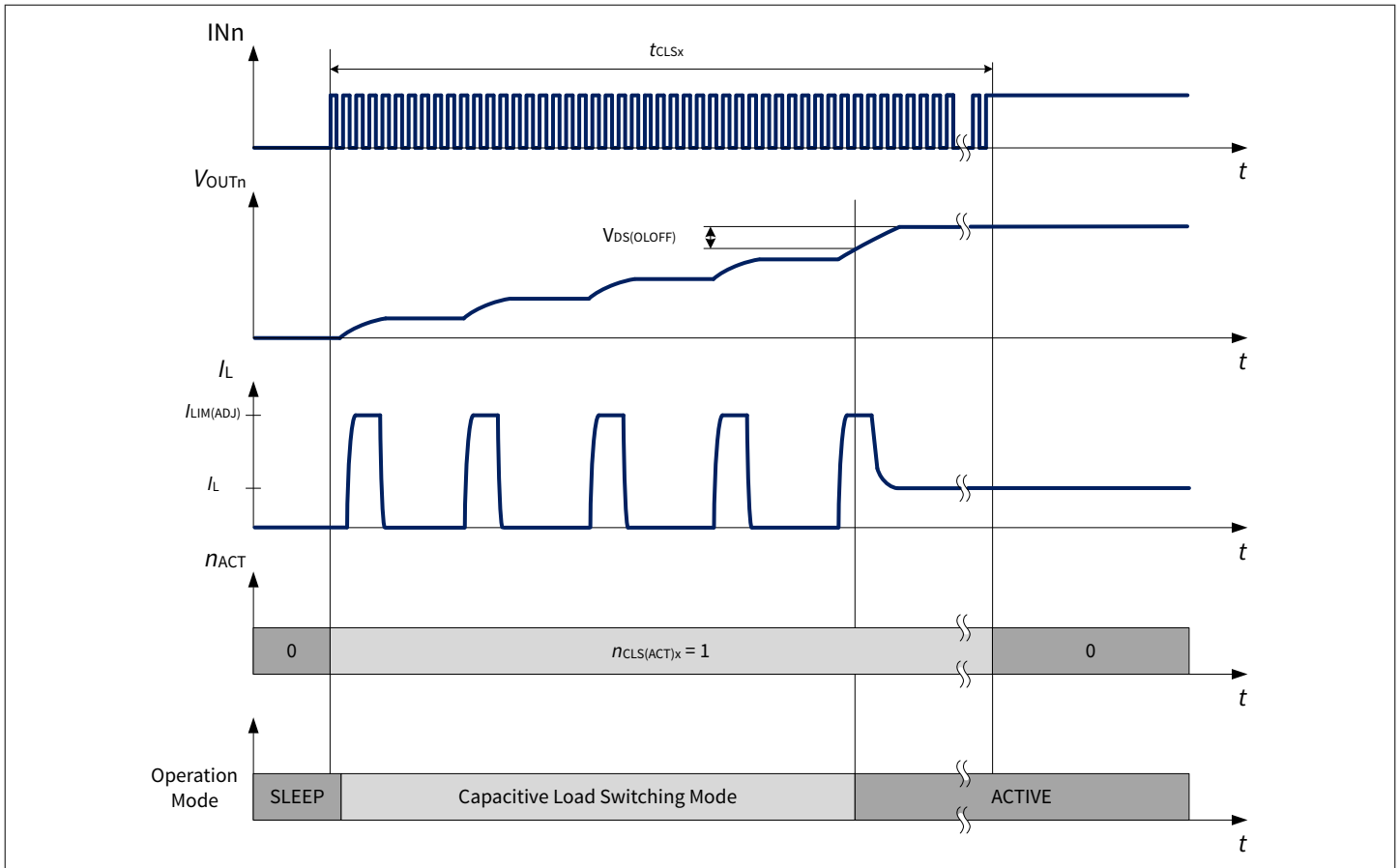


Figure 20 Capacitive load switching activations

## 6.3 Advanced switching characteristics

### 6.3.1 Inverse current behavior

When  $V_{OUT} > V_S$ , a current  $I_{L(INV)}$  flows into the power output transistor (see Figure 21). This condition is known as “Inverse Current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses, therefore, an increase of overall device temperature. This may lead to a switch OFF of unaffected channels due to overtemperature. If the channel is in ON state,  $R_{DS(INV)}$  can be expected and power dissipation in the output stage is comparable to normal operation in  $R_{DS(ON)}$ .

During inverse current condition, the channel remains in ON or OFF state as long as  $|I_L| < |I_{L(INV)}|$ .

The feature of InverseON allows to switch ON the channel during Inverse Current condition as long as  $|I_L| < |I_{L(INV)}|$ , see Figure 22.

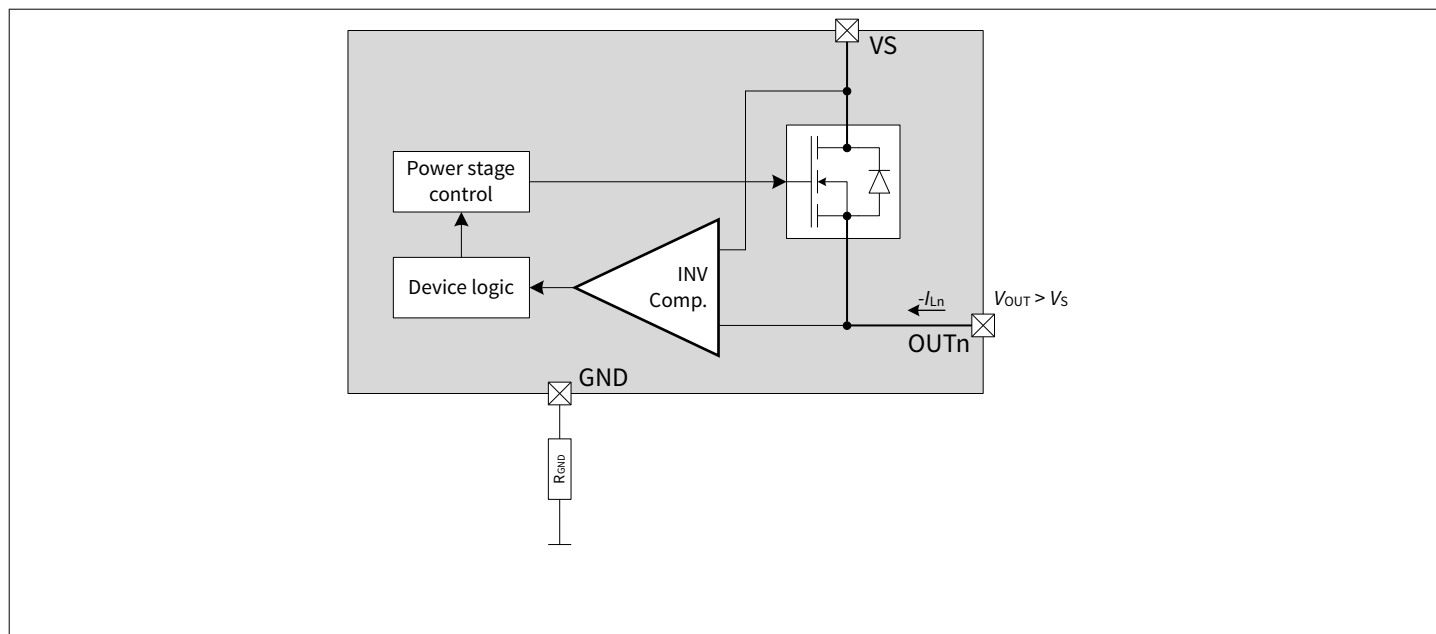


Figure 21 Inverse current circuitry

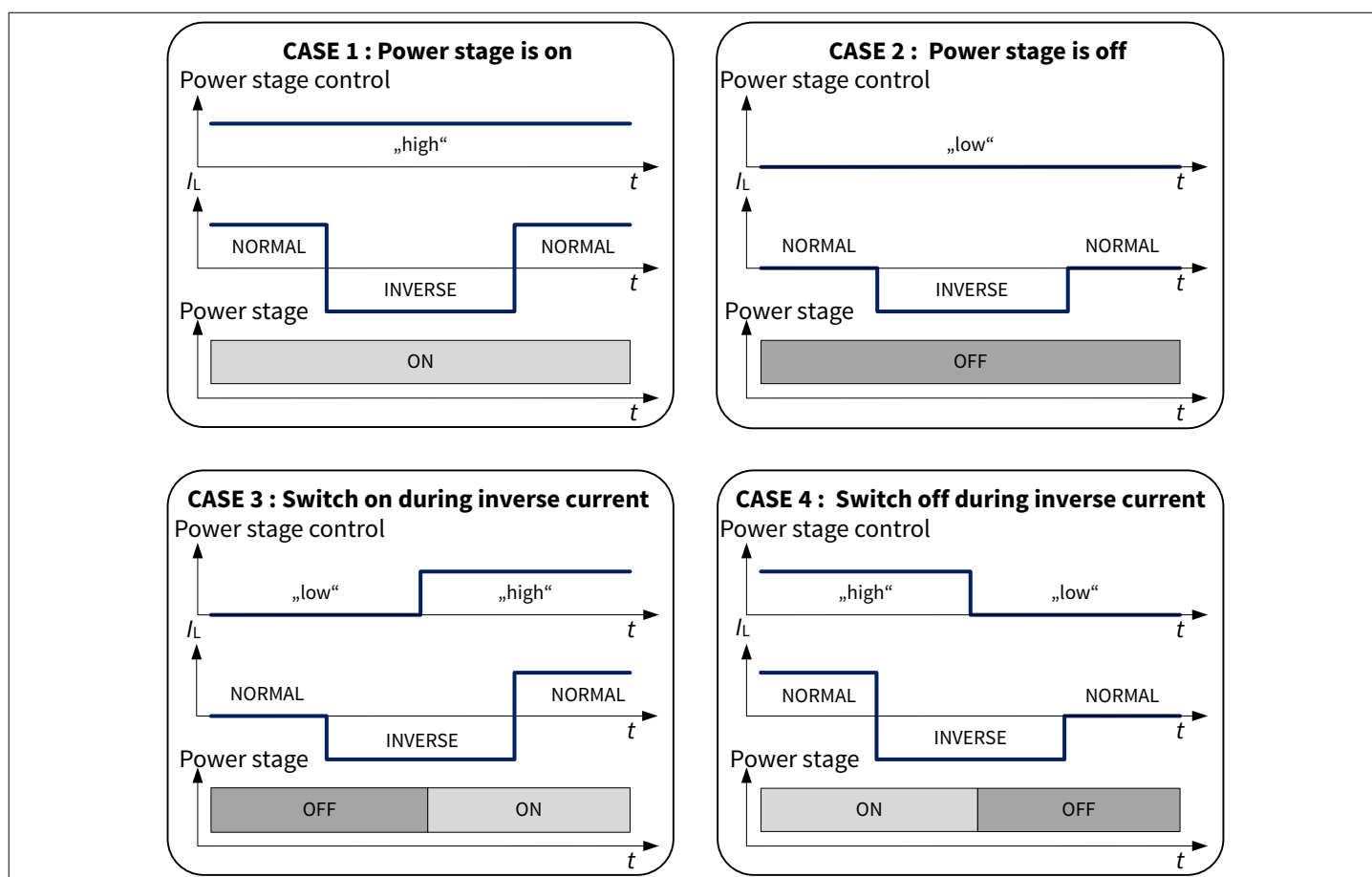


Figure 22 InverseON - Channel behavior in case of applied inverse current

## 6.4 Electrical characteristics power stage

$V_S = 4\text{ V to } 20\text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTG7050-1EPL:  $R_L = 4.7 \Omega$

**Table 8**                      **Electrical characteristics power stage**

| Parameter                                      | Symbol          | Values |      |      | Unit | Note or condition                                                                | P-Number |
|------------------------------------------------|-----------------|--------|------|------|------|----------------------------------------------------------------------------------|----------|
|                                                |                 | Min.   | Typ. | Max. |      |                                                                                  |          |
| Voltages                                       |                 |        |      |      |      |                                                                                  |          |
| Drain to source clamping voltage at TJ = -40°C | VDS(CLAMP)_-40  | 33     | 36.5 | 42   | V    | IL = 5 mA<br>TJ = -40°C<br>See <a href="#">Chapter 6.2.2</a>                     | PRQ-110  |
| Drain to source clamping voltage at TJ ≥ 25°C  | VDS(CLAMP)_25   | 35     | 38   | 44   | V    | <sup>1)</sup><br>IL = 5 mA<br>TJ ≥ 25°C<br>See <a href="#">Chapter 6.2.2</a>     | PRQ-111  |
| Timings                                        |                 |        |      |      |      |                                                                                  |          |
| Switch-ON delay                                | tON(DELAY)      | 10     | 70   | 130  | μs   | VS = 13.5 V<br>VOUT = 10% VS<br>IOCT = IOCT,MAX<br>See <a href="#">Figure 17</a> | PRQ-112  |
| Switch-OFF delay                               | tOFF(DELAY)     | 10     | 50   | 160  | μs   | VS = 13.5 V<br>VOUT = 90% VS<br>IOCT = IOCT,MAX<br>See <a href="#">Figure 17</a> | PRQ-113  |
| Switch-ON time                                 | tON             | 50     | 130  | 210  | μs   | VS = 13.5 V<br>VOUT = 90% VS<br>IOCT = IOCT,MAX<br>See <a href="#">Figure 17</a> | PRQ-114  |
| Switch-OFF time                                | tOFF            | 30     | 100  | 220  | μs   | VS = 13.5 V<br>VOUT = 10% VS<br>IOCT = IOCT,MAX<br>See <a href="#">Figure 17</a> | PRQ-115  |
| CLS activation delay                           | tON_CLS(DELAY)  | 10     | 70   | 200  | μs   | VS = 13.5 V<br>IOCT = IOCT,MAX<br>See <a href="#">Figure 19</a>                  | PRQ-664  |
| CLS de-activation delay                        | tOFF_CLS(DELAY) | 20     | 40   | 90   | μs   | VS = 13.5 V<br>IOCT = IOCT,MAX<br>See <a href="#">Figure 19</a>                  | PRQ-665  |
| Switch-ON/OFF Matching - tON - tOFF            | ΔtSW            | -60    | 25   | 90   | μs   | VS = 13.5V<br>IOCT = IOCT,MAX                                                    | PRQ-116  |

**(table continues...)**

**Table 8** (continued) **Electrical characteristics power stage**

| Parameter                                                              | Symbol                        | Values |       |       | Unit    | Note or condition                                                                                                     | P-Number |
|------------------------------------------------------------------------|-------------------------------|--------|-------|-------|---------|-----------------------------------------------------------------------------------------------------------------------|----------|
|                                                                        |                               | Min.   | Typ.  | Max.  |         |                                                                                                                       |          |
| Voltage slope                                                          |                               |        |       |       |         |                                                                                                                       |          |
| Switch-ON slew rate                                                    | (dV/dt) <sub>ON</sub>         | 0.16   | 0.27  | 0.39  | V/μs    | V <sub>S</sub> = 13.5 V<br>I <sub>OCT</sub> = I <sub>OCT,MAX</sub><br>V <sub>OUT</sub> = 30% to 70% of V <sub>S</sub> | PRQ-117  |
| Switch-OFF slew rate                                                   | (dV/dt) <sub>OFF</sub>        | -0.39  | -0.27 | -0.16 | V/μs    | V <sub>S</sub> = 13.5V<br>I <sub>OCT</sub> = I <sub>OCT,MAX</sub><br>V <sub>OUT</sub> = 70% to 30% of V <sub>S</sub>  | PRQ-118  |
| Slew rate matching -<br>(dV/dt)ON + (dV/dt)OFF                         | Δ(dV/dt) <sub>SW</sub>        | -0.15  | 0     | 0.15  | V/μs    | V <sub>S</sub> = 13.5V<br>I <sub>OCT</sub> = I <sub>OCT,MAX</sub>                                                     | PRQ-119  |
| CLS mode                                                               |                               |        |       |       |         |                                                                                                                       |          |
| Input frequency<br>for capacitive load<br>switching mode<br>activation | f <sub>VIN(CLS)</sub>         | 22     | 30    | 38    | kHz     | 2)<br>DC <sub>VIN(CLS)</sub> = 50%                                                                                    | PRQ-353  |
| Duty cycle for<br>capacitive load<br>switching mode<br>activation      | DC <sub>VIN(CLS)</sub>        | 30%    | 50%   | 70%   | –       | 2)<br>f <sub>VIN(CLS)</sub> = 30 kHz                                                                                  | PRQ-354  |
| Maximum time in CLS<br>mode                                            | t <sub>CLS1</sub>             | –      | –     | 25    | ms      | 2)<br>See Chapter 6.2.3                                                                                               | PRQ-355  |
| Maximum time in CLS<br>mode                                            | t <sub>CLS2</sub>             | –      | –     | 90    | ms      | 2)<br>See Chapter 6.2.3                                                                                               | PRQ-813  |
| Maximum number of<br>CLS mode activations                              | n <sub>CLS_ACT1</sub>         | –      | –     | 500   | kcycles | 2)<br>See Chapter 6.2.3                                                                                               | PRQ-812  |
| Maximum number of<br>CLS mode activations                              | n <sub>CLS_ACT2</sub>         | –      | –     | 50    | kcycles | 2)<br>See Chapter 6.2.3                                                                                               | PRQ-814  |
| Output characteristics                                                 |                               |        |       |       |         |                                                                                                                       |          |
| ON-state resistance at<br>T <sub>J</sub> = 25°C                        | R <sub>DS(ON)_25</sub>        | –      | 50    | –     | mΩ      | 2)<br>T <sub>J</sub> = 25°C                                                                                           | PRQ-793  |
| ON-state resistance at<br>T <sub>J</sub> = 150°C                       | R <sub>DS(ON)_150</sub>       | –      | –     | 100   | mΩ      | T <sub>J</sub> = 150°C<br>I <sub>L</sub> = 2 A                                                                        | PRQ-794  |
| ON-state resistance in<br>cranking at T <sub>J</sub> = 150°C           | R <sub>DS(ON)_CRANK_150</sub> | –      | –     | 110   | mΩ      | T <sub>J</sub> = 150°C<br>V <sub>S</sub> = 3.1 V<br>I <sub>L</sub> = 1 A                                              | PRQ-795  |

**(table continues...)**

**Table 8** (continued) Electrical characteristics power stage

| Parameter                                                           | Symbol            | Values |      |      | Unit | Note or condition                                                                               | P-Number |
|---------------------------------------------------------------------|-------------------|--------|------|------|------|-------------------------------------------------------------------------------------------------|----------|
|                                                                     |                   | Min.   | Typ. | Max. |      |                                                                                                 |          |
| ON-state resistance in inverse current at $T_J = 25^\circ\text{C}$  | $R_{DS(INV)_25}$  | –      | 50   | –    | mΩ   | 2)<br>$T_J = 25^\circ\text{C}$<br>$V_S = 13.5\text{ V}$<br>$I_L = -2\text{ A}$<br>See Figure 21 | PRQ-796  |
| ON-state resistance in inverse current at $T_J = 150^\circ\text{C}$ | $R_{DS(INV)_150}$ | –      | –    | 110  | mΩ   | $T_J = 150^\circ\text{C}$<br>$V_S = 13.5\text{ V}$<br>$I_L = -2\text{ A}$<br>See Figure 21      | PRQ-797  |
| Nominal load current per channel at $T_A = 85^\circ\text{C}$        | $I_{L(NOM)_85}$   | –      | 3    | –    | A    | 2)<br>$T_A = 85^\circ\text{C}$<br>$T_J \leq 150^\circ\text{C}$                                  | PRQ-798  |
| Output leakage current at $T_J \leq 85^\circ\text{C}$               | $I_{L(OFF)_85}$   | –      | 0.01 | 0.5  | μA   | 2)<br>$V_{OUT} = 0\text{ V}$<br>IN = "low"<br>$T_A \leq 85^\circ\text{C}$                       | PRQ-799  |
| Output leakage current at $T_J = 150^\circ\text{C}$                 | $I_{L(OFF)_150}$  | –      | 1.2  | 4    | μA   | $V_{OUT} = 0\text{ V}$<br>IN = "low"<br>$T_A = 150^\circ\text{C}$                               | PRQ-800  |
| Inverse Current Capability                                          | $I_{L(INV)}$      | –      | 3    | –    | A    | 2)<br>$V_S < V_{OUT}$<br>IN = "high"<br>See Figure 21                                           | PRQ-801  |

#### Voltages

|                            |                   |   |      |     |    |                                                     |         |
|----------------------------|-------------------|---|------|-----|----|-----------------------------------------------------|---------|
| Drain source diode voltage | $ V_{DS(DIODE)} $ | – | 550  | 700 | mV | $I_L = -190\text{ mA}$<br>$T_J = 150^\circ\text{C}$ | PRQ-802 |
| Switch-ON energy           | $E_{ON}$          | – | 1.2  | –   | mJ | 2)<br>$V_S = 20\text{ V}$<br>See Figure 17          | PRQ-803 |
| Switch-OFF energy          | $E_{OFF}$         | – | 1.25 | –   | mJ | 2)<br>$V_S = 20\text{ V}$<br>See Figure 17          | PRQ-804 |

1) Tested at  $T_J = 150^\circ\text{C}$

2) Not subject to production test - specified by design

## 7 Protection

The device is protected against overload, overtemperature and overvoltage.

Overtemperature and overload protection are operational in all operation modes, except when in sleep mode.

Overload protection is not active during inverse current condition.

Overtemperature and overload protection during inverse current condition is inactive on the channel which is in inverse condition.

Overvoltage protection is active in all operation modes.

### 7.1 Overcurrent protection

#### 7.1.1 Adjustable overcurrent threshold

The device is protected in case of overload and short circuit to ground.

The device offers an adjustable overcurrent limitation range from  $I_{LIM,MIN}$  to  $I_{LIM,MAX}$ . This feature offers protection against overstress for the load as well as for the power output stage. In case of DMOS temperature increase exceeding the device safe operating environment, overtemperature and dynamic temperature protection mechanism will be triggered as shown in [Figure 24](#) and [Figure 25](#).

For the adjustment of the current limitation for both output channels, the following equation can be considered:

$$I_{LIM} = (k_{ILIOCT} \cdot I_{OCT}) + \Delta I_{LIM} \quad \text{where,} \quad I_{OCT} = \frac{(I_{LIM} - \Delta I_{LIM})}{k_{ILIOCT}} \quad (2)$$

To select the proper resistor value  $R_{OCT}$  connected between the OCT pin and device ground, the following equation can be considered:

$$R_{OCT} = \frac{(V_{OCT} \cdot k_{ILIOCT})}{(I_{LIM} - \Delta I_{LIM})} \quad (3)$$

In case of an OCT pin open with the current not exceeding  $I_{OCT(OPEN)}$  the device will set the current limit value to  $I_{LIM(OCT(OPEN))}$ . In case of an OCT pin short to ground with the current exceeding  $I_{OCT(SHORT2GND)}$  the device will set the current limit value to  $I_{LIM(OCT(SHORT2GND))}$ . The behavior of how  $I_{OCT}$  is related to  $I_{LIM}$  is described in [Figure 23](#). However, due to the maximum rating of the allowed current through OCT pin  $I_{OCT}$ , it is not recommended to shorten the OCT pin to device GND. In the case of reverse battery condition, this could lead to violations of the maximum ratings, therefore  $I_{AI(REV)}$  needs to be considered.

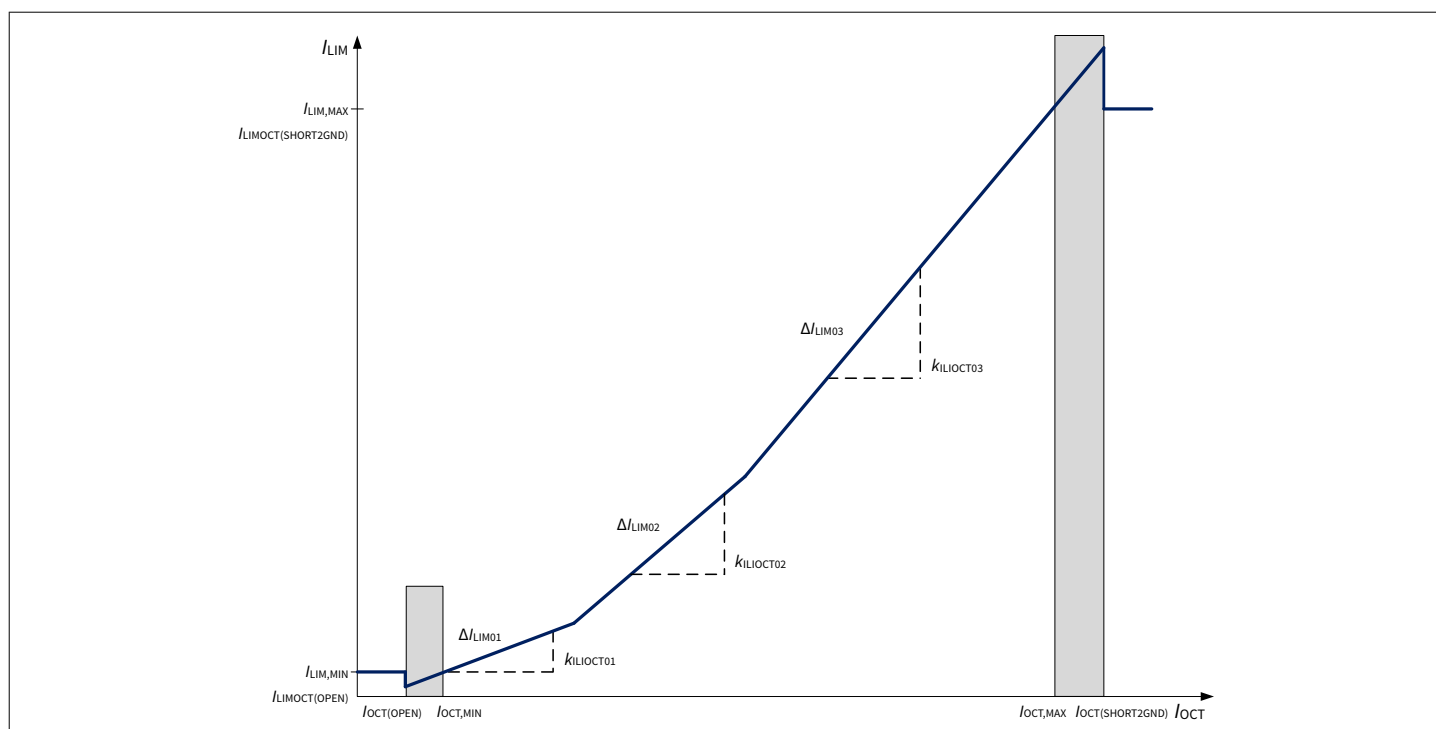


Figure 23 Adjustable overcurrent limitation behavior

## 7.2 Overtemperature protection

The device incorporates both an absolute ( $T_{J(ABS)}$ ) and a dynamic ( $T_{J(DYN)}$ ) temperature protection circuitry for each channel.

An increase in junction temperature  $T_J$  above either one of the two thresholds ( $T_{J(ABS)}$  or  $T_{J(DYN)}$ ) switches OFF the overheated channel. The affected channel will perform automatic restart attempts. The channel remains switched OFF until the junction temperature has reached the restart condition described in [Table 9](#) according to [Chapter 7.3.1](#). If the number of automatic restart attempts exceeds  $n_{RESTART(CR),TYP}$ , the affected channel latches OFF to prevent destruction. The behavior is shown in [Figure 24](#) and [Figure 25](#).  $T_{J(REF)}$  is the reference temperature used for dynamic temperature protection.

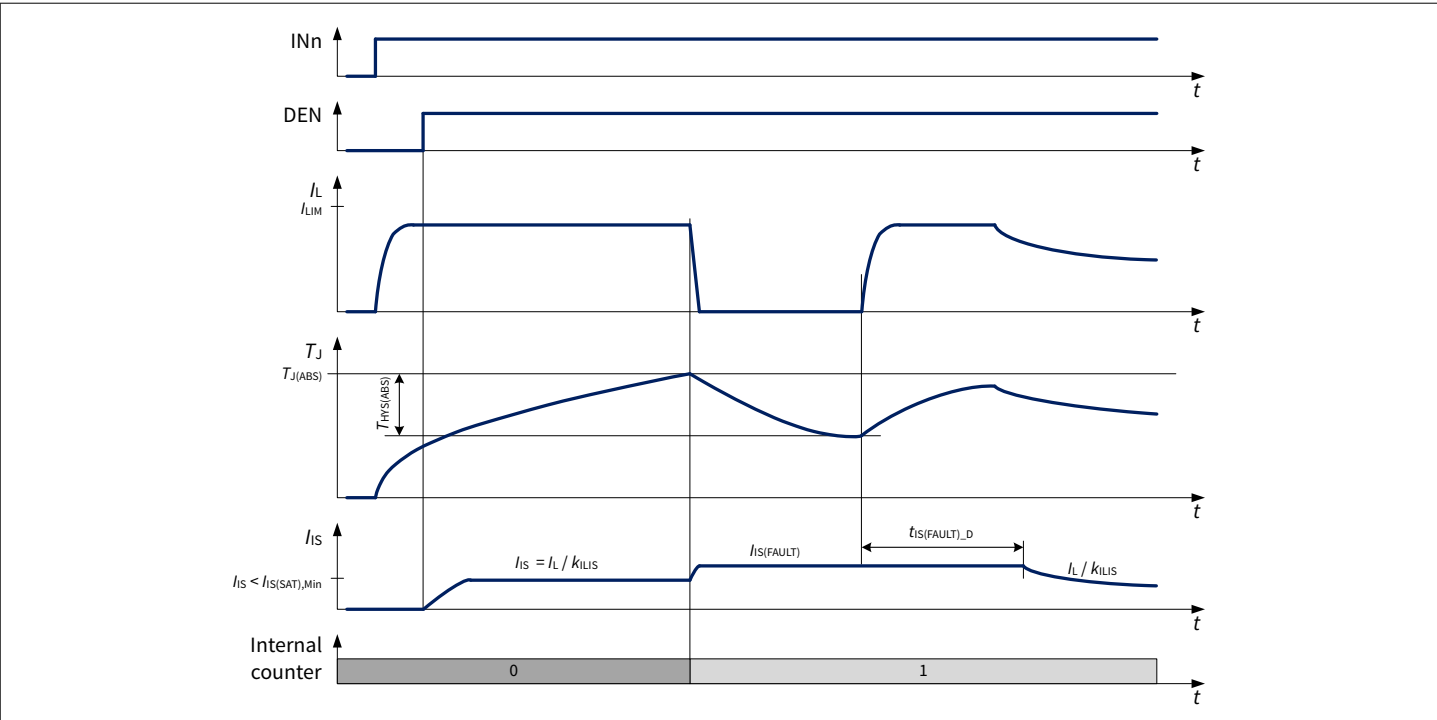


Figure 24 Overtemperature protection (absolute)

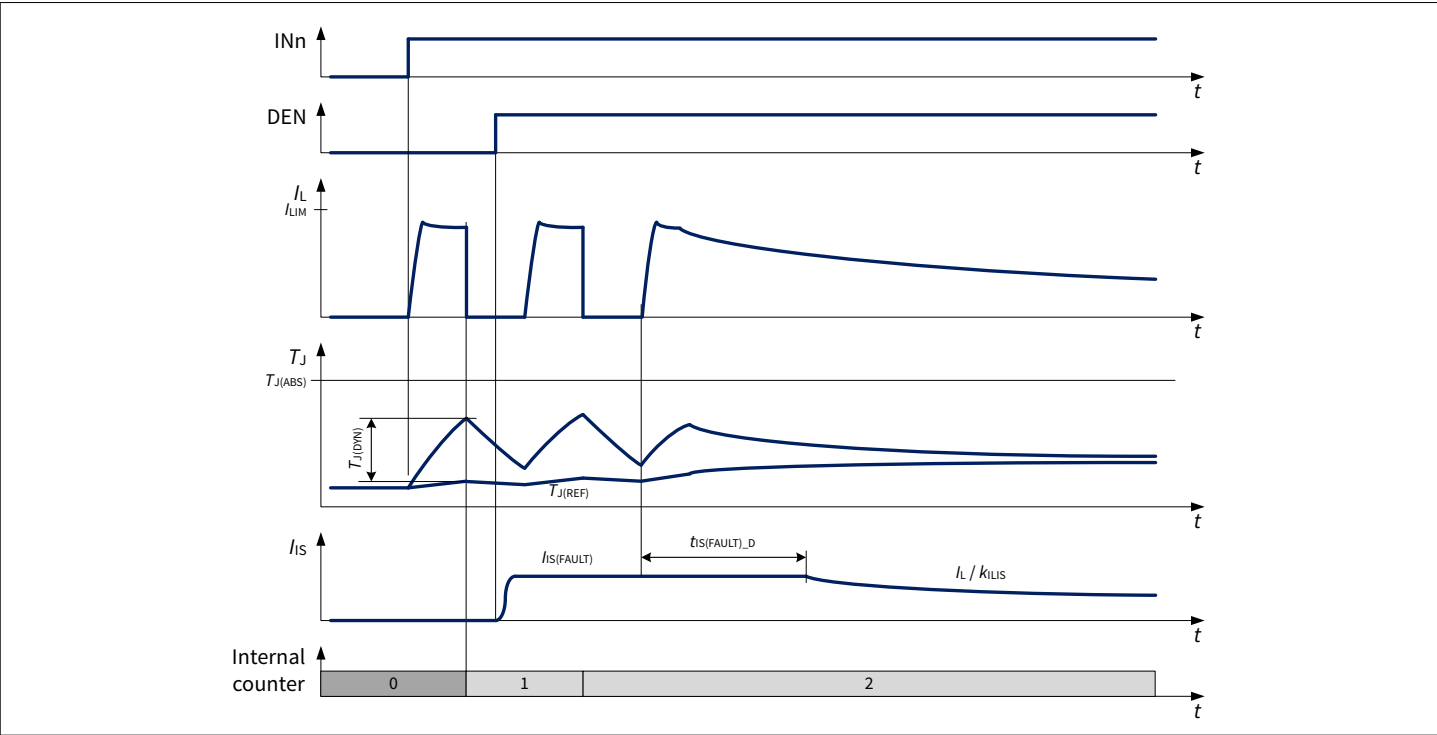


Figure 25 Overtemperature protection (dynamic)

When the overtemperature protection circuitry allows the channel to be switched ON again, the retry strategy described in [Chapter 7.3](#) is followed.

7.3 Protection and diagnosis in case of fault

Any event that triggers overtemperature protection has two consequences:

7 Protection

- The affected channel switches OFF according to [Chapter 7.3.1](#).
- If the diagnosis is active for the affected channel, a current  $I_{IS(FAULT)}$  is provided by IS pin (see [Chapter 8.2.2](#) for further details).

The channel can be switched ON again if all the protection mechanisms fulfill the “restart” conditions described in [Table 9](#) and  $n_{RESTART(CR)} < n_{RESTART(CR),typ}$ .

Table 9 Protection "restart" condition

| Fault condition | Switch OFF event                                              | "Restart" condition                                                             |
|-----------------|---------------------------------------------------------------|---------------------------------------------------------------------------------|
| Overtemperature | $T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$ | $T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis) |

7.3.1 Retry strategy

When IN is set to “high”, the power output stage is switched ON. If a fault condition is detected the power output stage is switched OFF. The device will apply the restart strategy and return to normal operation or latches OFF if the fault remains to be present after  $n_{RESTART(CR),TYP}$ .

The device has an internal retry counter  $n_{RESTART(CR)}$  (one for each channel) to maximize the robustness in case of fault.

The channel is allowed to switch ON for  $n_{RESTART(CR)}$  times before switching OFF. After  $n_{RESTART(CR),TYP}$  consecutive “restart” cycles, the channel latches OFF. To de-latch the power output stage and reset the internal counter it is necessary to set the input pin to “low” for a time longer than  $t_{DELAY(CR)}$ .

If the fault is no longer present and  $t_{DELAY(CR)}$  is observed the device will enter normal operation. In case the fault is still present, the device will trigger again the retry strategy.

The retry strategy is shown in [Figure 26](#).

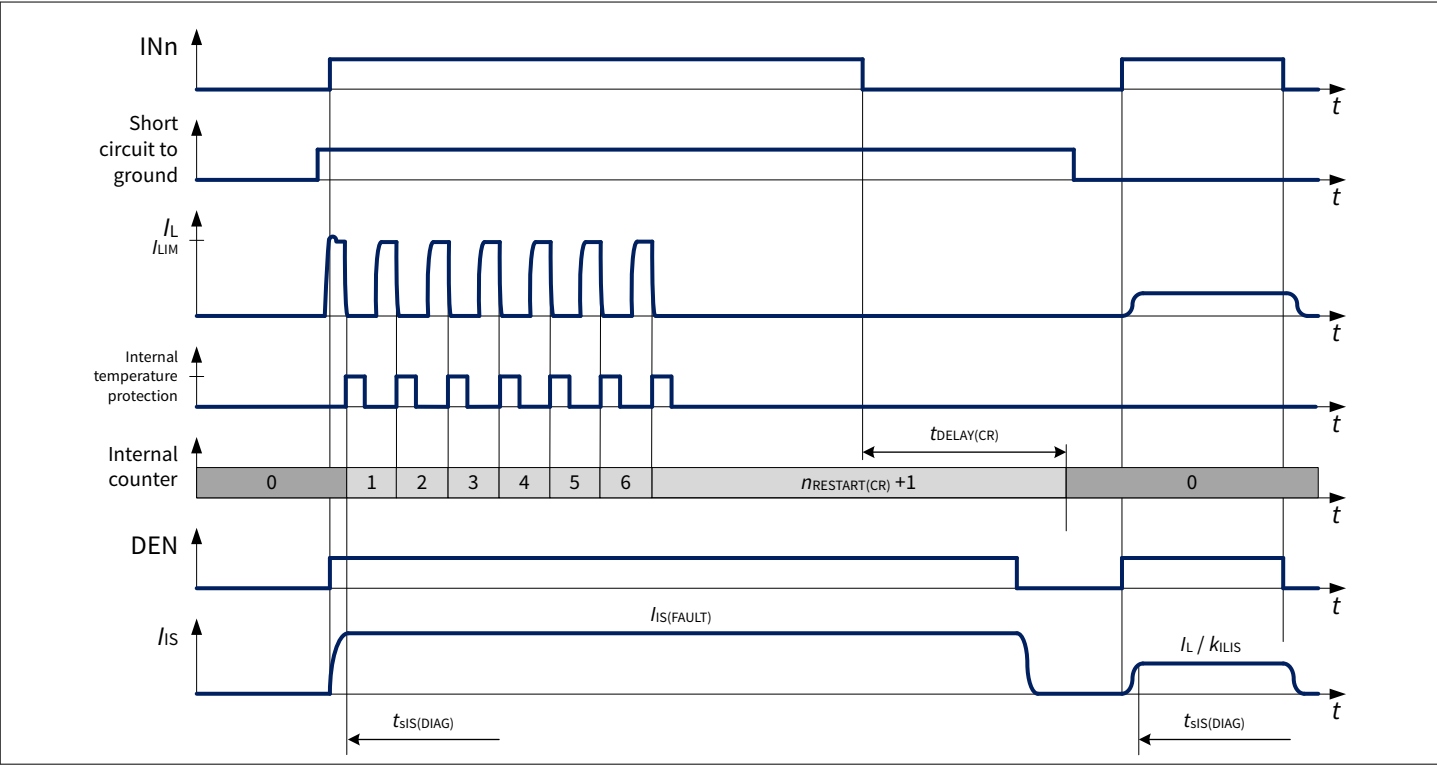


Figure 26 Retry strategy timing diagram

It is possible to “force” a reset of the internal counter without waiting for  $t_{DELAY(CR)}$  by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is “low”. The pulse applied to DEN pin must have a duration longer than  $t_{DEN(CR)}$  to ensure a reset of the internal counter.

The timings are shown in [Figure 27](#).

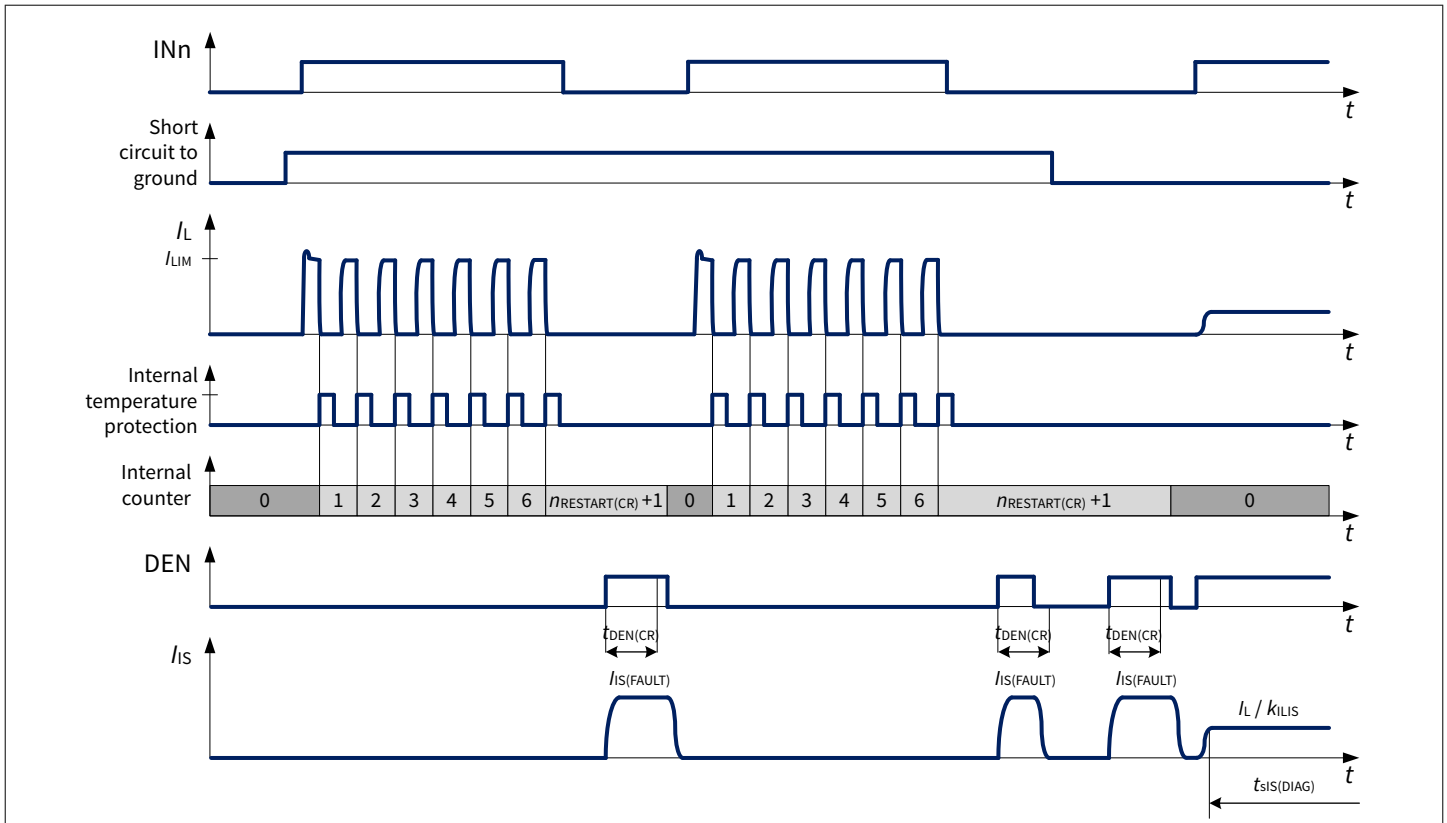


Figure 27 Retry strategy timing diagram with forced reset

## 7.4 Additional protection

### 7.4.1 Reverse polarity protection

In reverse polarity condition (also known as reverse battery), power dissipation is caused by the intrinsic body diode of the DMOS channel. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stages must be limited by the connected loads. The current through digital input pins has to be limited by an external resistor (please refer to the absolute maximum ratings listed in [Table 2](#) and to Application Information in [Chapter 9](#)).

### 7.4.2 Overvoltage protection

In the case of supply voltages between  $V_{S(EXT,UP)}$  and  $V_{BAT(LD)}$ , the output transistors are still operational and follow the input pin.

In addition to the output clamp for inductive loads as described in [Chapter 6.2.2](#), there is a clamp mechanism available for overvoltage protection for the logic and the output channels, monitoring the voltage between  $V_S$  and GND pins ( $V_{S(CLAMP)}$ ).

### 7.4.3 Loss of battery and loss of load

The loss of connection to the battery or the load does not influence device robustness as long as load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled.

The device can handle the inductivity of the wire harness up to 10  $\mu\text{H}$  with  $I_{L(NOM)}_{85}$ .

In case of applications where currents and/or the aforementioned inductivity are exceeded, an external suppressor diode (like diode  $D_{Z2}$  shown in [Chapter 9](#)) is recommended to handle the energy and to provide a well-defined path for the load current.

### 7.4.4 Loss of ground

It is recommended to have a resistor connected between any digital input pin and the microcontroller to ensure a channel switch OFF in case of a loss of device ground event (as described in [Chapter 9](#)).

#### Note

In case any digital input pin is pulled to ground (either by a resistor or active) a parasitic ground path is present, which could keep the device operational during a loss of device ground.

## 7.5 Electrical characteristics protection

$V_S = 4\text{ V to }20\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTG7050-1EPL:  $R_L = 4.7\ \Omega$

**Table 10** Electrical characteristics protection

| Parameter                                                                | Symbol               | Values |      |      | Unit             | Note or condition                                                                                           | P-Number |
|--------------------------------------------------------------------------|----------------------|--------|------|------|------------------|-------------------------------------------------------------------------------------------------------------|----------|
|                                                                          |                      | Min.   | Typ. | Max. |                  |                                                                                                             |          |
| Thermal shutdown temperature (absolute)                                  | $T_{J(ABS)}$         | 150    | 175  | 200  | $^\circ\text{C}$ | <sup>1) 2)</sup><br>See <a href="#">Figure 24</a>                                                           | PRQ-174  |
| Thermal shutdown hysteresis (absolute)                                   | $T_{HYS(ABS)}$       | –      | 30   | –    | K                | <sup>3)</sup><br>See <a href="#">Figure 24</a>                                                              | PRQ-356  |
| Thermal shutdown temperature (dynamic)                                   | $T_{J(DYN)}$         | –      | 80   | –    | K                | <sup>3)</sup><br>See <a href="#">Figure 24</a>                                                              | PRQ-357  |
| Thermal shutdown temperature (dynamic) in capacitive load switching mode | $T_{J(DYN)_CLS}$     | –      | 40   | –    | K                | <sup>3)</sup>                                                                                               | PRQ-177  |
| Power supply clamping voltage at $T_J = -40^\circ\text{C}$               | $V_{S(CLAMP)}_{-40}$ | 33     | 36.5 | 42   | V                | $I_{VS} = 5\text{ mA}$<br>$T_J = -40^\circ\text{C}$<br>See <a href="#">Chapter 6.2.2</a>                    | PRQ-179  |
| Power supply clamping voltage at $T_J \geq 25^\circ\text{C}$             | $V_{S(CLAMP)}_{25}$  | 35     | 38   | 44   | V                | <sup>2)</sup><br>$I_{VS} = 5\text{ mA}$<br>$T_J \geq 25^\circ\text{C}$<br>See <a href="#">Chapter 6.2.2</a> | PRQ-184  |
| Automatic restarts in case of fault after counter reset                  | $n_{RESTART(CR)}$    | –      | 6    | –    | –                | <sup>1)</sup><br>See <a href="#">Figure 26</a>                                                              | PRQ-186  |
| Counter reset delay time after fault condition                           | $t_{DELAY(CR)}$      | 40     | 70   | 100  | ms               | <sup>1)</sup><br>See <a href="#">Figure 26</a>                                                              | PRQ-188  |
| Minimum DEN pulse duration for counter reset                             | $t_{DEN(CR)}$        | 50     | 100  | 150  | $\mu\text{s}$    | <sup>3)</sup><br>See <a href="#">Figure 27</a>                                                              | PRQ-190  |

(table continues...)

**Table 10 (continued) Electrical characteristics protection**

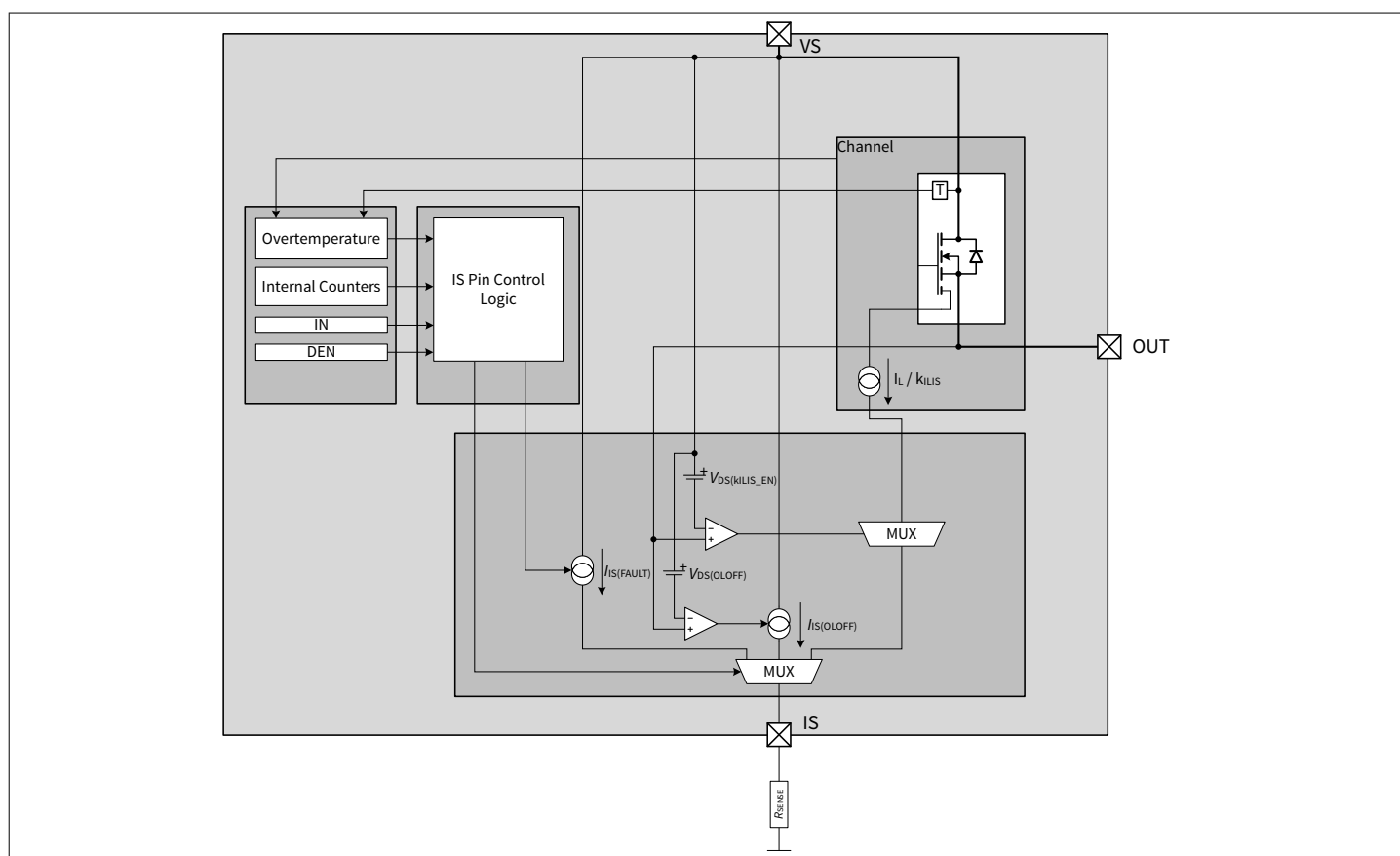
| Parameter                                                       | Symbol                  | Values |        |        | Unit | Note or condition                                                                         | P-<br>Number |
|-----------------------------------------------------------------|-------------------------|--------|--------|--------|------|-------------------------------------------------------------------------------------------|--------------|
|                                                                 |                         | Min.   | Typ.   | Max.   |      |                                                                                           |              |
| Adjustable overcurrent limitation                               |                         |        |        |        |      |                                                                                           |              |
| Adjustable overcurrent limitation accuracy (low)                | $I_{LIM(ACCURACY)}$     | -22.5% | –      | +22.5% | –    | <sup>3)</sup><br>$0.79\text{ A} \leq I_{LIM} < 1.67\text{ A}$<br>$V_{DS} = 3\text{ V}$    | PRQ-633      |
| Adjustable overcurrent limitation d-factor (low)                | $\Delta I_{LIM01}$      | –      | 0.102  | –      | A    | <sup>3)</sup><br>$0.79\text{ A} \leq I_{LIM} < 1.67\text{ A}$                             | PRQ-646      |
| Adjustable overcurrent limitation k-factor (low)                | $k_{ILIOCT01}$          | –      | 34449  | –      | –    | <sup>3)</sup><br>$0.79\text{ A} \leq I_{LIM} < 1.67\text{ A}$                             | PRQ-658      |
| Adjustable overcurrent limitation accuracy (medium)             | $I_{LIM(ACCURACY)}$     | -16%   | –      | +16%   | –    | <sup>3)</sup><br>$1.67\text{ A} \leq I_{LIM} < 3.27\text{ A}$<br>$V_{DS} = 3\text{ V}$    | PRQ-644      |
| Adjustable overcurrent limitation d-factor (medium)             | $\Delta I_{LIM02}$      | –      | -0.042 | –      | A    | <sup>3)</sup><br>$1.67\text{ A} \leq I_{LIM} < 3.27\text{ A}$                             | PRQ-647      |
| Adjustable overcurrent limitation k-factor (medium)             | $k_{ILIOCT02}$          | –      | 37301  | –      | –    | <sup>3)</sup><br>$1.67\text{ A} \leq I_{LIM} < 3.27\text{ A}$                             | PRQ-659      |
| Adjustable overcurrent limitation accuracy (high)               | $I_{LIM(ACCURACY)}$     | -18%   | –      | +18%   | –    | <sup>3)</sup><br>$3.27\text{ A} \leq I_{LIM} \leq 8.86\text{ A}$<br>$V_{DS} = 3\text{ V}$ | PRQ-634      |
| Adjustable overcurrent limitation d-factor (high)               | $\Delta I_{LIM03}$      | –      | -0.374 | –      | A    | <sup>3)</sup><br>$3.27\text{ A} \leq I_{LIM} \leq 8.86\text{ A}$                          | PRQ-648      |
| Adjustable overcurrent limitation k-factor (high)               | $k_{ILIOCT03}$          | –      | 40512  | –      | –    | <sup>3)</sup><br>$3.27\text{ A} \leq I_{LIM} \leq 8.86\text{ A}$                          | PRQ-660      |
| Current limitation value in case OCT pin open                   | $I_{LIMOCT(OPEN)}$      | 0.52   | 0.74   | 0.97   | A    | <sup>4)</sup><br>$I_{OCT} \leq I_{OCT(OPEN)}$                                             | PRQ-661      |
| Current limitation value in case OCT pin short to device ground | $I_{LIMOCT(SHORT2GND)}$ | 7.45   | 9.48   | 11.5   | A    | <sup>4)</sup><br>$I_{OCT} \geq I_{OCT(SHORT2GND)}$                                        | PRQ-662      |

- 1) Functional test only  
2) Tested at  $T_J = 150^\circ\text{C}$  only  
3) Not subject to production test - specified by design  
4) Tested at  $T_J = -40^\circ\text{C}$  only

A typical value is  $R_{\text{SENSE}} = 1.2 \text{ k}\Omega$ .

Due to the internal connection between IS pin and  $V_S$  supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed.

See [Figure 28](#) for details as an overview.



**Figure 28**                      **Diagnosis block diagram**

## 8.1 Overview

Table 11 gives a quick reference to the state of the IS pin during the device operation.

**Table 11**                      **SENSE signal as a function of application condition**

| Operation mode   | Input level | DEN level | V <sub>OUT</sub> | Diagnostic output                             |
|------------------|-------------|-----------|------------------|-----------------------------------------------|
| Normal operation | LOW/OFF     | HIGH      | ~ GND            | Z<br>$I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$ |

**(table continues...)**

**Table 11** (continued) **SENSE signal as a function of application condition**

| Operation mode                          | Input level    | DEN level | V <sub>OUT</sub>                                        | Diagnostic output                                                             |
|-----------------------------------------|----------------|-----------|---------------------------------------------------------|-------------------------------------------------------------------------------|
| Short circuit to GND                    |                |           | ~ GND                                                   | Z<br>$I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$                                 |
| Thermal shutdown temperature (absolute) |                |           | Z                                                       | $I_{IS(FAULT)}$                                                               |
| Thermal shutdown temperature (dynamic)  |                |           | Z                                                       | $I_{IS(FAULT)}$                                                               |
| Short circuit to V <sub>S</sub>         |                |           | = V <sub>S</sub>                                        | $I_{IS(OLOFF)}$<br>$I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$                   |
| Open load                               |                |           | < V <sub>S</sub> - V <sub>DS(OLOFF)</sub>               | Z                                                                             |
|                                         |                |           | > V <sub>S</sub> - V <sub>DS(OLOFF)</sub> <sup>1)</sup> | $I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$<br>if $n_{RESTART(CR)} > 0$ for both cases |
| Overcurrent pin fault                   |                |           | < V <sub>S</sub> - V <sub>DS(OLOFF)</sub>               | $I_{IS(OCT\_PIN\_FAULT)}$                                                     |
|                                         |                |           | > V <sub>S</sub> - V <sub>DS(OLOFF)</sub> <sup>1)</sup> | $I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$<br>if $n_{RESTART(CR)} > 0$ for both cases |
| Inverse current                         |                |           | ~ V <sub>INV</sub> = V <sub>OUT</sub> > V <sub>S</sub>  | $I_{IS(OLOFF)}$ or $I_{IS(FAULT)}$ if $n_{RESTART(CR)} > 0$                   |
| Normal operation                        |                |           | < V <sub>S</sub> - V <sub>DS(KILIS_EN)</sub>            | $I_{IS} = I_L / k_{ILIS}$                                                     |
| Short circuit to GND                    | HIGH/ON or CLS |           | ~ GND                                                   | $I_{IS(FAULT)}$                                                               |
| Thermal shutdown temperature (absolute) |                |           | Z                                                       | $I_{IS(FAULT)}$                                                               |
| Thermal shutdown temperature (dynamic)  |                |           | Z                                                       | $I_{IS(FAULT)}$                                                               |
| Short circuit to V <sub>S</sub>         |                |           | = V <sub>S</sub>                                        | $I_{IS} < I_L / k_{ILIS}$                                                     |
| Open load                               |                |           | ~ V <sub>S</sub> <sup>2)</sup>                          | $I_{IS} = I_{IS(EN)}$                                                         |
| Inverse current                         |                |           | ~ V <sub>INV</sub> = V <sub>OUT</sub> > V <sub>S</sub>  | $I_{IS} = I_{IS(EN)}$                                                         |
| Current limitation                      |                |           | < V <sub>S</sub>                                        | $I_{IS(FAULT)}$                                                               |
| Underload                               |                |           | ~ V <sub>S</sub> <sup>3)</sup>                          | $I_{IS(EN)} < I_{IS} < I_{L(NOM)} / k_{ILIS}$                                 |
| All conditions                          | n.a.           | LOW       | n.a.                                                    | Z                                                                             |

1) With additional pull up resistor

2) The output current has to be smaller than  $I_{L(OL)}$

3) The output current has to be higher than  $I_{L(OL)}$

### 8.1.1 SENSE signal truth table

Diagnosis can be activated or deactivated using the DEN pin, [Table 12](#).

**Table 12** Diagnostic truth table

| DEN    | IS           |
|--------|--------------|
| "low"  | Z            |
| "high" | SENSE output |

## 8.2 Diagnosis in ON state

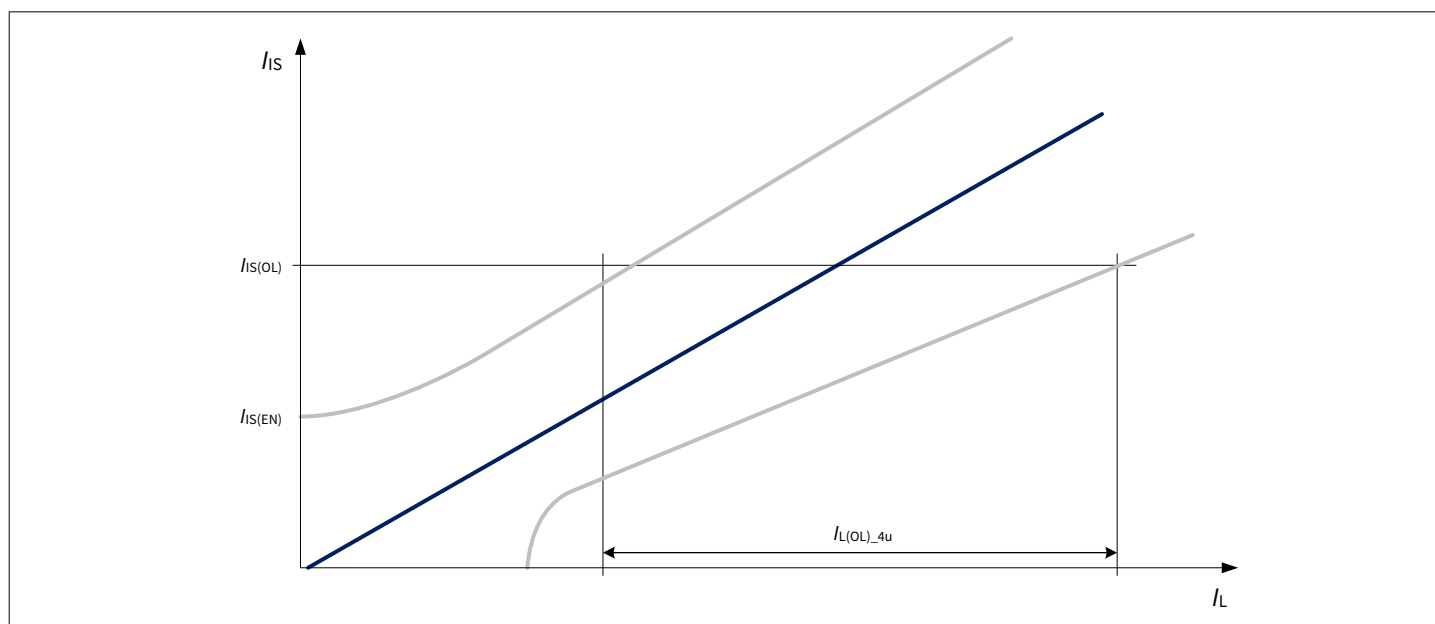
A current proportional to the load current ( $I_{IS} = I_L / k_{ILIS}$ ) is provided at pin IS when the following conditions are fulfilled:

- The power output stage is switched ON with  $V_{DS} < V_{DS(kILIS\_EN)}$
- The diagnosis is enabled for that channel
- No fault (as described in [Chapter 7.3](#)) is present or was present and not cleared yet (see [Chapter 8.2.2](#) for further details)

As long as a fault is present or was present and not cleared yet a current  $I_{IS(FAULT)}$  is provided at IS pin.

### 8.2.1 Current sense ( $k_{ILIS}$ )

$I_{IS}$  increases linearly with  $I_L$  output current until it reaches the saturation current  $I_{IS(SAT)}$ . In case of open load at the output stage ( $I_L$  close to 0 A), the maximum sense current  $I_{IS(EN)}$  (no load, diagnosis enabled) is specified. This condition is shown in [Figure 29](#). The center line represents the ideal  $k_{ILIS}$ , while the outer lines show the behavior of a typical product. An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1  $\mu$ s for the RC filter is recommended). The  $k_{ILIS}$  factor is specified with limits that take into account effects due to temperature, supply voltage, and manufacturing process.



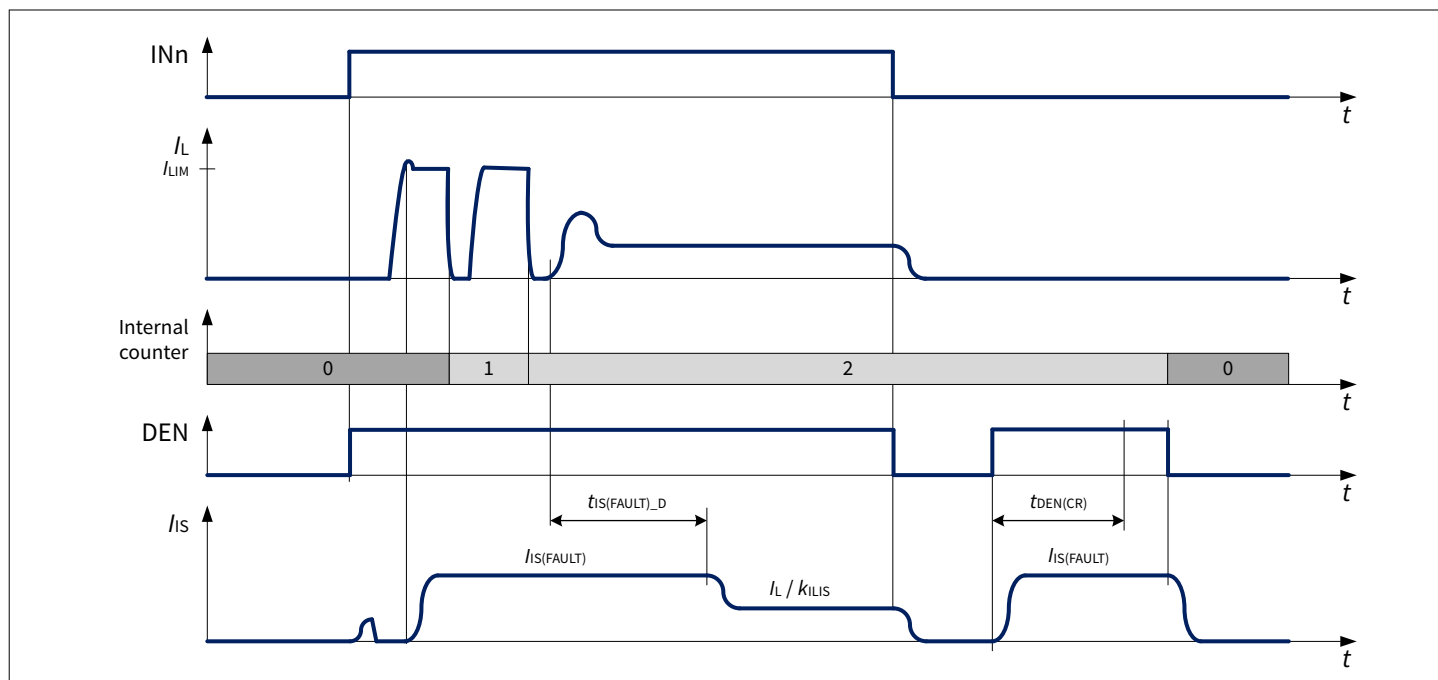
**Figure 29** Current sense ratio in open load at ON condition

### 8.2.2 Fault current ( $I_{IS(FAULT)}$ )

In case a fault is present and DEN is set to "high", a current  $I_{IS(FAULT)}$  is provided.

The following situations may occur:

- If the channel is ON and the number of restarts is less than " $n_{\text{RESTART}(\text{CR}),\text{TYP}}$ ", the current  $I_{\text{IS}(\text{FAULT})}$  is provided for a time  $t_{\text{IS}(\text{FAULT})\_D}$  after the channel is allowed to restart, and thereafter  $I_{\text{IS}} = I_{\text{L}}/k_{\text{ILIS}}$  (as shown in Figure 30). During a restart cycle the current  $I_{\text{IS}(\text{FAULT})}$  is provided each time the channel diagnosis is checked.
- If the channel is ON and the number of restarts is equal to " $n_{\text{RESTART}(\text{CR}),\text{TYP}}$ ", the current  $I_{\text{IS}(\text{FAULT})}$  is provided until the internal counter is reset. The internal counter can be cleared either by  $\text{INn} = \text{"low"}$  for  $t_{\text{DELAY}(\text{CR})}$  or by  $\text{INn} = \text{"low"}$  and DEN pin pulse for  $t_{\text{DEN}(\text{CR})}$ , as described in Chapter 7.3.1.
- While the channel is OFF and the internal counter value is not reset, the current  $I_{\text{IS}(\text{FAULT})}$  is provided.



**Figure 30**  $I_{\text{IS}(\text{FAULT})}$  at load switching

Figure 31 adds the behavior of SENSE signal to the timing diagram seen in Figure 26, while Figure 32 shows the relation between  $I_{\text{IS}} = I_{\text{L}}/k_{\text{ILIS}}$ ,  $I_{\text{IS}(\text{SAT})}$  and  $I_{\text{IS}(\text{FAULT})}$ .

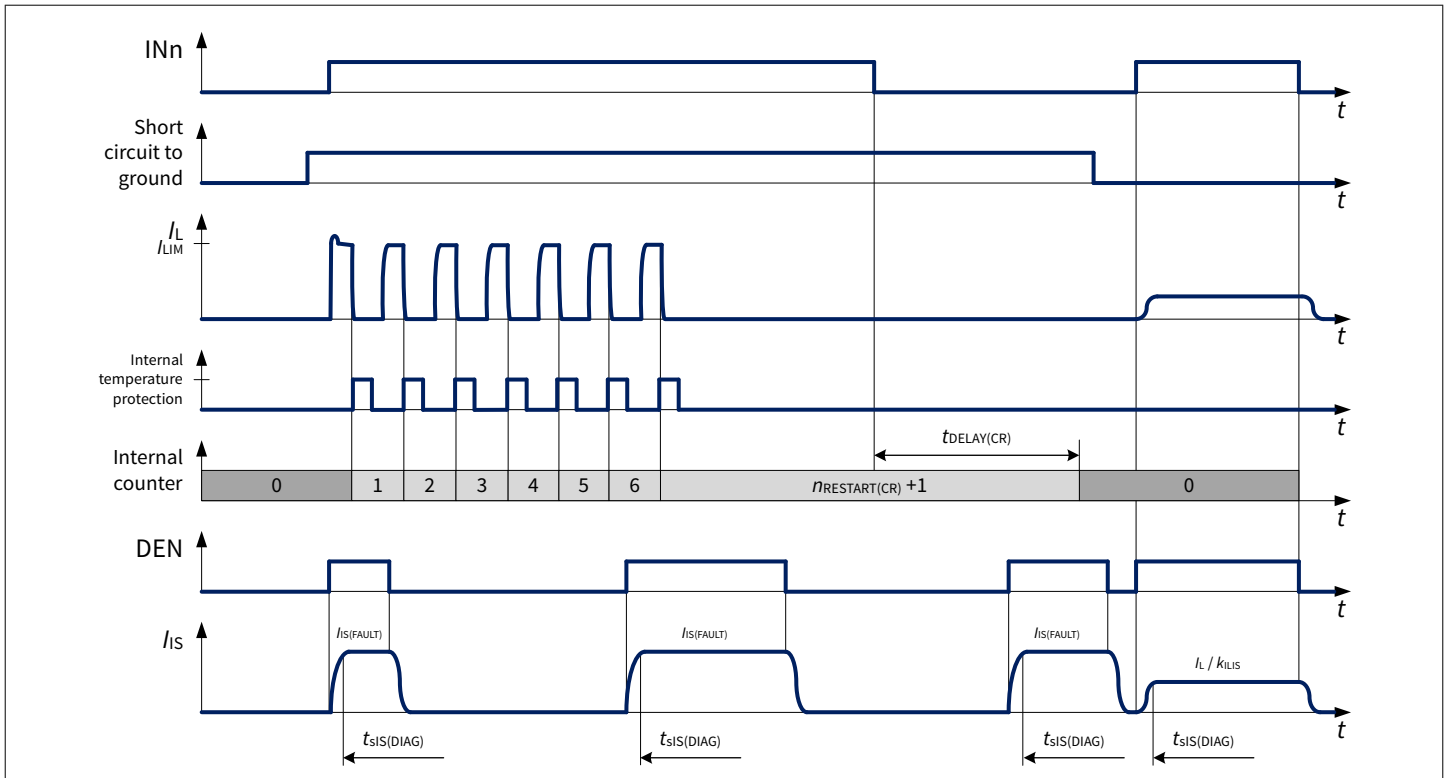


Figure 31 SENSE behavior in fault condition

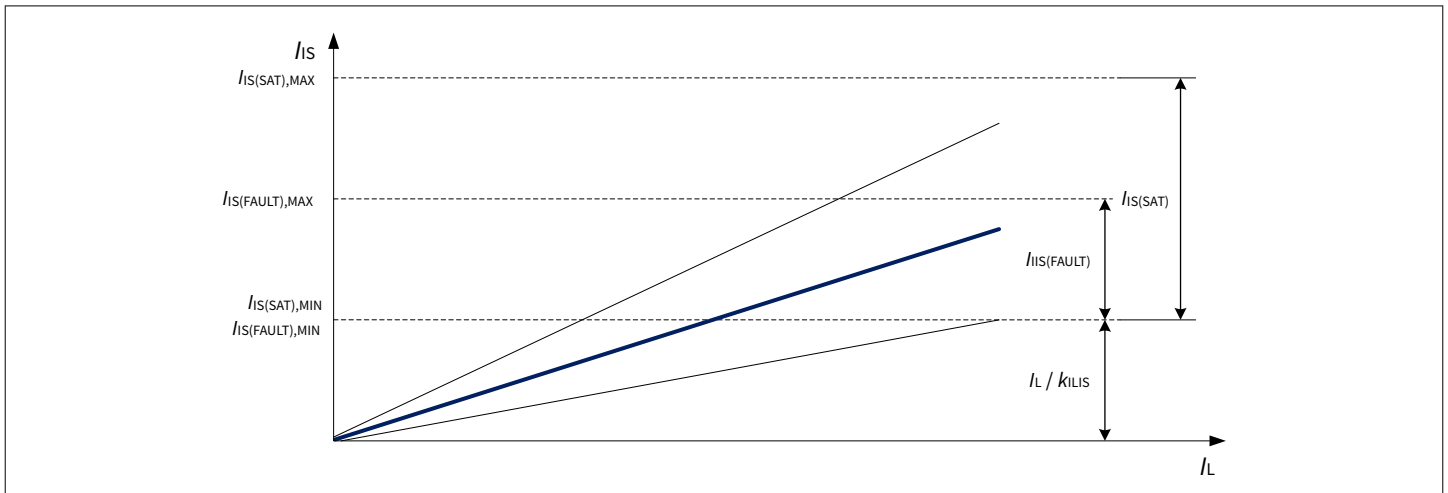


Figure 32 SENSE behavior - overview

### 8.3 Diagnosis in OFF State

When a power output stage is in OFF state, the device can measure the output voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source), it is possible to detect if the load is missing or if there is a short circuit to battery. If a fault condition was detected by the device (the internal counter has a value different from the reset value, as described in [Chapter 8.2.2](#) a current  $I_{IS(FAULT)}$  is provided by IS pin each time the channel diagnosis is checked also in OFF state. Additionally, the device can measure if the OCT pin is open  $I_{OCT(OPEN)}$  or shorted to device ground  $I_{OCT(SHORT2GND)}$ . In case of an fault condition on the OCT pin  $I_{IS(OCT\_PIN\_FAULT)}$  is provided. [Figure 33](#) shows the relationship between  $I_{IS(OLOFF)}$ ,  $I_{IS(FAULT)}$  and  $I_{IS(OCT\_PIN\_FAULT)}$  as functions of  $V_{DS}$ . The three currents do not overlap making it always possible to differentiate between open load in OFF, OCT pin fault and fault condition.

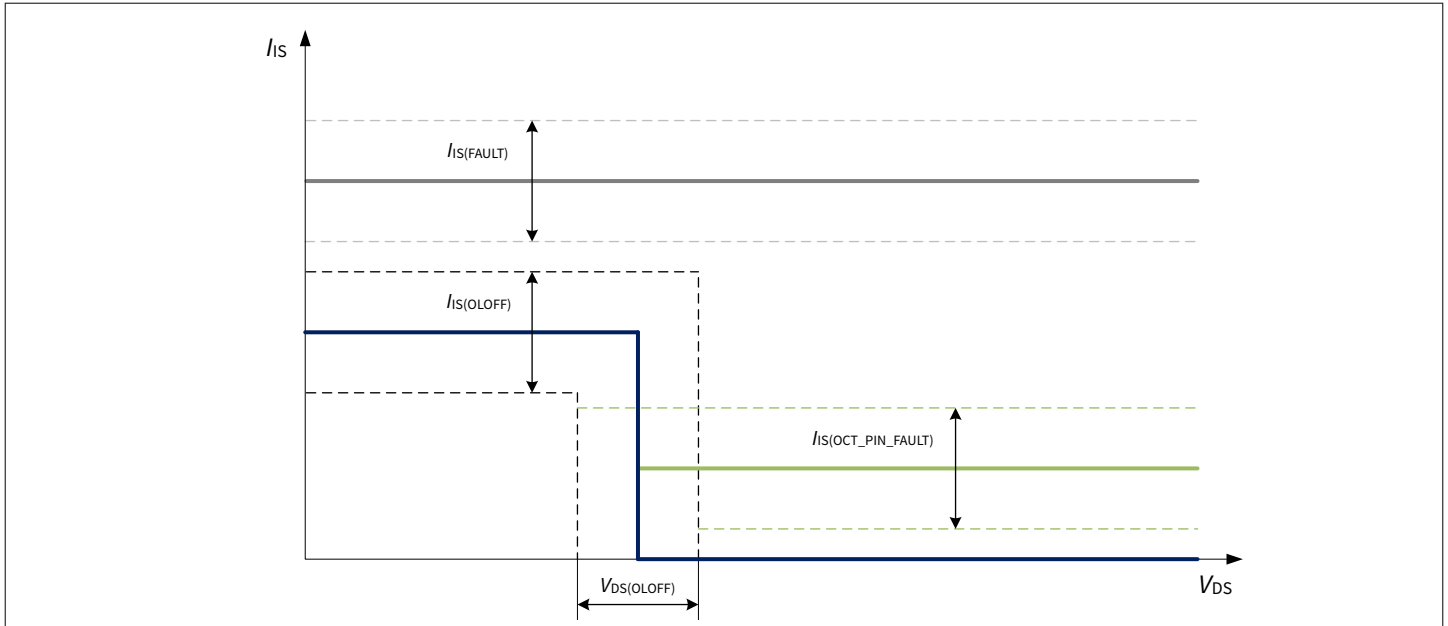


Figure 33  $I_{IS}$  in OFF state

### 8.3.1 Open load current

In OFF state, while DEN pin is set to “high”, the  $V_{DS}$  voltage is compared with a threshold voltage  $V_{DS(OLOFF)}$ . When the diagnosis is active and  $V_{DS} \leq V_{DS(OLOFF)}$ , a current  $I_{IS(OLOFF)}$  is provided by IS pin. If the load is properly connected and there is no short circuit to battery,  $V_{DS} \sim V_S$ , therefore,  $V_{DS} > V_{DS(OLOFF)}$  the IS pin is set to high impedance.

It is necessary to wait a time  $t_{IS(OLOFF)_D}$  between the falling edge of the input pin and the sensing at pin IS for Open Load in OFF diagnosis to allow the internal comparator to settle. In Figure 34 the timings for an Open Load detection are shown - the load is always disconnected.

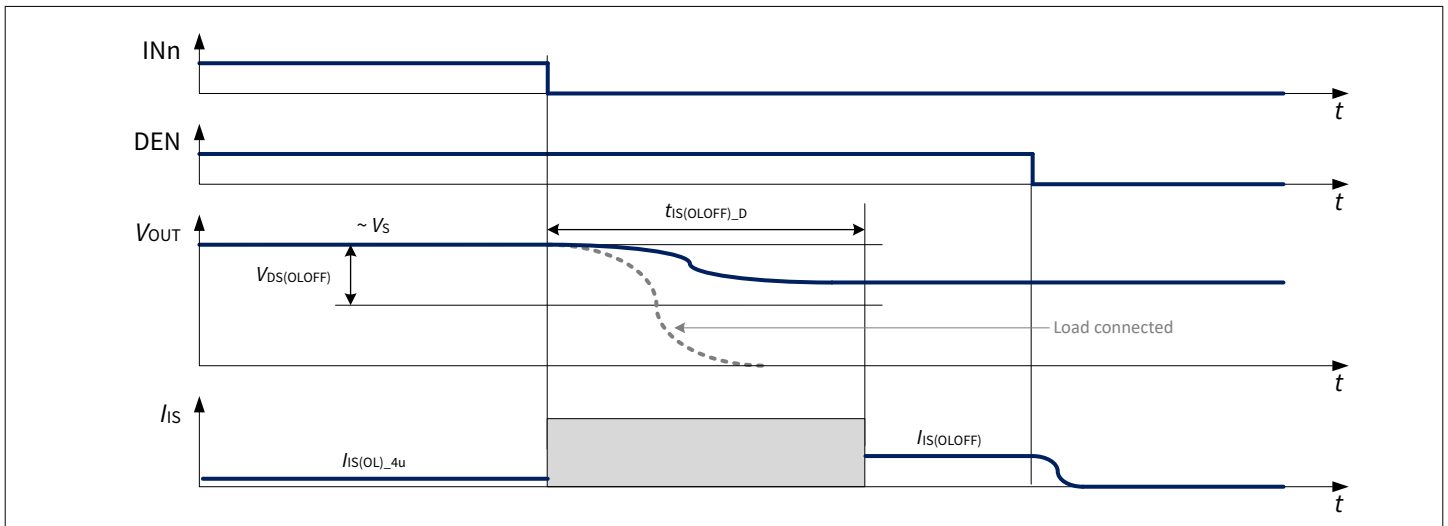


Figure 34 Open load in OFF timings - load disconnection

### 8.3.2 OCT pin fault current

When the device is in Inactive with Diagnosis mode and the OCT pin is open or shorted to device ground and  $V_{DS} \geq V_{DS(OLOFF)}$ , a current  $I_{IS(OCT\_PIN\_FAULT)}$  is provided by IS pin. Figure 33 shows  $I_{IS(OCT\_PIN\_FAULT)}$  as a function over  $V_{DS}$ .

## 8.4 SENSE timings

Figure 35 and Figure 36 show the timing during settling  $t_{\text{SIS(ON)}}$  and disabling  $t_{\text{SIS(OFF)}}$  of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before  $t_{\text{ON}}$ ),

$$t_{\text{SIS(DIAG)}} = t_{\text{SIS(ON)}} + t_{\text{ON}} \quad (4)$$

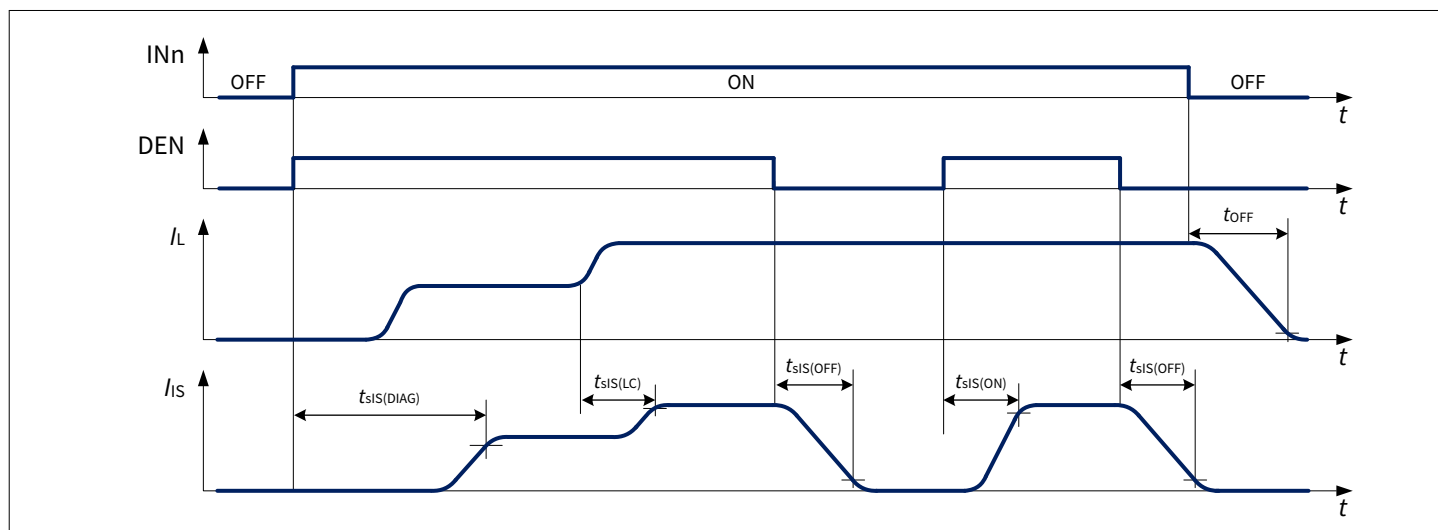


Figure 35 SENSE settling/disabling timing

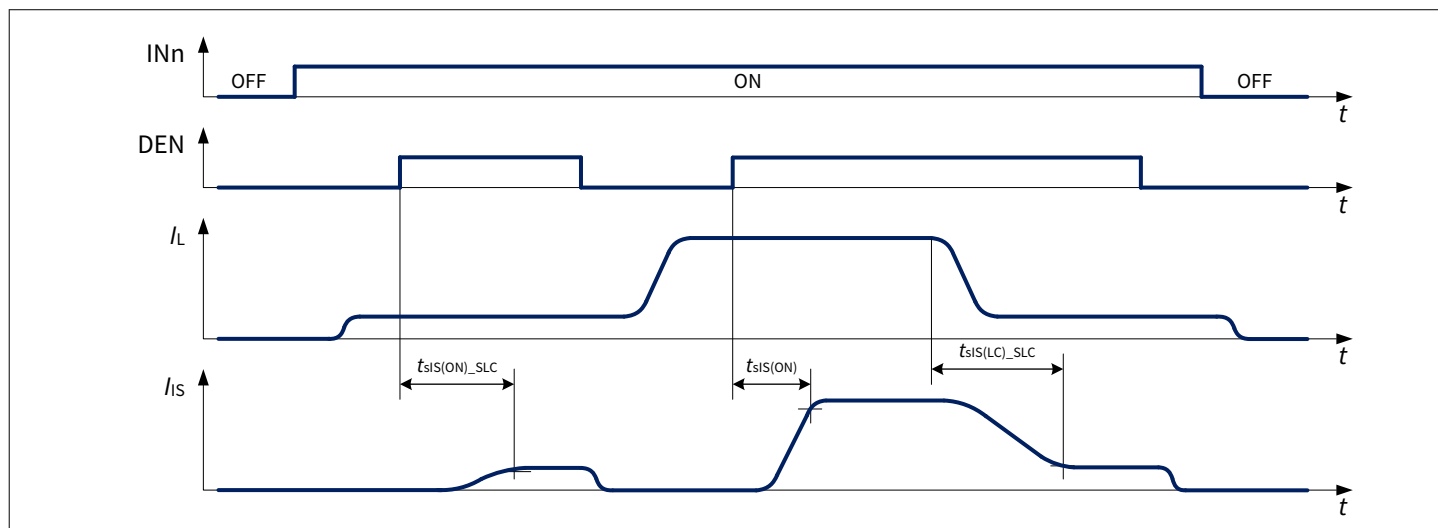


Figure 36 SENSE timing with small load current

## 8.5 Electrical characteristics diagnosis

$V_S = 4 \text{ V to } 20 \text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$

Unless otherwise specified typical values:  $V_S = 13.5 \text{ V}$ ,  $T_J = 25^\circ\text{C}$

Typical resistive loads connected to the outputs for testing (unless otherwise specified):

BTG7050-1EPL:  $R_L = 4.7 \Omega$

**Table 13**                      **Electrical characteristics diagnosis**

| Parameter                                                         | Symbol            | Values |      |      | Unit          | Note or condition                                                                                                           | P-Number |
|-------------------------------------------------------------------|-------------------|--------|------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------|----------|
|                                                                   |                   | Min.   | Typ. | Max. |               |                                                                                                                             |          |
| SENSE saturation current                                          | $I_{IS(SAT)}$     | 4.4    | –    | 15   | mA            | <sup>1)</sup><br>$V_S = 6\text{ V to }20\text{ V}$<br>$R_{SENSE} = 1.2\text{ k}\Omega$<br>See <a href="#">Figure 32</a>     | PRQ-215  |
| SENSE leakage current when disabled                               | $I_{IS(OFF)}$     | –      | 0.01 | 0.5  | $\mu\text{A}$ | DEN = "low"<br>$I_L \geq I_{L(NOM)}$<br>$V_{IS} = 0\text{ V}$                                                               | PRQ-219  |
| SENSE leakage current when enabled at $T_J \leq 85^\circ\text{C}$ | $I_{IS(EN)_85}$   | –      | 0.2  | 2    | $\mu\text{A}$ | <sup>1)</sup><br>$T_J \leq 85^\circ\text{C}$<br>DEN = "high"<br>$I_L = 0\text{ A}$<br>See <a href="#">Figure 29</a>         | PRQ-221  |
| SENSE leakage current when enabled at $T_J = 150^\circ\text{C}$   | $I_{IS(EN)_150}$  | –      | 0.2  | 2    | $\mu\text{A}$ | $T_J = 150^\circ\text{C}$<br>DEN = "high"<br>$I_L = 0\text{ A}$<br>See <a href="#">Figure 29</a>                            | PRQ-223  |
| Saturation voltage in kILIS operation (VS-VIS)                    | $V_{SIS\_k}$      | –      | 0.5  | 1    | V             | <sup>1)</sup><br>$V_S = 5\text{ V}$<br>IN = DEN = "high"                                                                    | PRQ-226  |
| Saturation voltage in open load at OFF diagnosis (VS-VIS)         | $V_{SIS\_OL}$     | –      | 0.5  | 1    | V             | <sup>1)</sup><br>$V_S = 5\text{ V}$<br>IN = "low"<br>DEN = "high"                                                           | PRQ-682  |
| Saturation voltage in fault diagnosis (VS-VIS)                    | $V_{SIS\_F}$      | –      | 0.5  | 1    | V             | <sup>1)</sup><br>$V_S = 5\text{ V}$<br>IN = "low"<br>DEN = "high"<br>counter > 0                                            | PRQ-684  |
| Saturation voltage in OCT pin fault diagnosis (VS-VIS)            | $V_{SIS\_OCT\_F}$ | –      | 0.5  | 1    | V             | <sup>1)</sup><br>$V_S = 5\text{ V}$<br>IN = "low"<br>DEN = "high"<br>$I_{OCT}$<br>= $I_{OCT(SHORT2GND)}$ or $I_{OCT(OPEN)}$ | PRQ-686  |

**(table continues...)**

**Table 13** (continued) **Electrical characteristics diagnosis**

| Parameter                                                              | Symbol                                   | Values |      |      | Unit          | Note or condition                                                                                                                                                                                                                    | P-Number |
|------------------------------------------------------------------------|------------------------------------------|--------|------|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
|                                                                        |                                          | Min.   | Typ. | Max. |               |                                                                                                                                                                                                                                      |          |
| Power supply to IS pin clamping voltage at $T_J = -40^\circ\text{C}$   | $V_{\text{SIS}(\text{CLAMP})_{-40}}$     | 33     | 36.5 | 42   | V             | $I_{\text{IS}} = 1\text{mA}$<br>$T_J = -40^\circ\text{C}$<br>See <a href="#">Chapter 6.2.2</a>                                                                                                                                       | PRQ-294  |
| Power supply to IS pin clamping voltage at $T_J \geq 25^\circ\text{C}$ | $V_{\text{SIS}(\text{CLAMP})_{25}}$      | 35     | 38   | 44   | V             | <sup>2)</sup><br>$I_{\text{IS}} = 1\text{mA}$<br>$T_J \geq 25^\circ\text{C}$<br>See <a href="#">Chapter 6.2.2</a>                                                                                                                    | PRQ-296  |
| SENSE fault current                                                    | $I_{\text{IS}(\text{FAULT})}$            | 4.4    | 5.5  | 10   | mA            | See <a href="#">Chapter 8</a>                                                                                                                                                                                                        | PRQ-298  |
| SENSE open load in OFF current                                         | $I_{\text{IS}(\text{OLOFF})}$            | 1.9    | 2.5  | 3.5  | mA            | See <a href="#">Chapter 8</a>                                                                                                                                                                                                        | PRQ-306  |
| SENSE OCT pin FAULT in OFF current                                     | $I_{\text{IS}(\text{OCT\_PIN\_FAULT})}$  | 0.2    | 1.2  | 1.7  | mA            | See <a href="#">Figure 33</a>                                                                                                                                                                                                        | PRQ-621  |
| SENSE delay time at channel switch ON after last fault condition       | $t_{\text{IS}(\text{FAULT})_{\text{D}}}$ | –      | 500  | –    | $\mu\text{s}$ | <sup>1)</sup><br>See <a href="#">Figure 30</a>                                                                                                                                                                                       | PRQ-308  |
| SENSE open load in OFF delay time                                      | $t_{\text{IS}(\text{OLOFF})_{\text{D}}}$ | 70     | 185  | 300  | $\mu\text{s}$ | $V_{\text{DS}} < V_{\text{DS}(\text{OLOFF})}$ from INn falling edge to<br>$I_{\text{IS}} = I_{\text{IS}(\text{OLOFF}),\text{MIN}} \cdot 0.9$<br>DEN = “high”<br>$n_{\text{RESTART}(\text{CR})} = 0$<br>See <a href="#">Figure 34</a> | PRQ-310  |
| VDS threshold for KILIS enable                                         | $V_{\text{DS}(\text{KILIS\_EN})}$        | 0.8    | 1.2  | 1.4  | V             | <sup>1)</sup>                                                                                                                                                                                                                        | PRQ-809  |
| Open load VDS detection threshold in OFF state                         | $V_{\text{DS}(\text{OLOFF})}$            | 1.3    | 1.8  | 2.3  | V             | See <a href="#">Chapter 8.3</a>                                                                                                                                                                                                      | PRQ-313  |
| SENSE settling time with nominal load current stable                   | $t_{\text{SIS}(\text{ON})}$              | –      | 5    | 20   | $\mu\text{s}$ | $I_{\text{L}} = I_{\text{L}(\text{NOM})}$ from DEN rising edge to $I_{\text{IS}} = I_{\text{L}} / (k_{\text{ILIS},\text{MAX}} @ I_{\text{L}}) \cdot 0.9$<br>See <a href="#">Figure 35</a>                                            | PRQ-315  |
| SENSE settling time with small load current stable                     | $t_{\text{SIS}(\text{ON})_{\text{SLC}}}$ | –      | –    | 60   | $\mu\text{s}$ | <sup>1)</sup><br>$I_{\text{L}} = I_{\text{L01}}$ from DEN rising edge to $I_{\text{IS}} = I_{\text{L}} / (k_{\text{ILIS},\text{MAX}} @ I_{\text{L}}) \cdot 0.9$<br>See <a href="#">Figure 36</a>                                     | PRQ-317  |

(table continues...)

**Table 13** (continued) Electrical characteristics diagnosis

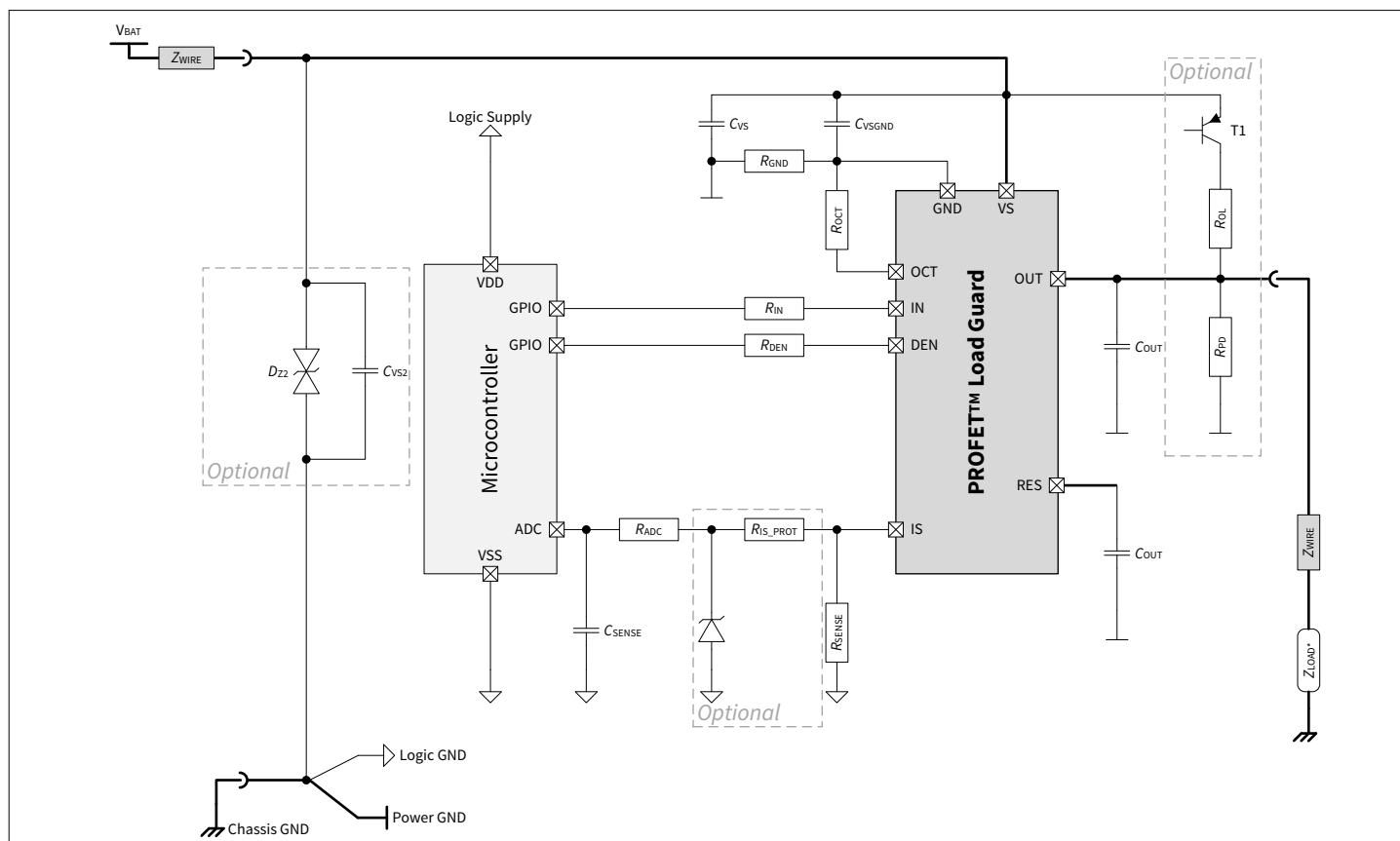
| Parameter                                                     | Symbol                   | Values |      |        | Unit          | Note or condition                                                                                                                           | P-Number |
|---------------------------------------------------------------|--------------------------|--------|------|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------|----------|
|                                                               |                          | Min.   | Typ. | Max.   |               |                                                                                                                                             |          |
| SENSE disable time                                            | $t_{\text{SIS(OFF)}}$    | –      | 5    | 20     | $\mu\text{s}$ | 1)<br>$I_L = I_{L(\text{NOM})}$<br>From DEN falling edge to $I_{\text{IS}} = I_{\text{IS(OFF)}}$<br>See Figure 35                           | PRQ-319  |
| SENSE settling time after load change                         | $t_{\text{SIS(LC)}}$     | –      | 5    | 20     | $\mu\text{s}$ | 1)<br>from $I_L = I_{L(\text{NOM})}/2$ to $I_L = I_{L(\text{NOM})}$<br>See Figure 35                                                        | PRQ-321  |
| SENSE settling time after load change with small load current | $t_{\text{SIS(LC)_SLC}}$ | –      | 250  | 400    | $\mu\text{s}$ | 1)<br>DEN = "high" from load change to $I_{\text{IS}} = I_L/(k_{\text{ILIS}} @ I_L)$ from $I_{L(\text{NOM})}$ to $I_{L01}$<br>See Figure 36 | PRQ-323  |
| Open load output current at $I_{\text{IS}} = 4 \mu\text{A}$   | $I_{L(\text{OL})\_4\mu}$ | 2      | 9.5  | 17     | mA            | $I_{\text{IS}} = I_{\text{IS(OL)}} = 4 \mu\text{A}$                                                                                         | PRQ-580  |
| Current sense ratio at $I_L = I_{L02}$                        | $k_{\text{ILIS02}}$      | -26%   | 2230 | +26%   | –             | $I_{L02} = 20 \text{ mA}$                                                                                                                   | PRQ-585  |
| Current sense ratio at $I_L = I_{L04}$                        | $k_{\text{ILIS04}}$      | -23.5% | 2030 | +23.5% | –             | $I_{L04} = 50 \text{ mA}$                                                                                                                   | PRQ-588  |
| Current sense ratio at $I_L = I_{L05}$                        | $k_{\text{ILIS05}}$      | -20%   | 2030 | +20%   | –             | $I_{L05} = 100 \text{ mA}$                                                                                                                  | PRQ-590  |
| Current sense ratio at $I_L = I_{L08}$                        | $k_{\text{ILIS08}}$      | -10%   | 2030 | +10%   | –             | $I_{L08} = 250 \text{ mA}$                                                                                                                  | PRQ-594  |
| Current sense ratio at $I_L = I_{L11}$                        | $k_{\text{ILIS11}}$      | -9.5%  | 2030 | +9.5%  | –             | $I_{L11} = 1 \text{ A}$                                                                                                                     | PRQ-598  |
| Current sense ratio at $I_L = I_{L13}$                        | $k_{\text{ILIS13}}$      | -6%    | 2030 | +6%    | –             | $I_{L13} = 2 \text{ A}$                                                                                                                     | PRQ-601  |
| Current sense ratio at $I_L = I_{L15}$                        | $k_{\text{ILIS15}}$      | -5%    | 2030 | +5%    | –             | $I_{L15} = 4 \text{ A}$                                                                                                                     | PRQ-604  |

1) Not subject to production test - specified by design

2) Tested at  $T_J = 150^\circ\text{C}$

## 9 Application information

**Note:** The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.



**Figure 37** Application diagram

**Table 14** Suggested component values

| Reference | Value                          | Purpose                                                                                                                                 |
|-----------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| $R_{IN}$  | 4.7 k $\Omega$                 | Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground     |
| $R_{DEN}$ | 4.7 k $\Omega$                 | Protection of the microcontroller during overvoltage and reverse polarity. Necessary to switch OFF the output during loss of ground     |
| $R_{OCT}$ | 2.2 k $\Omega$ - 25 k $\Omega$ | Adjustable overcurrent limitation resistor connected to device ground. Protection of the device during overvoltage and reverse polarity |
| $R_{PD}$  | 47 k $\Omega$                  | Output polarization (pull-down). Ensures polarization of the outputs to distinguish between open load and short to VS in OFF diagnosis  |
| $R_{OL}$  | 1.5 k $\Omega$                 | Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis                                      |
| $C_{OUT}$ | 10 nF                          | Protection of the output during ESD events and BCI                                                                                      |
| $T_1$     | BC 807                         | Switch the battery voltage for open load in OFF diagnosis                                                                               |
| $C_{VS}$  | 100 nF                         | Filtering of voltage spikes on the battery line                                                                                         |

(table continues...)

**Table 14** (continued) **Suggested component values**

| Reference      | Value          | Purpose                                                                                                                                                     |
|----------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $C_{VSGND}$    | 47 nF          | Buffer capacitor for fast transient                                                                                                                         |
| $D_{Z2}$       | 33V TVS Diode  | Transient voltage suppressor diode. Protection during overvoltage and in case of loss of battery while driving an inductive load                            |
| $C_{VS2}$      | –              | Filtering/buffer capacitor located at VBAT connector                                                                                                        |
| $R_{SENSE}$    | 1.2 k $\Omega$ | SENSE resistor                                                                                                                                              |
| $R_{IS\_PROT}$ | 4.7 k $\Omega$ | Protection during overvoltage, reverse polarity, loss of ground Value to be tuned according to microcontroller specifications                               |
| $D_{Z1}$       | 7 V Z-Diode    | Protection of microcontroller during overvoltage                                                                                                            |
| $R_{ADC}$      | 4.7 k $\Omega$ | Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications |
| $C_{SENSE}$    | 220 pF         | Sense signal filtering. A time constant ( $R_{ADC} \cdot C_{SENSE}$ ) longer than 1 $\mu$ s is recommended                                                  |
| $R_{GND}$      | 47 $\Omega$    | Protection in case of overvoltage and loss of battery while driving inductive loads                                                                         |

- Please contact us for information regarding the pin behavior assessment
- For further information you may contact <http://www.infineon.com>

## 10 Package outlines

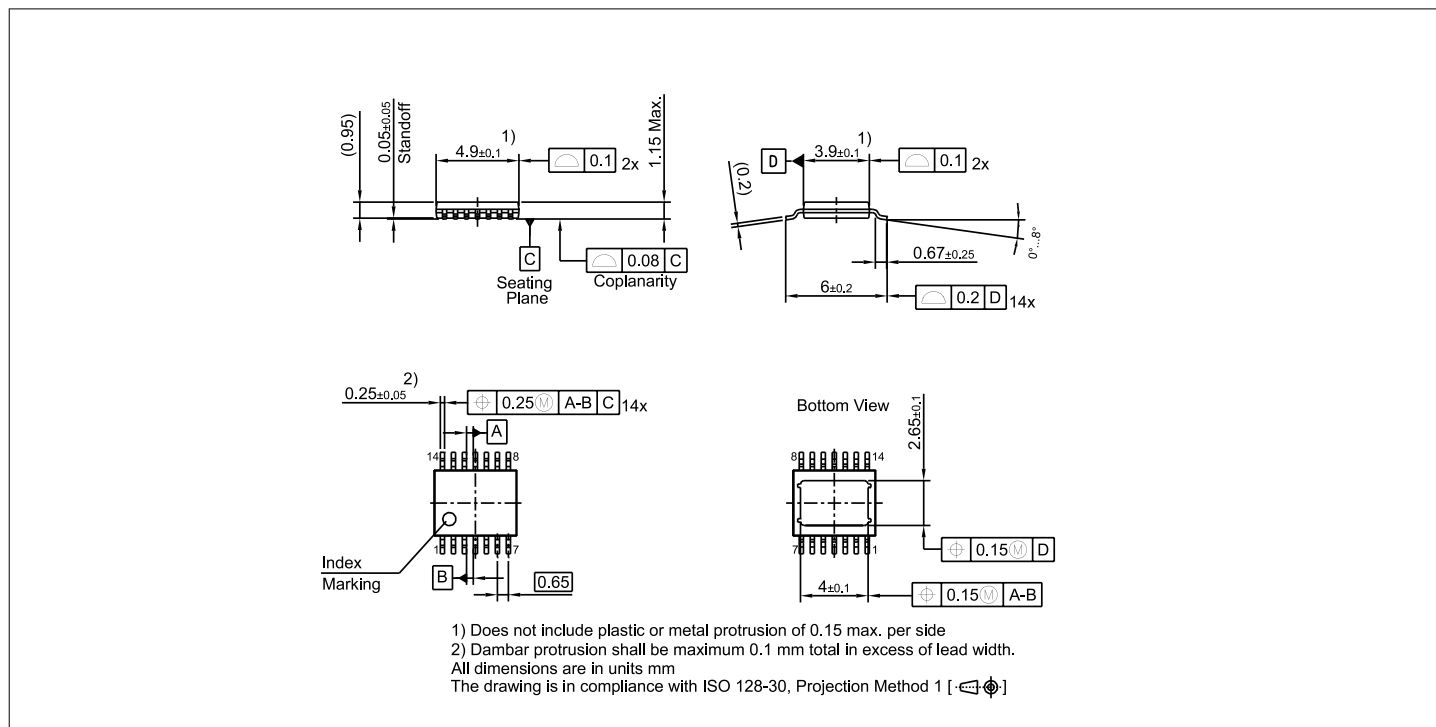


Figure 38 PG-TSDSO-14 dual small outline package dimensions

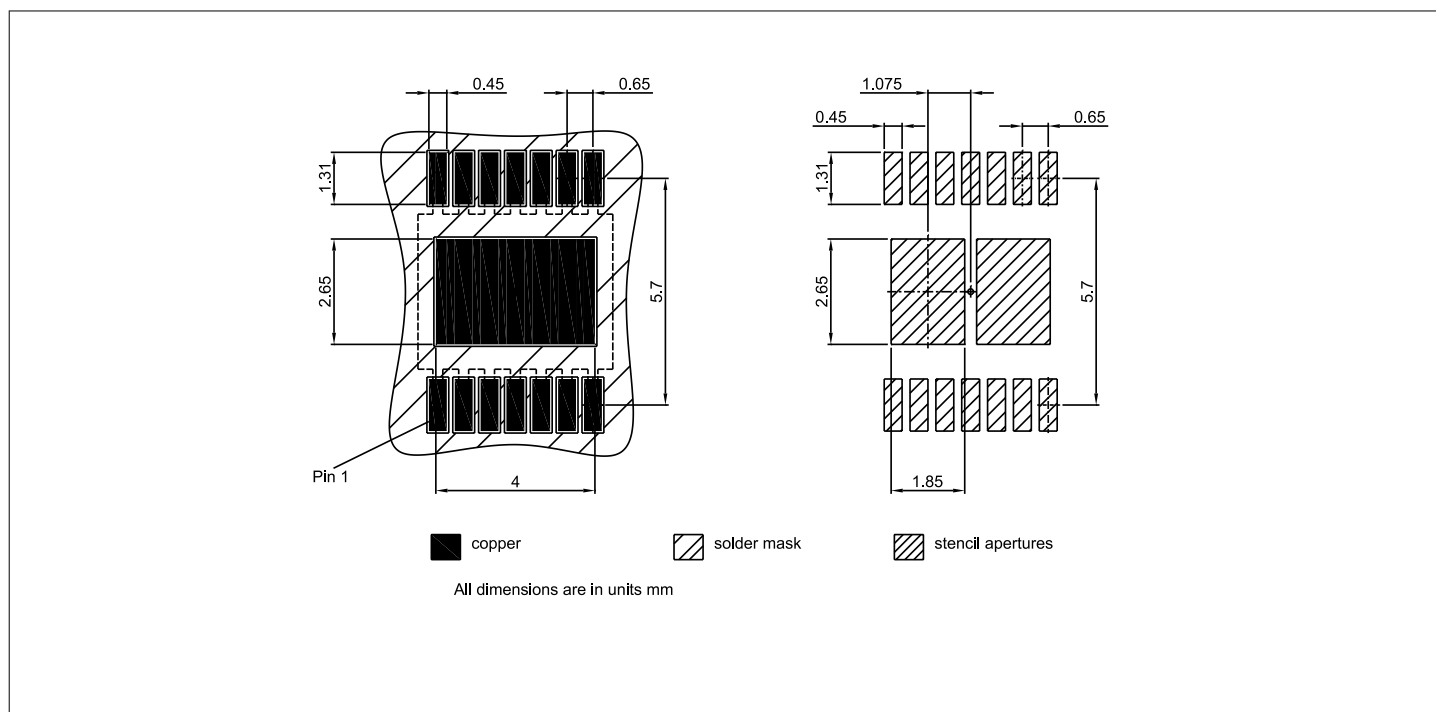


Figure 39 PG-TSDSO-14 dual small outline footprint dimensions

**Note:** To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Further information on packages** <https://www.infineon.com/packages>



11 Revision history

Table 15 Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| Rev.1.00         | 2022-09-20      | Initial Datasheet      |

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