PCM186x-Q1 Automotive, 4-Channel or 2-Channel, 192-kHz, Audio ADCs

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Temperature Grade 1: –40°C ≤ T_A ≤ +125°C
  - HBM ESD Classification Level 2
  - CDM ESD Classification Level C5
- High SNR Performance:
  - 110-dB SNR (PCM1861-Q1/63-Q1/65-Q1)
  - 103-dB SNR (PCM1860-Q1/62-Q1/64-Q1)
- ADC Sample Rate (f_S) = 8 kHz to 192 kHz
- Up To Four Independent ADC Channels Available
- Single-Ended, 2.1-V_{RMS} Full-Scale (FS) Input
- Differential, 4.2-V_{RMS} FS Input
- Hardware (HW) Control: PCM1860-Q1/61-Q1
- Software (SW) Control (I^2C or SPI): PCM1862-Q1/63-Q1/64-Q1/65-Q1
- Support for Up To Four Digital Microphones (SW-Controlled Devices)
- Programmable Gain Amplifier (PGA):
  - Fixed Gain: 0 dB, 12 dB, 32 dB (PCM1860-Q1/61-Q1)
  - SW-Controlled Gain: –12 dB to +32 dB (PCM1862-Q1/63-Q1/64-Q1/65-Q1)
- Integrated High-Performance Audio PLL
- Single 3.3-V Power-Supply Operation
- Power Dissipation at 3.3 V:
  - < 85 mW (PCM1860-Q1/61-Q1/62-Q1/63-Q1)
  - < 145 mW (PCM1864-Q1/65-Q1)
- *Energysense* Audio Content Detector for Auto System Wakeup and Sleep
- Master or Slave Audio Interface
- Automatic PGA Clipping Suppression Control
- PCB-Footprint Compatibility Across All Devices

2 Applications

- Automotive Head Units
- External Car Amplifiers
- Telematics Control Unit (TCU)

3 Description

The PCM186x-Q1 family (PCM1860-Q1, PCM1861-Q1, PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, and PCM1865-Q1) of audio front-end devices take a new approach to audio-function integration to ease compliance with European Ecodesign legislation, while enabling high-performance end products at reduced cost. The PCM186x-Q1 support single-supply operation at 3.3 V, and offer an integrated programable gain amplifier (PGA) in a small package; this configuration makes it feasible to implement smaller and smarter products at a reduced cost.

The PCM186x-Q1 audio front end supports single-ended input levels from small-mV microphone inputs to 2.1-V_{RMS} line inputs, without external resistor dividers. The front-end mixer (MIX), multiplexer (MUX), and PGA also support differential (Diff), pseudo-differential, and single-ended (SE) inputs, making these devices an ideal interface for products that require interference suppression. The PCM186x-Q1 integrate many system-level functions that assist or replace some DSP functions.

An integrated band-gap voltage reference provides excellent PSRR, so that a dedicated analog 3.3-V rail may not be required.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM186x-Q1	TSSOP (30)	7.80 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Application Diagram

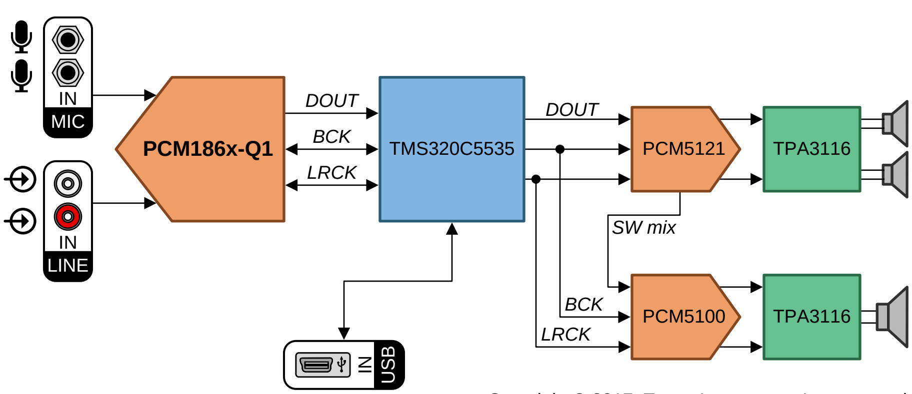


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2014) to Revision A — **Page**

- Changed title for clarity ... 1
- Added PCM1860-Q1, PCM1861-Q1, PCM1862-Q1, PCM1863-Q1, and PCM1864-Q1 devices and associated new content to data sheet ... 1
- Added AEC-Q100 and high SNR Performance feature bullets ... 1
- Added feature bullets to clarify hardware- and software-controlled devices ... 1
- Changed one feature subbullet from "Fixed Mic Pregain Select: 20, 32 dB (Analog)" to two subbullets, "Fixed Gain: 12 dB, 32 dB (PCM1860-Q1, PCM1861-Q1)" and "Software-Controlled Gain: (PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, PCM1865-Q1)" ... 1
- Deleted subbullet, "Additional 1.8 V Core and Interface for Lower Power Consumption" ... 1
- Deleted feature subbullet, "Zero Crossing PGA Gain Changes" ... 1
- Changed application bullets to align with automotive applications ... 1
- Changed *Description* section text to clarify 3.3-V supply, integrated PGA, and additional front-end features ... 1
- Deleted Table 1, Typical Performance (3.3-V Supply, –1 dB-FS Input); redundant content ... 6
- Changed *Device Comparison Table*; updated for clarity ... 6
- Changed XO (pin 9) I/O from "—" to "O". ... 10

Revision History (continued)

- Added operating ambient temperature and junction temperature to *Absolute Maximum Ratings* table 11
- Changed ground voltage differences range from "AGND, DGND" to "AGND to DGND" 11
- Changed storage temperature max value from 125°C to 150°C............ 11
- Changed CDM value from ±1500 V to ±750 V and updated *ESD Ratings* table to align with automotive devices 11
- Changed "Operating junction temperature range" to "Operating ambient temperature, T_A" in *Recommended Operating Conditions* table 11
- Changed Thermal Information table to standard automotive format 11
- Changed *Electrical Characteristics: Primary PGA and ADC performance* to include secondary ADC performance data, and deleted separate *Electrical Characteristics: Secondary ADC Performance* table 12
- Added new table note to clarify test condition at 32-dB PGA gain............ 12
- Added min value of 85 dB to *input channel signal-to-noise ratio* for 32 dB 12
- Added min value of –76 dB to *input channel THD+N, differential input* for 32 dB 12
- Deleted "per input pin" and "out of phase" from *full-scale voltage input* parameter in *Electrical Characteristics* 12
- Changed *input channel signal-to-noise ratio*, single-ended input value for PCM1865-Q1 from 110 dB to 106 dB; differential conditions used previously............ 12
- Changed "*Energysense* Detection Threshold" to " 12
- Default *Energysense* Signal Detection Threshold" in *Electrical Characteristics, Secondary ADC Performance*............ 12
- Changed *secondary ADC sampling rate* from "same as audio sampling rate" to min of 8 kHz and max of 192 kHz 12
- Changed *Electrical Characteristics, DC* conditions from master to slave mode; system clock from 256 × f_S to 512 x f_S.... 13
- Changed POWER section of the *Electrical Characteristics, DC*; updated section structure for clarity............ 13
- Deleted all rows with XTAL as condition; not required for normal operation 13
- Deleted all rows with Powerdown; not a valid operating mode 13
- Changed *AVDD current* typ value for 2-channel, 3.3-V, active mode from 16 mA to 18 mA 13
- Changed *Total power* value for 2-channel, 3.3 V, sleep mode from 24 mW to 17.6 mW............ 13
- Changed *DVDD current* for 2-channel, 3.3 V, standby mode from 353 µA to 0.015 mA............ 13
- Changed *Total power* for 2-channel, 3.3 V, standby mode for software device from 0.59 mW to 0.64 mW 13
- Changed *Total power* for 2-channel, 3.3 V and 1.8 V active mode from 68 mW to 69.2 mW............ 13
- Changed *Total power* for 4-channel, 3.3 V, active mode from 145 mW to 135.3 mW 13
- Changed *Total power* for 4-channel, 3.3 V and 1.8 V, active mode from 128 mW to 117.3 mW............ 14
- Deleted redundant text "Valid with recommended values on analog rails (AVDD, VREF, and so on)" from PSRR 14
- Changed "HPF frequency response" to "HPF –3-dB cutoff frequency" in *Electrical Characteristics: Digital Filter*............ 15
- Added maximum BCK frequency rows to *Timing Requirements, External Clock* table 15
- Added Figure 3; replaces old Figure 4 with new data for the PCM1865-Q1............ 20
- Changed Figure 4; now associated to PCM1860-Q1, PCM1862-Q1, PCM1864-Q1............ 20
- Added new Figure 5; replaces old Figure 5 with new data for the PCM1865-Q1 20
- Changed Figure 6; now associated to PCM1860-Q1, PCM1862-Q1, PCM1864-Q1............ 20
- Changed all FFT plot X axes from log scale to linear scale............ 20
- Added new Figure 7; replaces old Figure 6 with new data for the PCM1865-Q1 20
- Changed Figure 8; now associated to PCM1860-Q1, PCM1862-Q1, PCM1864-Q1............ 20
- Added new Figure 9; replaces old Figure 7 with new data for the PCM1865-Q1 21
- Changed Figure 10; now associated to PCM1860-Q1, PCM1862-Q1, PCM1864-Q1............ 21
- Deleted Figure 10, FFT With -1 dBFS Input............ 21
- Added new Figure 11; replaces old Figure 8 with new data for the PCM1865-Q1 21
- Deleted Figure 11, FFT With –60 dBFS Input............ 21
- Changed Figure 12; now associated to PCM1860-Q1, PCM1862-Q1, PCM1864-Q1............ 21
- Added new paragraph to start of *Overview* section 24

Revision History (continued)

Revision History (continued)

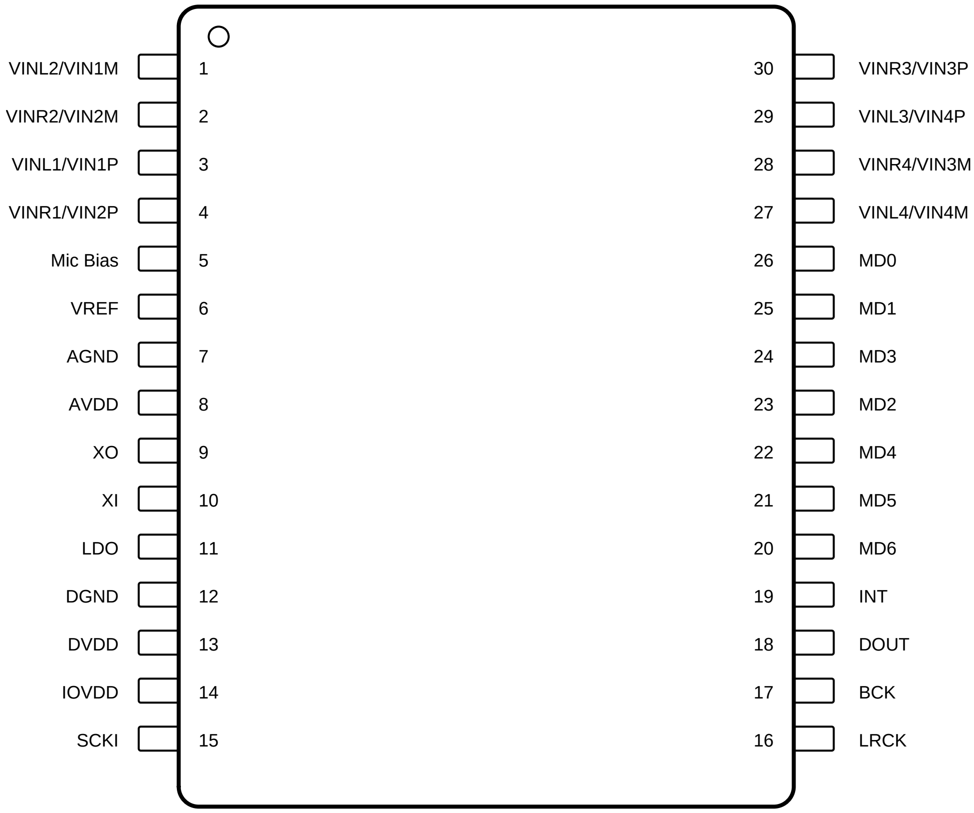
- Changed text in *Bypassing the Internal LDO to Reduce Power Consumption* section to clarify TDM mode with 1.8-V IOVDD operation 61
- Added text "The I²C control port.." to the *I²C Interface* section 64
- Changed pin numbers in Table 22 from "15, 16, 14" to "23, 24, 25" 64
- Added *Real World Software Configuration using EnergySense and Controlsense* section 65
- Added more detail to*Programming DSP Coefficients on Software-Controlled Devices* section, and moved to new location 68
- Added *Hardware Control* section 71
- Added *Dual PCM186x-Q1 TDM Functionality* section 73
- Added new paragraph to end of *Analog Front-End Circuit For Single-Ended, Line-In Applications* section 74
- Added design examples and associated subsections to *Typical Application* section 75
- Changed *1.8-V Support* section; clarified that both IOVDD and LDO must be driven with 1.8 V in 1.8-V mode 79
- Added *Brownout Conditions* section 79
- Added test condition to step 3 in *Power Up Sequence* section; (PLL requires < 250 µs) 80
- Changed *Layout* section for clarity 84
- Deleted old Figure 64, *PCM1865-Q1 EVM Signal Partitioning*; redundant, and same information shown in Figure 74 84
- Changed Figure 75 for clarity 85
- Changed "0xFF" to "0xFE" in last sentence of *Register Map Description* section 85
- Changed values for register 3, bits 6-0; changed from "RSV" to correct bit names 86
- Changed bits 4 and 3 from 1 and 0 to RSV, respectively, in register 27 86
- Changed register 44 (0x2C) from reserved ("RSV") to actual bit names 87
- Changed registers 52 and 53 to registers 51 and 52, respectively 87
- Changed TX_WLEN bit option 00 description from "Reserved" to "32-bit" in Page 0, register 11 95
- Changed GPIO0_FUNC for 001 from "SPI MISO (Out:Default)" to "Digital MIC Input 0 (In)" and for 010 from "RESERVED" to "SPI MISO (Out)" in register 16 98
- Changed "DPGA" to "APGA" in description column for bits 3, 2, 1, and 0 in register 25 104
- Changed DIV_NUM default value in page 0, register 33 from "000 0001" to "000 0000" 106
- Changed names and descriptions of master mode clock dividers in registers 37, 38, and 39 for clarity 108
- Changed "Divider" to "Multiplier" in R[3:0] description for register 42 110
- Changed values for R[3:0] from 1, 1/2, 1/3, 1/4, and 1/16 to 1, 2, 3, 4, and 16, respectively 110
- Changed "Divider" to "Multiplier" in J[5:0] description for register 43 111
- Changed "Divider" to "Multiplier" in D_LSB[7:0] description for register 44 111
- Changed "Divider" to "Multiplier" in D_MSB[5:0] description for register 45 111
- Changed register 52 to register 51 114
- Changed register 53 to register 52 115
- Changed bit 3 from CLKERR to RSV in register 96 123
- Deleted bit 3 from CLKERR to RSV in register 97 124
- Changed default values in page 1: register 1 for bits 4, 2, 1, and 0 from "1" to "0", and updated descriptions for clarity. 129

5 Device Comparison Table

<table>
<tr><th>PART NUMBER</th><th>PCM1860-Q1</th><th>PCM1861-Q1</th><th>PCM1862-Q1</th><th>PCM1863-Q1</th><th>PCM1864-Q1</th><th>PCM1865-Q1</th></tr>
<tr><td>Control method</td><td colspan="2">H/W</td><td colspan="4">I^2C or SPI</td></tr>
<tr><td>Differential SNR performance A weighted data</td><td>103 dB</td><td>110 dB</td><td>103 dB</td><td>110 dB</td><td>103 dB</td><td>110 dB</td></tr>
<tr><td>Analog front end</td><td colspan="2">2.1 V_{RMS} MUX with fixed PGA gains</td><td colspan="4">2.1 V_{RMS} MUX, MIX, PGA and auxiliary ADC</td></tr>
<tr><td>Simultaneous channel capability</td><td colspan="2">2</td><td colspan="2">2</td><td colspan="2">4</td></tr>
<tr><td>Energysense signal detect</td><td colspan="2">Yes (fixed threshold)</td><td colspan="4">Yes (programmable threshold)</td></tr>
<tr><td>Energysense signal loss</td><td colspan="2">No</td><td colspan="4">Yes (programmable threshold)</td></tr>
<tr><td>Controlsense</td><td colspan="2">No</td><td colspan="4">Yes (programmable threshold)</td></tr>
<tr><td>Interrupt controller</td><td colspan="2">No</td><td colspan="4">Yes</td></tr>
<tr><td>Digital microphone support</td><td colspan="2">No</td><td colspan="2">Yes (2)</td><td colspan="2">Yes (4)</td></tr>
<tr><td>Clock PLL</td><td colspan="2">BCK to generate internal master clock</td><td colspan="4">Fully programmable</td></tr>
<tr><td>Lowest power standby mode (1.8-V IOVDD)</td><td colspan="2">7.96 mW</td><td colspan="4">0.22 mW</td></tr>
<tr><td>Digital mixing with digital and analog inputs</td><td colspan="2">No</td><td colspan="4">Yes</td></tr>
<tr><td>Digital output formats</td><td colspan="2">Left-justified, I^2S</td><td colspan="4">Left-justified, right-justified, I^2S, TDM</td></tr>
<tr><td>Interrupt capabilities</td><td colspan="2">Energysense signal detect</td><td colspan="4">Energysense signal loss and detect, controlsense, post PGA clipping, RX digital toggle</td></tr>
</table>

6 Pin Configuration and Functions

DBT Package: PCM1860-Q1 and PCM1861-Q1
30-Pin TSSOP
Top View



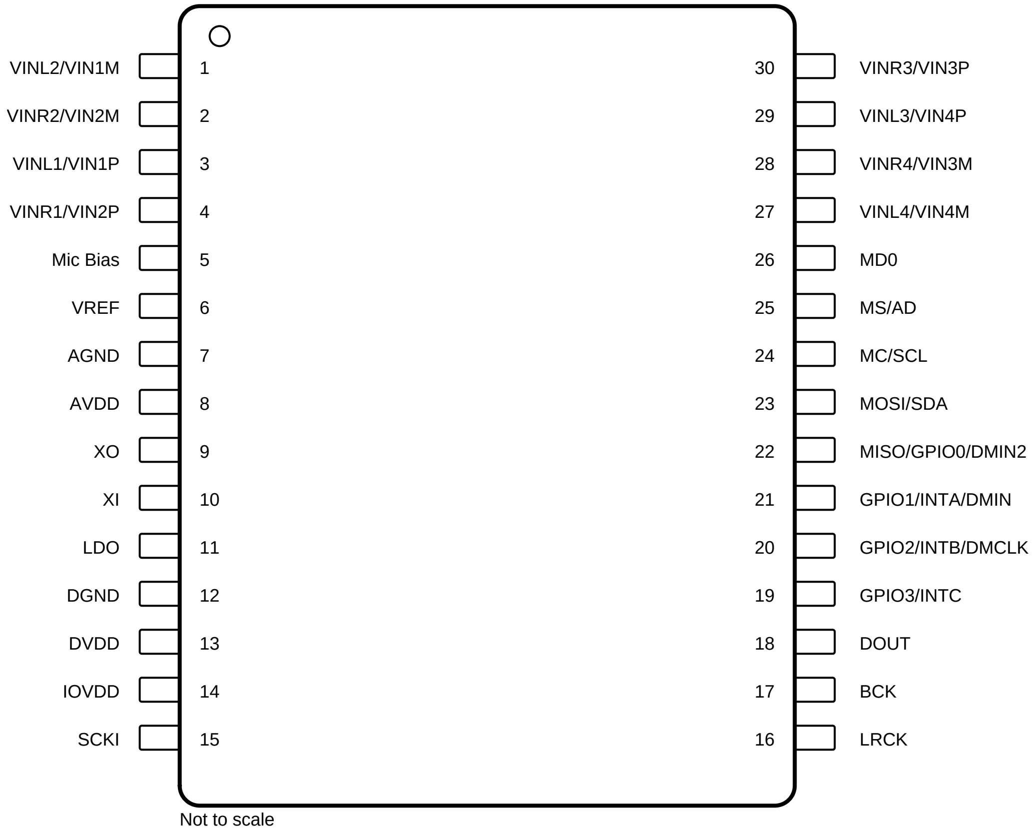
Not to scale

Pin Functions: PCM1860-Q1 and PCM1861-Q1

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VINL2/VIN1M	Analog input	Analog input 2, L-channel (or differential M input for input 1)
2	VINR2/VIN2M	Analog input	Analog input 2, R-channel (or differential M input for input 2)
3	VINL1/VIN1P	Analog input	Analog input 1, L-channel (or differential P input for input 1)
4	VINR1/VIN2P	Analog input	Analog input 1, R-channel (or differential P input for input 2)
5	Mic Bias	Power	Microphone bias output
6	VREF	Power	Reference voltage output decoupling point (typically, 0.5 AVDD). Connect 1-µF capacitor from this pin to AGND.
7	AGND	Power	Analog ground
8	AVDD	Power	Analog power supply (typically, 3.3 V). Connect 0.1-µF and 10-µF capacitors from this pin to AGND.
9	XO	Digital output	Crystal oscillator output
10	XI	Digital input	Crystal oscillator input or master clock input (1.8-V CMOS signal)
11	LDO	Power	Internal low-dropout regulator (LDO) decoupling output, or external 1.8-V input to bypass LDO. Connect 0.1-µF and 10-µF capacitors from this pin to DGND.
12	DGND	Power	Digital ground
13	DVDD	Power	Digital power supply (typically, 3.3 V). Connect 0.1-µF and 10-µF capacitors from this pin to DGND.
14	IOVDD	Power	Power supply for I/O voltages (typically, 3.3 V or 1.8 V).
15	SCKI	Digital input	CMOS level (3.3 V) master clock input
16	LRCK	Digital input/output	Audio data word clock (left right clock) input/output(1)
17	BCK	Digital input/output	Audio data bit clock input/output(1)
18	DOUT	Digital output	Audio data digital output
19	INT	Analog output	Interrupt output (for analog input detection). Pull high for active mode, pull low for idle.
20	MD6	Analog input	Analog MUX and gain selection using MD6, MD5, and MD2 pins, respectively: 000: SE Ch 1 (VINL1 and VINR1) 001: SE Ch 2 (VINL2 and VINR2) 010: SE Ch 3 (VINL3 and VINR3) 011: SE Ch 4 (VINL4 and VINR4) 100: SE Ch 4 with 12-dB gain 101: SE Ch 4 with 32-dB gain 110: Diff Ch 1 (VIN1P and VIN1M, VIN2P and VIN2M) 111: Diff Ch 2 (VIN3P and VIN3M, VIN4P and VIN4M) with 12-dB gain
21	MD5	Analog input	Analog MUX and gain selection (see MD6 pin for description)
22	MD4	Analog input	Audio format: high = left-justified, low = I^2S
23	MD2	Analog input	Analog MUX and gain selection (see MD6 pin for description)
24	MD3	Digital Input	Filter select: 0 = FIR decimation filter, 1 = IIR low latency decimation filter
25	MD1	Analog input	Audio interface mode selection using MD1 and MD0 pins, respectively: 00: Slave mode, 256 × f_S, 384 × f_S, 512 × f_S autodetect 01: Master mode (512 × f_S) 10: Master mode (384 × f_S) 11: Master mode (256 × f_S)
26	MD0	Analog input	Audio interface mode selection (see MD1 pin for description)
27	VINL4/VIN4M	Analog input	Analog input 4, L-channel (or differential M input for input 4)
28	VINR4/VIN3M	Analog input	Analog input 4, R-channel (or differential M input for input 3)
29	VINL3/VIN4P	Analog input	Analog input 3, L-channel (or differential P input for input 4)
30	VINR3/VIN3P	Analog input	Analog input 3, R-channel (or differential P input for input 3)

(1) Schmitt trigger input with internal pull-down (50 kΩ, typically).

DBT Package: PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, and PCM1865-Q1
30-Pin TSSOP
Top View



NOTE: The DMIN2 option for pin 22 is only available on the PCM1864-Q1 and PCM1865-Q1 devices.

Pin Functions: PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, and PCM1865-Q1

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VINL2/VIN1M	Analog input	Analog input 2, L-channel (or differential M input for input 1)
2	VINR2/VIN2M	Analog input	Analog input 2, R-channel (or differential M input for input 2)
3	VINL1/VIN1P	Analog input	Analog input 1, L-channel (or differential P input for input 1)
4	VINR1/VIN2P	Analog input	Analog input 1, R-channel (or differential P input for input 2)
5	Mic Bias	Power	Microphone bias output
6	VREF	Power	Reference voltage output decoupling point (typically, 0.5 AVDD). Connect 1-µF capacitor from this pin to AGND.
7	AGND	Power	Analog ground
8	AVDD	Power	Analog power supply (typically, 3.3 V). Connect 0.1-µF and 10-µF capacitors from this pin to AGND.
9	XO	Digital output	Crystal oscillator output
10	XI	Digital input	Crystal oscillator input or master clock input (1.8-V CMOS signal)
11	LDO	Power	Internal LDO decoupling output, or external 1.8-V input to bypass LDO. Connect 0.1-µF and 10-µF capacitors from this pin to DGND.
12	DGND	Power	Digital ground
13	DVDD	Power	Digital power supply (typically, 3.3 V). Connect 0.1-µF and 10-µF capacitors from this pin to DGND.
14	IOVDD	Power	Power supply for I/O voltages (typically, 3.3 V or 1.8 V).
15	SCKI	Digital input	CMOS level (3.3 V) master clock input
16	LRCK	Digital input/output	Audio data world clock (left right clock) input/output(1)
17	BCK	Digital input/output	Audio data bit clock input/output(1)
18	DOUT	Analog output	Audio data digital output
19	GPIO3/INTC	Digital input/output	GPIO 3 or interrupt C
20	GPIO2/INTB/DMCLK	Digital input/output	GPIO 2, interrupt B, or digital microphone clock output
21	GPIO1/INTA/DMIN	Digital input/output	GPIO 1, interrupt A, or digital microphone input
22	MISO/GPIO0/DMIN2	Digital input/output	In SPI mode: master in, slave out In I^2C mode: GPIO0 (or DMIN2 for PCM1864-Q1 and PCM1865-Q1 only)
23	MOSI/SDA	Digital input/output	In SPI mode: master out, slave in In I^2C mode: SDA
24	MC/SCL	Digital input	In SPI mode: serial bit clock In I^2C mode: serial bit clock
25	MS/AD	Digital input	In SPI mode: chip select In I^2C mode: address pin
26	MD0	Digital input	Control method select pin: I^2C (tied low or not connected) or SPI (tied high)
27	VINL4/VIN4M	Analog input	Analog input 4, L-channel (or differential M input for input 4)
28	VINR4/VIN3M	Analog input	Analog input 4, R-channel (or differential M input for input 3)
29	VINL3/VIN4P	Analog input	Analog input 3, L-channel (or differential P input for input 4)
30	VINR3/VIN3P	Analog input	Analog input 3, R-channel (or differential P input for input 3)

(1) Schmitt trigger input with internal pull-down (50 kΩ, typically).

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AGND	–0.3	3.9	V
	DVDD to DGND	–0.3	3.9	
	IOVDD to DGND	–0.3	3.9	
Ground voltage differences	AGND to DGND	–0.3	0.3	V
Digital input voltage	Digital input to DGND	–0.3	IOVDD + 0.3	V
	XI to DGND	–0.3	2.1	
Analog input voltage	VINxx to AGND	–1.7	5.0	V
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
POWER						
AVDD	Analog supply voltage to AGND		3.0	3.3	3.6	V
DVDD	Digital supply voltage to DGND		3.0	3.3	3.6	V
IOVDD	IO supply voltage to DGND	at 1.8 V	1.62	1.8	1.98	V
		at 3.3 V	3.0	3.3	3.6	V
LDO	LDO pin voltage to DGND (LDO is an input when using external 1.8-V power supply)		IOVDD – 0.3	IOVDD	IOVDD + 0.3	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		PCM186x-Q1 DBT (TSSOP) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: PGA and ADC AC Performance

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 × f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PRIMARY PGA AND ADC							
	Input channel signal-to-noise ratio, differential input	0-dB PGA gain, –60-dB input signal, master mode at Diff input	PCM1860-Q1 PCM1862-Q1 PCM1864-Q1	97	103		dB
			PCM1861-Q1 PCM1863-Q1 PCM1865-Q1	97	110		dB
		32-dB PGA gain[1], –86-dB input signal, master mode at Diff input		85	90		dB
	Input channel THD+N, differential input	0-dB PGA gain, –1-dB input signal, master mode at Diff input		–85	–93		dB
		32-dB PGA gain, –33-dB input signal, master mode at Diff input		–76	–84		dB
	L channel to R channel separation line input	0-dB PGA gain, –1-dB input signal, master mode			–105		dB
	L channel to R channel separation mic input	20-dB PGA gain, –1-dB input signal, master mode			–105		dB
	L1 channel to L2 channel separation line input	0-dB PGA gain, –1-dB input signal, master mode			–105		dB
	R1 channel to R2 channel separation line input	0-dB PGA gain, –1-dB input signal, master mode			–105		dB
	L1 channel to L2 channel separation mic input	20-dB PGA gain, –1-dB input signal, master mode			–105		dB
	R1 channel to R2 channel separation mic input	20-dB PGA gain, –1-dB input signal, master mode			–105		dB
	Range of analog PGA	–12 to +12 dB (1-dB step), 20 dB, and 32 dB		–12[2]		32	dB
	Accuracy of PGA + ADC				0.5		dB
	Matching between PGA + ADCs on-chip				0.05		dB
	Full-scale voltage input	Single-ended mode				2.1	V_{RMS}
		Differential mode (2.1 V_{RMS} per pin)				4.2	V_{RMS}
	Input channel signal-to-noise ratio, single-ended input	0-dB PGA gain, –60-dB input signal, master mode at SE input	PCM1860-Q1 PCM1862-Q1 PCM1864-Q1		103		dB
			PCM1861-Q1 PCM1863-Q1 PCM1865-Q1		106		dB
		32-dB PGA gain, –92-dB input signal, master mode at SE input			75		dB
	Input channel THD+N, single-ended input	0-dB PGA gain, –1-dB input signal, master mode at SE input			87		dB
		32-dB PGA gain, –33-dB input signal, master mode at SE input			68		dB
	Input impedance per analog input pin	PCM1864-Q1 and PCM1865-Q1			10		kΩ
		PCM1860-Q1, PCM1861-Q1, PCM1862-Q1, and PCM1863-Q1			20		kΩ
CMRR	Common-mode rejection ratio	Differential input, 1-kHz signal on both pins and measure level at output			56		dB
SECONDARY ADC PERFORMANCE							
	Default *Energysense* signal detection threshold	At 1 kHz			–57		dBFS
	Energysense signal bandwidth				10		kHz
	Energysense accuracy[2]				3		dB
	Secondary ADC accuracy				12		bits
	Secondary ADC sampling rate			8		192	kHz

(1) 32-dB gain when using differential mode inputs is only available in SW-controlled devices.
(2) Specified by design.

7.6 Electrical Characteristics: DC

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, slave mode, single-speed mode, f_S = 48 kHz, system clock = 512 × f_S, and 24-bit data (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER					
AVDD current	2-channel device, AVDD = DVDD = IOVDD = 3.3 V, active mode		18		mA
DVDD current			0.01		mA
IOVDD current			6.2		mA
Total Power			80		mW
AVDD current	2-channel device, AVDD = DVDD = IOVDD = 3.3 V, sleep mode		2.8		mA
DVDD current			0.353		mA
IOVDD current			2.2		mA
Total power			17.6		mW
AVDD current	2-channel device, AVDD = DVDD = IOVDD = 3.3 V, standby mode for software device		0.06		mA
DVDD current			0.015		mA
IOVDD current			0.12		mA
Total power			0.64		mW
AVDD current	2-channel device, AVDD = DVDD = IOVDD = 3.3 V, standby mode for hardware device		1.3		mA
DVDD current			0.353		mA
IOVDD current			1.6		mA
Total power			10.725		mW
AVDD current	2-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, active mode		18		mA
DVDD current			0.015		mA
IOVDD and LDO Current			5.4		mA
Total power			69.2		mW
AVDD current	2-channel device, AVDD = DVDD = 3.3 V IOVDD = LDO = 1.8 V, sleep mode		2.8		mA
DVDD current			0.353		mA
IOVDD and LDO Current			2		mA
Total power			13.995		mW
AVDD current	2-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, standby mode for software device		0.06		mA
DVDD current			0.007		mA
Total power(1)			0.221		mW
AVDD current	2-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, standby mode for hardware device		1.3		mA
DVDD current			0.35		mA
IOVDD and LDO Current			1.4		mA
Total power			7.965		mW
AVDD current	4-channel device, AVDD = DVDD = IOVDD = 3.3 V, active mode		31		mA
DVDD current			0.01		mA
IOVDD current			10		mA
Total power			135.3		mW
AVDD current	4-channel device, AVDD = DVDD = IOVDD = 3.3 V, sleep mode		2.8		mA
DVDD current			0.35		mA
IOVDD current			2.2		mA
Total power			17.655		mW
AVDD current	4-channel device, AVDD = DVDD = IOVDD = 3.3 V, standby mode for software device		0.06		mA
DVDD current			0.015		mA
IOVDD current			0.12		mA
Total power			0.644		mW
AVDD current	4-channel device, AVDD = DVDD = IOVDD = 3.3 V, standby mode for hardware device		1.3		mA
DVDD current			0.35		mA
IOVDD current			0.16		mA
Total power			10.725		mW

(1) IOVDD and LDO current consumption is negligible for software-controlled devices in standby mode.

Electrical Characteristics: DC (continued)

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, slave mode, single-speed mode, f_S = 48 kHz, system clock = 512 × f_S, and 24-bit data (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	AVDD current	4-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, active mode		31		mA
	DVDD current			0.01		mA
	IOVDD and LDO Current			8.3		mA
	Total power			117.3		mW
	AVDD current	4-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, sleep mode		2.8		mA
	DVDD current			0.35		mA
	IOVDD and LDO Current			2		mA
	Total power			13.995		mW
	AVDD current	4-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, standby mode for software device		0.06		mA
	DVDD current			0.007		mA
	Total power(1)			0.221		mW
	AVDD current	4-channel device, AVDD = DVDD = 3.3 V, IOVDD = LDO = 1.8 V, standby mode for hardware device		1.3		mA
	DVDD current			0.35		mA
	IOVDD and LDO Current			1.4		mA
	Total power			7.965		mW
	Additional current consumption	on IOVDD when XTAL is used		0.5		mA
		on DVDD in BCK PLL mode		1.5		mA
		on IOVDD when master mode is enabled		2		mA
		IOVDD = 3.3 V or IOVDD = LDO = 1.8 V, f_S = 192 kHz, 2-channel active mode		4		mA
		IOVDD = 3.3 V or IOVDD = LDO = 1.8 V, f_S = 192 kHz, 4-channel active mode		7.5		mA
PSRR	Power-supply rejection ratio			80		dB
MIC BIAS						
	Mic bias noise			5		μV_{RMS}
	Mic bias current drive			4		mA
	Mic bias voltage			2.6		V
DIGITAL I/O						
V_{OH}	Output logic high voltage level	I_{OH} = 2 mA		75		%IOVDD
V_{OL}	Output logic low voltage level	I_{OL} = –2 mA		25		%IOVDD
$\lvert I_{IH}\rvert$1	Input logic high current level	All digital pins			10	µA
$\lvert I_{IL}\rvert$1	Input logic low current level	All digital pins			–10	µA

7.7 Electrical Characteristics: Digital Filter

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 × f_S, and 24-bit data (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLASSIC FIR					
Pass band			0.454		f_S
Stop band			0.583		f_S
Pass-band ripple			±0.05		dB
Stop-band attenuation			–65		dB
Group delay or latency			30		Samples
HPF –3-dB cutoff frequency			1		Hz
LOW LATENCY IIR					
Pass band			0.454		f_S
Stop band			0.546		f_S
Pass-band ripple			±0.02		dB
Stop-band attenuation			–75		dB
Group delay or latency			10		Samples
HPF –3-dB cutoff frequency			1		Hz

7.8 Timing Requirements: External Clock

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 × f_S, 24-bit data (unless otherwise noted)

		MIN	TYP	MAX	UNIT
XTAL support		15		35	MHz
MCLK frequency	3.3 V on MCLK pin	1		50	MHz
MCLK	1.8 V MCLK input on XI pin	1		50	MHz
MCLK input duty cycle	1.8 V MCLK	48%		52%	
Maximum BCK frequency	IOVDD = 3.3 V			50	MHz
	IOVDD = 1.8 V			25	MHz

7.9 Timing Requirements: I²C Control Interface

		CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard		100	kHz
		Fast		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	Standard	4.7		µs
		Fast	1.3		
t_{LOW}	Low period of the SCL clock	Standard	4.7		µs
		Fast	1.3		
t_{HI}	High period of the SCL clock	Standard	4.0		µs
		Fast	600		ns
$t_{RS\text{-}SU}$	Setup time for repeated START condition	Standard	4.7		µs
		Fast	600		ns
$t_{S\text{-}HD}$	Hold time for START condition	Standard	4.0		µs
		Fast	600		ns
$t_{RS\text{-}HD}$	Hold time for repeated START condition	Standard	4.0		µs
		Fast	600		ns
$t_{D\text{-}SU}$	Data setup time	Standard	250		ns
		Fast	100		
$t_{D\text{-}HD}$	Data hold time	Standard	0	900	ns
		Fast	0	900	
$t_{SCL\text{-}R}$	Rise time of SCL signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
$t_{SCL\text{-}R1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
$t_{SCL\text{-}F}$	Fall time of SCL signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
$t_{SDA\text{-}R}$	Rise time of SDA signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
$t_{SDA\text{-}F}$	Fall time of SDA signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
$t_{P\text{-}SU}$	Setup time for STOP condition	Standard	4.0		µs
		Fast	600		ns
C_B	Capacitive load for SDA and SCL line			400	pF
t_{SP}	Pulse duration of spike suppressed	Fast		50	ns
V_{NH}	Noise margin at high level for each connected device (including hysteresis)		$0.2V_{DD}$		V

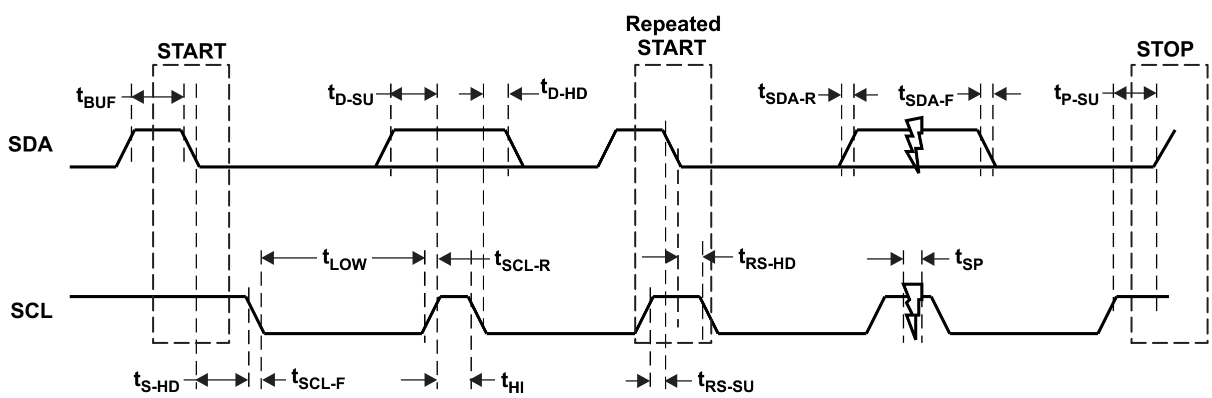


Figure 1. I²C Control Interface Timing

7.10 Timing Requirements: SPI Control Interface

		MIN	MAX	UNIT
t_{MCY}	MC pulse period	100		ns
t_{MCL}	Pulse duration, MC low	40		ns
t_{MCH}	Pulse duration, MC high	40		ns
t_{MHH}	Pulse duration, MS high	20		ns
t_{MSS}	MS falling edge to MC rising edge	30		ns
t_{MSH}	MS hold time (1)	30		ns
t_{MDH}	MOSI hold time	15		ns
t_{MDS}	MOSI setup time	15		ns
t_{MOS}	MC rising edge to MDO stable		20	ns

(1) MC falling edge for LSB to MS rising edge.

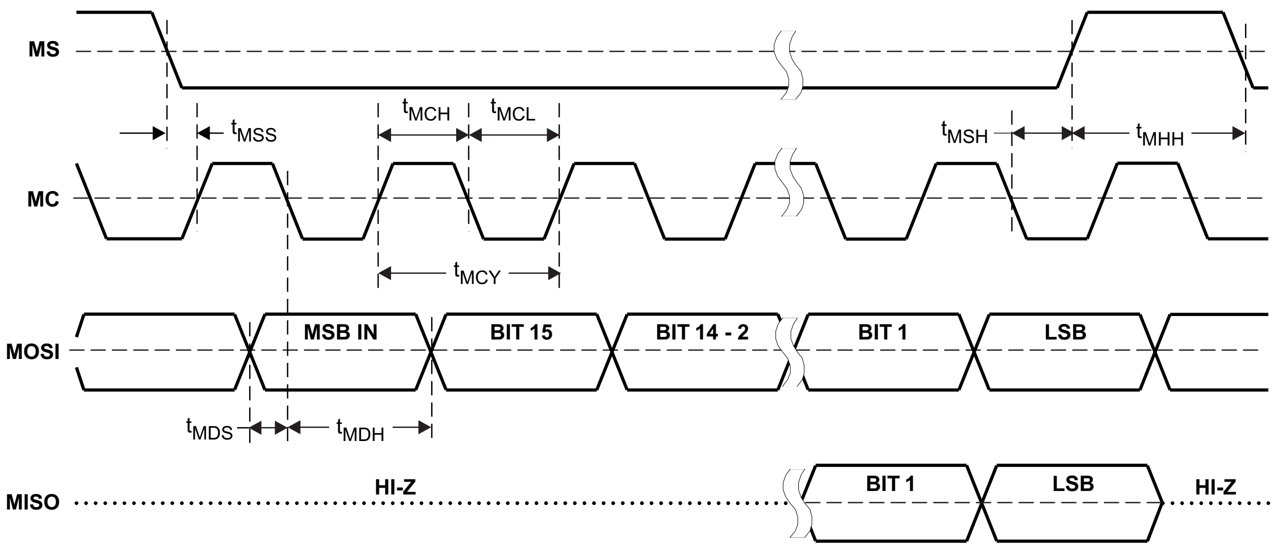


Figure 2. SPI Control Interface Timing

7.11 Timing Requirements: Audio Data Interface for Slave Mode

PARAMETER[(1)]		MIN	TYP	MAX	UNIT
t_{BCKP}	BCK period	1 / (64 × f_S)			ns
t_{BCKH}	BCK pulse duration high	1.5 × t_{SCKI}			ns
t_{BCKL}	BCK pulse duration low	1.5 × t_{SCKI}			ns
t_{LRSU}	LRCK set up time to BCK rising edge	50			ns
t_{LRHD}	LRCK hold time to BCK rising edge	10			ns
t_{LRCP}	LRCK period	10			µs
t_{CKDO}	Delay time BCK falling edge to DOUT valid	–10		40	ns
t_{LRDO}	Delay time LRCK edge to DOUT valid	–10		40	ns
t_R	Rise time of all signals			20	ns
t_F	Fall time of all signals			20	ns

(1) Timing measurement reference level is 1.4 V for input and 0.5VDD for output. Rise and fall times are measured from 10% to 90% of the IN/OUT signals swing. Load capacitance of DOUT is 20 pF. t_{SCKI} means SCKI period.

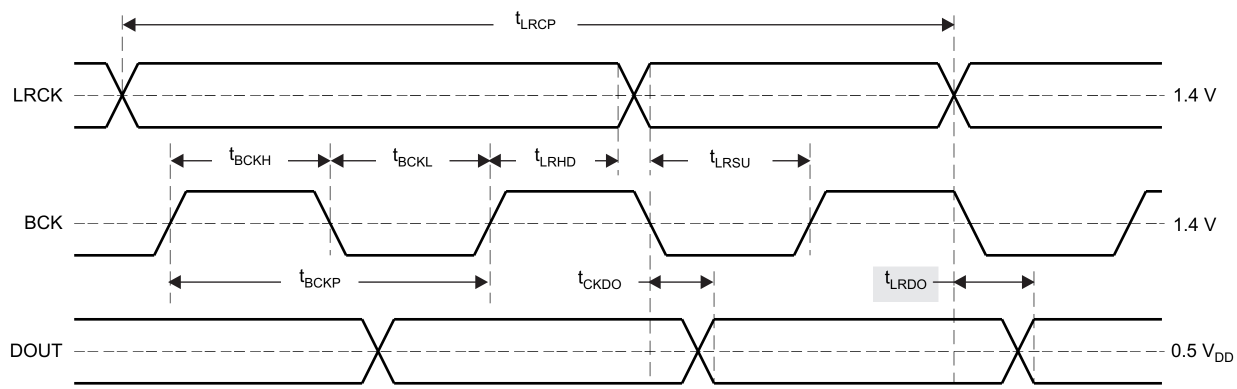


Figure 3. Audio Data Interface Timing, Slave Mode: LRCK and BCK as Inputs

7.12 Timing Requirements: Audio Data Interface for Master Mode

PARAMETER(1)		MIN	TYP	MAX	UNIT
t_{BCKP}	BCK period	150	1 / (64 × f_S)	2000	ns
t_{BCKH}	BCK pulse duration high	65		1000	ns
t_{BCKL}	BCK pulse duration low	65		1000	ns
t_{CKLR}	Delay time BCK falling edge to LRCK valid	–10		20	ns
t_{LRCP}	LRCK period	10	$1/f_S$	125	µs
t_{CKDO}	Delay time BCK falling edge to DOUT valid	–10		20	ns
t_{LRDO}	Delay time LRCK edge to DOUT valid	–10		20	ns
t_R	Rise time of all signals			20	ns
t_F	Fall time of all signals			20	ns
t_{SCKBCK}	Delay time SCKI rising edge to BCK edge(2)	5		30	ns

(1) Timing measurement reference level is 0.5 V_{DD}. Rise and fall times are measured from 10% to 90% of the IN/OUT signals swing. Load capacitance of all signals are 20 pF.
(2) Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Load capacitance of BCK is 20 pF. This timing is applied when SCKI frequency is less than 25 MHz.

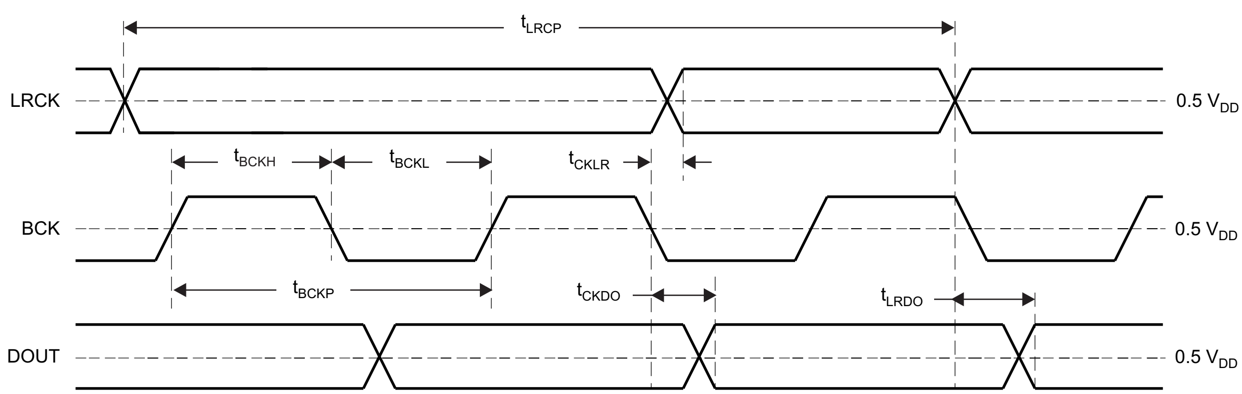


Figure 4. Audio Data Interface Timing, Master Mode: LRCK and BCK as Outputs

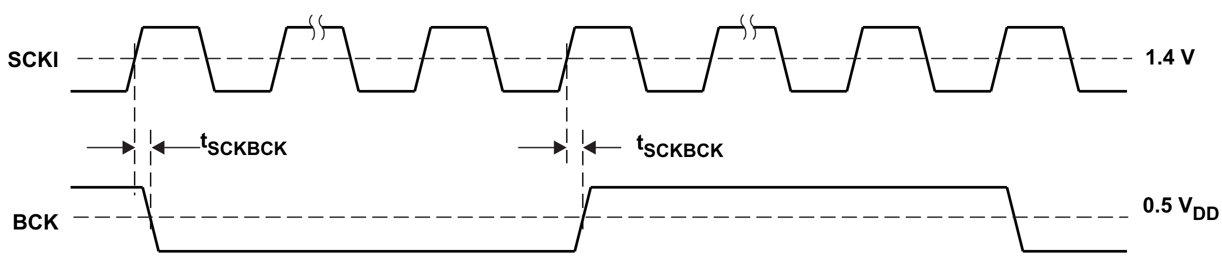
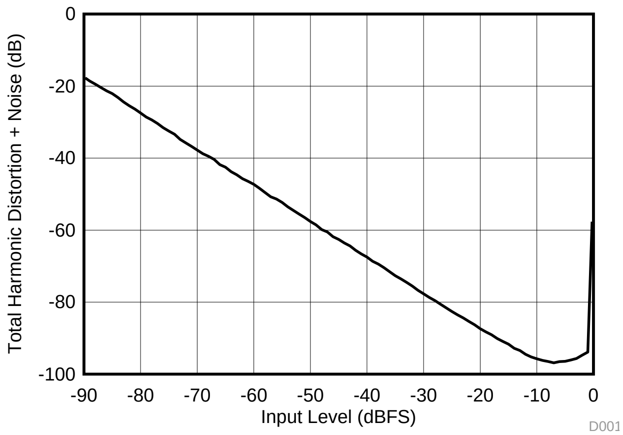


Figure 5. Audio Data Interface Timing, Master Mode: BCK as Outputs

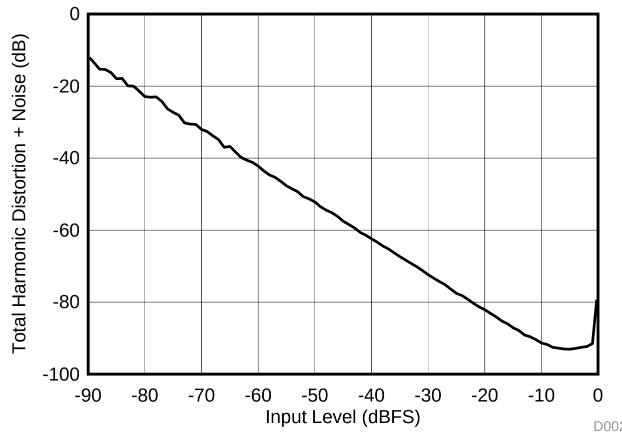
7.13 Typical Characteristics

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 × f_S, and 24-bit data (unless otherwise noted)



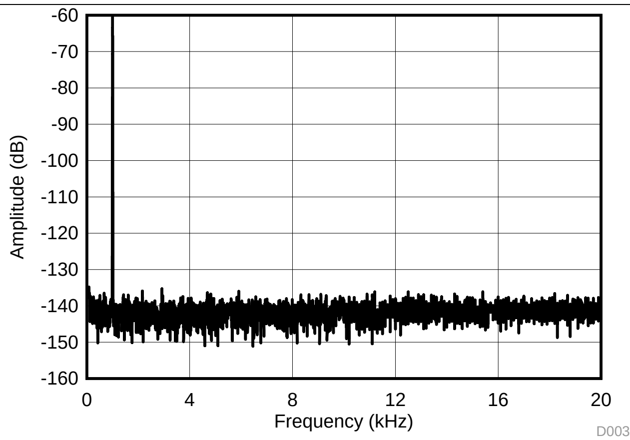
PCM1861-Q1, PCM1863-Q1, and PCM1865-Q1

Figure 6. THD+N vs Input Level



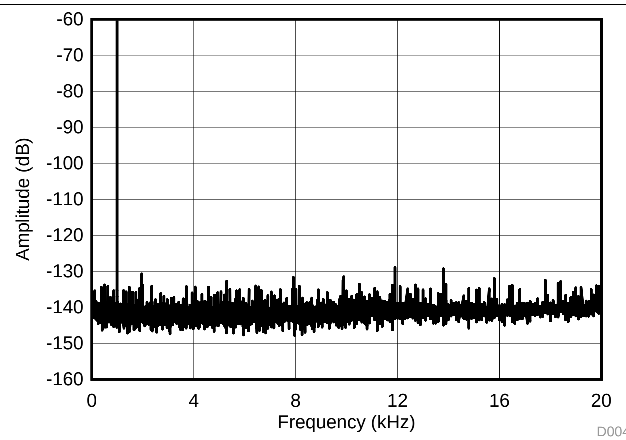
PCM1860-Q1, PCM1862-Q1, and PCM1864-Q1

Figure 7. THD+N vs Input Level



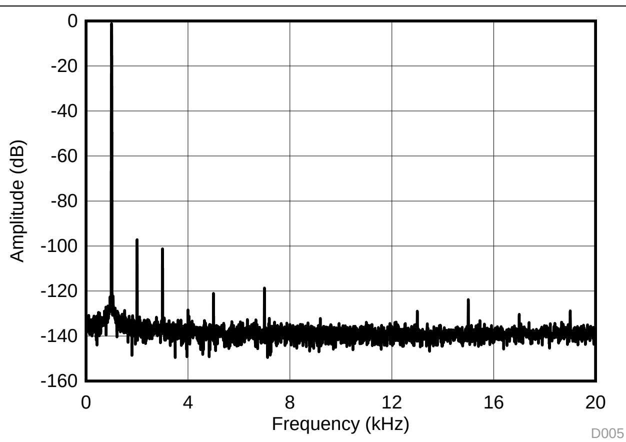
PCM1861-Q1, PCM1863-Q1, and PCM1865-Q1
Input = –60 dBFS at 1 kHz

Figure 8. Main ADC Output FFT



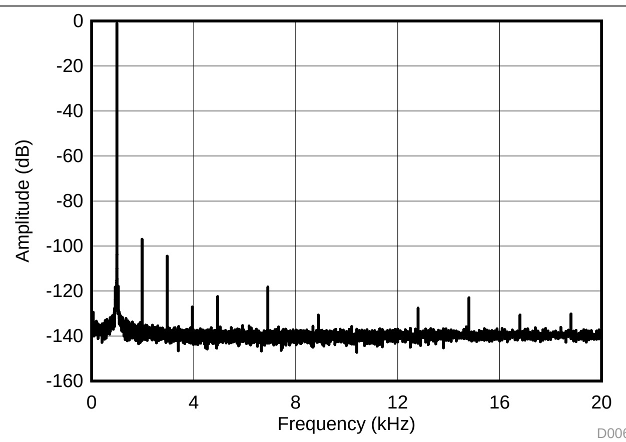
PCM1860-Q1, PCM1862-Q1, and PCM1864-Q1
Input = –60 dBFS at 1 kHz

Figure 9. Main ADC Output FFT



PCM1861-Q1, PCM1863-Q1, and PCM1865-Q1
Input = –1 dBFS at 1 kHz

Figure 10. Main ADC Output FFT

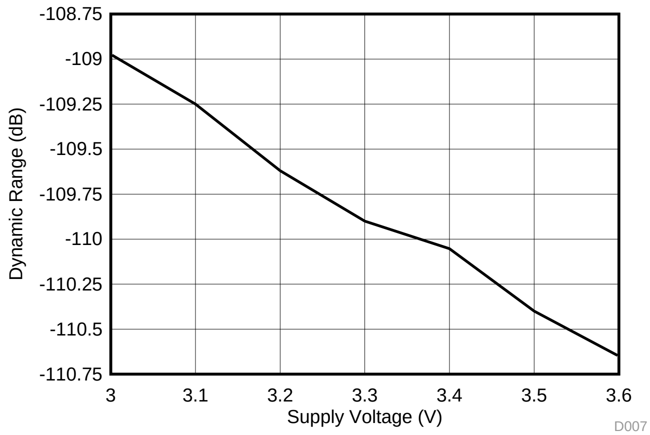


PCM1860-Q1, PCM1862-Q1, and PCM1864-Q1
Input = –1 dBFS at 1 kHz

Figure 11. Main ADC Output FFT

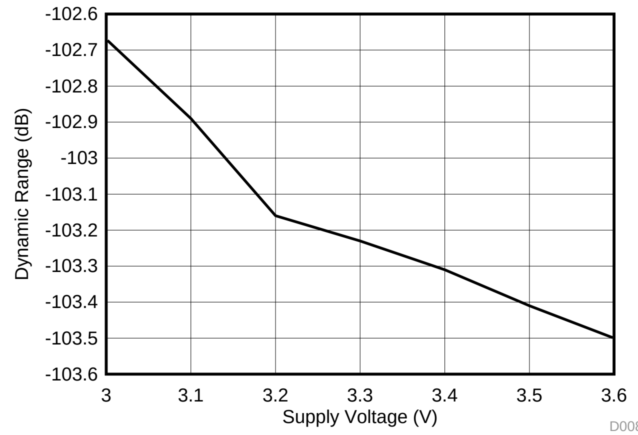
Typical Characteristics (continued)

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 × f_S, and 24-bit data (unless otherwise noted)



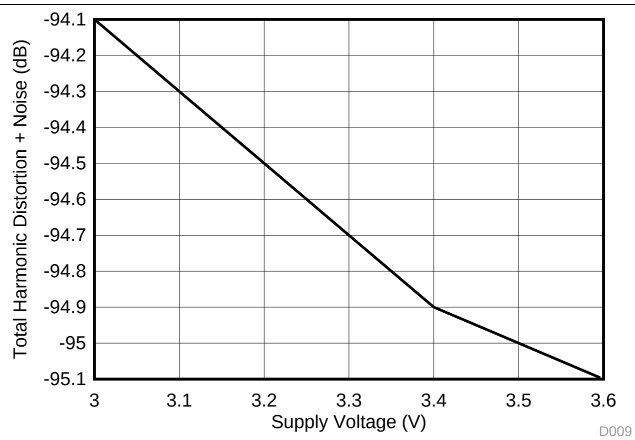
PCM1861-Q1, PCM1863-Q1, and PCM1865-Q1

Figure 12. Dynamic Range vs Supply Voltage



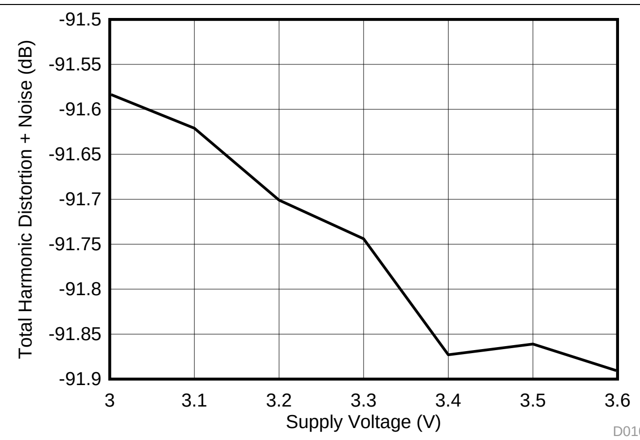
PCM1860-Q1, PCM1862-Q1, and PCM1864-Q1

Figure 13. Dynamic Range vs Supply Voltage



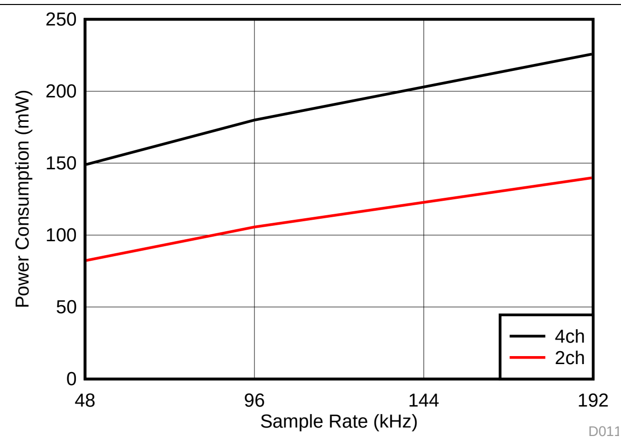
PCM1861-Q1, PCM1863-Q1, and PCM1865-Q1

Figure 14. THD+N vs Supply Voltage



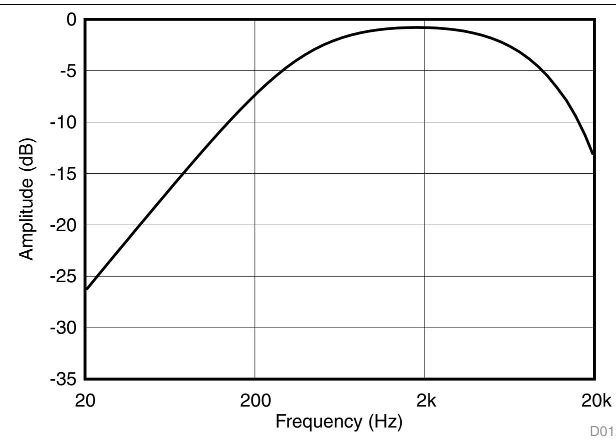
PCM1860-Q1, PCM1862-Q1, and PCM1864-Q1

Figure 15. THD+N vs Supply Voltage



At f_S = 48 kHz, 96 kHz, and 192 kHz

Figure 16. Power Consumption vs Sample Rate

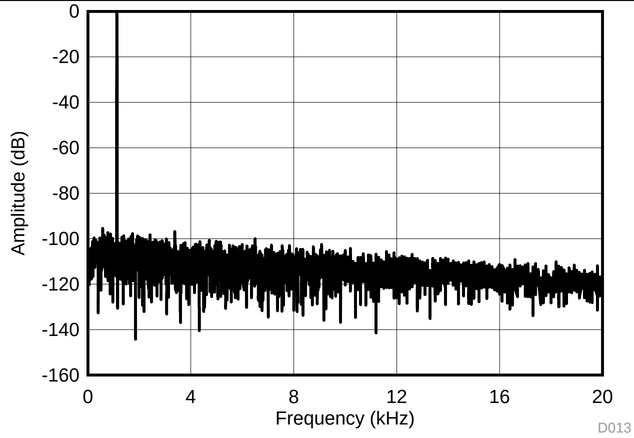


f_S = 48 kHz

Figure 17. Secondary ADC Frequency Response

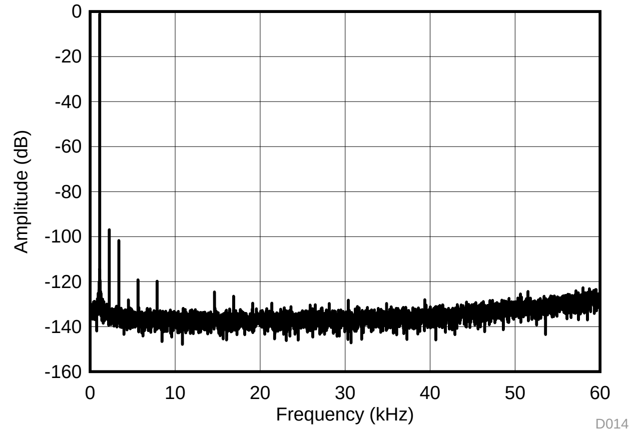
Typical Characteristics (continued)

all specifications at T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, IOVDD = 3.3 V, master mode, single-speed mode, f_S = 48 kHz, system clock = 256 × f_S, and 24-bit data (unless otherwise noted)



f_S = 48 kHz

Figure 18. Secondary ADC FFT



f_S = 192 kHz, BW = 60 kHz, Input = –1 dBFS

Figure 19. High Bandwidth FFT of THD Components

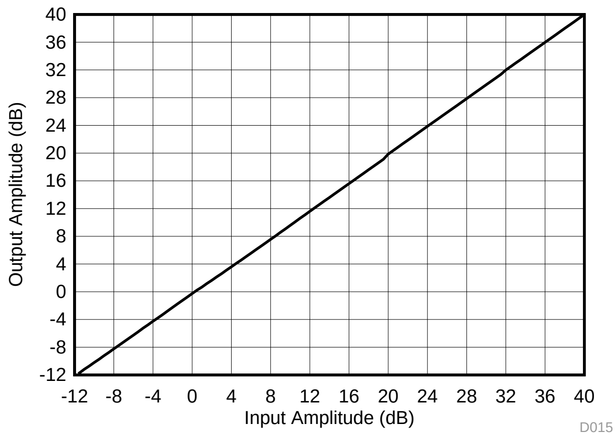


Figure 20. PGA ADC Gain

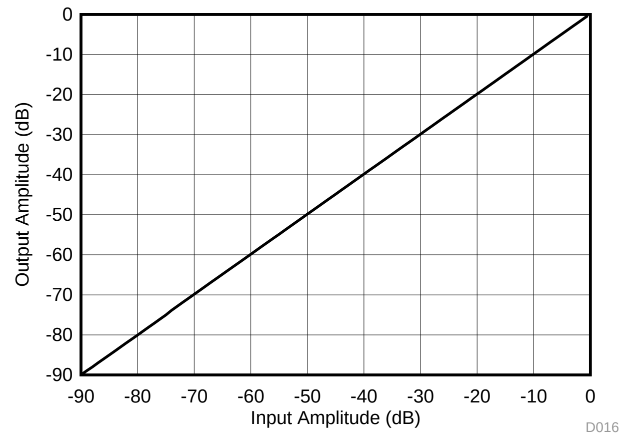


Figure 21. Linearity, Input vs Output

8 Parameter Measurement Information

All typical characteristics for the devices are measured using the respective PCM186x evaluation module (EVM) and an Audio Precision SYS-2722 Audio Analyzer. A programmable serial interface adapter (PSIA) is used to allow the I^2S interface to be driven directly into the SYS-2722. The EVM schematic is shown in Figure 22.

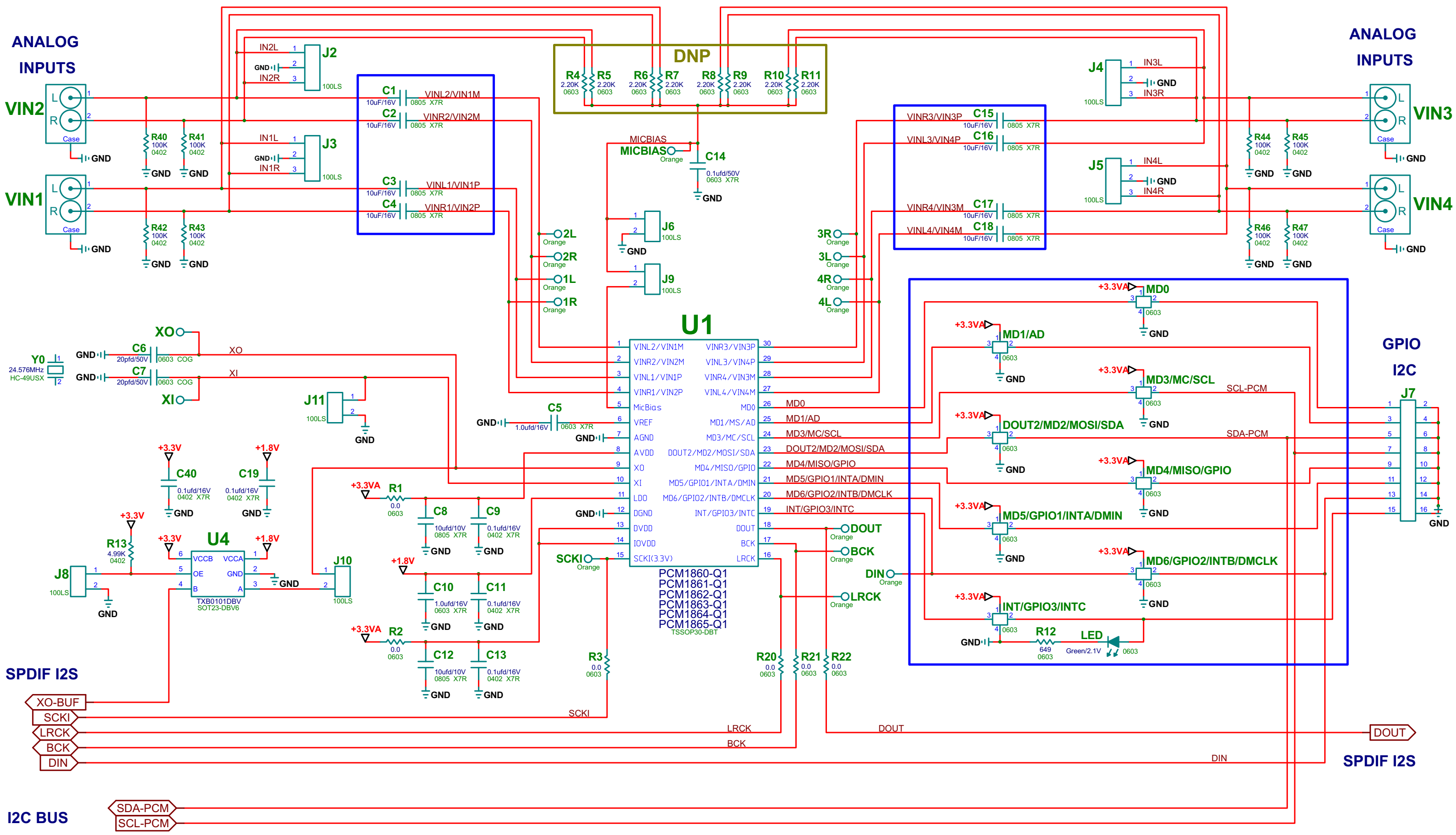


Figure 22. PCM186x-Q1 Test Circuit

9 Detailed Description

9.1 Overview

The PCM186x-Q1 family of automotive-audio, analog-to-digital converters (ADCs) features a highly flexible, audio front end that supports input levels from small millivolt microphone inputs to 2.1-V_{RMS} line inputs. The analog front end can be configured to support either differential or single-ended inputs, providing optimal performance when using differential inputs. Mixing single-ended and differential inputs is possible. A digital microphone interface is available in the software-controlled devices.

These devices support advanced clocking with the aid of an integrated oscillator circuit and an on-chip analog phase-locked loop (PLL). The integrated oscillator circuit allows for the use of an external crystal or an external master clock as the clock source in master mode. In addition, the PLL can be used to generate an on-chip master clock that can be shared with the rest of the system, all from a bit clock input. This feature is useful in systems where the audio source has no master clock to drive digital-to-analog converters (DACs) and amplifiers. The on-chip clock monitoring system can also be monitored by the system microcontroller, in case clocks are lost and the device enters sleep or standby state.

The secondary analog-to-digital converter (ADC) is a low-power, non-audio ADC that is used in sleep mode to monitor the analog inputs. The secondary ADC is also used in *controlsense* mode to measure dc voltages in a system, such as battery voltage and control potentiometers. In addition, *controlsense* features offer an option to generate interrupts after detected voltages cross specific thresholds, allowing the microcontroller to be in a lower-power sleep mode while the control voltages being measured are stable.

Control registers in this data sheet are shown as *REGISTER_BIT_or_BYTE_NAME* (*page.x hex_address*).

9.2 Functional Block Diagrams

The high level block diagrams, Figure 23 to Figure 25, show the differences between the PCM186x-Q1 family. An internal block diagram of the PCM186x-Q1 family is shown in Figure 26.

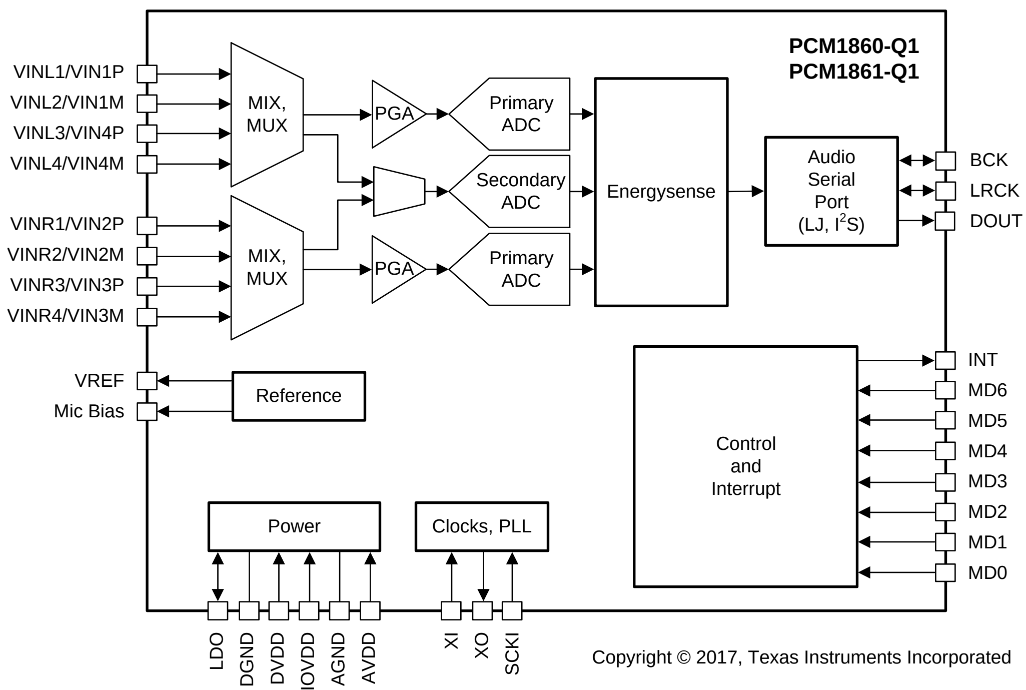


Figure 23. PCM1860-Q1 and PCM1861-Q1

Functional Block Diagrams (continued)

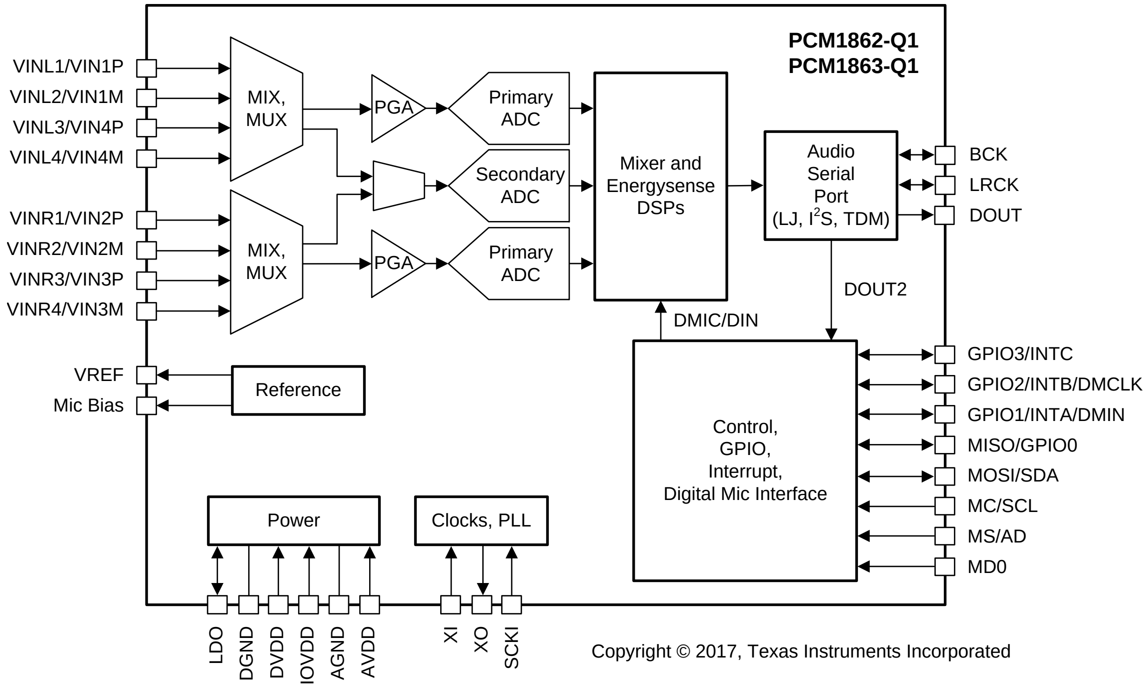


Figure 24. PCM1862-Q1 and PCM1863-Q1

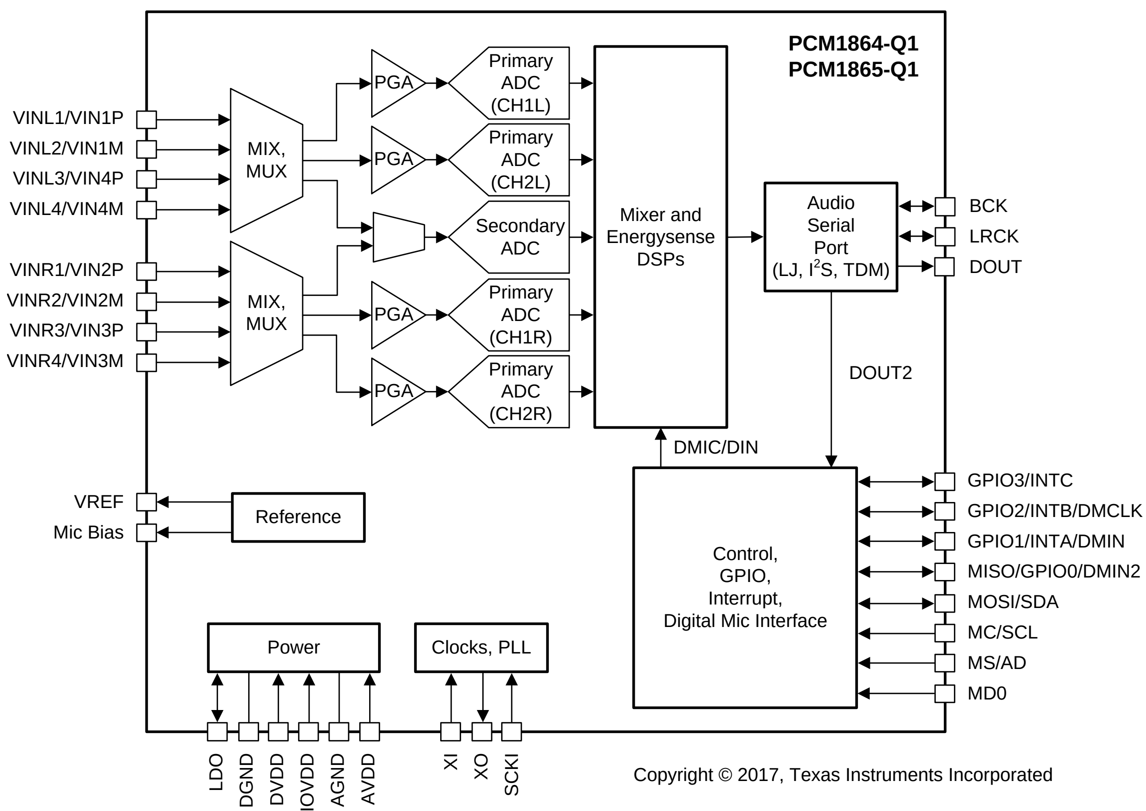


Figure 25. PCM1864-Q1 and PCM1865-Q1

Functional Block Diagrams (continued)

Power supplies and references have been omitted from this diagram for simplicity. Dotted lines, for the programmable gain amplifier (PGA) and the additional ADCs, are for the 4-channel devices only. Greyed-out pins are multifunction pins only.

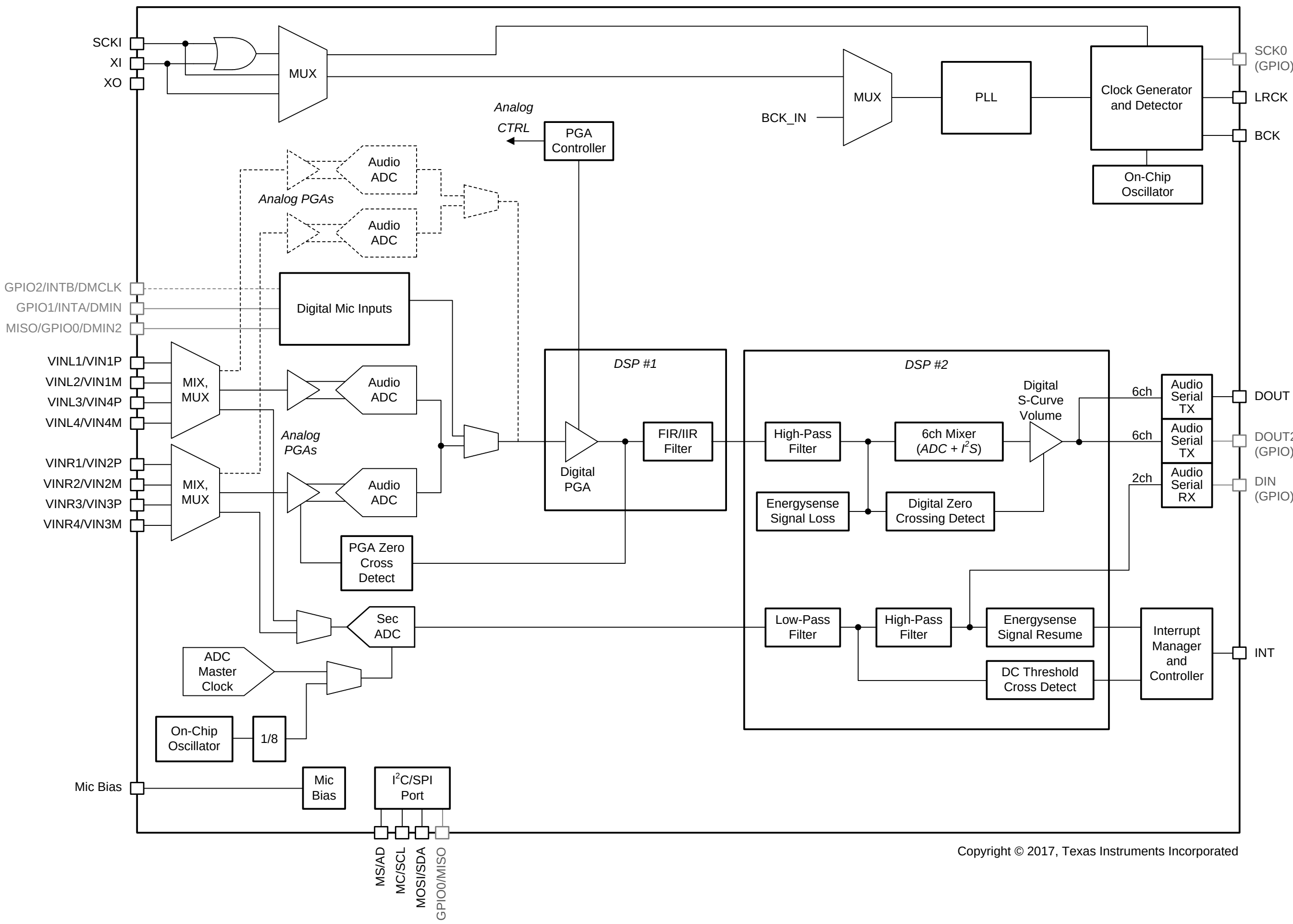


Figure 26. Internal Block Diagram of the PCM186x-Q1

9.3 Features Description

9.3.1 Analog Front End

The PCM186x-Q1 has a flexible front end that accepts either differential or single-ended inputs. The device supports up to 2.1 VRMS in single-ended mode, and up to 4.2 VRMS in differential mode.

The MIX and MUX circuit before the PGA allows the analog inputs to be mixed and multiplexed in both single-ended and differential modes. Mixing functionality is available in software-controlled devices only. No individual gain controls are available before the PGA. A high-level diagram of the front-end circuitry is shown in Figure 27.

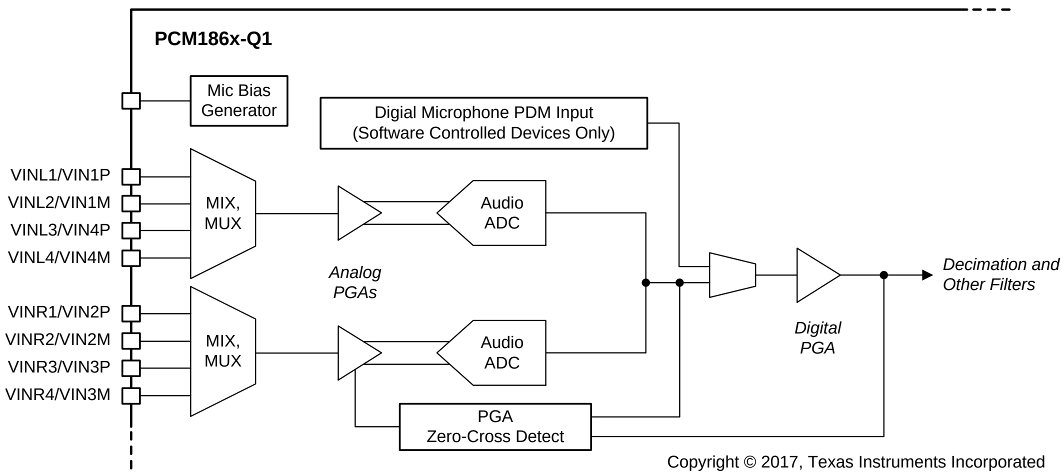


Figure 27. High Level View of PCM186x-Q1 Front End-Circuitry

DC blocking capacitors are required on the analog inputs to make sure that correct dc bias conditions are established. Because the value of the output short-circuit protection resistor in the source product is typically unknown, issues such as gain error and dc shift may occur if dc blocking capacitors are not used.

For systems where external amplifiers are used before the PCM186x-Q1, dc blocking capacitors are still recommended because the input pins are designed to bias to AVDD / 2. The common mode voltage range is still limited to the maximum input voltage of the device.

Do not connect unused analog input pins.

Features Description (continued)

9.3.2 Microphone Support

The PCM186x-Q1 supports analog and digital microphones. Analog signals are treated the same way as line-level signals, except for the requirement for mic bias. Digital microphone Inputs (PDM inputs) use GPIOs on the device. Two-channel ADC variants of the PCM186x-Q1 family can support two digital microphones using a single data pin and a single clock pin. The 4-channel variants can support up to 4 digital microphones (2 data pins).

The PCM1860-Q1 and PCM1861-Q1 offer three pin-selectable gain options, 0 dB, 12 dB, or 32 dB.

The PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, and PCM1865-Q1 offer programmable gain options from –12 dB to +32 dB with –0.5-dB step intervals.

Digital microphones typically have a PDM output that can be brought into an ADC digital decimation filter. PDM microphones require power and a clock. Power should be handled from an external source.

Digital microphone mode gain can be added in the digital PGA and in the mixer. In digital microphone mode, the PCM1862-Q1 and PCM1863-Q1 offer up to 18-dB gain (mixer only); whereas, the PCM1864-Q1 and PCM1865-Q1 offer up to 30-dB gain (18 dB from mixer and 12 dB from digital PGA).

On the PCM1864-Q1 and PCM1865-Q1, a 2-channel digital mic + 2-channel ADC mode is possible. With the PCM1862-Q1 or PCM1863-Q1, four channels are only possible with a ADC + I^2S input configuration.

9.3.2.1 Mic Bias

The PCM186x-Q1 can provide a microphone bias to power and bias microphones at 2.6 V on pin 5. Decouple or filter the Mic Bias pin with an external capacitor. Mic Bias is typically used with a electret microphone. The internal regulator, as well as an on-chip terminating resistor to GND can also be enabled using register MIC_BIAS_CTRL (Page.3, 0x15). By default, the device is configured to bypass the on-chip resistor. The mic bias pin can be left unconnected if not used.

9.3.3 Input Multiplexer (PCM1860-Q1 and PCM1861-Q1)

The hardware-controlled devices can support a wide gain range using the MD2, MD5 and MD6 configuration pins as shown in Table 1.

Table 1. Channel and Gain Selection for Hardware-Controlled Devices

MD6	MD5	MD2	ADC1_L / PGA1_L	ADC1_R / PGA1_R
L	L	L	S.E - VINL1 / 0 dB	S.E - VINR1 / 0 dB
L	L	H	S.E - VINL2 / 0 dB	S.E - VINR2 / 0 dB
L	H	L	S.E - VINL3 / 0 dB	S.E - VINR3 / 0 dB
L	H	H	S.E - VINL4 / 0 dB	S.E - VINR4 / 0 dB
H	L	L	S.E - VINL4 / 12 dB	S.E - VINR4 / 12 dB
H	L	H	S.E - VINL4 / 32 dB	S.E - VINR4 / 32 dB
H	H	L	Diff(VIN1P/VIN1M) / 0 dB	Diff(VIN2P/VIN2M) / 0 dB
H	H	H	Diff(VIN3P/VIN3M) / 12 dB	Diff(VIN4P/VIN4M) / 12 dB

9.3.4 Mixers and Multiplexers (PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, and PCM1865-Q1)

The PCM186x-Q1 software-controlled devices offer a mix and multiplex level of functionality on the front end, as shown in Figure 27. The switches integrated into the multiplexer can also be switched on in parallel, offering a direct mix of inputs. This function can be selected by register for each ADC input selection, ADCX1_INPUT_SEL_X (Page.0, 0x06 → 0x09). In single ended mode, each Audio ADC is tightly coupled to a dedicated PGA and MUX. ADC1L (and ADC2L on the PCM1864-Q1 and PCM1865-Q1) is connected a mux that has input pins VINLx, (x = 1 to 4). ADC1R (and ADC2R on the PCM1864-Q1 and PCM1865-Q1) is connected to a mux that has input pins VINRx (x = 1 to 4).

Mixing between the left channels of stereo pairs is possible in the mux dedicated to ADC1L and right channels of stereo pairs in the mux dedicated to ADC1R. In addition, polarity of the inputs can be inverted using the MSB of the select register. Mixing left and right sources to create mono mixes can only be done in the digital mixer, post ADC conversion, or alternatively, other analog inputs can be connected for mixing.

The examples available are shown in Table 2, where [SE] is single-ended, and [DIFF] is a differential input.

Table 2. MUX, MIX, and Polarity Input Selection(1)

REGISTER CODE	ADC1L AND ADC2L	ADC1R AND ADC2R
0x00	No Selection (Mute)	No Selection (Mute)
0x01	**VINL1[SE] (Default)**	**VINR1[SE] (Default)**
0x02	**VINL2[SE]**	**VINR2[SE]**
0x03	VINL2[SE] + VINL1[SE]	VINR2[SE] + VINR1[SE]
0x04	**VINL3[SE]**	**VINR3[SE]**
0x05	VINL3[SE] + VINL1[SE]	VINR3[SE] + VINR1[SE]
0x06	VINL3[SE] + VINL2[SE]	VINR3[SE] + VINR2[SE]
0x07	VINL3[SE] + VINL2[SE] + VINL1[SE]	VINR3[SE] + VINR2[SE] + VINR1[SE]
0x08	**VINL4[SE]**	**VINR4[SE]**
0x09	VINL4[SE] + VINL1[SE]	VINR4[SE] + VINR1[SE]
0x0A	VINL4[SE] + VINL2[SE]	VINR4[SE] + VINR2[SE]
0x0B	VINL4[SE] + VINL2[SE] + VINL1[SE]	VINR4[SE] + VINR2[SE] + VINR1[SE]
0x0C	VINL4[SE] + VINL3[SE]	VINR4[SE] + VINR3[SE]
0x0D	VINL4[SE] + VINL3[SE] + VINL1[SE]	VINR4[SE] + VINR3[SE] + VINR1[SE]
0x0E	VINL4[SE] + VINL3[SE] + VINL2[SE]	VINR4[SE] + VINR3[SE] + VINR2[SE]
0x0F	VINL4[SE] + VINL3[SE] + VINL2[SE] + VINL1[SE]	VINR4[SE] + VINR3[SE] + VINR2[SE] + VINR1[SE]
0x10	**{VIN1P, VIN1M}[DIFF]**	**{VIN2P, VIN2M}[DIFF]**
0x20	**{VIN4P, VIN4M}[DIFF]**	**{VIN3P, VIN3M}[DIFF]**
0x30	{VIN1P, VIN1M}[DIFF] + {VIN4P, VIN4M}[DIFF]	{VIN2P, VIN2M}[DIFF] + {VIN3P, VIN3M}[DIFF]

(1) **Bold** items are channel options for hardware-controlled devices.

9.3.5 Programmable Gain Amplifier

The PCM186x-Q1 has a two-stage programmable gain amplifier (PGA). Coarse gain adjustment is done in the analog domain, and fine gain adjustment is done in the digital domain. The ±12-dB analog gain steps are designed for varying line level inputs, whereas the 20 dB and 32 dB are primarily designed for microphone inputs, and will likely need additional gain that can be done in the digital domain. The analog gain steps between –12 dB and +12 dB are in 1-dB steps. Half-dB steps between those points are done in the digital PGA. Gain steps between 12 dB and 20 dB are all done in the digital domain. (for example, 18-dB gain = 12-dB analog + 6-dB digital). The gain structure in the PCM186x-Q1 is shown in Figure 28.

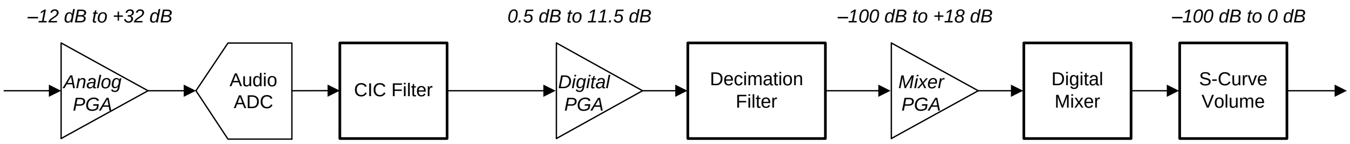


Figure 28. PCM186x-Q1 Complete Gain Structure (PGAs and Attenuator)

The analog gain steps within the analog PGA are shown in Figure 29. Again, from –12 dB to +12 dB, the steps are 1 dB each. The digital PGA has granularity down to 0.5 dB.

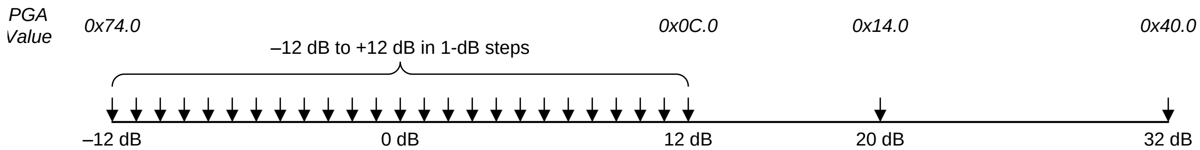


Figure 29. Analog Gain Steps With Software-Controlled Devices

The PGA in the PCM186x-Q1 is a hybrid analog and digital programmable gain amplifier. The devices integrate a lookup table with the optimal gain balance between analog and digital gain, allowing the gain to be set in a single register per channel. For example, set 18 dB gain, and the system allocates 12 dB to the analog PGA, and 6 dB to the digital PGA. This function is called auto gain mapping.

The PGA is a zero crossing detect type, and has the ability to set target gain, and have the device work towards it (with a timeout if there is no zero crossing). Any changes in the Analog PGA and digital PGA are designed to step towards the final level. However, any changes in the mixer PGA are immediate. Take care when changing gain levels in the digital mixer PGA. Alternatively, multiple writes can be made of small enough values that do not cause significant pops or clicks.

NOTE

Changing gain in the PGA requires the on-chip DSP to be clocked. The DSP is used to calculate the steps to the target gain. This is not an issue in master mode, but can be a challenge in slave mode, if the system master is not active yet.

For example, if the current level = 0 dB, then set the target as 3.5 dB. The PGA then increases gain in 0.5-dB steps towards 3.5 dB.

The auto gain mapping function can by bypassed if required, using manual gain mapping. Manual gain mapping is useful when using digital microphones, as the PDM input signal bypasses the analog PGA and must be amplified using the digital PGA. (PGA_MODE (Page.0, 0x19). Digital PGA update is only available in the 4-channel devices because the digital gain in 2-channel devices is fixed to 0 dB when manual gain mapping is enabled.

NOTE

Using the device with a differential inputs increases the full-scale voltage to 4.2 V_{RMS} (that's 2.1 V_{RMS} per pin, out of phase).

9.3.6 Automatic Clipping Suppression

The PCM186x-Q1 software-controlled devices have the ability to automatically lower the gain in 0.5 dB steps under the following conditions if the ADC is clipping.

The device detects clipping after the decimation filter in the signal chain, shown in Figure 30, and counts the number of successive clips before responding.

The device also generates an internal interrupt that can be mapped to a GPIO or interrupt pin, allowing the system microcontroller to make the decision to increase the gain and consider the clipping an isolated event, or make the decision that the new gain setting is appropriate.

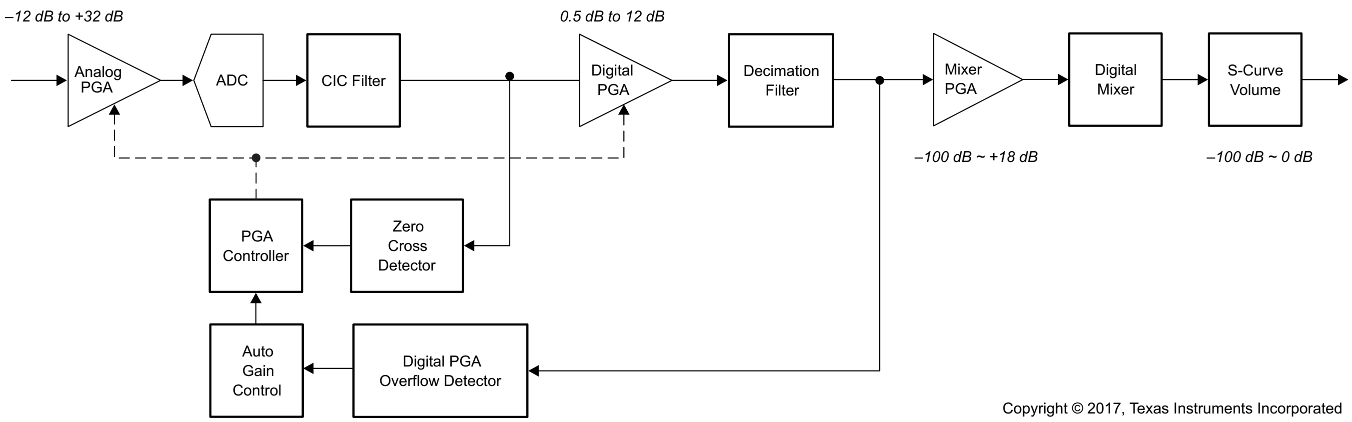


Figure 30. Sampling Points Within the PCM186x-Q1 for Auto Clipping Suppression

9.3.6.1 *Attenuation Level*

This feature is not designed to be a complete analog gain control. This feature was defined to avoid clipping, and to inform the system microcontroller of a clipping event, to allow the microcontroller (or the end user) to decide if the gain should be increased again.

The attenuation is programmable to –3 dB, –4 dB, –5 dB, or –6 dB.

9.3.6.2 *Channel Linking*

Depending on the application, users may not want to link input channels, however, for the majority of stereo input applications, its strongly recommended to set the system to track gain across inputs, to maintain balance.

The auto PGA clipping suppression control has the settings shown in Table 3.

Table 3. Auto Clipping Suppression Control Registers

REGISTER NAME	REGISTER LOCATION	USAGE	VALUES
AGC_EN	Pg0 0x05	Enable auto gain control	0: Disable (Default) 1: Enable
CLIP_NUM[1:0]	Pg0 0x05	Start auto gain control after detects CLIP_NUM times of ADC sample clips	0: 80 1: 40 2: 20 3: 10 (Default)
MAX_ATT[1:0]	Pg0 0x05	Maximum automatic attenuation	0: –3 dB (Default) 1: –4 dB 2: –5 dB 3: –6 dB
DPGA_CLIP_EN	Pg0 0x05	Enable clipping detection after the digital PGA. Note that digital PGA is post ADC, meaning that there is a short delay before clipping is detected.	0: Disable (Default) 1: Enable
LINK	Pg0 0x05	Link all channels together if dealing with stereo sources to maintain balance.	0: Independent control (Default) 1: Ch1[R]/Ch2[L]/Ch2[R] follow Ch1[L] PGA value.
SMOOTH	Pg0 0x05	Enable smooth transition from step to step (zero crossing).	0: Immediate change 1: Smooth change (default)

9.3.7 Zero Crossing Detect

The PCM186x-Q1 uses a zero crossing detector to make gain changes only when the incoming signal crosses the halfway point between negative and positive swing, reducing zipper noise.

There are two sources for the controller, the output of the ADC modulator and the output from the digital PGA. The analog PGA is sampled at four times the audio sampling rate to detect the zero crossing. The digital PGA is sampled at a similar rate.

The process for changing gain in the PCM186x-Q1 is as follows:

1. Detect a zero crossing of the oversampled analog input channel.
2. Increment or decrement the gain toward the target PGA value step by 0.5 dB.
3. Repeat from (1) until arrival at the target PGA value.
4. If zero crossing does not occur for 8192 sample times (= time out), change the gain per sample.

This process does not require intervention by the user. This data serves as information only. Also, please note that DSPs must be running (clocked) for this functionality to work.

9.3.8 Digital Inputs

9.3.8.1 Stereo PCM Sources

The PCM186x-Q1 can support stereo PCM data on GPIO pins so that I^{2}S sources, such as wireless modules can have their data mixed with the incoming analog content. The clock rate of the incoming data (known as DIN) must be synchronous with the PCM186x-Q1 software-controlled device main clocks. There is no integrated sample rate converter on-chip. The DIN signal can be received on GPIO0, 1, 2, or 3, and configured on GPIO_FUNC_X (Page.0 0x10 and 0x11). The incoming data are then driven to the digital mixer running on DSP2.

The audio format can be configured separately from the output serial port using register RX_TDM_OFFSET (P0, 0x0E).

Inputs can be mixed and volume-controlled before routing to a digital amplifier. Typical uses could be the connection to a Bluetooth™ module. The mixing and crossfading is done all in the PCM186x-Q1, rather than a hard switch in external logic. The on-chip PLL also helps create the system master clock (SCKOUT) for poorly designed I^{2}S Bluetooth modules that do not provide a system clock to drive the system DACs.

If the stereo PCM data source has a requirement to drive the audio clock pins when transmitting in a system where the PCM186x-Q1 has not been set to slave yet, the PCM186x-Q1 does not suffer any damage during clock driver contention. However, the PCM186x-Q1 will have some irregular output due to clock errors. In systems with additional stereo PCM sources that need to be master (such as a S/PDIF receive), set the PCM186x-Q1 to always be a clock slave, or switch the device from master to slave mode, before enabling the stereo PCM source.

9.3.8.2 Digital PDM Microphones

Up to four digital microphones are supported on the PCM1864-Q1 and PCM1865-Q1, using a shared output clock (configured from GPIO2) and two data lines, GPIO0 or GPIO1. Two digital microphones are supported on the PCM1862-Q1 and PCM1863-Q1, mainly using GPIO1 as the data input. The PCM1860-Q1 or PCM1861-Q1 does not support digital microphones. The typical connection and protocol diagrams for these microphones are shown in Figure 31 and Figure 32.

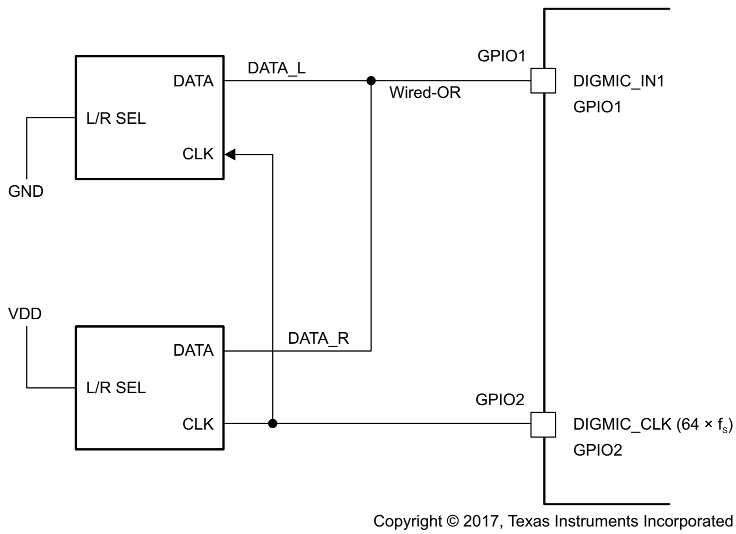


Figure 31. Digital Microphone Example Connection

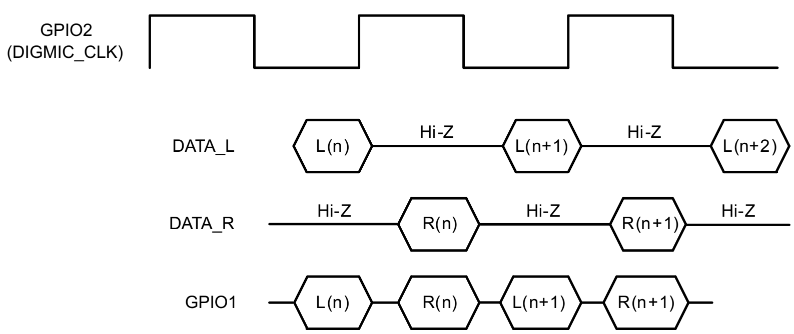


Figure 32. Digital Microphone Protocol

Supported Digital Microphone clock frequency is as follows, and the frequency depends on required operating sampling frequency as follows:

- 2.0480 MHz (32 kHz × 64)
- 2.8224 MHz (44.1 kHz × 64)
- 3.072 MHz (48 kHz × 64)
- 3.072 MHz (96 kHz × 32)

The recommended operating conditions for the Digital MIC are:

- Sampling frequency is 32 kHz or 44.1 kHz
- SCK is 256 × f_S.
- Enable Auto Clock Detector (Default)

9.3.9 Clocks

9.3.9.1 Description

The PCM186x-Q1 family has an extremely flexible clocking architecture. All converters require a master clock (typically, a 2^n power of the sampling rate known as MCK), a bit clock (BCK) that is used to clock the data bit-by-bit out of the device (typically running at 64-f_S to allow up to 32 bits per channel output), and finally a wordclock (left-right clock, LRCK) that is used to set the exact sampling point for the ADC.

The PCM186x-Q1 family can be a clock master (where BCK and LRCK can be internally divided from a provided master clock) or can be a clock slave, where all clocks (MCK, BCK and LRCK) must be provided by an external source.

Unlike many competing devices, the PCM186x-Q1 family can source its master clock from two different sources, either an external crystal, or a CMOS level (3.3 V or 1.8 V) clock, eliminating the usual external crystal oscillator circuit required to source a CMOS clock signal.

The PCM186x-Q1 also differentiates itself by integrating an on-chip phase locked loop (PLL) that can generate real audio-rate clocks from any clock source between 1 MHz and 50 MHz. The PCM1860-Q1 or PCM1861-Q1 hardware-controlled devices have the ability to detect an absence of MCK in slave mode and automatically generate a MCK signal. Software-controlled devices, such as the PCM1862-Q1, PCM1863-Q1, PCM1864-Q1 and PCM1865-Q1 can have their PLL programmed to generate audio clocks based on any incoming clock rate. For example, a 12 MHz clock in the system can be used to generate clocks for a 44.1-kHz system.

9.3.9.2 External Clock-Source Limits

The three different clock sources for the device each have some limits in terms of their input circuitry, as shown in Table 4. These limits are separate from the internal PLL capability.

On PCM1860-Q1 and PCM1861-Q1, the highest standard frequency supported by an XTAL is 96 kHz, because the lowest divider ratio of master clock to LRCK is 256 (24.576 MHz / 256 = 96 kHz). This limitation is not present in the software-controlled devices because the divider ratio is programmable. However, 192 kHz can be supported by using an external CMOS source.

Table 4. External Clock-Source Limitations and Notes

CLOCK SOURCE	LIMITS	NOTES
XTAL	15 MHz → 35 MHz	
3.3-V CMOS MCLK	1 MHz → 50 MHz	Should be input to SCKI pin. 3.3 V CMOS can be input, even when IOVDD is 1.8 V
1.8-V CMOS MCLK	1 MHz → 50 MHz	Should be input to XI pin.

9.3.9.3 Device Clock Distribution and Generation

PLLs can be used in all modes to generate the clocks required to run both fixed-function DSPs. The dividers are automatically configured based on the clock rate detection. The clock architecture shown in Figure 33 allows non-audio clock sources to be used as clock sources and the PCM186x-Q1 to continue to run in a master mode, providing all PCM and I^2S clocks for other converters in the system.

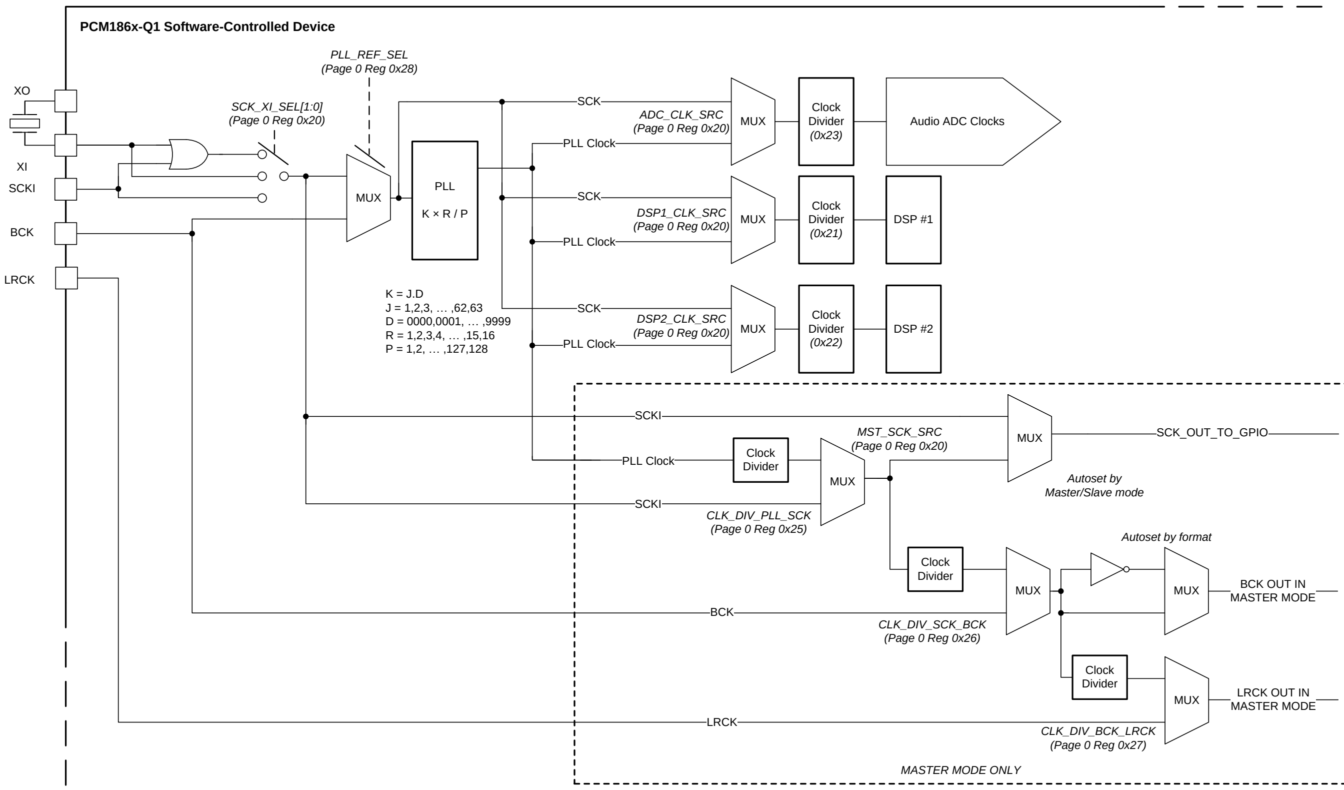


Figure 33. PCM186x-Q1 Main Audio Clock Tree and Clock Generation

Target Clock Rates for the ADC, DSP1 and DSP2 can be seen in Table 9 and Table 10. In manual clock configuration modes, the dividers should be set to achieve these targets. In short, for 2-channel devices, DSP1 and DSP2 should be 256x the sampling rate; for 4-channel devices, DSP1 should be configured for 512x the sampling rate, and DSP2 should be 256x.

9.3.9.4 Clocking Modes

As shown in Table 5, there are four different clocking modes available on the device that take advantage of the onboard PLL and clock detection. Advanced clock detection and a smart internal state engine in the PCM186x-Q1 can automatically configure the various dividers in the device (see the *Device Clock Distribution and Generation* section) with optimized values. Automatic clock configuration is enabled by default, using the register **CLKDET_EN (Page.0, 0x20)**.

Table 5. PCM186x-Q1 Clocking Modes

NAME	DEVICE	External XTAL/MCK INPUT	BCK, LRCK DIRECTION	PLL CONFIGURATION
ADC master mode	PCM186x-Q1	YES	OUT	Not required
ADC slave mode	PCM186x-Q1	YES	IN	Not required
ADC slave PLL mode	PCM186x-Q1	NO	IN	Automatic for standard audio rates
ADC non-audio MCK	PCM1862-Q1 PCM1863-Q1 PCM1864-Q1 PCM1865-Q1	YES	OUT	Manual

9.3.9.4.1 Clock Configuration and Selection for Hardware-Controlled Devices

The PCM1860-Q1 and PCM1861-Q1 hardware-controlled devices offer both master and slave functionality. In master mode, a source master clock (of 256x, 384x, or 512x the sampling rate) can be sourced from either an external crystal (XI/XO) or on an incoming SCK. (see the *External Clock-Source Limits* section for input rate limitations on SCK sources) The clock from XI and SCK are OR-ed internally, allowing either to be used.

These hardware-controlled devices can generate the other I^2S clocks (BCK and LRCK) in master mode (with dividers set in MD0 and MD1) or be a clock slave to MCK,BCK and LRCK. In this scenario, the device auto-detects the clock divider ratio.

In master mode, BCK per LRCK is fixed at 64, and allows up to 32 bits per channel.

Selection of the appropriate master or slave, and clock ratio between MCK and f_S can be done using MD0 and MD1.

Table 6 shows the suggested master clock rates for each of the sample rates supported. For slave mode, set BCK per LRCK to 64.

Table 6. External Master Clock Rate Versus Sampling Frequency

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	256 × f_S	384 × f_S	512 × f_S
8.0	2.048	3.072	4.096
16.0	4.096	6.144	8.192
32.0	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48.0	12.2880	18.4320	24.5760
64.0	16.3840	24.5760	32.7680
88.2	22.5792	33.8688	45.1584
96.0	24.5760	36.8640	49.1520
176.4	45.1584	—	—
192.0	49.1520	—	—

9.3.9.4.2 Clock Sources for Software-Controlled Devices

The PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, and PCM1865-Q1 software-controlled devices support a wide range of options for generating the clocks required to operate the ADC section, as well as an interface and other control blocks, as shown in Figure 34.

The clocks for the PLL require a source reference clock. This clock source can be configured on software devices as the XTAL, SCK or BCK.

These software-controlled devices share a similar clock tree for the generation and distribution of clocks, as shown in Figure 33.

Register CLK_MODE (Page.0 0x20) is used to configure the clock configuration. Bits [5:7] configure the OR and MUX for the incoming MCLK.

Register MST_MODE (Page.0 0x20) is used to set the device in master or slave mode. Bits [1:3] set clock sources for the ADC, DSP1 and DSP2. These can mostly be ignored for the most common applications, but are provided for advanced users.

Register MST_SCK_SRC (Page.0 0x20) is used to set the source of the SCKO in master mode. The master mode BCK and LRCK will be a division of this. The selection is either SCKI/XTI or PLL. PLL can be used when you have a non-audio rate reference clock (BCK or SCKI), as well as when you have an SCKI that is much too slow for what is required for SCKO.

Most applications will use XTI/SCKI as the source for master mode SCK.

The CLKDET_EN (Page.0, 0x20) register bit (auto clock detector) is important; the clock detector is mainly functional for slave modes, and for master modes where the master clock is a 256×, 384×, or 512× multiple of the incoming data rate.

The relation between the master mode configuration registers is shown in Table 7.

NOTE

Non audio related master clock sources can be used with the PCM186x-Q1 software - controlled devices providing the PLL is programmed manually. CLKDET_EN should be set to 0.

The result of configurations can be checked by reading registers FS_INFO / CURRENT_BCK_RATIO (Page.0 0x73 and 0x74).

NOTE

In master mode on software-controlled devices, only the following BCK to LRCK ratios are supported: 32x, 48x, 64x and 256x. 128x is not supported

Table 7. Master Mode Clock Configuration Registers

CLOCK MULTIPLEXER	FUNCTION	BITS
MST_SCK_SRC	Master mode SCK source	Page 0, register 0x20, bits[5]
DIVIDER	**FUNCTION**	**BITS**
CLK_DIV_PLL_SCK	Clock divider of PLL to SCKOUT divider (for example, master mode or BCK PLL slave mode with SCK for the rest of the system)	Pg0, reg 0x25, bits[0:6]
CLK_DIV_SCK_BCK	Ratio of master clock (SCK) to bit clock (BCK)	Pg0, reg 0x26, bits[0:6]
CLK_DIV_BCK_LRCK	Ratio of bit clock (BCK) to left-right clock (LRCK)	Pg0, reg 0x27, bits[0:6]

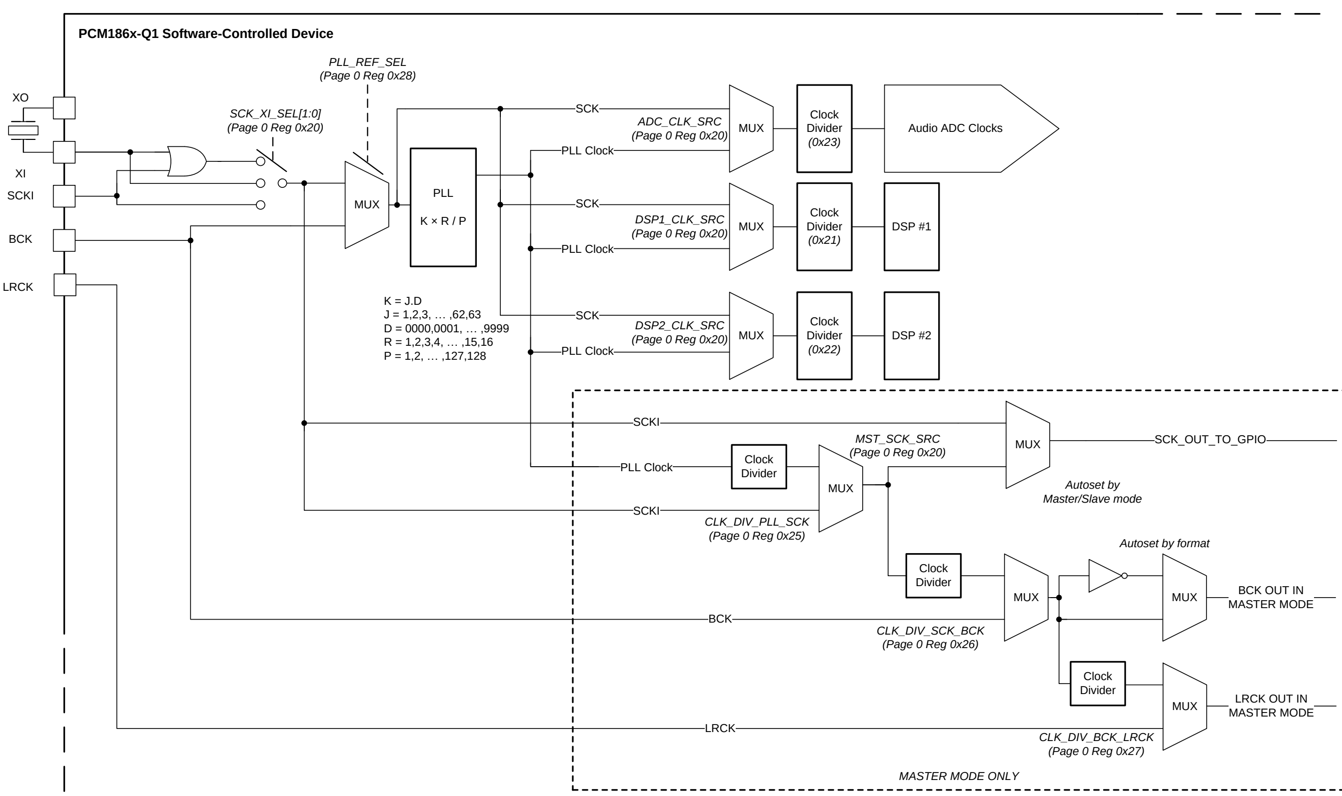


Figure 34. PLL Clock Source and Clock Distribution

9.3.9.4.3 Clocking Configuration and Selection for Software-Controlled Devices

9.3.9.4.3.1 Target Clock Rates for ADC, DSP1 and DSP2

The ADC, DSP1 and DSP2 each have specific minimum clock requirements that can be driven from either the incoming SCK or the output of the PLL, as shown in Table 8.

Table 8. Minimum Required Clock Ratios for ADC, DSP1 and DSP2

CORE	2-CHANNEL DEVICE RATIO	4-CHANNEL DEVICE RATIO
ADC	128x output sampling rate	128x output sampling rate
DSP #1	256x output sampling rate	512x output sampling rate
DSP #2	256x output sampling rate	256x output sampling rate

9.3.9.4.3.2 Configuration of Master Mode

If an external, high-quality MCLK is available (either on the SCK pin or XTAL), then configure the PCM186x-Q1 to run in master mode where possible, with the ADC and serial ports being driven from the MCLK or SCK source. The on-chip DSPs may continue to require clocks from the PLL, as they run from a much higher clock rate.

Clock MUXs and overall configuration can be done in register Page0, 0x20. For the best performance in master mode, the automatic clock configuration circuitry configures the clocks as shown in Table 9 and Table 10, if the device is a PCM186x-Q1 2-channel or 4-channel, software-controlled device. The tables below show data at 48 kHz multiples, the ratios for multiples of 44.1 kHz are identical, while the absolute MHz values will be multiples of 44.1 kHz instead of 48 kHz.

This automatic configuration can be bypassed using registers, starting from CLKDET_EN (Page.0, 0x20).

Table 9. PCM1862-Q1 and PCM1863-Q1 (2-Channel) Clock Divider and Source Control in the Presence of External SCK

f_S	SCK RATIO	SCK FREQ (MHz)	PLL RATIO	PLL FREQ (MHz)	PLL CONFIG	DSP1 CLOCK (MHz)	DSP1 CLOCK		DSP 2 CLOCK (MHz)	DSP2 CLOCK		ADC CLOCK (MHz)	ADC CLOCK	
							SOURCE	DIVIDER		SOURCE	DIVIDER		SOURCE	DIVIDER
8 kHz	128	1.024	12288	98.304	P=1,R=2, J=48, D=0	2.048	PLL	48	2.048	PLL	48	1.024	PLL	96
	256	2.048	12288	98.304	P=1,R=2, J=24, D=0	2.048	SCK	1	2.048	SCK	1	1.024	SCK	2
	384	3.072	12288	98.304	P=1,R=2, J=16, D=0	2.048	SCK	1	2.048	SCK	1	1.024	SCK	3
	512	4.096		Off		2.048	SCK	2	2.048	SCK	2	1.024	SCK	4
	768	6.144		Off		3.072	SCK	2	3.072	SCK	2	1.024	SCK	6
16 kHz	128	2.048	6144	98.304	P=1,R=2, J=24, D=0	4.096	PLL	24	4.096	PLL	24	2.048	PLL	48
	256	4.096	6144	98.304	P=1,R=2, J=12, D=0	4.096	SCK	1	4.096	SCK	1	2.048	SCK	2
	384	6.144	6144	98.304	P=1,R=2, J=8, D=0	6.144	SCK	1	6.144	SCK	1	2.048	SCK	3
	512	8.192		Off		4.096	SCK	2	4.096	SCK	2	2.048	SCK	4
	768	12.288		Off		6.144	SCK	2	6.144	SCK	2	2.048	SCK	6
48 kHz	128	6.144	2048	98.304	P=1,R=2, J=8, D=0	12.288	PLL	8	12.288	PLL	8	6.144	PLL	16
	256	12.288	2048	98.304	P=2,R=2, J=8, D=0	12.288	SCK	1	12.288	SCK	1	6.144	SCK	2
	384	18.432	2048	98.304	P=3,R=2, J=8, D=0	18.432	SCK	1	18.432	SCK	1	6.144	SCK	3
	512	24.576		Off		12.288	SCK	2	12.288	SCK	2	6.144	SCK	4
	768	36.864		Off		18.432	SCK	2	18.432	SCK	2	6.144	SCK	6
96 kHz	128	12.288	1024	98.304	P=4,R=2, J=16, D=0	24.756	PLL	4	24.756	PLL	4	6.144	SCK	2
	256	24.576	1024	98.304	P=8,R=2, J=16, D=0	24.756	SCK	1	24.756	SCK	1	6.144	SCK	4
	384	36.864	1024	98.304	P=12,R=2, J=16, D=0	24.756	SCK	1	24.756	SCK	1	6.144	SCK	6
	512	49.152		Off		24.756	SCK	2	24.756	SCK	2	6.144	SCK	8
192 kHz	128	24.576	512	98.304	P=4,R=2, J=8, D=0	49.152	PLL	2	49.152	PLL	2	6.144	SCK	4
	256	49.152	512	98.304	P=8,R=2, J=8, D=0	49.152	SCK	1	49.152	SCK	1	6.144	SCK	8

Table 10. PCM1864-Q1 and PCM1865-Q1 (4-Channel) Clock Divider and Source Control With External SCK

f_S	SCK RATIO	SCK FREQ (MHz)	PLL RATIO	PLL FREQ (MHz)	PLL CONFIG	DSP1 CLOCK (MHz)	DSP1 CLOCK		DSP 2 CLOCK (MHz)	DSP2 CLOCK		ADC CLOCK (MHz)	ADC CLOCK	
							SOURCE	DIVIDER		SOURCE	DIVIDER		SOURCE	DIVIDER
8 kHz	128	1.024	12288	98.304	P=1,R=2, J=48, D=0	4.096	PLL	24	2.048	PLL	48	1.024	PLL	96
	256	2.048	12288	98.304	P=1,R=2, J=24, D=0	4.096	PLL	24	2.048	SCK	1	1.024	SCK	2
	384	3.072	12288	98.304	P=1,R=2, J=16, D=0	4.096	PLL	24	2.048	SCK	1	1.024	SCK	3
	512	4.096		Off		4.096	SCK	1	2.048	SCK	2	1.024	SCK	4
	768	6.144	6144	98.304	P=1,R=2, J=8, D=0	4.096	PLL	24	3.072	SCK	2	1.024	SCK	6
16 kHz	128	2.048	6144	98.304	P=1,R=2, J=24, D=0	8.192	PLL	12	4.096	PLL	24	2.048	PLL	48
	256	4.096	6144	98.304	P=1,R=2, J=12, D=0	8.192	PLL	12	4.096	SCK	1	2.048	SCK	2
	384	6.144	6144	98.304	P=1,R=2, J=8, D=0	8.192	PLL	12	6.144	SCK	1	2.048	SCK	3
	512	8.192		Off		8.192	SCK	1	4.096	SCK	2	2.048	SCK	4
	768	12.288	2048	98.304	P=4,R=2, J=16, D=0	8.192	PLL	12	6.144	SCK	2	2.048	SCK	6
48 kHz	128	6.144	2048	98.304	P=1,R=2, J=8, D=0	24.576	PLL	4	12.288	PLL	8	6.144	PLL	16
	256	12.288	2048	98.304	P=4,R=2, J=16, D=0	24.576	PLL	4	12.288	SCK	1	6.144	SCK	2
	384	18.432	2048	98.304	P=3,R=2, J=8, D=0	24.576	PLL	4	18.432	SCK	1	6.144	SCK	3
	512	24.576		Off		24.576	SCK	1	12.288	SCK	2	6.144	SCK	4
	768	36.864	2048	98.304	P=3,R=2, J=4, D=0	24.576	PLL	4	18.432	SCK	2	6.144	SCK	6
96 kHz	128	12.288	1024	98.304	P=4,R=2, J=16, D=0	49.152	PLL	2	24.756	PLL	4	6.144	SCK	2
	256	24.576	1024	98.304	P=4,R=2, J=8, D=0	49.152	PLL	2	24.756	SCK	1	6.144	SCK	4
	384	36.864	1024	98.304	P=12,R=2, J=16, D=0	49.152	PLL	2	24.756	SCK	1	6.144	SCK	6
	512	49.152		Off		49.152	SCK	1	24.756	SCK	2	6.144	SCK	8
192 kHz	128	24.576	512	98.304	P=4,R=2, J=8, D=0	98.304	PLL	1	49.152	PLL	2	6.144	SCK	4
	256	49.152	512	98.304	P=8,R=2, J=8, D=0	98.304	PLL	1	49.152	SCK	1	6.144	SCK	8

9.3.9.4.4 BCK Input Slave PLL Mode

The PCM186x-Q1 software-controlled devices can generate an internal MCLK system clock using the PLL (referenced from an external input BCK) in slave mode. Supported sampling frequencies are listed in Table 11. While the PCM186x-Q1 can support down to 8 kHz, analog performance is not tested at this rate.

Table 11. Auto PLL BCK Requirements

SAMPLING FREQUENCY	BCK RATIO TO LRCK	BCK FREQUENCY
8 kHz	256	2.048
16 kHz	64	1.024
	256	4.096
48 kHz	32	1.536
	48	2.304
	64	3.072
	256	12.288
96 kHz	32	3.072
	48	4.608
	64	6.144
	256	24.576
192 kHz	32	6.144
	48	9.216
	64	12.288
	256	49.152

In software SPI or I^2C mode, a PCM186x-Q1 software-controlled device can use the on-chip crystal oscillator, if a CMOS clock source is not available. Audio clocks can be generated through the PLL from the non-audio standard CMOS or crystal frequency (and then can be divided down as described previously). This function is not available in hardware mode.

The 8-kHz sampling rate is only supported if an external MCK is provided. The autodetect and PLL system support frequencies as low as 32 kHz. Analog performance is not tested in this mode.

The clock tree can also be programmed manually, with the settings shown in Table 12 and Table 13.

Table 12. PCM1862-Q1 and PCM1863-Q1 (2-Channel) PLL BCK Settings

f_S	BCK RATIO	BCK FREQ (MHz)	PLL RATIO	PLL FREQ (MHz)	PLL CONFIG	DSP1 CLOCK (MHz) 2-CHANNEL	DSP1 CLOCK DIVIDER 2-CHANNEL MODE		DSP2 CLOCK (MHz)	DSP2 CLOCK DIVIDER		ADC CLOCK (MHz)	ADC CLOCK DIVIDER	
							SOURCE	DIVIDER		SOURCE	DIVIDER		SOURCE	DIVIDER
8 kHz	256	2.048	12288	98.304	P=1,R=2, J=24, D=0	2.048	PLL	48	2.048	PLL	48	1.024	PLL	96
16 kHz	64	1.024	6144	98.304	P=1,R=2, J=48, D=0	4.096	PLL	24	4.096	PLL	24	2.048	PLL	48
	256	4.096	6144	98.304	P=2,R=2, J=24, D=0	4.096	PLL	24	4.096	PLL	24	2.048	PLL	48
48 kHz	32	1.536	2048	98.304	P=1,R=2, J=32, D=0	12.288	PLL	8	12.288	PLL	8	6.144	PLL	16
	48	2.304	2048	92.16	P=1,R=2, J=20, D=0	15.36	PLL	6	15.36	PLL	6	6.144	PLL	15
	64	3.072	2048	98.304	P=1,R=2, J=16, D=0	12.288	PLL	8	12.288	PLL	8	6.144	PLL	16
	256	12.288	2048	98.304	P=4,R=2, J=16, D=0	12.288	PLL	8	12.288	PLL	8	6.144	PLL	16
96 kHz	32	3.072	1024	98.304	P=1,R=2, J=16, D=0	24.576	PLL	4	24.576	PLL	4	6.144	PLL	16
	48	4.608	1024	98.304	P=3,R=2, J=32, D=0	24.576	PLL	4	24.576	PLL	4	6.144	PLL	16
	64	6.144	1024	98.304	P=2,R=2, J=16, D=0	24.576	PLL	4	24.576	PLL	4	6.144	PLL	16
	256	24.576	1024	98.304	P=8,R=2, J=16, D=0	24.576	PLL	4	24.576	PLL	4	6.144	PLL	16
192 kHz	32	6.144	512	98.304	P=2,R=2, J=16, D=0	49.152	PLL	2	49.152	PLL	2	6.144	PLL	16
	48	9.216	512	98.304	P=3,R=2, J=16, D=0	49.152	PLL	2	49.152	PLL	2	6.144	PLL	16
	64	12.288	512	98.304	P=4,R=2, J=16, D=0	49.152	PLL	2	49.152	PLL	2	6.144	PLL	16
	256	49.152	512	98.304	P=16,R=2, J=16, D=0	49.152	PLL	2	49.152	PLL	2	6.144	PLL	16

Table 13. PCM1864-Q1 and PCM1865-Q1 (4-Channel) PLL BCK Settings

f_S	BCK RATIO	BCK FREQ (MHz)	PLL RATIO	PLL FREQ (MHz)	PLL CONFIG	DSP1 CLOCK (MHz) 4-CHANNEL	DSP1 CLOCK DIVIDER 4-CHANNEL MODE		DSP2 CLOCK (MHz)	DSP2 CLOCK DIVIDER		ADC CLOCK (MHz)	ADC CLOCK DIVIDER	
							SOURCE	DIVIDER		SOURCE	DIVIDER		SOURCE	DIVIDER
8 kHz	256	2.048	12288	98.304	P=1,R=2, J=24, D=0	4.096	PLL	24	2.048	PLL	48	1.024	PLL	96
16 kHz	64	1.024	6144	98.304	P=1,R=2, J=48, D=0	8.192	PLL	12	4.096	PLL	24	2.048	PLL	48
	256	4.096	6144	98.304	P=2,R=2, J=24, D=0	8.192	PLL	12	4.096	PLL	24	2.048	PLL	48
48 kHz	32	1.536	2048	98.304	P=1,R=2, J=32, D=0	24.576	PLL	4	12.288	PLL	8	6.144	PLL	16
	48	2.304	2048	92.16	P=1,R=2, J=20, D=0	30.72	PLL	3	15.36	PLL	6	6.144	PLL	15
	64	3.072	2048	98.304	P=1,R=2, J=16, D=0	24.576	PLL	4	12.288	PLL	8	6.144	PLL	16
	256	12.288	2048	98.304	P=4,R=2, J=16, D=0	24.576	PLL	4	12.288	PLL	8	6.144	PLL	16
96 kHz	32	3.072	1024	98.304	P=1,R=2, J=16, D=0	49.152	PLL	2	24.576	PLL	4	6.144	PLL	16
	48	4.608	1024	98.304	P=3,R=2, J=32, D=0	49.152	PLL	2	24.576	PLL	4	6.144	PLL	16
	64	6.144	1024	98.304	P=2,R=2, J=16, D=0	49.152	PLL	2	24.576	PLL	4	6.144	PLL	16
	256	24.576	1024	98.304	P=8,R=2, J=16, D=0	49.152	PLL	2	24.576	PLL	4	6.144	PLL	16
192 kHz	32	6.144	512	98.304	P=2,R=2, J=16, D=0	98.304	PLL	1	49.152	PLL	2	6.144	PLL	16
	48	9.216	512	98.304	P=3,R=2, J=16, D=0	98.304	PLL	1	49.152	PLL	2	6.144	PLL	16
	64	12.288	512	98.304	P=4,R=2, J=16, D=0	98.304	PLL	1	49.152	PLL	2	6.144	PLL	16
	256	49.152	512	98.304	P=16,R=2, J=16, D=0	98.304	PLL	1	49.152	PLL	2	6.144	PLL	16

9.3.9.4.5 Software-Controlled Devices ADC Non-Audio MCK PLL Mode

This mode is mainly used for systems driving TDM ports or systems where the MCK is not related to the audio sampling rate. For example, where the audio ADC must share a clock source with the central processor (commonly, 12 MHz, 24 MHz, or 27 MHz.)

Under these conditions, set automatic configuration register CLKDET_EN (Page 0, 0x20) to 0, and manually configure the PLL using registers (Page 0, 0x28 - 0x2D); see *Software-Controlled Devices Manual PLL Calculation*. The clock tree must also be set to use the PLL output as the master mode SCKOUT source, and have the appropriate SCK-to-BCK and BCK-to-LRCK dividers set.

9.3.9.5 Software-Controlled Devices Manual PLL Calculation

The PCM186x-Q1 has an on-chip PLL with fractional multiplication to generate the clock frequency required by the audio ADC, modulator and digital signal processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input supports clocks varying from 1 MHz to 50 MHz, and is register programmable to enable generation of required sampling rates with fine precision.

The PLL by default is enabled because the on-chip fixed function DSPs require high clock rates to complete all various decimation, mixing, and level-detection functions. The PLL output clock PLLCK is given by Equation 1:

$$\mathrm{PLLCK} = \frac{\mathrm{PLLCKIN} \times \mathrm{R} \times \mathrm{JD}}{\mathrm{P}} \quad \text{or} \quad \mathrm{PLLCK} = \frac{\mathrm{PLLCKIN} \times \mathrm{R} \times \mathrm{K}}{\mathrm{P}}$$

where

- R = 1, 2, 3, 4, ….. 15, 16
- J = 1, 2, 3, 4,...63, and D = 0000, 0001, 0002...9999
- K = J.D
- P = 1, 2, 3...15 (1)

R, J, D, and P are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000 (that is, an integer multiple), the following conditions must be satisfied:

1 MHz ≤ (PLLCKIN / P) ≤ 20 MHz
64 MHz < (PLLCKIN × K × R / P) < 100 MHz
1 ≤ J ≤ 63

When the PLL is enabled and D ≠ 0000 (that is, a noninteger multiple), the following conditions must be satisfied:

6.667 MHz ≤ (PLLCLKIN / P) ≤ 20 MHz
64 MHz < (PLLCKIN x K x R / P) < 100 MHz
4 ≤ J ≤ 11
R = 1

When the PLL is enabled,

$f_S$ref = (PLLCLKIN × K × R) / (N × P) :
N is selected so that $f_S$ref × N = PLLCLKIN × K × R / P is in the allowable range.

Example:

MCLK = 12 MHz and $f_S$ref = 44.1 kHz, (N=2048)
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

MCLK = 12 MHz and $f_S$ref = 48.0 kHz, (N=2048)
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

The PLL can be programmed using page 0, registers 0x28 thru 0x2D. Turn on the PLL using page 0, register 0x28, D(0). The variable P can be programmed using page 0, register 0x29, D(3:0). The variable R can be programmed using page 0, register 0x2A, D(3:0). The variable J can be programmed using page 0, register 0x2B, D(5:0). The variable D is 14-bits and is programmed into two registers. The MSB portion is programmed using page 0, register 0x2D, D(5:0), and the LSB portion is programmed using page 0, register 0x2C, D(7:0). The variable D is set when the LSB portion is programmed.

Values are programmed in the registers in Table 14.

Table 14. PLL Coefficient Registers

REGISTER	FUNCTION	BITS
PLL_EN	PLL enable, lock status and PLL reference	Page 0, register 0x28
PLL_P	PLL P	Page 0, register 0x29
PLL_J	PLL J	Page 0, register 0x2B
PLL_Dx	PLL D	Page 0, register 0x2C (least significant bits)
		Page 0, register 0x2D (most significant bits)
PLL_R	PLL R	Page 0, register 0x2A

9.3.9.6 Clock Halt and Error

The status of the halt and error detector can be read from register CLK_ERR_STAT (Page.0, 0x75).

9.3.9.7 Clock Halt and Error Detect

The PCM186x-Q1 has a clock error detection block inside that continues to monitor the ratio of BCK to LRCK.

If a clock error is detected (such as an unexpected number of BCKs per LRCK), then the device goes into standby mode.

If all the clocks are stopped going into the device, then the device shifts into sleep state, and begins *Energysense* signal detect mode.

When a clock error occurs, the PCM186x-Q1 starts the following sequence:

1. Mute audio output immediately (without volume ramp down)
2. Wait until proper clock is supplied (known as *Clock Waiting State*)
3. Restart clock detection. The PLL and all clock dividers are reconfigured with the result of the detection.
4. Start fade-in

If the device stops transmitting data, the first step is to read CLK_ERR_STAT (Page.0 0x72). The least significant nibble shows the device status. Value 0x01 suggests *Clock Waiting State*, at which point the clock error status can be read in register STATE (Page.0 0x75). The clock detection logic is shown in Table 15.

Table 15. Summary of Clock Detection Logic

SCK	BCK	LRCK	RESULT	ACTION
ACTIVE	ACTIVE	ACTIVE	No error	Normal operation
ACTIVE	ACTIVE	HALT	Clock error	Enter clock waiting state
ACTIVE	HALT	ACTIVE	Clock error	Enter clock waiting state
ACTIVE	HALT	HALT	Clock error	Enter SLEEP
HALT	ACTIVE	ACTIVE	No error	Enter BCK PLL mode
HALT	ACTIVE	HALT	Clock error	Enter clock waiting state
HALT	HALT	ACTIVE	Clock error	Enter clock waiting state
HALT	HALT	HALT	Clock error	Enter SLEEP

In addition, the device uses an on-chip oscillator to detect errors in the rate of present clocks. That logic is shown in Table 16.

Table 16. Summary of Clock Error Logic

SCK/LRCK Ratio	BCK/LRCK RATIO	LRCK	ERROR DETECT	ACTION
-	-	< 8 kHz or > 192 kHz	f_S error	Enter clock waiting state
Not 128 / 256 / 384 / 512 / 768	-	8 / 16 / 32 / 44.1 / 48 kHz	SCK error	Enter the clock waiting state, tie I^2S output to 0
Not 128 / 256 / 384 / 512	-	88.2 / 96 kHz	SCK error	Enter the clock waiting state, tie I^2S output to 0
Not 128 / 256	-	176.4 / 192 kHz	SCK error	Enter the clock waiting state, tie I^2S output to 0
	Not 256 / 64 / 48 / 32	8 / 16 / 32 / 44.1 / 48 / 88.2 / 96 / 174.6 / 196 kHz	BCK error	Enter the clock waiting state, tie I^2S output to 0
		>192 kHz	f_S error	Enter the clock waiting state, tie I^2S output to 0

In an application with a non-audio standard SCK coming into the product, the clock error detection on the SCK pin can be ignored by disabling the auto clock detector (CLKDET_EN Page.0 0x20).

9.3.9.8 Changes in Clock Sources and Sample Rates

In slave mode, when changing clock sources, the PCM186x-Q1 requires at least three BCK clocks of no clock or data for the device to reconfigure after clocks resume (if the device is in auto clock config mode).

For example, auto clock config mode: StateA = 48 kHz, change to StateB = 44.1 kHz

For changing from state A to State B:
- Leaving State A
- Hold clocks (or HiZ from external) for 3 BCK minimum
- Change clocks
- Allow ~100 µs (at least 3 BLKs at 48 kHz) for the device to reconfigure
- Data ramp back in on zero-crossing ramp (if zero crossing has not been disabled in software mode)
- Transition to State B complete

In master mode, simply switching the I/O pins on the hardware-controlled devices, or changing the sampling rate register should change the sampling rate.

NOTE

Hardware-controlled devices cannot switch from XTAL master mode to external slave mode because the XTAL continues clocking the internal SCLK and not be in sync to the new external clocks. However, this switch can be done in software mode.

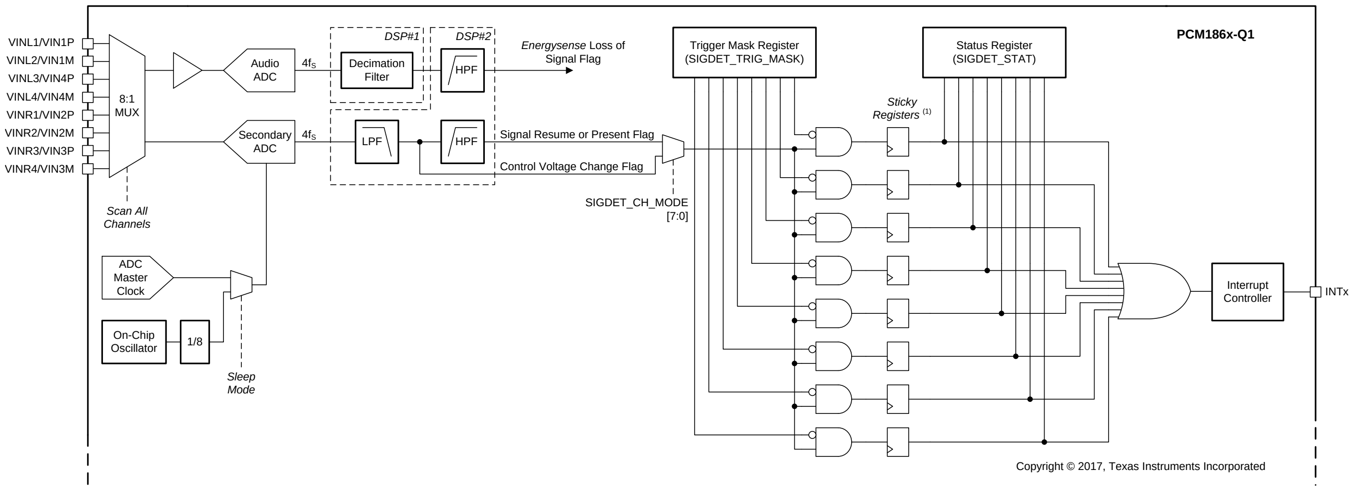
9.3.10 Analog-to-Digital Converters (ADCs)

9.3.10.1 Main Audio ADCs

The SNR of the primary ADCs in the PCM186x-Q1 are 103 dB (for PCM1860-Q1, PCM1862-Q1, PCM1864-Q1), or 110 dB (for PCM1861-Q1, PCM1863-Q1, PCM1865-Q1), with 40-kHz bandwidth that is tightly coupled to dedicated PGAs and input multiplexers. Often in this document, references are made to ADC1L and ADC1R (or CH1_L and CH1_R), the main left and right ADCs present in the PCM1862-Q1, PCM1863-Q1, PCM1864-Q1 and PCM1865-Q1. References to ADC2L and ADC2R are the other pair of left and right ADCs present only in the PCM1864-Q1 and PCM1865-Q1.

9.3.10.2 Secondary ADC: Energysense and Analog Control

The PCM186x-Q1 has a secondary ADC, shown in Figure 35, that is used for signal level detection or dc level change detection.



(1) Reset ports not shown.

Figure 35. Secondary ADC Architecture

The secondary ADC has two main purposes in the PCM186x-Q1 family. The primary purpose is to act as a low power signal detection system, to aid with system wakeup from sleep. TI calls this functionality *energysense*. Other functionality includes the ability to use any spare analog inputs as generic ADC inputs, for connection to simple analog sources, such as voltages from control potentiometers. TI calls this functionality *controlsense* or dc control.

The secondary ADC is a one-bit, delta-sigma type ADC. The sampling rate is directly connected to the main ADC audio sampling clocks during ACTIVE functionality. When the device is in sleep state, then the secondary ADC switches the clock source to an on-chip oscillator (if there are no other clock sources).

In sleep mode, the inputs are all treated as single-ended inputs. Differential inputs are not supported in this mode because the PGA must be powered up, and thus, consume more power.

In active mode, *energysense* audio signal detection on any channels other than the primary is not available; however, other inputs can be read using the secondary ADC channel driven in *controlsense* mode.

In sleep mode, each input pin can be configured to perform either *energysense* or *controlsense*. Both functions can generate interrupts when their thresholds are crossed. All inputs will be cycled through and converted continuously, performing either an *enerysense* or a *controlsense* function.

In active mode, any dc based controls will either need to be polled continuously by the systems host, or streamed out continuously in a 6ch TDM mode. In an application, this may mean that the main input is being converted, while the system battery level, or analog volume control knob position is polled using *controlsense*.

To make the secondary ADC as flexible as possible in both *energysense* and *controlsense* modes, the following controls and coefficients are available in the register map. More details on each are in the relevant following sections.

- Coefficients for the secondary ADC low-pass filter
- Coefficients for the secondary ADC high-pass filter
- Reference voltage and interrupt voltage delta for each input in *controlsense* mode
- Signal loss conditions (time and threshold)
- Signal resume conditions (threshold)
- Interrupt behavior (for example, ping every *x* ms if host does not clear)
- Scan time for each single ended input

9.3.10.2.1 Secondary ADC Analog Input Range

To match the dynamic range of the secondary ADC to an incoming line level signal, an overall attenuation is applied to the incoming signal. This attenuation is also present in *controlsense* mode. The impact of this is that the secondary ADC in *controlsense* mode can only detect control signals up to 4.3 V. Exact values will vary a small amount from device to device along with the gain error.

Input impedance of the secondary ADC is designed to be 20 kΩ.

9.3.10.2.2 Frequency Response of the Secondary ADC

The natural response of the secondary ADC is not flat by frequency. However, the frequency response can be flattened, so that all frequencies are equally sensitive to the *energysense* detector by modifying the LPF or HPF biquads in the DSP.

9.3.10.3 Secondary ADC Controlsense DC Level Change Detection

This function is used for external analog controls, such as potentiometers to set volume, tone control, or a sensor. The data for control sense has no high pass filter applied to it, even if the main audio path does have a HPF enabled.

AS shown in Figure 36, there are two parameters for the dc level change detection: reference level (REF_LEVEL) and difference level (DIFF_LEVEL). Each input pin (input 1 through 8) has a different reference and difference level.

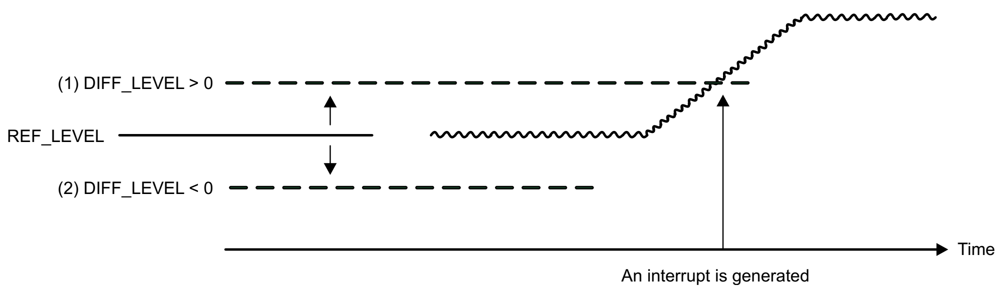


Figure 36. DC Detection Function

Users set a reference point, and a difference point. If the voltage at the control point crosses the difference point then an interrupt is driven from the device. This is useful for filtering out noise, as well as reducing the load on the host processor for controls that tend to be *set and forget* (such as volume).

The data from the secondary ADC can also be streamed out of the device in TDM form and directly from the I^2C register map. AUXADC_DATA_CTRL (Page.0 0x58) is used to configure and check the status of the DC detector.

This feature (thresholds and interrupts) is available in both active and sleep modes. In sleep mode, the device automatically scans through each channel designated a *controlsense* input. In active mode, the scanning will need to be done manually by a host microcontroller by modifying the SEC_ADC_INPUT_SEL (Page.0, 0x0A) register.

Most applications requiring the use of a potentiometer for control can simply use the SIGDET_DC_LEVEL_CHx_x registers to read the 8-bit value. To enable the SIGDET_DC_LEVEL_CHx_x registers to work, then the DC_NOLATCH AUXADC_DATA_CTRL (Page.0, 0x58, B[7]) should be set to 1, and the appropriate input pins should be set to *controlsense* inputs SIGDET_CH_MODE (Page.0, 0x30)

Direct 16-bit two's compliment reads from the secondary ADC can be done using AUXADC_DATA_CTRL (Page.0, 0x58) includes a latch function that is used to read the data the secondary ADC on demand in 16-bit two's compliment format from registers 0x59 and 0x5A.

9.3.11 *Energysense*

Energysense functionality has been added to the PCM186x-Q1 to aid with auto-sleep and auto-wakeup for end equipment systems that are expected to be sold within the European Union. The latest Ecodesign legislation in Europe has demanded that products consume less than 500 mW in standby. Most off-the-shelf external power adaptors can consume 300 mW when idling, leaving the system with only 200 mW available. In many systems that require that almost everything be powered down in sleep mode after there is no more content to be played, and then to be powered back up when signal enters the system again.

Energysense is designed to work in collaboration with a microcontroller to trigger interrupts notifying the microcontroller to change the state of the PCM186x-Q1, and the rest of the board (for example, amplifiers, and so on). The PCM186x-Q1 does not automatically switch between sleep and wake modes.

Energysense is split into two functions: signal loss flag and signal resume flag. Both are available on the PCM186x-Q1 software-controlled devices. The PCM1860-Q1 and PCM1861-Q1 only support signal resume, as shown in Table 17. By default, the signal resume threshold is set at –57 dBFS. Signal resume (autowakeup) only functions when the device has been set to sleep.

Table 17. *Energysense* States

MODE	PURPOSE	CONDITIONS	POSITIVE OUTCOME	WORST CASE
SLEEP (Signal Detect Mode)	Detect Input Signal and Wake up from SLEEP	BCK and LRCK stopped (not locked) or register Set. Trigger Interrupt when input crosses above (threshold) Trigger for 1ms every X seconds until clocks start (x=1 by default)	Host Wakes and services interrupt (reads register) Host Starts BCK/LRCK. (Moving system to ACTIVE mode) or writes to register.	Host Doesn't respond or start clocks. PCM186x-Q1 keeps triggering interrupts until host responds.
ACTIVE (Signal Loss Mode)	Detect content below (threshold) over time Assist system to sleep after audio inactivity (for example, Source is off, but speaker still on)	BCK and LRCK are currently running If no content above -(threshold) dB for Y minutes, drive interrupt.	System can choose to go to sleep or not. If not, reset interrupt If System decides to sleep, stop BCK/LRCK. This will move PCM186x-Q1 to SLEEP mode.	If system does not sleep, remain in Mode 2, and prompt every Y. MCU will need to mask that interrupt.

9.3.11.1 *Energysense Signal Loss Flag*

The main ADC constantly monitors the input signal level while in ACTIVE mode. Should the input level remain below a register defined threshold (for example –60 dB - Virtual Coefficient 0x2C, programmable through Page 1.) for a register defined amount of time (for example 1 minute - set by SIGDET_LOSS_TIME (Page.0, 0x33)), an interrupt can be generated.

If the system MCU decides to move to sleep mode, the PCM186x-Q1 can be moved to SLEEP by stopping BCK/LRCK or using PWRDN_CTRL (Page.0, 0x70); see Table 17 for details.

If BCK and LRCK are stopped by the host after the interrupt, the device goes to the sleep state as shown in Figure 37. Otherwise, the interrupt continues for a few seconds, defined by SIGDET_INT_INTVL (Page.0, 0x36) unless the interrupt and timeout counter is reset.

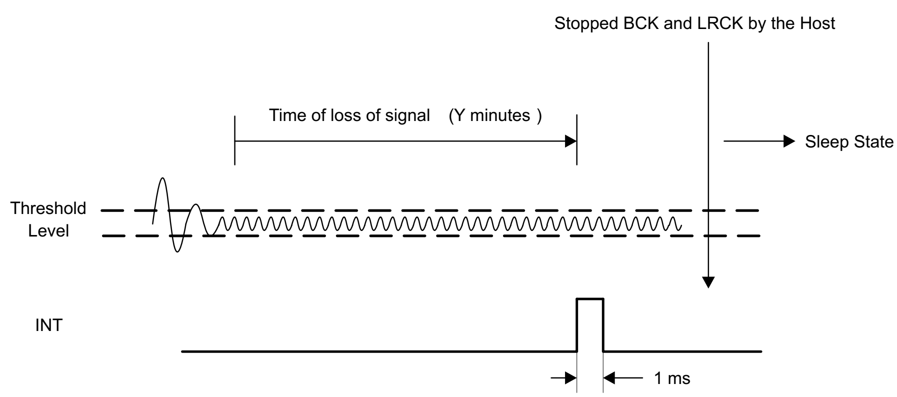


Figure 37. *Energysense* Signal Loss

In a typical application, the host MCU will note and reset this register multiple times until a system sleep number is hit. For example, a 5-minute signal loss could be implemented by using the default 1-minute timeout on the PCM186x-Q1, and counting five interrupts. An example is shown in Figure 38.

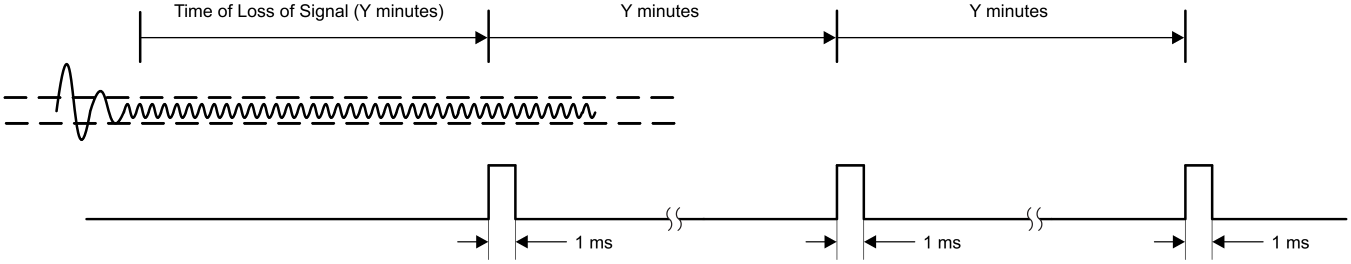


Figure 38. Interrupt Behavior for Signal Loss

Alternatively, the **SIGDET_LOSS_TIME (Page.0, 0x33)** register in the device can be changed from one minute (default) to five minutes. This timeout is sample rate dependant. The expected sample rate is 48 kHz, but should the system be running at 96 kHz, then the time will be halved. (192 kHz = quarter the register setting).

The duration of the interrupt can also be modified using INT_PLS (Page.0 0x62) to be pulses, or to be a *sticky* flag, where sticky is defined as the interrupt is on until cleared.

9.3.11.2 Energysense Signal Detect Circuitry

In sleep mode (BCK and LRCK stop, or by register), the PCM186x-Q1 monitors the signal level or dc level change using the secondary ADC. All eight channels are converted one after the other in a circular manner. The scan time is specified with register SIGDET_SCAN_TIME. All eight channels are measured, even if some have the respective interrupt outputs muted. Accuracy and frequency response are a function of scan time. A long scan time allows detection of lower frequency content. The energysense signal wakeup logic is shown Figure 39.

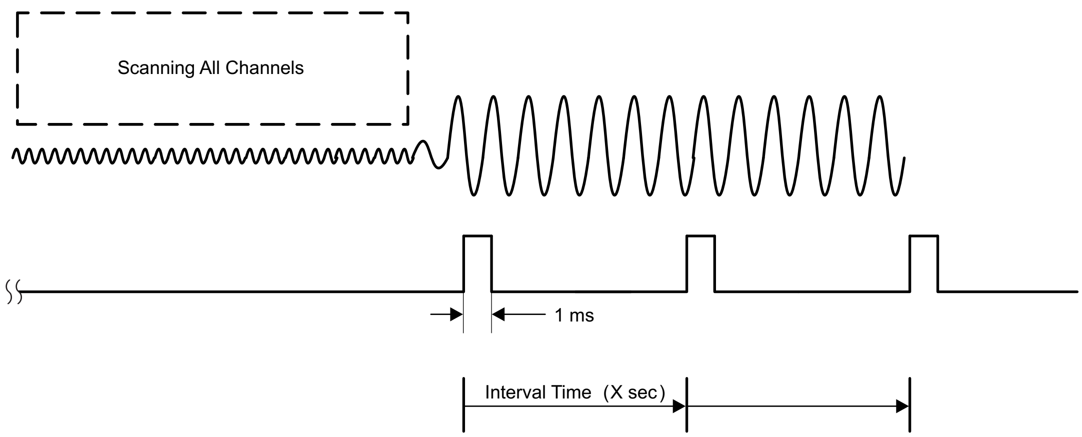


Figure 39. *Energysense* Signal Wakeup Logic

There is a balance between lowest frequency detectable, and time on that particular channel. There are three options in register SIGDET_INT_INTVL (Page.0 0x36):

- 50-Hz detect (160 ms per channel)
- 100-Hz detect (80 ms per channel)
- 200-Hz detect (40 ms per channel)

9.3.11.2.1 Energysense Threshold Levels for Both Signal Loss and Signal Detect

There are two threshold levels used for *Energysense*, as shown in Figure 40. One is the loss of signal level, another one is the resume of signal level.

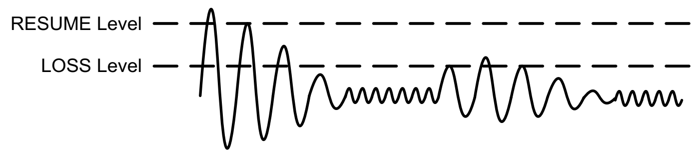


Figure 40. Dual Thresholds for *Energysense*

As both thresholds are DSP based, their coefficients are stored in virtual coefficient space that is programmed through the device register map.

For example, to change the resume threshold value to –30 dB (0x040C37):

Write 0x00 0x01 ; # change to register page 1

Write 0x02 0x2D ; # write the memory address of resume threshold

Write 0x04 0x04 ; # bit[23:15]

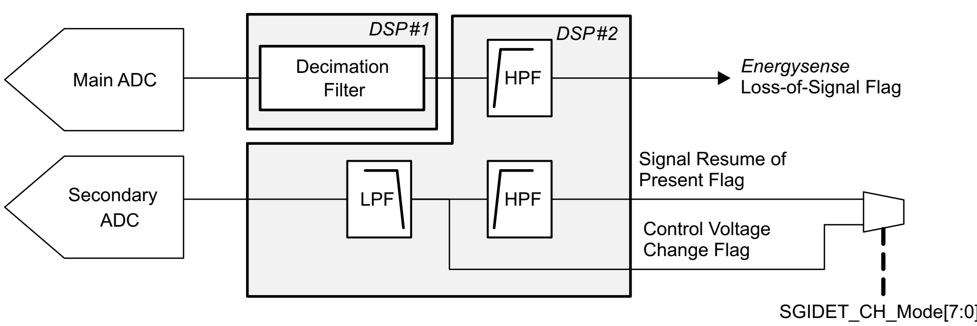
Write 0x05 0x0C ; # bit[15:8]

Write 0x06 0x37 ; # bit[7:0]

Write 0x01 0x01 ; # execute write operation

9.3.11.3 Programming Various Coefficients for Energysense

Programming the DSP coefficients for the *energysense* secondary ADC is done through the indirect virtual programming registers in Page1. The low-pass filter (LPF) and high-pass filter (HPF) coefficients can be written to flatten out the frequency response, as well as the *energysense* loss and resume thresholds. Visually, one can imagine the DSP flow as shown in Figure 41.



Copyright © 2016, Texas Instruments Incorporated

Figure 41. *Energysense* Process Flow

To flatten out the response of the secondary ADC, so that all frequencies are detected evenly, write the biquads shown in Table 18 to the virtual DSP memory, using the techniques discussed in the *Programming DSP Coefficients on Software-Controlled Devices* section.

Table 18. Secondary ADC Biquad Coefficients at 48-kHz Sampling

COEFFICIENT	VIRTUAL RAM ADDRESS
LPF_B0	0x20
LPF_B1	0x21
LPF_B2	0x22
LPF_A1	0x23
LPF_A2	0x24
HPF_B0	0x25
HPF_B1	0x26
HPF_B2	0x27
HPF_A1	0x28
HPF_A2	0x29

9.3.12 Audio Processing

Both DSP1 and DSP2 are fixed function processors that are not custom-programmable. They are used in this device to perform multiple filtering, mixing functions, signal detection and housekeeping functions. Programming the DSP coefficients is done indirectly using registers on Page1. The data and target DSP memory address are stored in registers, and once the DSPs are ready for the data (that is done by request) the data is then latched into the DSP memory.

This indirect method of programming the DSP allows multiple registers to be written, without consuming valuable register map space. More details can be found in the *Programming DSP Coefficients on Software-Controlled Devices* section.

9.3.12.1 DSP1 Processing Features

9.3.12.1.1 Digital Decimation Filters

The main audio path uses a selectable decimation filter used to convert the high-data-rate modulator to I^2S rates. A choice between a classic FIR response and a low-latency IIR response is available. A high-pass filter, separate from that used for the secondary ADC, is also available to remove any dc bias that may be present in the signal. This feature is enabled by default.

Details can be found in the DSP_CTRL register (Page.0, 0x71).

9.3.12.1.2 Digital PGA

As discussed in the *Programmable Gain Amplifier* section, the digital PGA gain can be controlled by the auto gain mapping function, that will use the analog gain settings in register PGA_VAL_CH1_L (Page.0 0x01) and related registers to achieve the target gain with a combination of digital and analog gain. However, digital gain can be also controlled directly by disabling the auto gain mapping function using register PGA_CONTROL_MAPPING (Page.0 0x19). Manual update of digital PGA is only available in 4-channel devices because the digital PGA gain is fixed to 0 dB when manual gain mapping is enabled.

9.3.12.2 DSP2 Processing Features

9.3.12.2.1 Digital Mixing Function

This function allows post ADC mixing, as well as ADC + incoming I^2S mix. Volume control functionality can be performed prior to outputting the signal to an I^2S DAC or Amplifier.

Gain range is from –120 dB to +18 dB (4.20 format). Phase Inversion can be done by performing the two's compliment of the positive gain coefficient. two's compliment can be performed by inverting all bits in the binary coefficient, and adding 1 to the LSB.

As the DSP coefficients are directly written, no soft ramping is available. Use of I^{2}S receive sacrifices two digital mic channels due to pin limitations.

Coefficients are written indirectly to virtual memory addresses using the registers on page 1. Details of the registers are shown in the *Register Map* section.

A diagram of the digital mixing functionality is shown in Figure 42.

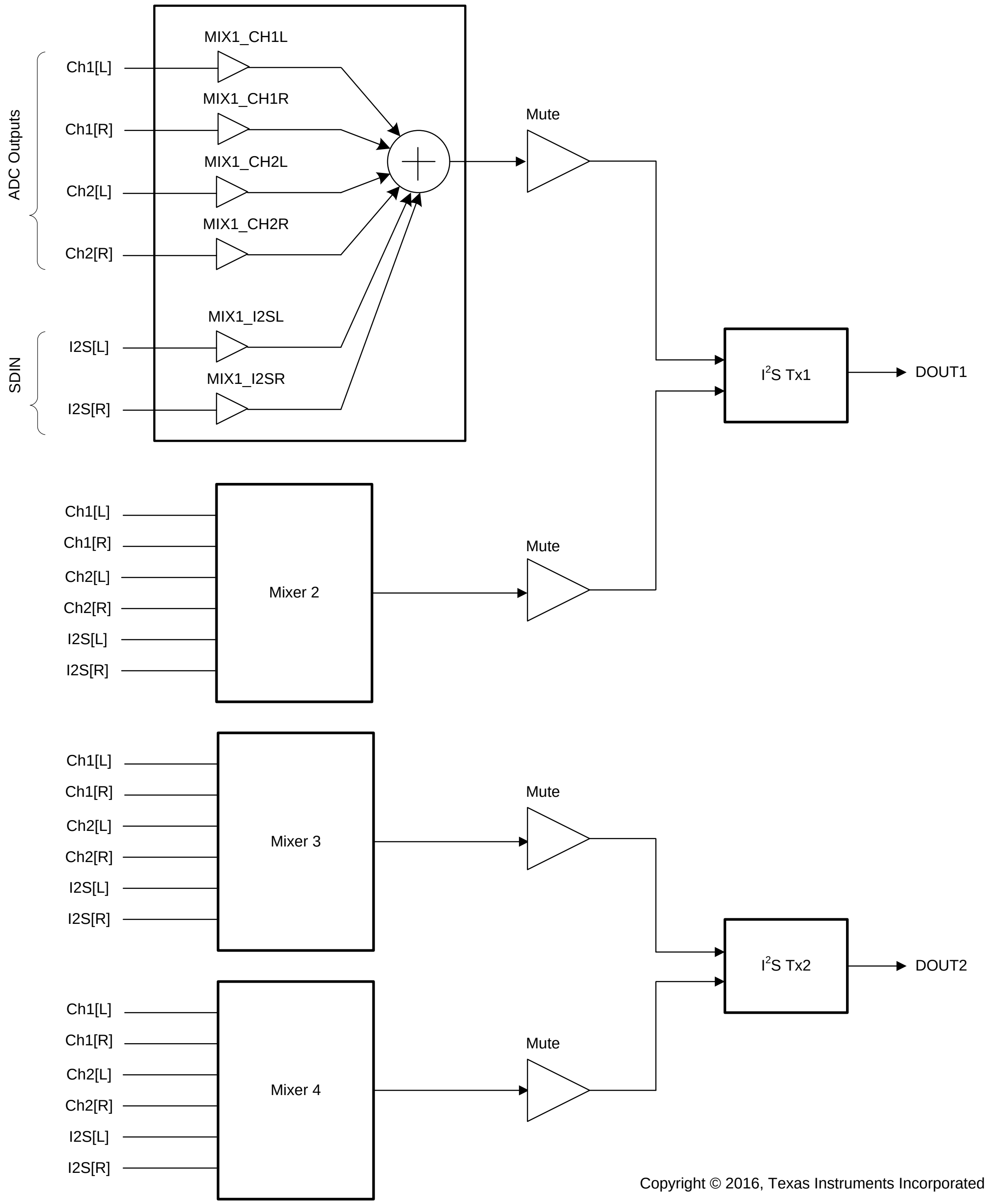


Figure 42. Digital Mixer Functionality

9.3.13 Fade-In and Fade-Out Functions

The PCM186x-Q1 has fade-in and fade-out functions on DOUT to avoid pop noise. This function is engaged on device power up or down, and mute or unmute. The level changes from 0 dB to mute, or mute to 0 dB, are performed using pseudo S-shaped characteristics calculation with zero-cross detection. Because of the zero-cross detection, the time needed for the fade-in and fade-out depends upon the analog input frequency (f_{IN}). Fade takes 48 / f_{IN} until processing is completed. If there is no zero cross during 8192 / f_S, DOUT is faded in or out by force during 48 /f_S (TIME OUT). Figure 43 illustrates the fade-in and fade-out operation processing.

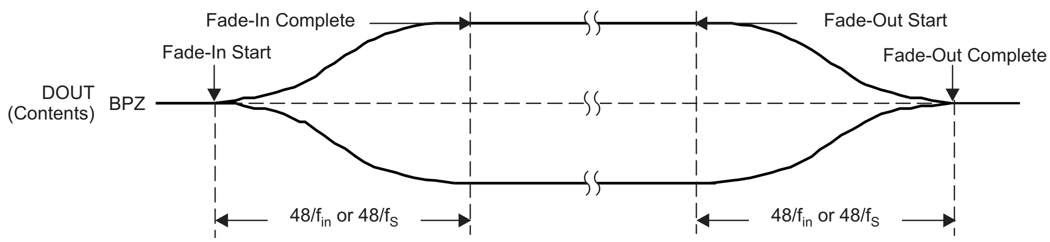


Figure 43. Fade-In and Fade-Out Operations

9.3.14 Mappable GPIO Pins

All the GPIO pins on thePCM186x-Q1 software-controlled devices can be configured for various functions. They can each have their polarity inverted to make control of following circuits easier. See the control registers for each GPIO for a better explanation of mapping. (such as GPIO1_FUNC at Page.0 0x10)

The type of function can also be controlled, including such behavior as regular inputs, inputs with toggle detection, or sticky bits. The device can also be configured as an open drain output, so that multiple interrupt outputs from different devices in the system can be connected together.

9.3.15 Interrupt Controller

The hardware-controlled PCM1860-Q1 and PCM1861-Q1 has the *energysense* signal detect as the default output on the INT pin. There are no other interrupt sources. The INT pin on the PCM1860-Q1 and PCM1861-Q1 is also used to put the device into power-down mode. Figure 44 shows the interrupt logic

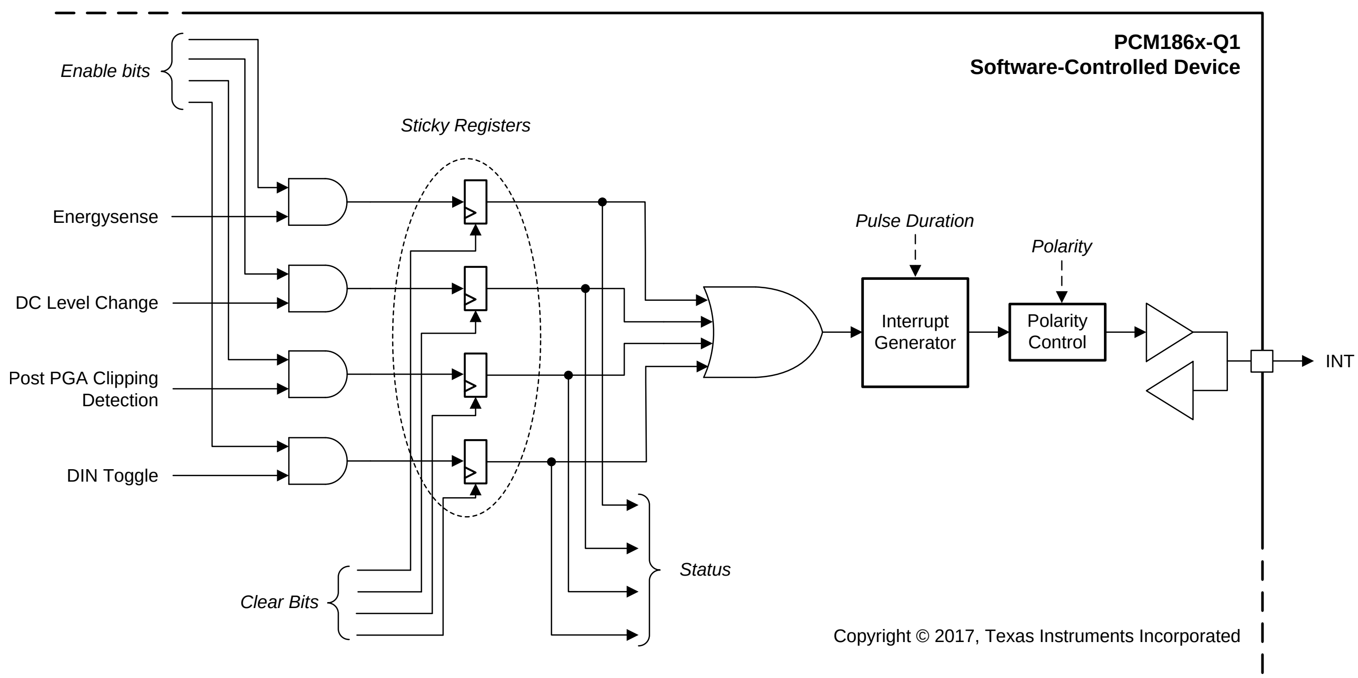


Figure 44. Interrupt Logic

The software-controlled devices have multiple signals that can be mapped to the interrupt outputs. These include:

- *Energysense* (default)
- Secondary ADC *controlsense* interrupt
- Post PGA clip
- DIN toggle

The Interrupt controller has the following features

- The Interrupt sources can be filtered by the enable register (INT_EN).
- The Interrupt flags can be monitored by reading the status register (INT_STAT).
- The interrupt flags can be cleared by writing the status register.
- The polarity of the interrupt signal can be changed between active high, active low and Open Collector (High Impedance is pulled to GND) (INT_PLS).
- The pulse width of the interrupt signal can be changed between 1ms, 2ms, 3ms and 4ms.
- The interrupt controlled cannot remain asserted, the status bits can be sticky, but the interrupt pin itself has no hold function.

Using a combination of these features, as well as the interrupt sources, allows the PCM186x-Q1 to alert a host microcontroller of an event, using whichever polarity signal required (pull high, pull low, Hi-Z open collector). The host controller can then communicate with the device to poll the interrupt flag register to find out what happened. Additional registers can then be read for more details. (For instance, which input triggered an *energysense* event.). From a register point of view, there is no difference between INT A, INT B and INT C logic, other than their signaling (positive, negative or open drain).

9.3.15.1 DIN Toggle Detection

DIN toggle can be used to trigger from an external PCM audio data source or any other digital data source (such as a IR remote control UART stream) where there is a toggling logic state. (from 0 V to 3.3 V, or vice versa). All GPIO pins support DIN toggle detection, other than GPIO2.

This function is only enabled in sleep mode.

9.3.15.2 Clearing Interrupts

Each Interrupt type has a specific method to clear. When clearing or resetting an interrupt, always remove the source of the interrupt first.

9.3.15.2.1 Reset Energysense Loss (in Active Mode)

Background: In active mode, the threshold is set to a system-level defined loss threshold (for example, –80 dBFS), and the timeout set to 1 minute.

After 1 minute, the interrupt triggers. To reset energysense loss, take the following steps:

Step 1: Disable the interrupt in INT_EN (Page.0 0x60)

Step 2: Look at INT_STAT (Page.0 0x61). What is the *energysense* interrupt?

The interrupt status register INT_STAT (Page.0 0x61) is *sticky* in active mode. After being set, this register cannot be reset without clearing SIGDET_STAT (Page.0 0x32).

Step 3 Option 1:The easiest way to clear the register is to move to sleep mode. PWRDN_CTRL (Page.0 0x70)

Step 3 Option 2: To ignore the interrupt, or to clear it and remain in active mode (and wait another minute)

Step 4: Set the signal loss threshold to –110 dB (so that the interrupt is no longer generated by internal logic)

Step 5: Clear the SIGDET_STAT (Page.0 0x32) register by:

Write 0xFF to SIGDET_STAT (Page.0 0x32)

Read SIGDET_STAT (Page.0 0x32). The register should be 0x00

Step 6: Now set signal loss threshold to the original –80 dBFS

Step 7: Enable the interrupt again INT_EN (Page.0 0x60)

9.3.15.2.2 Reset Energysense Detect (In Sleep Mode)

Background: The device is in sleep mode, with the wake threshold set as a DSP memory coefficient.

INT_STAT (Page.0 0x61) is *sticky* and SIGDET_STAT (Page.0 0x32) is not *sticky* in this mode. The Interrupt pin triggers dynamically as the audio crosses the threshold. The SIGDET_STAT (Page.0 0x32) register shows which input is causing the input only while that particular input is causing the interrupt. The INT_STAT (Page.0 0x61) register shows the *energysense* interrupt has been triggered until it is cleared.

The system host controller responds to the interrupt in one of two ways:

Option 1: Move to active mode. PWRDN_CTRL (Page.0 0x70)

Option 2: Ignore the interrupt in the system controller, or disable the interrupt for a set amount of time using INT_EN (Page.0 0x60)

9.3.15.2.3 Reset Controlsense (Active and Sleep Modes)

If a potentiometer has been moved and the interrupt asserts, the following steps should be taken:

Step 1: Read the INT_STAT (Page.0 0x61) to confirm it is a *controlsense* event.

Step 2: Disable the *controlsense* interrupt temporarily: INT_EN (Page.0 0x60)

Step 3: Read the SIGDET_STAT (Page.0 0x32) to see which channel changed

Step 4: Read the appropriate SIGDET_DC_LEVEL_CHx_x to find the new value

Step 5: Copy the value to the appropriate SIGDET_DC_REF_CHx_x register. This action should stop the interrupt being caused internally.

Step 6: Re-enable the Interrupt INT_EN (Page.0 0x60)

9.3.15.2.4 Reset DIN Toggle (In Sleep Mode)

Background: The DIN toggle mode can detect if there is a toggle on an external data pin. For The INT pin will pulse as and when the Internal ADC flow clips. Despite the dynamic nature of the interrupt output pin, INT_STAT (Page.0 0x61) is a *sticky* register. To clear this register, take the following steps:

Step 1: Read the INT_STAT (Page.0 0x61) to confirm it is a PGA clipping event.

Step 2: Lower the gain of the current input channel INT_EN (Page.0 0x60)

Step 3: Reset the interrupt using INT_EN (Page.0 0x60). Set bit 5 to 0, then back to 1

Step 4: Bit 5 of INT_STAT (Page.0 0x61) should now be 0. If not, go to step 2 again.

9.3.15.2.5 Reset PGA Clipping (Active)

Background: PGA Clipping is a dynamic interrupt. The INT pin will pulse as and when the Internal ADC flow clips. Despite the dynamic nature of the interrupt output pin, INT_STAT (Page.0 0x61) is a *sticky* register. To clear this register, take the following steps:

Step 1: Read the INT_STAT (Page.0 0x61) to confirm it is a PGA clipping event.

Step 2: Lower the gain of the current input channel INT_EN (Page.0 0x60)

Step 3: Reset the interrupt using INT_EN (Page.0 0x60). Set bit 5 to 0, then back to 1.

Step 4: Bit 5 of INT_STAT (Page.0 0x61) should now be 0. If not, go to step 2 again.

9.3.16 Audio Format Selection and Timing Details

9.3.16.1 Audio Format Selection

Format selection for the PCM1860-Q1 and PCM1861-Q1 is controlled using a hardware pin configuration. There is a choice of left-justified data (known as LJ) or I^2S.

On the PCM186x-Q1 software-controlled devices, format selection is done with the registers in I2S_FMT (Page.0 0x0B), which offers additional support for right-justified (RJ) and time division multiplexed (TDM) data for multiple channels.

The PCM186x-Q1 software-controlled devices also offer an additional DOUT pin that can be driven through the GPIO pins. For an example, see the register details at GPIO1_FUNC (Page.0 0x10).

9.3.16.2 Serial Audio Interface Timing Details

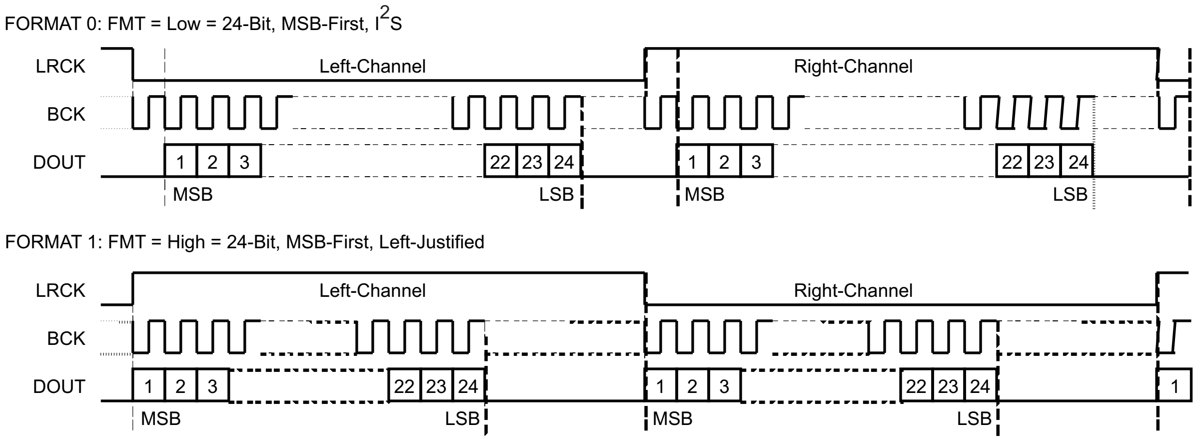


Figure 45. Audio Data Format
(LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

9.3.16.3 Digital Audio Output 2 Configuration

The PCM186x-Q1 four-channel software-controlled devices offer an additional DOUT through the use of a GPIO that has its rate synchronized with the primary DOUT. DOUT2 is configured using the digital mixer, shown in *Digital Mixing Function*. In TDM Modes, DOUT2 is not available.

The GPIO used for DOUT2 can be set using registers. GPIO0 is used for SPI-MOSI in SPI mode, however, it can be retasked for DOUT2 duties if MOSI is not required.GPIO0_FUNC (Page.0 0x10), GPIO1_FUNC (Page.0 0x10), GPIO2_FUNC (Page.0 0x11), or GPIO3_FUNC (Page.0 0x11) can be used to set GPIOx to DOUT2

9.3.16.4 Time Division Multiplex (TDM Support)

The software-controlled devices can support TDM for both slave and master modes. In many devices, this is also known as *DSP Mode*.

Data on the TDM stream can be between two and four channels of audio content from each PCM186x-Q1 mixer output. By default, each mixer passes data from the respective ADC in a bypass or passthrough configuration. Data from the secondary ADC can also be output on channels five and six. The frame rate in TDM mode fixed to 256 BCK per frame, and the duty cycle of the LRCK (or frame sync signal) can be either a 50 / 50 duty cycle, or a single bit at the start of the frame.

Up to 32 bits per channel are available. In 32-bit mode, 24 bits of data and 8 bits of padding (zero) are used per channel. In 24-, 20-, and 16-bit data, no padding is provided between channels. In 24-bit mode, channel two begins transmitting on bit clock 25.

In data formats lower than 24 bits, the data is simply truncated, not dithered to 16 bits.

In slave mode, only a rising edge on the first bit is required to start the frame. (similar to MSB-first, left-justified).

In master mode, only a 50% duty cycle on the output is possible. This configuration is made by setting TDM_LRCK_MODE (Page.0 0x0B) to 0.

Typically when interfacing to a DSP, only the rising edge on the first bit of data of the frame is required.

While the device is not transmitting data (but still being clocked), the DOUT pin will be Hi-Z (high impedance) to allow other devices on the bus to transmit their data.

TDM mode is configured using I2S_FMT (Page.0 0x0B), TDM_LRCK_MODE (Page.0 0x0B), TDM_OSEL (Page.0 0x0C)

The timing limits for the interface signals are defined by the *Serial Audio Data Interface Configuration* section with the addition that the BCK period minimum must at least 1 / (512 × f_S) to ensure that data is clocked in correctly.

The audio format is shown below. The 24-bit data can fit up to 10 channels of data in a 256x bitclock stream; however, the I²C-controlled devices only have two possible I²C addresses. The eight channels of audio data should be no issue.

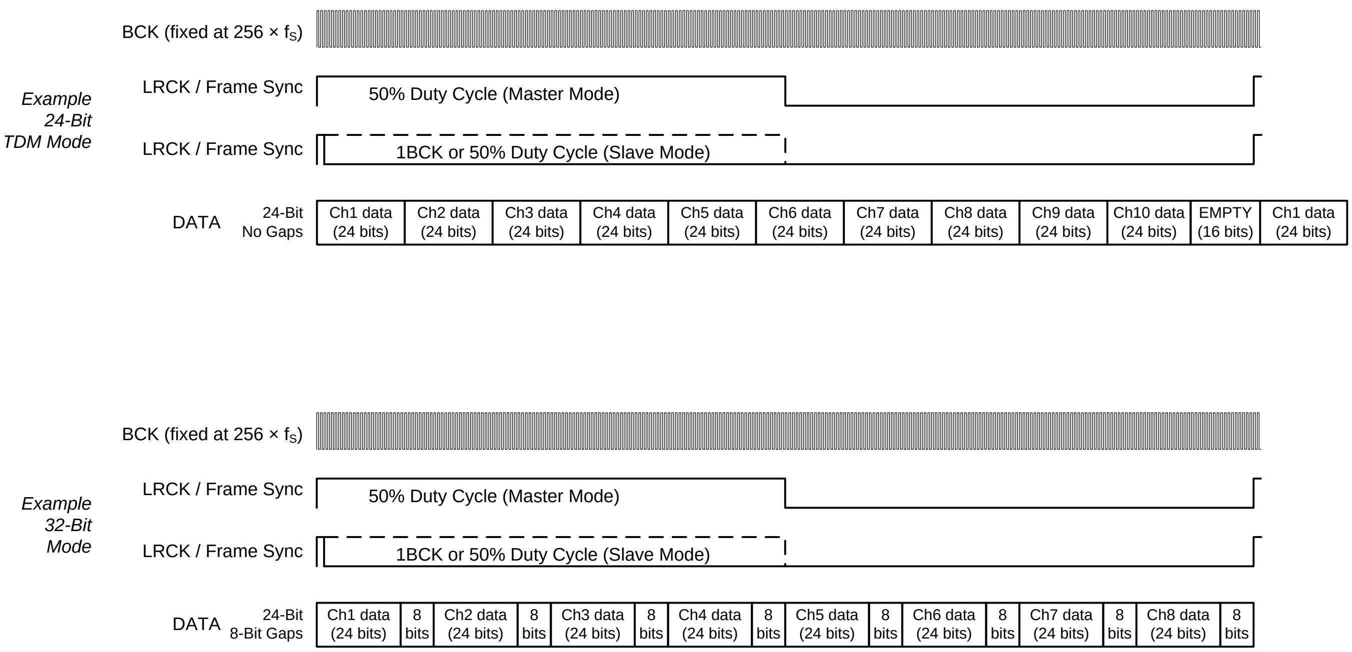


Figure 46. Audio Format for TDM

NOTE

TDM mode can only function up to 96 kHz sampling rate when IOVDD is 1.8 V. This is due to an I/O limitation of 25 MHz at 1.8 V.

9.3.16.5 Decimation Filter Select

The PCM186x-Q1 offers a choice of two different digital filters, a Classic FIR response and a low latency IIR.

9.3.16.6 Serial Audio Data Interface Configuration

The PCM186x-Q1 devices interface to the audio system through LRCK, BCK and DOUT.

The PCM186x-Q1 hardware-controlled devices are configured using pin MD4 to select between left-justified data and I^2S.

The PCM186x-Q1 software-controlled devices are configured using register I2S_FMT (Page.0 0x0B). Use register I2S_TX_OFFSET (Page.0 0x0D) when dealing with TDM systems to offset the data transmit.

In addition, the offset required for receiving 24-bit data is programmed using RX_TDM_OFFSET (P0, R0x0E).

9.4 Device Functional Modes

9.4.1 Power Mode Descriptions

The PCM186x-Q1 family has multiple power modes: active, sleep, idle, and standby. Table 19 lists the power modes and functions.

- *Active mode*: describes the mode where the device is targeting full performance and functionality.
- *Idle mode*: describes the mode where the digital output is muted and the analog side (such as PGAs) are still powered up.
- *Sleep mode*: describes the mode where the main ADCs are not in use, but the device continues to do *Energysense* input level detection.
- *Standby mode*: drops the power into an ultra-low power mode where only the control port is available.

Table 19. Power Modes

FUNCTIONS	ACTIVE OR IDLE (MUTE)	SLEEP (*Energysense*)	STANDBY
ANALOG FUNCTIONS			
Programmable Gain Amps	ON	OFF	OFF
ADC	ON	OFF	OFF
ADC Reference	ON	OFF	OFF
CMBF	ON	ON	ON
Reference	ON	ON	ON
Mic Bias	ON	ON	OFF
Secondary ADC PGA	ON	ON	OFF
Secondary PGA	ON	ON	OFF
ACCESSORY FUNCTIONS			
LDO	ON	ON	ON
Oscillator	ON	ON	ON
Clock Halt Detection	ON	ON	ON
PLL	ON	ON	OFF
Digital Cores	ON	20% ON	5% ON (Control Port Only)

9.4.1.1 PCM1860-Q1 and PCM1861-Q1 Hardware Device Power Down Functions

9.4.1.1.1 Enter Standby Mode (From Active Mode)

The external host should drive the INT pin (GPIO3) high (whilst there is no interrupt pending) to place the device in Idle mode.

The INT pin is configured as an *energysense* interrupt output on the hardware-controlled device; therefore, the external host microcontroller should use it as multi-function pin. (MCU pin configured as INPUT when no requirement exists to move to standby, MCU pin as OUTPUT driving HIGH when a need exists to place the device in an idle state.)

NOTE

While the device is driving its interrupt high, any external voltage on the INT pin will be ignored by the device, until the interrupt event (and pulse) is finished.

9.4.1.1.2 Exit From Standby Mode Back to Active

The external MCU host releases the INT pin (GPIO3). This typically involves reconfiguring the external MCU GPIO into an INPUT or HI-Z.

9.4.1.1.3 Enter or Exit Sleep or Energysense Mode to Active

Enter sleep mode: Halt BCK and LRCK

Exit sleep mode: Resume BCK and LRCK

9.4.1.2 PCM186x-Q1 Software Device Power Down Functions

9.4.1.2.1 Enter or Exit Stand-by Mode

Enter standby mode: Send power down command by writing register PWRDN_CTRL (Page.0 0x70)

Exit standby mode: Send power up command by writing register PWRDN_CTRL (Page.0 0x70)

9.4.1.2.2 Enter Sleep Mode

Send sleep command by writing register PWRDN_CTRL (Page.0 0x70) or

Halt BCK and LRCK when I^2S is configured as I^2S slave mode

9.4.1.2.3 Exit Sleep Mode

Send resume from (exit) sleep command by writing register PWRDN_CTRL (Page.0 0x70) or

Resume BCK and LRCK when I^2S is configured as I^2S slave mode

9.4.1.3 Bypassing the Internal LDO to Reduce Power Consumption

The PCM186x-Q1 has an integrated LDO allowing single 3.3-V supply operation. However, developers desiring to minimize power consumption can bypass the on-chip LDO and provide 1.8 V to IOVDD and to LDO under the following conditions:

- TDM mode is limited to BCK driving a maximum of 25 MHz, because the BCK and DATA cells cannot exceed 25 MHz when IOVDD is 1.8 V. Consequently, a maximum of 96-kHz sampling frequency operation is possible.
- IOVDD MUST be 1.8 V along with LDO, if an external 1.8 V supply is used to bypass the internal LDO.

9.5 Programming

9.5.1 Control

9.5.1.1 Hardware Control Configuration

PCM186x-Q1 devices require the following functions to be configured on startup. Hardware-controlled devices require a subset of these configurations:

- Control interface type and address for PCM186x-Q1 software-controlled devices
- The clock mode and rate (automatic in slave mode, or divider ratio in master mode) for hardware-controlled devices. For more details see the *Clocks* section.
- The interface audio data format for hardware-controlled devices.
- Digital filter selection (FIR or IIR) for hardware-controlled devices; requires a power cycle to change.
- Analog input channels and PGA gain for hardware-controlled devices.

9.5.1.2 Software-Controlled Device Configuration

PCM186x-Q1 software-controlled devices are configured and controlled by using either I^2C or SPI using MD0 and MD1. Table 20 shows the MD0 control protocols, and Table 21 shows the MD1 mode selection.

Table 20. MD0: Control Protocol Select

MD0	Control Protocol
Low (or floating)	I^2C Mode
High	SPI Mode

Table 21. MD1: I^2C Address or SPI Chip Select

MODE	MD1 USE	STATIC MD1 VALUE	CONFIGURATION
I^2C	Address pin	Low	I^2C Address: 0x94
I^2C	Address pin	High	I^2C Address: 0x96
SPI	MS (SPI Chip Select)	N/A	N/A

9.5.1.3 SPI Interface

The SPI interface is a 4-wire synchronous serial port that operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers.

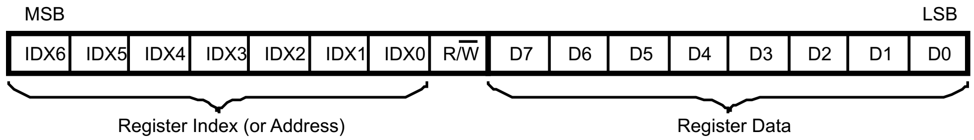
The control interface includes MISO, MOSI, MC, and MS. MISO (master in slave out) is the serial data output, used to read back the values of the mode registers; MOSI (master out slave in) is the serial data input, used to program the mode registers.

MC is the serial bit clock, used to shift data in and out of the control port on the MC falling edge. MS is the active-low mode control enable, used to enable the internal mode register access. If data from the device is not required, the MISO pin can be assigned to GPIO1 by register control.

9.5.1.3.1 Register Read and Write Operation

All read and write operations for the serial control port use 16-bit data words. Figure 47 shows the control data word format. The most significant bit is the read and write (R/W) bit. For write operations, the bit must be set to 0. For read operations, the bit must be set to 1. There are seven bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to, or the data that was read from, the register specified by IDX[6:0].

Figure 48 and Figure 49 show the functional timing diagram for writing or reading through the serial control port. MS should be held at logic 1 state until a register needs to be written or read. To start the register write or read cycle, MS should be set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MOSI and readback data on MISO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MISO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data, MS should be set to logic 1 once.



NOTE: B8 is used for selection of write or read. Setting = 0 indicates a write, while = 1 indicates a read. Bits 15–9 are used for register address. Bits 7–0 are used for register data.

Figure 47. Control Data Word Format for MDI

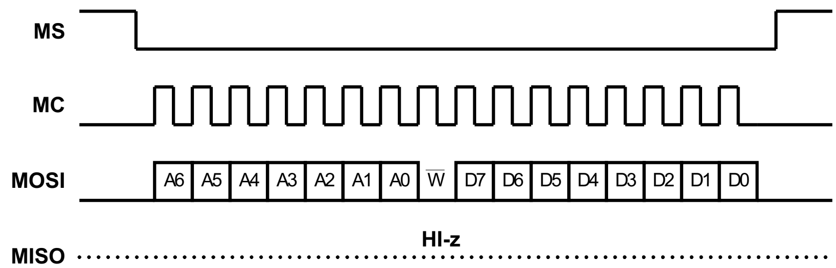


Figure 48. Serial Control Format for Write

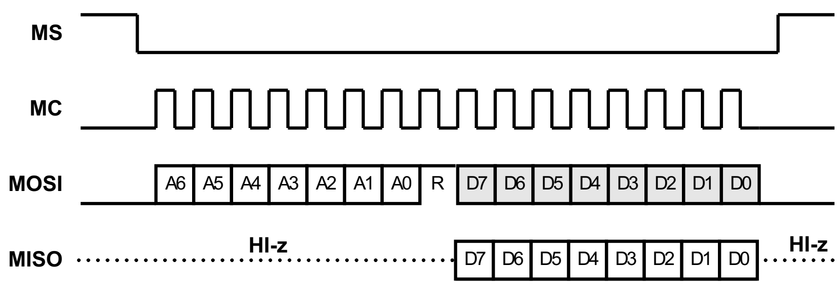


Figure 49. Serial Control Format for Read

9.5.1.4 I²C Interface

The PCM186x-Q1 software-controlled devices support the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in I²C specification 2.0.

The I²C control port is available even in the absence of any other clocks in the system.

In I²C mode, the control pins are changed as shown in Table 22.

Table 22. I²C Pins and Functions

PIN NAME	PIN NUMBER	PROPERTY	DESCRIPTION
SDA	23	Input / Output	I²C data
SCL	24	Input	I²C clock
AD	25	Input	I²C address 1

9.5.1.4.1 Slave Address

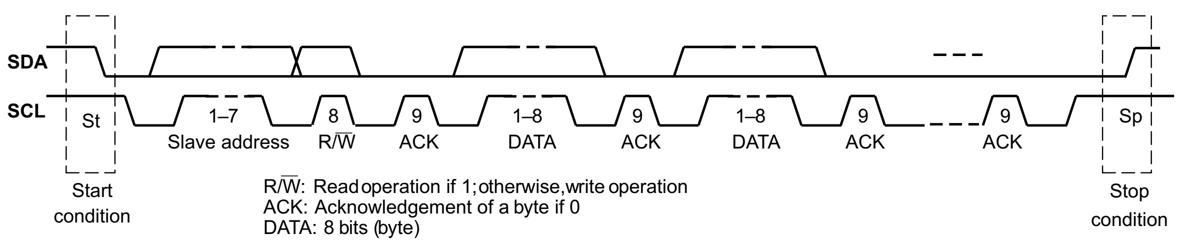
The PCM186x-Q1 software-controlled devices have a 7-bit slave address, as shown in Table 23. The first six bits (MSBs) of the slave address are factory preset to 1001 01. The next bit of the address byte is the device select bit, which can be user-defined by the AD pin. A maximum of two PCM186x-Q1 devices can be connected on the same bus at one time. Each device responds when receiving the respective slave address.

Table 23. I²C Slave Address

MSB							LSB
1	0	0	1	0	1	AD	R/$\overline{W}$

9.5.1.4.2 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM186x-Q1 software-controlled devices support only slave receivers and slave transmitters. Figure 50 shows the basic I²C framework.



write operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	R/$\overline{W}$	ACK	DATA	ACK	DATA	ACK	------------	ACK	Sp

read operation

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	R/$\overline{W}$	ACK	DATA	ACK	DATA	ACK	------------	ACK	Sp

M: Master Device *S: Slave Device*

St: Start Condition Sp: Stop Conditiion

Figure 50. Basic I²C Framework

9.5.2 Current Status Registers

Page.0, registers 0x72 through 0x75 and 0x78 can be used to read the device status at any time. Sample rate, power rail status, clock error, and clock ratios can all be read from these registers.

9.5.3 Real World Software Configuration using *Energysense* and *Controlsense*

To gain the benefit of many of the PCM186x-Q1 features, use a microcontroller to monitor and control the device. There are two main modes withing the device, *Active* and *Sleep*. Using a microcontroller to process the interrupts for both *energysense* and *controlsense* allows the system to intelligently wake and sleep as well as update system controls. Figure 51 and Figure 52 show flow diagrams for both active and sleep modes, respectively. Extended I^{2}C register settings are shown in **Bold Text**.

9.5.3.1 Active Mode Flow Diagram

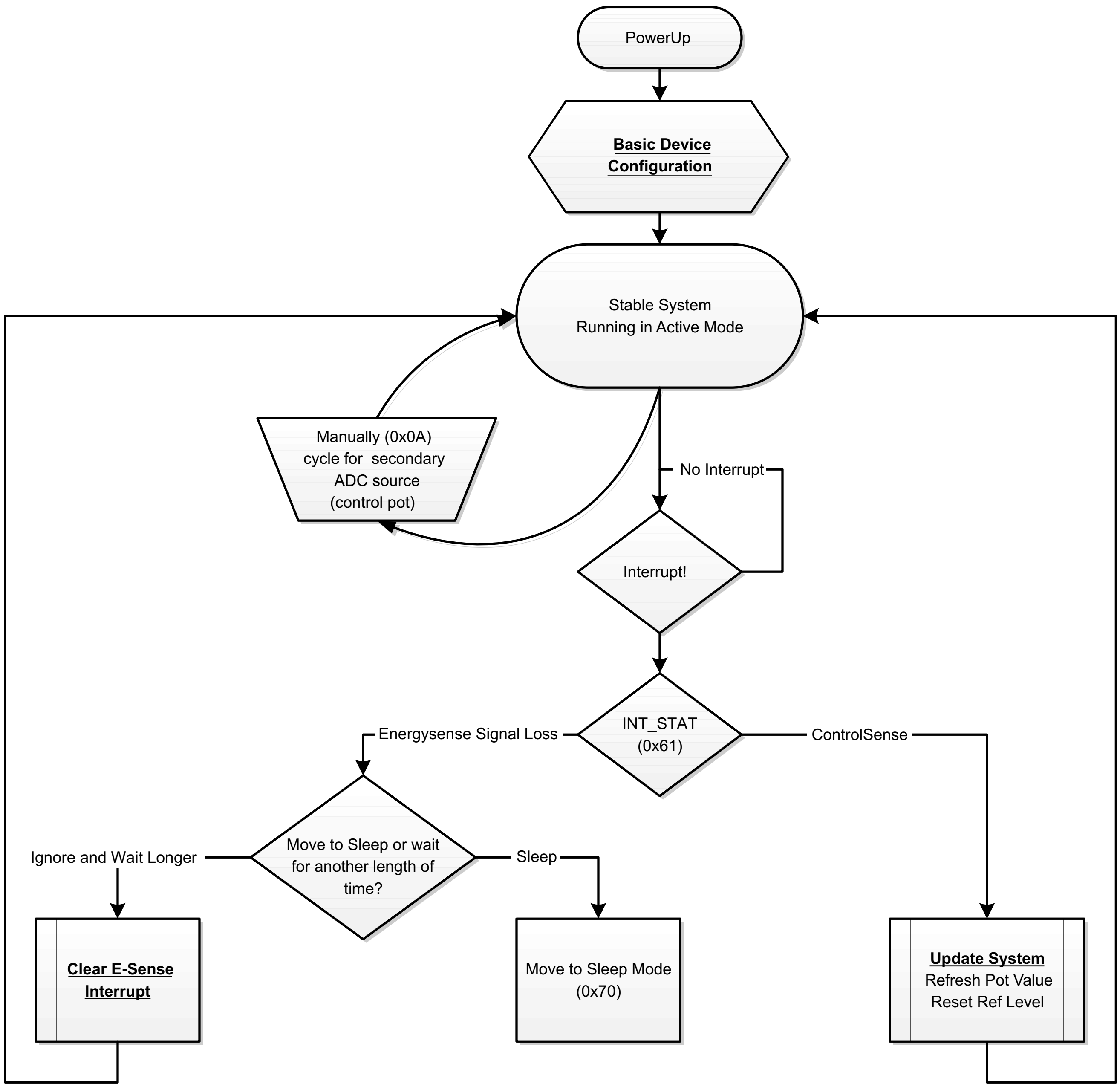


Figure 51. Active Mode Flow Chart

9.5.3.2 Basic Device Configuration

The device by default starts in slave mode at 48 kHz (per the EVM)

Set global loss level to be –50 dB using the DSP coefficient method.

Set 4R as *controlsense* input (for example, a control voltage for volume control) using SIGDET_CH_MODE (0x30)

Configure active mode secondary to be channel 4R using SEC_ADC_INPUT_SEL (0x0A)

Set *Read Data without latch* in register AUXADC_DATA_CTRL (0x58)

Set interrupts (*energysense* and *controlsense*) using INT_EN (0x60)

Set interrupt pulse for 3 mS (makes it easier to see it visually using INT_PLS (0x62)

9.5.3.3 Clear Energysense Interrupt

Disable the *energysense* interrupt in INT_STAT register (0x61)

Remove the interrupt source by changing the loss detect threshold to 110 dB (ADC noise level) using the DSP coefficient method.

Write 0xFF to the SIGDET_STAT (0x32) register.

Write 0x00 to the SIGDET_STAT (0x32) register.

Change the loss detect threshold back to –50 dB using the DSP coefficient method.

Re-enable the *energysense* interrupt in INT_STAT register (0x61)

9.5.3.4 Update System Settings

Read interrupt status INT_STAT register(0x61)

Clear interrupt enable INT_EN (0x60)

Check which input caused the interrupt; in this case, looking for (4R) SIGDET_STAT (0x32)

Read new 4R data (for example, SIGDET_DC_LEVEL_CH4_R 0x57).

Host would normally process as needed. (foe example, change volume in the amplifier)

Set SIGDET_DC_REF_CH4_R (0x55) to be the new value.

Now that interrupt source is removed, we can clear the SIGDET_STAT register (0x32)

Write 0xFF to SIGDET_STAT register (0x32).

Write 0x00 to SIGDET_STAT register (0x32).

Re-enable control Sense Interrupt in INT_EN (0x60)

9.5.3.5 Sleep Mode Flow Diagram

The sleep mode flow chart is shown in Figure 52.

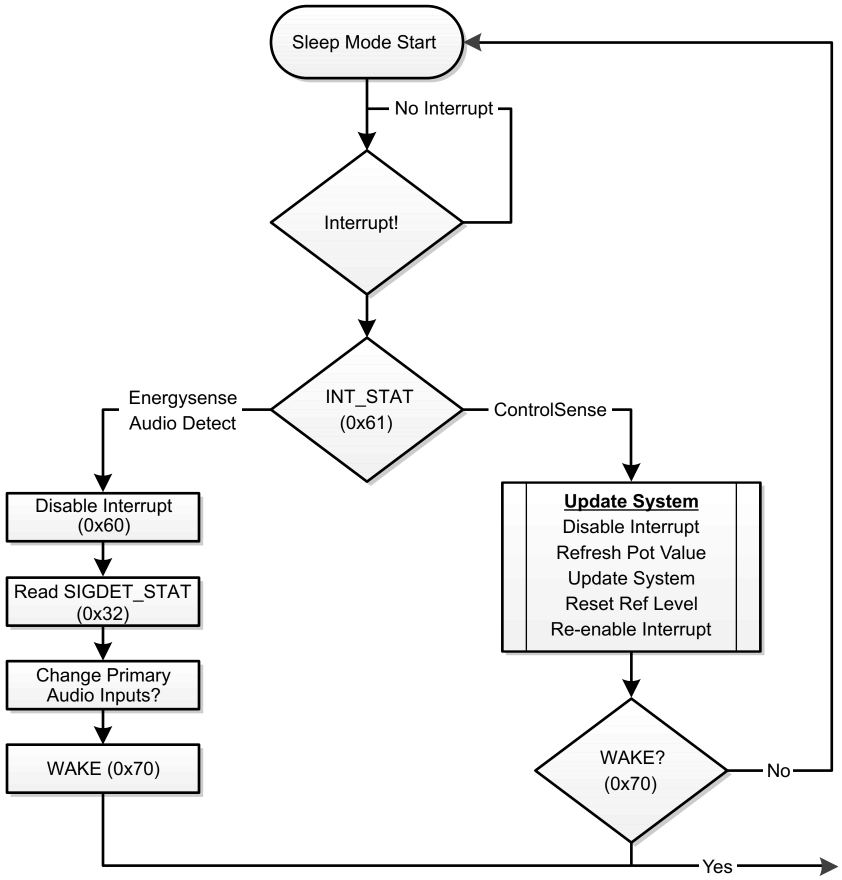


Figure 52. Sleep Mode Flow Chart

9.5.3.6 Update Controlsense values in Sleep Mode

9.5.3.6.1 Update System Settings

In sleep mode, any channels set as *controlsense* inputs are scanned through automatically. The read and writes to SIGDET_DC_REF_CHx_x and SIGDET_DC_LEVEL_CHx_x should be selected based on whichever input caused the interrupt.

Read interrupt status INT_STAT register(0x61)

Clear *controlsense* interrupt enable INT_EN (0x60)

Check which input caused the interrupt SIGDET_STAT (0x32)

Read new data (for example, SIGDET_DC_LEVEL_CHx_x).

Host would normally process as needed (for example, change volume in the amplifier)

Set SIGDET_DC_REF_CHx_x to be the new value.

Now that interrupt source is removed, we can clear the SIGDET_STAT register (0x32) --

Write 0xFF to SIGDET_STAT register (0x32).

Write 0x00 to SIGDET_STAT register (0x32).

Re-enable *controlsense* interrupt in INT_EN (0x60)

9.5.4 Programming and Register Reference

9.5.4.1 Coefficient Data Formats

All mixer gain coefficients are 24-bit coefficients using a 4.20 number format. Numbers formatted as 4.20 numbers have 4 bits to the left of the binary point and 20 bits to the right of the binary point.

The most significant bit of the 4.20 number format is the sine bit. It is used, as part of a two's complement number to invert the phase of that mixer input.

See SLAC663 for a calculator to convert from dB to the hexadecimal coefficient required.

9.5.5 Programming DSP Coefficients on Software-Controlled Devices

The two fixed function DSPs on chip can have coefficients for filters and mixers programmed to them. This is done indirectly using specific registers on page 1. The devices integrate a memory arbiter that copies the coefficient from the I^2C or SPI register space to the appropriate DSP memory address, when the DSP has completed its instructions for that sample. The refresh mechanism for the memory arbiter to update the I^2C or SPI register space requires two dummy I^2C writes to move from the DSP internal memory, through the arbiter and onwards to be visible in the I^2C or SPI register space. See *Figure 53*

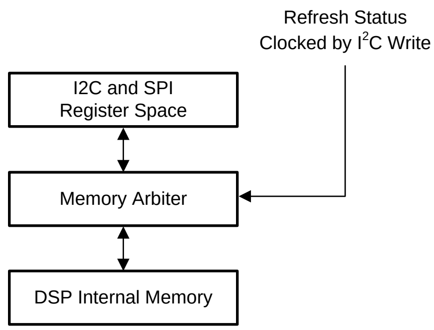


Figure 53. Register to DSP Memory Structure

Each 24-bit coefficient can be written once every audio sample. This allows a single sample update of a mixer coefficient, however, biquad coefficients will require multiple audio samples for all of the coefficients to be written. Under such conditions, the device should be muted until all coefficients are written. Otherwise, the biquad could become unstable.

In addition, DSP Internal memory can only be written to when the DSP is provided a clock from either the PLL or an external master clock source. Requesting a WREQ = 1 Register 0x01 of page 0x01 will have no effect, if the DSP is not currently running. This is of relevance if the system is running as a clock slave, and the clocks stop.

For example, to write to these registers, change the *energysense* resume threshold value to –30 dB (0x040C37)

1. Write 0x00 0x01 ; # change to register bank 1
2. Write 0x00 0x01 ; # two dummy writes to update the status of the write busy bit
3. Write 0x00 0x01 ; # ^^^^
4. Read Register 0x01 # if value is 0x00 then continue (check if system is still writing/reading). Otherwise, do another dummy write and check again.
5. Write 0x02 0x2D ; # write the memory address of resume threshold
6. Write 0x04 0x04 ; # bit[23:15]
7. Write 0x05 0x0C ; # bit[15:8]
8. Write 0x06 0x37 ; # bit[7:0]
9. Write 0x01 0x01 ; # execute write operation

See SLAC663 for more details.

The internal DSP coefficient memory space is mapped as shown in Table 24.

Table 24. Virtual 24-Bit DSP Coefficient Registers

NAME	COEFFICIENT	ADDRESS	DESCRIPTION
Mixer-1	MIX1_CH1L	0x00	4.20 format
	MIX1_CH1R	0x01	
	MIX1_CH2L	0x02	
	MIX1_CH2R	0x03	
	MIX1_I2SL	0x04	
	MIX1_I2SR	0x05	
Mixer-2	MIX2_CH1L	0x06	4.20 format
	MIX2_CH1R	0x07	
	MIX2_CH2L	0x08	
	MIX2_CH2R	0x09	
	MIX2_I2SL	0x0A	
	MIX2_I2SR	0x0B	
Mixer-3	MIX3_CH1L	0x0C	4.20 format
	MIX3_CH1R	0x0D	
	MIX3_CH2L	0x0E	
	MIX3_CH2R	0x0F	
	MIX3_I2SL	0x10	
	MIX3_I2SR	0x11	
Mixer-4	MIX4_CH1L	0x12	4.20 format
	MIX4_CH1R	0x13	
	MIX4_CH2L	0x14	
	MIX4_CH2R	0x15	
	MIX4_I2SL	0x16	
	MIX4_I2SR	0x17	
Secondary ADC LPF and HPF Coefficients	LPF_B0	0x20	1.23 format
	LPF_B1	0x21	
	LPF_B2	0x22	
	LPF_A1	0x23	
	LPF_A2	0x24	
	HPF_B0	0x25	
	HPF_B1	0x26	
	HPF_B2	0x27	
	HPF_A1	0x28	
	HPF_A2	0x29	
Energysense	Loss_threshold	0x2C	1.23 format
	Resume_threshold	0x2D	

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The PCM186x-Q1 family is extremely flexible, and this flexibility gives rise to a number of design questions that define the design requirements for a given application.

10.1 Application Information

In this section, the design choices are described, followed by a typical system implementation. The simplified application diagrams shown in Figure 64 and Figure 66 illustrate a typical system that would require the following architecture decisions to be made:

- *Device Control Method*
  - Hardware Control (PCM1860-Q1, PCM1861-Q1)
  - Software Control (PCM1862-Q1, PCM1863-Q1, PCM1864-Q1 and PCM1865-Q1)
    - SPI
    - I^2C
- *Power-Supply Options*
  - Single supply
  - Separate analog and digital supplies
  - Separate IO supply
- *Master Clock Source*
  - External CMOS-level clock
  - External crystal with integrated oscillator
- *Analog Input Configuration*
  - Single-ended
  - Differential

An example application diagram is shown in Figure 54.

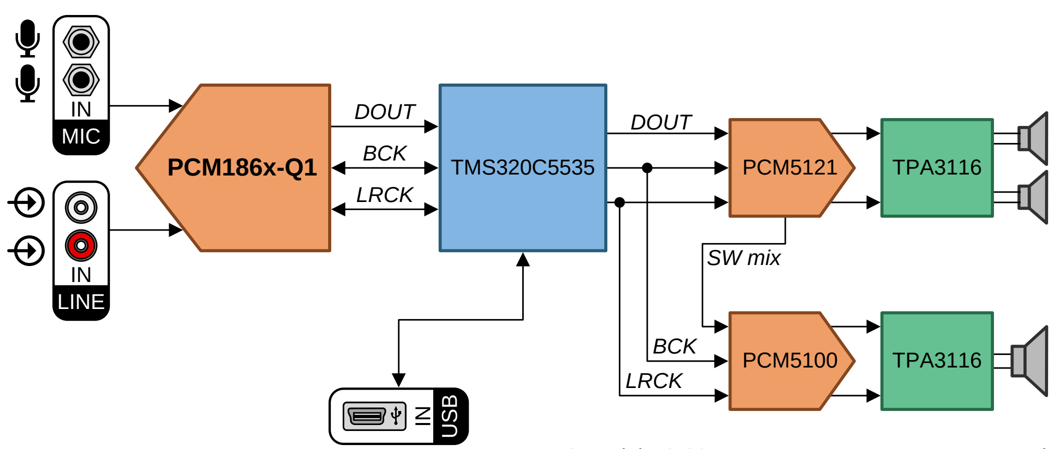


Figure 54. Example Application Diagram

Application Information (continued)

10.1.1 Device Control Method

10.1.1.1 Hardware Control

The PCM1860-Q1 and PCM1861-Q1 are controlled with pullup or pulldown voltages on pins MD0 through MD6. The INT pin is ideally designed to be used with a microcontroller that can treat the pin as both an input (when used as an interrupt) and as an output to pull the pin high, and force power down. See the *Pin Configuration and Functions* for the PCM1860-Q1 and PCM1861-Q1 for specific configuration details. The hardware control interface is shown in Figure 55.

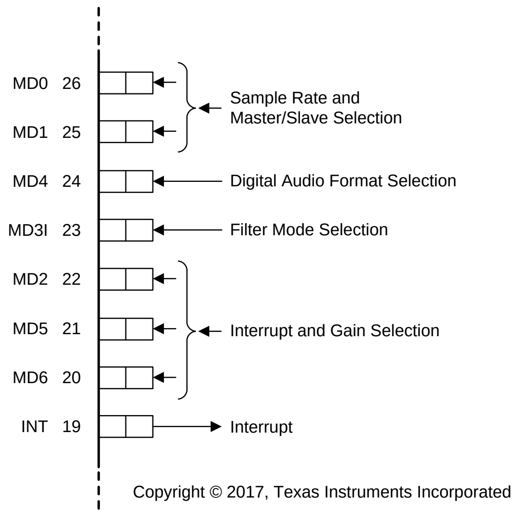


Figure 55. PCM1860-Q1 and PCM1861-Q1 Hardware Control Interface

10.1.1.2 Software Control

10.1.1.2.1 SPI Control

SPI control is selected by the MD0 pin; in this case, MDO connects to 3.3 V, so that the device acts as an SPI slave. The SPI control interface is shown in Figure 56.

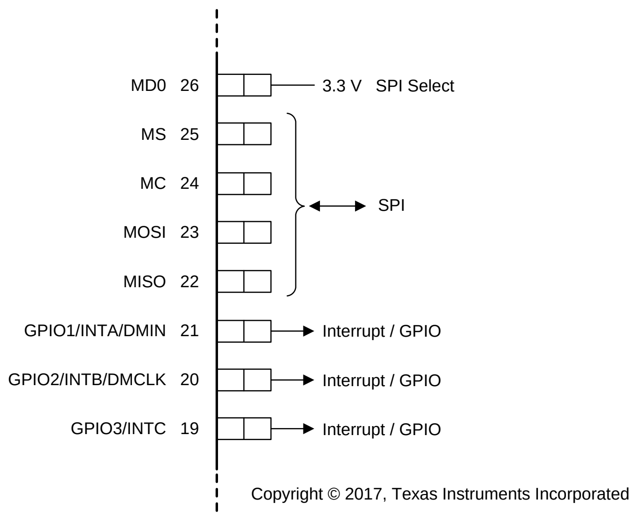


Figure 56. SPI Control Interface Including Interrupt Signals

Application Information (continued)

10.1.1.2.2 I²C Control

I²C control is selected by the MD0 pin; in this example, MDO is pulled down to ground, so that the device acts as an I²C slave. One address line is supported to select between two devices on the same bus. The I²C control interface is shown in Figure 57.

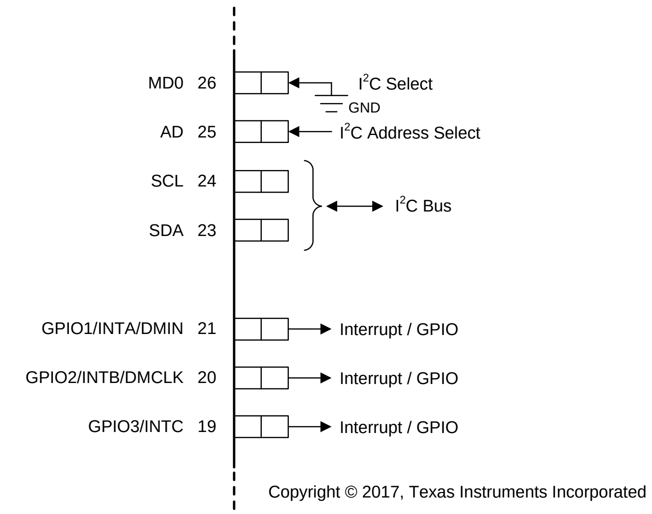


Figure 57. I²C Control Interface Including Interrupt Signals

10.1.2 Power-Supply Options

10.1.2.1 3.3-V AVDD, DVDD, and IOVDD

The *3.3-V AVDD, DVDD, and IOVDD Example* is the most typical power-supply configuration. The 3.3-V single supply is shown in Figure 58.

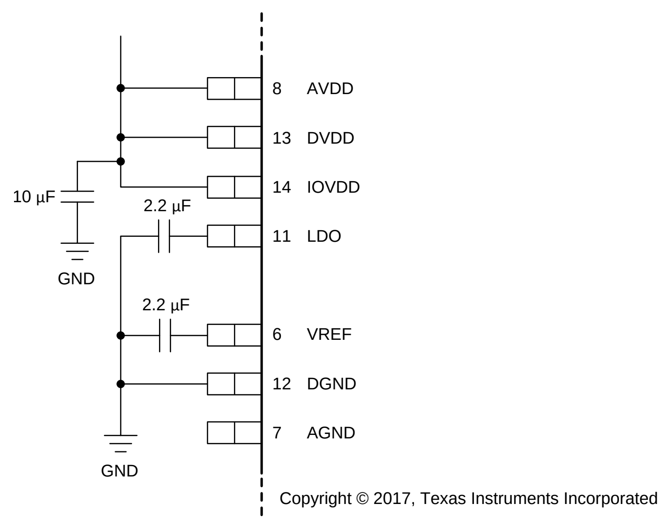


Figure 58. Single 3.3-V Supply

10.1.2.2 3.3-V AVDD, DVDD, and 1.8-V IOVDD

For details regarding lower-power applications, see *3.3-V AVDD, DVDD With 1.8-V IOVDD Example for Lower-Power Applications* for lower-power applications.

Application Information (continued)

10.1.3 Master Clock Source

The PCM186x-Q1 family offers three different clock sources. For the highest performance, run the ADC in master mode from a stable, well-known SCK source, such as a CMOS SCK, or a external crystal (XTAL). The PCM186x-Q1 is easy to hook up to a crystal, simply connect to XI and XO, and add capacitors to ground, as suggested in the XTAL manufacturer's data sheet (typically 15 pF).

External CMOS clock sources can be brought directly into the SCKI pin (for 3.3-V sources) or into the XI pin (1.8 V sources).

The PLL must be enabled if the clock source is unrelated to the audio rate. For instance, a 12-MHz USB crystal requires custom PLL settings to generate the 48-kHz rate clocks and the 44.1-kHz rate clocks required by many audio systems. An example with a 12-MHz clock is shown in *Software-Controlled Devices Manual PLL Calculation*.

For timing limits on XTAL and SCKI, see the *Specifications* section.

10.1.4 Dual PCM186x-Q1 TDM Functionality

Two PCM186x-Q1 software-controlled devices can be used together to create an 8-channel (or higher) channel count system using a TDM. In Figure 59, Device A is used as the TDM clock master, and Device B is configured to be a TDM slave and transmit on channels 5, 6, 7, and 8 of the TDM stream. The key difference is that Device A most likely has a crystal, or an SCKI source, and is configured to be the TDM master, whereas Device B does not require an XTAL or SCKI source because Device B uses the internal PLL to generate the required system clocks. Another two channels can be added to the stream from a stereo device; however, I^2C address management is required because the PCM186x-Q1 software-controlled devices can only have one of two I^2C addresses.

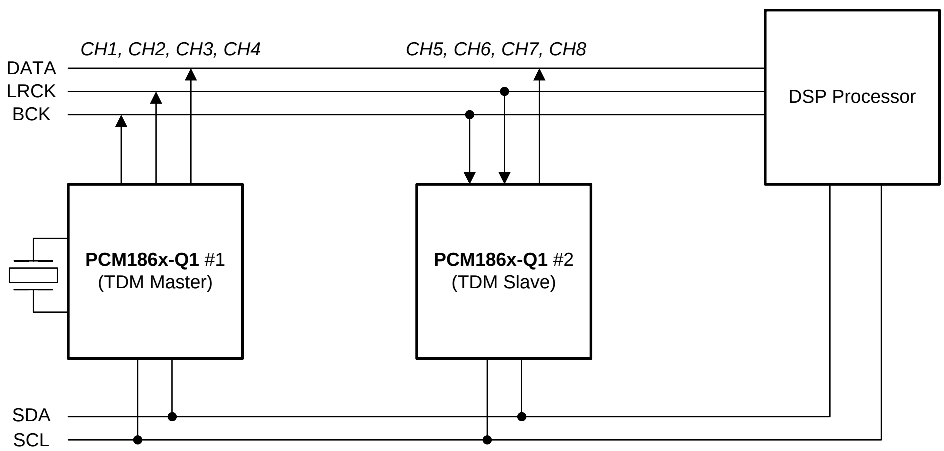


Figure 59. TDM With Two PCM186x-Q1

Application Information (continued)

10.1.5 Analog Input Configuration

10.1.5.1 Analog Front-End Circuit For Single-Ended, Line-In Applications

Most systems can simply use an input filter similar to the one shown in Figure 60. However, for systems with significant out-of-band noise, a simple filter such as that shown in Figure 61 can be used for pre-ADC, antialiasing filtering. The recommended resistor value for the antialiasing filter is 100 Ω. Place film-type capacitors of 0.01 µF as close as possible to the VINLx and VINRx pins, and terminate to GND as close as possible to the AGND pin in order to maximize the dynamic performance of the ADC.

Adding this filter resistor also adds some input current limiting into the device, if the ESD diodes begin to clamp the signal when the maximum input voltage is exceeded. Keep the current through the input ESD diodes as low as possible, with ~5 mA treated as a absolute maximum. Any higher and the ESD diodes may fail because of the thermal constraints.

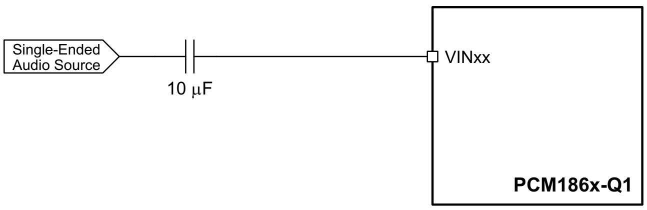


Figure 60. Analog Input Circuit for Single-Ended Input Applications

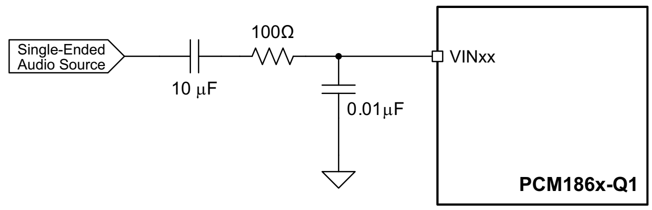


Figure 61. Analog Input Circuit With Additional Anti Aliasing Filter for Single-Ended Applications

10.1.5.2 Analog Front-End Circuit for Differential, Line-In Applications

As in single-ended applications, most systems can simply use an input filter similar to Figure 62. However, for systems with significant out-of-band noise, a simple filter such as that shown in Figure 63 can be used for pre-ADC, antialiasing filtering. The recommended resistor value for the antialiasing filter is 47 Ω. Place film-type capacitors of 0.01 µF as close as possible to the VINLx and VINRx pins, and terminate to GND as close as possible to the AGND pin in order to maximize the dynamic performance of ADC. To maintain common-mode rejection, match the series resistors as closely as possible.

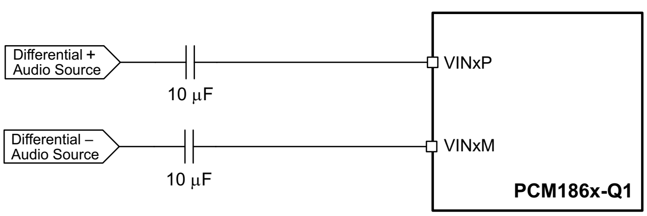


Figure 62. Analog Input Circuit for Differential Input Applications

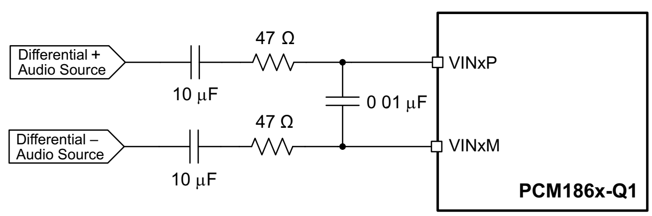
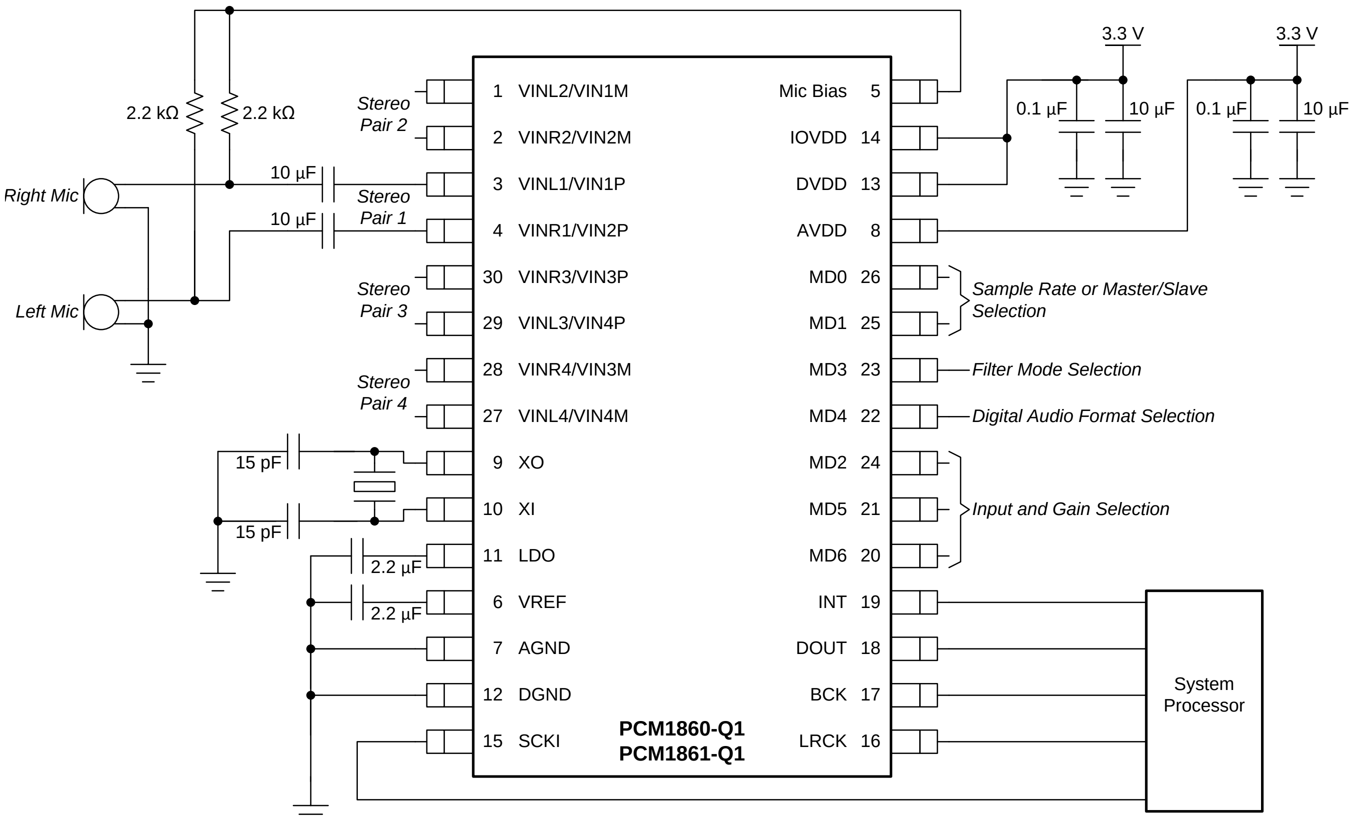


Figure 63. Differential Input Circuit With Additional AntiAliasing Filter

10.2 Typical Applications

10.2.1 Stereo Recording Application for PCM186x-Q1 Hardware-Controlled Devices in Master Mode



NOTE: Pins not shown in specific order.

Figure 64. Stereo Recording Application for PCM186x-Q1 Hardware-Controlled Devices in Master Mode

Typical Applications (continued)

10.2.1.1 Design Requirements

- Device control method: Hardware control by digital GPIO pins of a microcontroller
- XTAL used for master mode
- Single-ended analog inputs

10.2.1.2 Detailed Design Procedure

- Device control method: Hardware control by digital GPIO pins of a microcontroller
- Select XTAL capacitors by reading the XTAL data sheet
- Single-ended analog inputs
  - MD2, MD5, MD6 configuration (see the *Pin Configuration and Functions* for the PCM1860-Q1 and PCM1861-Q1)
- Audio slave mode
  - MD0, MD1 grounded (see Figure 64, and the *Pin Configuration and Functions* for the PCM1860-Q1 and PCM1861-Q1)
- The power rails in this application allow the usage of X7R Ceramic capacitors. A maximum voltage rating of 6.3 V should be enough for the power supply capacitors.
- Configure the microcontroller INT pin to be an input for interrupts, or change the function to output to pull high to power down the PCM1860-Q1 and PCM1861-Q1.

10.2.1.3 Application Curves

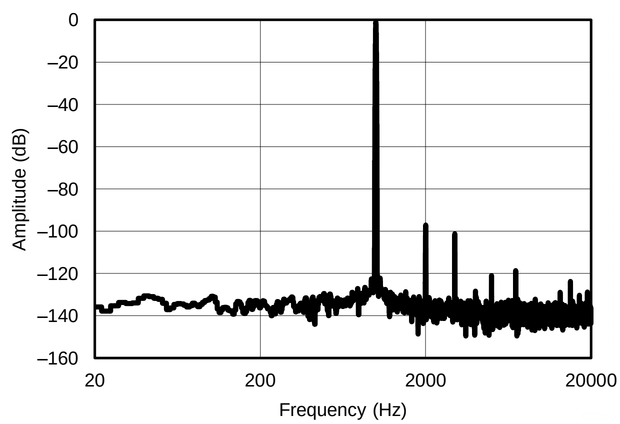
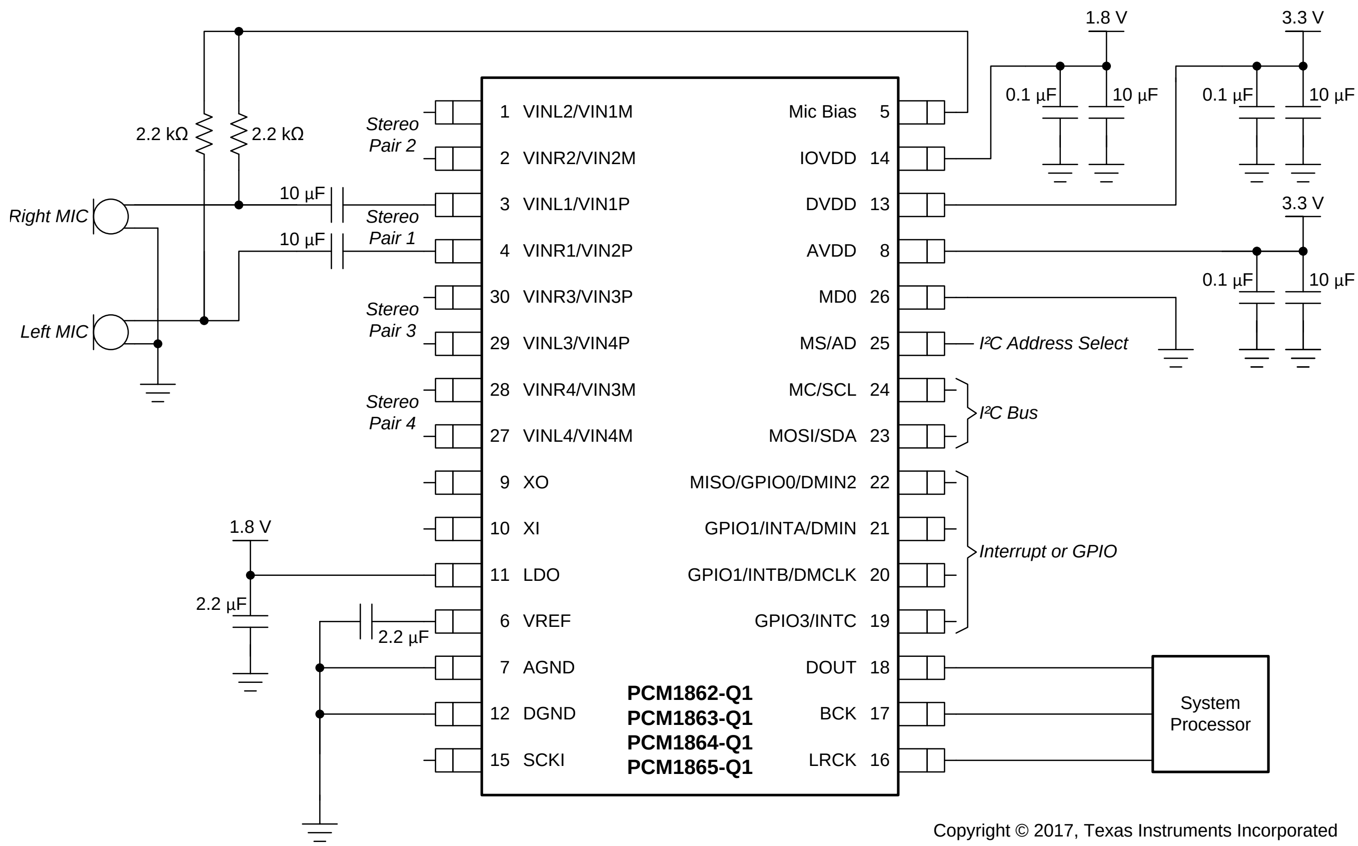


Figure 65. Frequency Response with –1-dB Input at 1 kHz

Typical Applications (continued)

10.2.2 Stereo Recording Application for PCM186x-Q1 Software-Controlled Devices in Slave PLL Mode with 1.8-V IOVDD



NOTE: Pins not shown in specific order.

Figure 66. Stereo Recording Application for PCM186x-Q1 Software-Controlled Devices in Slave PLL Mode with 1.8-V IOVDD

Typical Applications (continued)

10.2.2.1 Design Requirements

- Device control method: Software control by I^2C
- Clock slave to a 1.8-V device that only supplies BCK and LRCK (such as a Bluetooth module)
- Single-ended analog inputs

10.2.2.2 Detailed Design Procedure

- Device control method: Configure for I^2C by pulling MD0 to GND, and setting I^2C address by setting the AD pin high or low
- Make sure that BCK is configured in clock master device to be 64 × f_S for automatic PLL setting to function.
- Single-ended analog inputs
  - MD2, MD5, MD6 configuration; see
- Audio slave mode
  - Configure appropriate clock registers
  - Page 0, 0x20 - Set MST_MODE = 1 (I^2S slave)
- The power rails in this application allow the usage of X7R ceramic capacitors. A maximum voltage rating of 6.3 V should be enough for the power-supply capacitors.

10.2.2.3 Application Curves

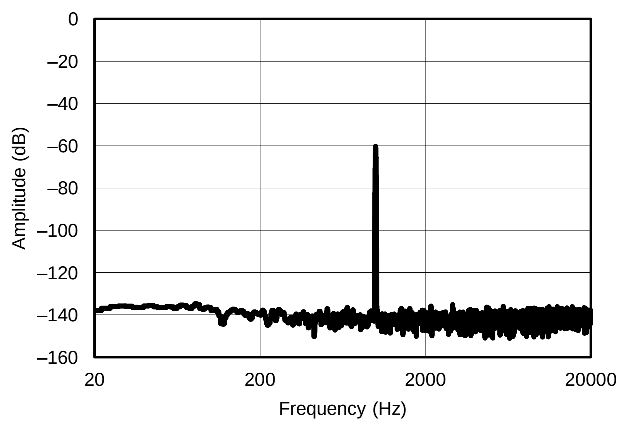


Figure 67. Frequency Response With –60-dB Input at 1 kHz

11 Power Supply Recommendations

11.1 Power-Supply Distribution and Requirements

The PCM186x-Q1 powers the device using the pins shown in Figure 68.

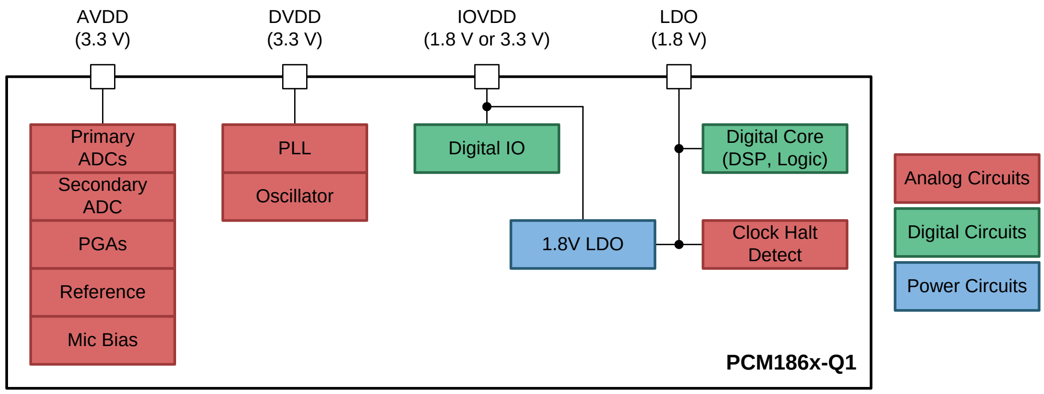


Figure 68. PCM186x-Q1 Power Distribution Tree

The PCM186x-Q1 uses a combination of 3.3-V functional blocks and 1.8-V functional blocks to achieve high analog performance, combined with high levels of digital integration. As such, the device has three internal power rails. AVDD provides the analog circuits with a clean 3.3-V rail. DVDD is used for 3.3-V digital clock circuits. Externally, AVDD and DVDD can be connected together without significant impact to performance. The final rail, IOVDD, is used for driving the input/output digital circuitry.

The PCM186x-Q1 integrates an on-chip LDO to convert an external 3.3 V to the 1.8 V required by the digital core. The LDO input is derived from IOVDD. Power-supply pin descriptions are listed in Table 25.

Table 25. Power-Supply Pin Descriptions

NAME	DESCRIPTION
AVDD	Analog voltage supply (3.3 V) that powers the ADC, PGA, reference, and secondary ADC.
DVDD	Digital voltage supply (3.3 V) that is used for the PLL and the oscillator circuit.
IOVDD	Input/output pin voltage. Also used as a source for the internal LDO for the digital circuit.
LDO	Output from the on-chip LDO that is used with a 0.1-µF decoupling capacitor. Can be driven (used as power input) with a 1.8-V supply to bypass the on-chip LDO for lower power consumption.
AGND	Analog ground
DGND	Digital ground

11.2 1.8-V Support

All PCM186x-Q1 devices can support external devices with a 1.8 V I/O. This operating mode is configured by driving IOVDD and LDO with 1.8 V.

11.3 Brownout Conditions

The PCM186x-Q1 devices do not have a brownout detector, or a reset pin to hold while the system is powering up. Make sure that the system design meets minimum AVDD, DVDD and IOVDD requirements.

11.4 Power-Up Sequence

The power-up sequence consists of the following steps:

1. Power-on reset
   (a) Power up AVDD, DVDD and IOVDD
   (b) Check if LDO is being driven with an external 1.8 V, or is an output. Enable LDO if required.
   (c) Release digital reset
2. Wait until analog voltage reference is stable
3. Configure clock (PLL requires < 250 µs)
4. Fade-in audio ADC content

11.5 Lowest Power-Down Modes

To achieve the lowest levels of power down and sleep current, the following recommended write sequences are suggested on PCM186x-Q1 software-controlled devices:

11.5.1 Lowest Power In Standby Mode (AVDD = DVDD = IOVDD = 3.3 V)

Consumption as low as 0.59 mW

```
0x00=0x00 //select page0
0x70=0x14 //power down reference
0x00=0x03 //select page3
0x12=0x41 //disable OSC
0x00=0x00 //select page0
```

11.5.2 Lowest Power in Sleep or *Energysense* Mode (AVDD = DVDD = IOVDD = 3.3 V)

Consumption as low as 14 mW

Clocks must be running during this process

0x00=0x00 //select page0

0x70=0x72 //enter in sleep mode

0x00=0xfd //select page253

0x14=0x10 //change global bias current

0x00=0x00 //select page0

Now stop the clocks

11.5.3 Lower Power in Sleep or *Energysense* Mode (AVDD = DVDD 3.3 V and IOVDD = 1.8 V)

Consumption as low as 11.15 mW

Clocks must be running during this process

0x00=0x00 //select page0

0x70=0x72 //enter in sleep mode

0x00=0xfd //select page253

0x14=0x10 //change global bias current

0x00=0x00 //select page0

stop the clocks (note: make sure the clock IO is 1.8 V)

11.6 Power-On Reset Sequencing Timing Diagram

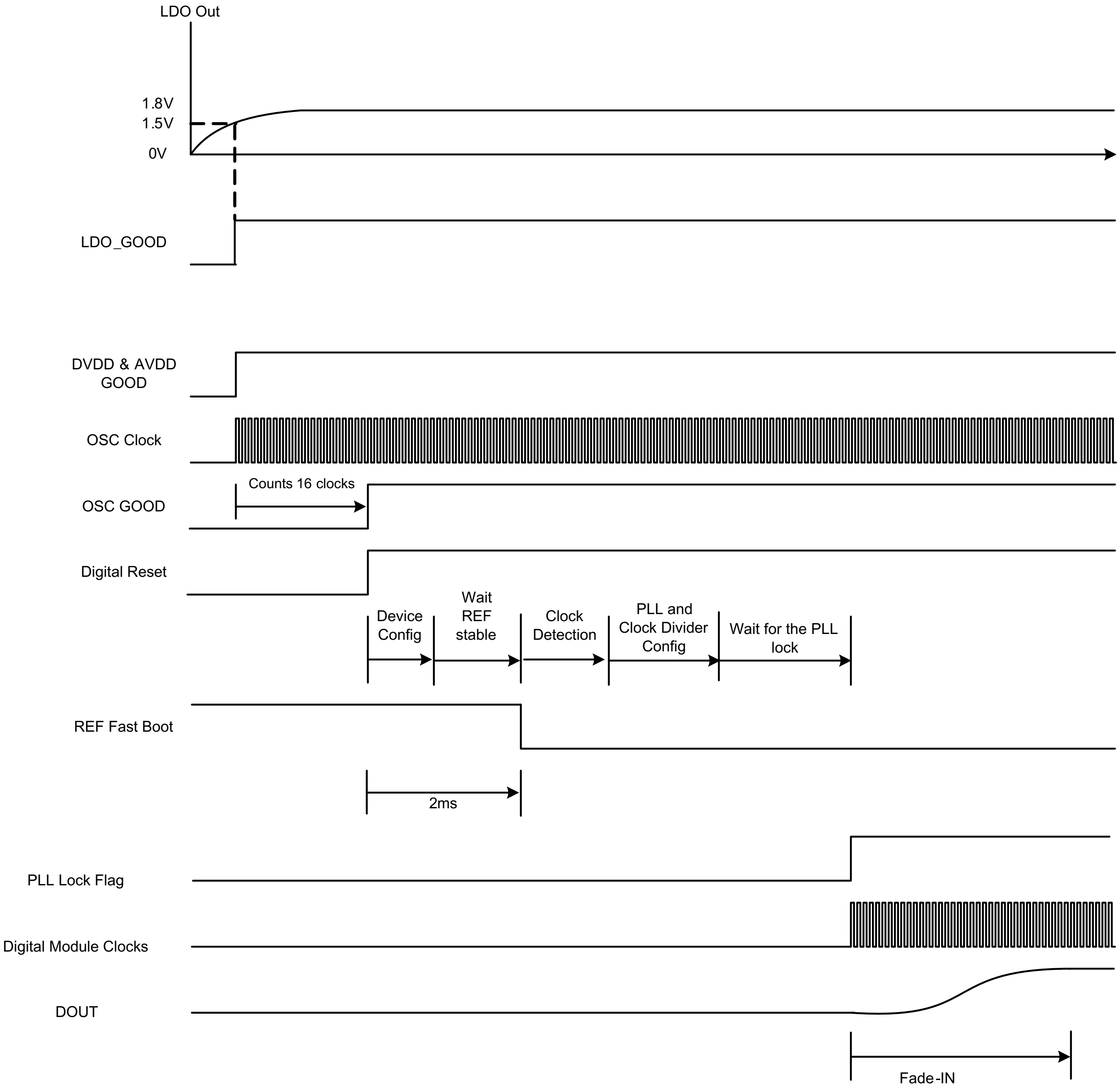


Figure 69. Power-On Reset Timing Diagram

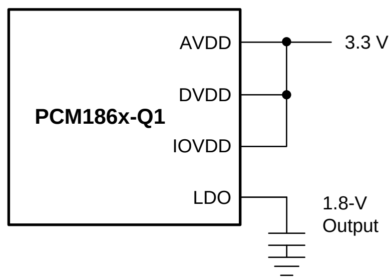
11.7 Power Connection Examples

11.7.1 3.3-V AVDD, DVDD, and IOVDD Example

This example shows the most typical usage. One single supply, shared between all three supply voltage inputs. Rail-connected decoupling capacitors are not shown. Figure 70 shows 3.3-V supply for all supplies. Figure 71 shows separate 3.3 V for AVDD and DVDD.

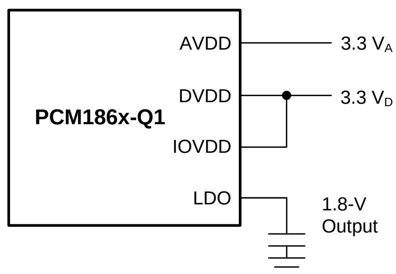
NOTE

There is no disadvantage in separating the AVDD and DVDD, as the device waits until both are present before powering up.



Copyright © 2017, Texas Instruments Incorporated

Figure 70. 3.3 V for All Supplies

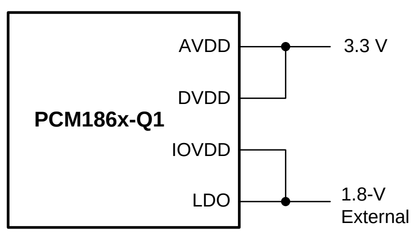


Copyright © 2017, Texas Instruments Incorporated

Figure 71. Separate 3.3 V for AVDD and DVDD

11.7.2 3.3-V AVDD, DVDD With 1.8-V IOVDD Example for Lower-Power Applications

The PCM186x-Q1 also supports interfacing to lower power 1.8-V processors, as shown in Figure 72. In the presence of an external 1.8 V connected to LDO, the internal LDO that takes DVDD (3.3 V) and converts it to the 1.8-V core voltage is bypassed. Under such conditions, IOVDD will then be used as the 1.8-V source for the digital core of the device. In such systems, it is still important to have 3.3 V for DVDD, as specific sections of the digital core in the device run from 3.3 V.



Copyright © 2017, Texas Instruments Incorporated

Figure 72. 1.8-V IOVDD With 3.3 V for AVDD and DVDD

11.8 Fade In

This sequence is the final stage of the power up and is illustrated in Figure 73. After the PLL has locked, the ADC starts running, and the data follows the fade-in sequence according to the following steps:

1. Detect a zero crossing audio input.
2. Increment the volume towards 0 dB with S-shaped volume.
3. Repeat from step 1 until the result is 0 dB. The number of steps from mute to 0 dB is 48 steps.
4. If zero crossing does not occur for 8192 sample times (= time out), change the volume-per-sample time.

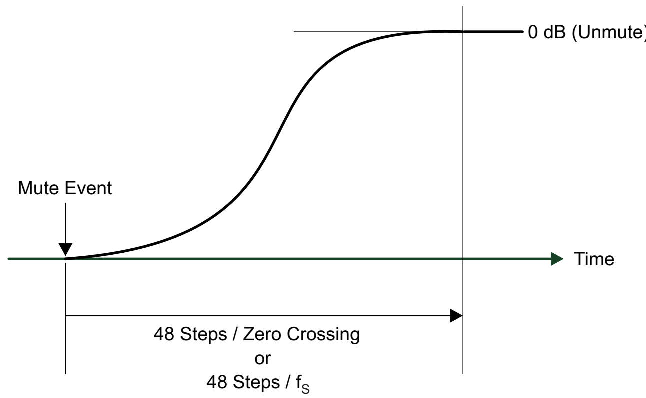


Figure 73. S-Curve Fade-In Behavior

12 Layout

12.1 Layout Guidelines

Employ best design practices when laying out a printed circuit board (PCB) for both analog and digital components. The PCM186x-Q1 audio ADC is a relatively simple device to lay out, even on a two-layer PCB. The following basic recommendations for layout of the PCM186x-Q1 help achieve the best possible performance of the device.

- Separate analog and digital sections where layout permits. Route analog lines away from digital lines. This routing technique prevents digital noise from coupling back into analog signals.
- The bottom copper plane can be a shared ground, whereas a ground plane can be used on the top layer as well. Separated planes for analog and digital grounds are not required to achieve data sheet performance.
- Place decoupling capacitors as close as possible to the supply pins, and in the same layer of the device, to yield the best results. Do not place vias between decoupling capacitors and the device.
- Place ground planes between the input traces to achieve the lowest crosstalk performance.

The EVM user's guide shows the schematics, a bill of material, and a more detailed PCB layout.

12.1.1 Grounding and System Partitioning

Use the same plane for analog and digital grounds to avoid any potential voltage difference between these grounds. On the PCM186x-Q1 EVM, maximum SNR performance is achieved by using a single ground plane, and making sure that the return currents for digital signals are not near the AGND pin or the input signals.

As shown in Figure 74, the pin layout of the PCM186x-Q1 is partitioned into two sections: analog and digital. No digital return currents (for example, clocks) are generated in the analog circuitry, as long as the system is partitioned in such a way that digital signals are routed away from the analog sections.

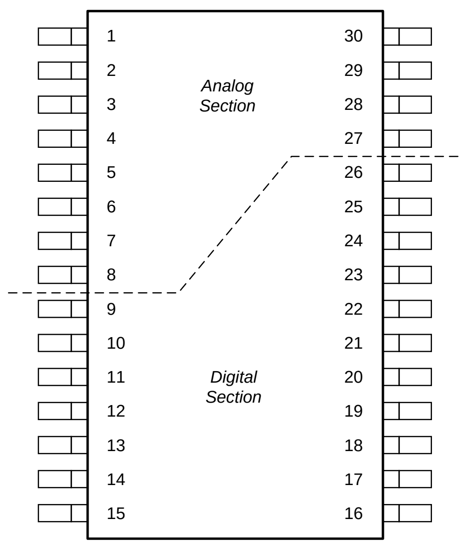


Figure 74. Single Ground With Analog Pins Partitioned to the Top and Digital Pins at the Bottom

12.2 Layout Example

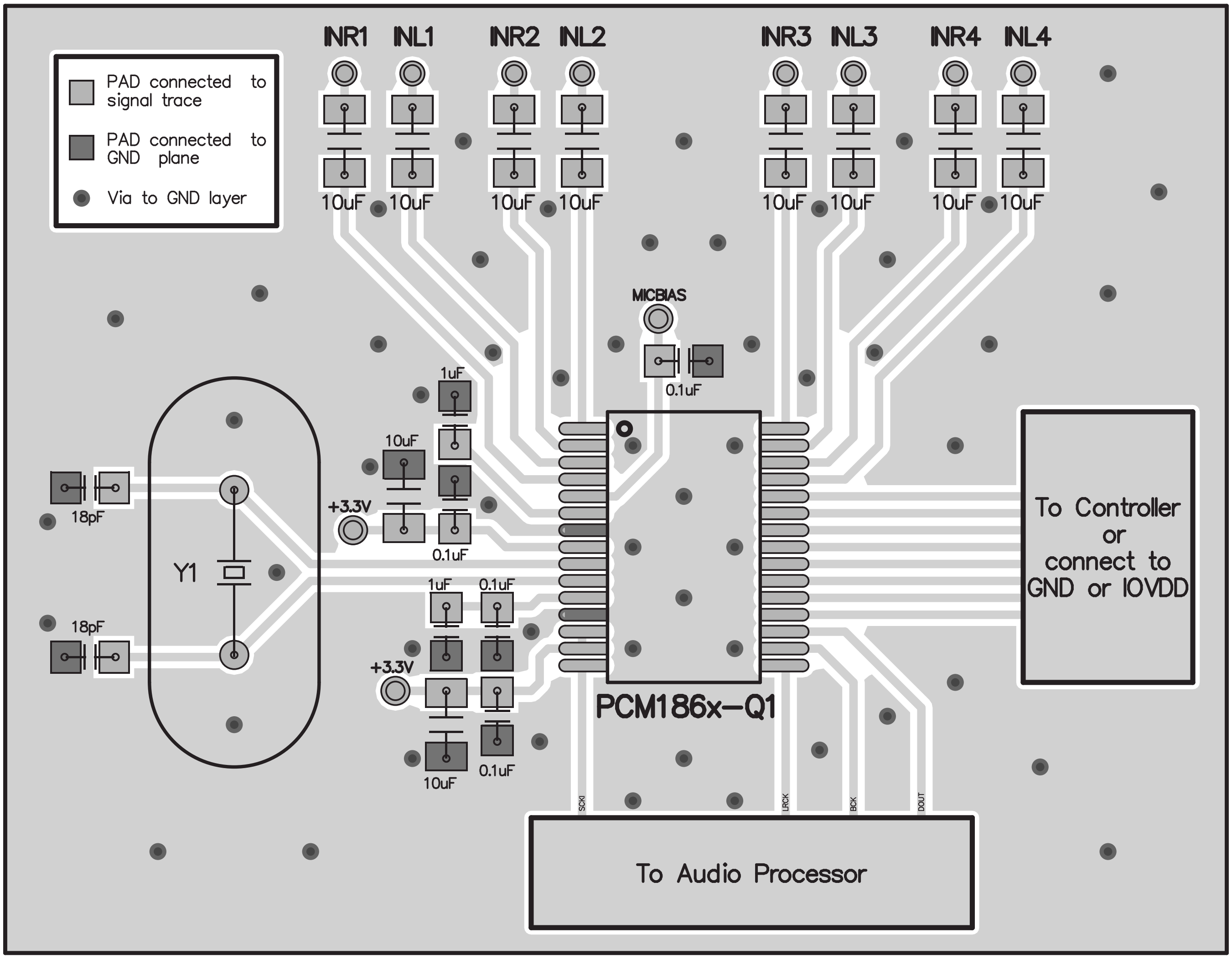


Figure 75. Layout Example

13 Register Map

13.1 Register Map Description

The register map is the primary way to configure the PCM186x-Q1 software-controlled devices. The register map is separated into four pages: 0,1,3, and 253. Page 0 handles all of the device configuration. Page 1 is used to indirectly program coefficients into the two fixed function DSPs on the PCM186x-Q1. Page 3 and page 253 contain additional registers for lower-power use. All undocumented registers are considered reserved; do not write to undocumented registers.

Change pages by writing to register 0x00 with the required page.

Reset registers by writing 0xFE to register 0x00.

13.2 Register Map Summary

Table 26. Register Map Summary

DEC	HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Page 0									
1	0x01	PGA_VAL_CH1_L							
2	0x02	PGA_VAL_CH1_R							
3	0x03	PGA_VAL_CH2_L							
4	0x04	PGA_VAL_CH2_R							
5	0x05	SMOOTH	LINK	DPGA_CLIP_EN	MAX_ATT		START_ATT		AGC_EN
6	0x06	POL	RSV	SEL_L					
7	0x07	POL	RSV	SEL_R					
8	0x08	POL	RSV	SEL_L					
9	0x09	POL	RSV	SEL_R					
10	0x0A	RSV				SEL			
11	0x0B	RX_WLEN		RSV	TDM_LRCK_MODE	TX_WLEN		FMT	
12	0x0C	RSV						TDM_OSEL	
13	0x0D	TX_TDM_OFFSET							
14	0x0E	RX_TDM_OFFSET							
15	0x0F	DPGA_VAL_CH1_L							
16	0x10	GPIO1_POL	GPIO1_FUNC			GPIO0_POL	GPIO0_FUNC		
17	0x11	GPIO3_POL	GPIO3_FUNC			GPIO2_POL	GPIO2_FUNC		
18	0x12	RSV	GPIO1_DIR			RSV	GPIO0_DIR2		
19	0x13	RSV	GPIO3_DIR2			RSV	GPIO2_DIR2		
20	0x14	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT	GPIO0_OUT	GPIO3_IN	GPIO2_IN	GPIO1_IN	GPIO0_IN
21	0x15	PULL_DOWN_DIS[3]	PULL_DOWN_DIS[2]	PULL_DOWN_DIS[1]	PULL_DOWN_DIS[0]	RSV			
22	0x16	DPGA_VAL_CH1_R							
23	0x17	DPGA_VAL_CH2_L							
24	0x18	DPGA_VAL_CH2_R							
25	0x19	DPGA_CH2_R	DPGA_CH2_L	DPGA_CH1_R	DPGA_CH1_L	APGA_CH2_R	APGA_CH2_L	APGA_CH1_R	APGA_CH1_L
26	0x1A	DIGMIC_IN1_SEL		DIGMIC_IN0_SEL		RSV		DIGMIC_4CH	DIGMIC_EN
27	0x1B	RSV						DIN_RESAMP	
32	0x20	SCK_XI_SEL		MST_SCK_SRC	MST_MODE	ADC_CLK_SRC	DSP2_CLK_SRC	DSP1_CLK_SRC	CLKDET_EN
33	0x21	RSV	DIV_NUM						
34	0x22	RSV	DIV_NUM						
35	0x23	RSV	DIV_NUM						
37	0x25	RSV	DIV_NUM						
38	0x26	RSV	DIV_NUM						
39	0x27	DIV_NUM							
40	0x28	RSV			LOCK	RSV		PLL_REF_SEL	PLL_EN
41	0x29	RSV	P						

Table 26. Register Map Summary (continued)

DEC	HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
42	0x2A	RSV				R			
43	0x2B	RSV		J					
44	0x2C	D_LSB							
45	0x2D	RSV		D_MSB					
48	0x30	CH4R	CH4L	CH3R	CH3L	CH2R	CH2L	CH1R	CH1L
49	0x31	CH4R	CH4L	CH3R	CH3L	CH2R	CH2L	CH1R	CH1L
50	0x32	CH4R	CH4L	CH3R	CH3L	CH2R	CH2L	CH1R	CH1L
51	0x33	RSV			TIME				
52	0x34	RSV					TIME		
54	0x36	RSV					INT_INTVL		
64	0x40	REF							
65	0x41	DIFF							
66	0x42	LEVEL							
67	0x43	REF							
68	0x44	DIFF							
69	0x45	LEVEL							
70	0x46	REF							
71	0x47	DIFF							
72	0x48	LEVEL							
73	0x49	REF							
74	0x4A	DIFF							
75	0x4B	LEVEL							
76	0x4C	REF							
77	0x4D	DIFF							
78	0x4E	LEVEL							
79	0x4F	REF							
80	0x50	DIFF							
81	0x51	LEVEL							
82	0x52	REF							
83	0x53	DIFF							
84	0x54	LEVEL							
85	0x55	REF							
86	0x56	DIFF							
87	0x57	LEVEL							
88	0x58	DC_NOLATCH	AUXADC_RDY	DC_RDY	AUXADC_LATCH	AUXADC_DATA_TYPE	DC_CH		
89	0x59	AUXADC_DATA_LSB							
90	0x5A	AUXADC_DATA_MSB							
96	0x60	RSV			POSTPGA_CP	RSV	DC_CHANG	DIN_TOGGLE	ENGSTR
97	0x61	RSV			POSTPGA_CP	RSV	DC_CHANG	DIN_TOGGLE	ENGSTR
98	0x62	RSV		POL1	POL0	RSV		WIDTH	

Table 26. Register Map Summary (continued)

DEC	HEX	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
112	0x70	RSV					PWRDN	SLEEP	STBY
113	0x71	2CH	RSV	FLT	HPF_EN	MUTE_CH2_R	MUTE_CH2_L	MUTE_CH1_R	MUTE_CH1_L
114	0x72	RSV				STATE			
115	0x73	RSV					INFO		
116	0x74	RSV	BCK_RATIO2			RSV	SCK_RATIO2		
117	0x75	RSV	LRCKHLT	BCKHLT	SCKHTL	RSV	LRCKERR	BCKERR	SCKERR
120	0x78	RSV					DVDD	AVDD	LDO
Page 1									
1	0x01	RSV			DONE	RSV	BUSY	R_REQ	W_REQ
2	0x02	RSV	MEM_ADDR						
4	0x04	MEM_WDATA_0							
5	0x05	MEM_WDATA_1							
6	0x06	MEM_WDATA_2							
7	0x07	MEM_WDATA3	RSV						
8	0x08	MEM_RDATA_0							
9	0x09	MEM_RDATA_1							
10	0x0A	MEM_RDATA_2							
11	0x0B	MEM_RDATA_3	RSV						
Page 3									
18	0x12	RSV							PD
21	0x15	RSV							PDZ
Page 253									
20	0x14	PGA_ICI		REF_ICI		RSV			

13.3 Page 0 Registers

13.3.1 Page 0: Register 1 (address = 0x01) [reset = 0x00]

Figure 76. Page 0: Register 1

7	6	5	4	3	2	1	0
PGA_VAL_CH1_L							
R/W-0000 0000b							

Table 27. Page 0: Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA_VAL_CH1_L	R/W	0000 0000b	PGA Value Channel 1 Left Global channel gain for ADC1L. (analog + digital). Analog gain only, if manual gain mapping is enabled. (0x19) Specify two's complement value with 7.1 format. 1110 1000: –12.0 dB (Min) … 1111 1110: –1.0 dB 1111 1111: 0.5 dB 0000 0000: 0.0 dB (default) 0000 0001: 0.5 dB … 0000 0010: 1.0 dB … 0001 1000: 12.0 dB … 0010 1000: 20.0 dB … 0100 0000: 32.0 dB … 0101 0000: 40.0 dB (Max)

13.3.2 Page 0: Register 2 (address = 0x02) [reset = 0x00]

Figure 77. Page 0: Register 2

7	6	5	4	3	2	1	0
PGA_VAL_CH1_R							
R/W-0000 0000b							

Table 28. Page 0: Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA_VAL_CH1_R	R/W	0000 0000b	PGA Value Channel 1 Right Programmable gain value, channel 1 right (see Page 0, 0x01 for complete description)

13.3.3 Page 0: Register 3 (address = 0x03) [reset = 0x00]

Figure 78. Page 0: Register 3

7	6	5	4	3	2	1	0
PGA_VAL_CH2_L							
R/W-0000 0000b							

Table 29. Page 0: Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA_VAL_CH2_L	R/W	0000 0000b	PGA Value Channel 2 Left Programmable gain value, channel 2 left (see Page 0, 0x01 for complete description)

13.3.4 Page 0: Register 4 (address = 0x04) [reset = 0x00]

Figure 79. Page 0: Register 4

7	6	5	4	3	2	1	0
PGA_VAL_CH2_R							
R/W-0000 0000b							

Table 30. Page 0: Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA_VAL_CH2_R	R/W	0000 0000b	PGA Value Channel 2 Right Programmable gain value, channel 2 right (see Page 0, 0x01 for complete description)

13.3.5 Page 0: Register 5 (address = 0x05) [reset = 0x86]

Figure 80. Page 0: Register 5

7	6	5	4	3	2	1	0
SMOOTH	LINK	DPGA_CLIP_EN	MAX_ATT		START_ATT		AGC_EN
R/W-1b	R/W-0b	R/W-0b	R/W-00b		R/W-11b		R/W-0b

Table 31. Page 0: Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
7	SMOOTH	R/W	1b	PGA Control Enable PGA smooth change 0: Immediate change 1: Smooth change (default)
6	LINK	R/W	0b	Link PGA Control 0: Independent control (default) 1: Ch1[R] / Ch2[L] / Ch2[R] follow Ch1[L] PGA value.
5	DPGA_CLIP_EN	R/W	0b	Enable Clipping Detection After Digital PGA 0: Disable (default) 1: Enable
4-3	MAX_ATT	R/W	00b	Attenuation Limit of the Automatic Clipping Suppression 00: –3 dB (default) 01: –4 dB 10: –5 dB 11: –6 dB
2-1	START_ATT	R/W	11b	Start Automatic Clipping Suppression After Clipping is Detected CLIP_NUM Times 00: 80 01: 40 10: 20 11: 10 (default)
0	AGC_EN	R/W	0b	Enable Automatic Clipping Suppression 0: Disable (default) 1: Enable

13.3.6 Page 0: Register 6 (address = 0x06) [reset = 0x41]

Figure 81. Page 0: Register 6

7	6	5	4	3	2	1	0
POL	RSV	SEL_L					
R/W-0b	R/W-1b	R/W-00 0001b					

Table 32. Page 0: Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
7	POL	R/W	0b	Change ADC1_INPUT_SEL_L Signal Polarity 0: Normal (default) 1: Inverted
6	RSV	R/W	1b	Reserved. Always write 1.
5-0	SEL_L	R/W	00 0001b	ADC 1 Input Channel Select (ADC1L) 00 0000: No select 00 0001: VINL1[SE] (default) 00 0010: VINL2[SE] 00 0011: VINL2[SE] + VINL1[SE] 00 0100: VINL3[SE] 00 0101: VINL3[SE] + VINL1[SE] 00 0110: VINL3[SE] + VINL2[SE] 00 0111: VINL3[SE] + VINL2[SE] + VINL1[SE] 00 1000: VINL4[SE] 00 1001: VINL4[SE] + VINL1[SE] 00 1010: VINL4[SE] + VINL2[SE] 00 1011: VINL4[SE] + VINL2[SE] + VINL1[SE] 00 1100: VINL4[SE] + VINL3[SE] 00 1101: VINL4[SE] + VINL3[SE] + VINL1[SE] 00 1110: VINL4[SE] + VINL3[SE] + VINL2[SE] 00 1111: VINL4[SE] + VINL3[SE] + VINL2[SE] + VINL1[SE] 01 0000: {VIN1P, VIN1M}[DIFF] 10 0000: {VIN4P, VIN4M}[DIFF] 11 0000: {VIN1P, VIN1M}[DIFF] + {VIN4P, VIN4M}[DIFF]

13.3.7 Page 0: Register 7 (address = 0x07) [reset = 0x41]

Figure 82. Page 0: Register 7

7	6	5	4	3	2	1	0
POL	RSV	SEL_R					
R/W-0b	R/W-1b	R/W-00 0001b					

Table 33. Page 0: Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
7	POL	R/W	0b	Change ADC1_INPUT_SEL_R Signal Polarity 0: Normal (default) 1: Inverted
6	RSV	R/W	1b	Reserved. Do not access.
5-0	SEL_R	R/W	00 0001b	ADC 1 Input Channel Select (ADC1R) 00 0000: No select 00 0001: VINR1[SE] (default) 00 0010: VINR2[SE] 00 0011: VINR2[SE] + VINR1[SE] 00 0100: VINR3[SE] 00 0101: VINR3[SE] + VINR1[SE] 00 0110: VINR3[SE] + VINR2[SE] 00 0111: VINR3[SE] + VINR2[SE] + VINR1[SE] 00 1000: VINR4[SE] 00 1001: VINR4[SE] + VINR1[SE] 00 1010: VINR4[SE] + VINR2[SE] 00 1011: VINR4[SE] + VINR2[SE] + VINR1[SE] 00 1100: VINR4[SE] + VINR3[SE] 00 1101: VINR4[SE] + VINR3[SE] + VINR1[SE] 00 1110: VINR4[SE] + VINR3[SE] + VINR2[SE] 00 1111: VINR4[SE] + VINR3[SE] + VINR2[SE] + VINR1[SE] 01 0000: {VIN2P, VIN2M}[DIFF] 10 0000: {VIN3P, VIN3M}[DIFF] 11 0000: {VIN2P, VIN2M}[DIFF] + {VIN3P, VIN3M}[DIFF]

13.3.8 Page 0: Register 8 (address = 0x08) [reset = 0x42]

Figure 83. Page 0: Register 8

7	6	5	4	3	2	1	0
POL	RSV	SEL_L					
R/W-0b	R/W-1b	R/W-00 0010b					

Table 34. Page 0: Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
7	POL	R/W	0b	Change ADC2_INPUT_SEL_L Signal Polarity 0: Normal (default) 1: Inverted
6	RSV	R/W	1b	Reserved. Do not access.
5-0	SEL_L	R/W	00 0010b	ADC 2 Input Channel Select (ADC2L) 00 0000: No select 00 0001: VINL1[SE] (default) 00 0010: VINL2[SE] 00 0011: VINL2[SE] + VINL1[SE] 00 0100: VINL3[SE] 00 0101: VINL3[SE] + VINL1[SE] 00 0110: VINL3[SE] + VINL2[SE] 00 0111: VINL3[SE] + VINL2[SE] + VINL1[SE] 00 1000: VINL4[SE] 00 1001: VINL4[SE] + VINL1[SE] 00 1010: VINL4[SE] + VINL2[SE] 00 1011: VINL4[SE] + VINL2[SE] + VINL1[SE] 00 1100: VINL4[SE] + VINL3[SE] 00 1101: VINL4[SE] + VINL3[SE] + VINL1[SE] 00 1110: VINL4[SE] + VINL3[SE] + VINL2[SE] 00 1111: VINL4[SE] + VINL3[SE] + VINL2[SE] + VINL1[SE] 01 0000: {VIN1P, VIN1M}[DIFF] 10 0000: {VIN4P, VIN4M}[DIFF] 11 0000: {VIN1P, VIN1M}[DIFF] + {VIN4P, VIN4M}[DIFF]

13.3.9 Page 0: Register 9 (address = 0x09) [reset = 0x42]

Figure 84. Page 0: Register 9

7	6	5	4	3	2	1	0
POL	RSV	SEL_R					
R/W-0b	R/W-1b	R/W-00 0010b					

Table 35. Page 0: Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
7	POL	R/W	0b	Change ADC2_INPUT_SEL_R Signal Polarity 0: Normal (default) 1: Inverted
6	RSV	R/W	1b	Reserved. Do not access.
5-0	SEL_R	R/W	00 0010b	ADC 2 Input Channel Select (ADC2R) 00 0000: No select 00 0001: VINR1[SE] (default) 00 0010: VINR2[SE] 00 0011: VINR2[SE] + VINR1[SE] 00 0100: VINR3[SE] 00 0101: VINR3[SE] + VINR1[SE] 00 0110: VINR3[SE] + VINR2[SE] 00 0111: VINR3[SE] + VINR2[SE] + VINR1[SE] 00 1000: VINR4[SE] 00 1001: VINR4[SE] + VINR1[SE] 00 1010: VINR4[SE] + VINR2[SE] 00 1011: VINR4[SE] + VINR2[SE] + VINR1[SE] 00 1100: VINR4[SE] + VINR3[SE] 00 1101: VINR4[SE] + VINR3[SE] + VINR1[SE] 00 1110: VINR4[SE] + VINR3[SE] + VINR2[SE] 00 1111: VINR4[SE] + VINR3[SE] + VINR2[SE] + VINR1[SE] 01 0000: {VIN2P, VIN2M}[DIFF] 10 0000: {VIN3P, VIN3M}[DIFF] 11 0000: {VIN2P, VIN2M}[DIFF] + {VIN3P, VIN3M}[DIFF]

13.3.10 Page 0: Register 10 (address = 0x0A) [reset = 0x00]

Figure 85. Page 0: Register 10

7	6	5	4	3	2	1	0
RSV				SEL3			
R/W-0000b				R/W-0000b			

Table 36. Page 0: Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSV	R/W	0000b	Reserved. Do not access.
3-0	SEL	R/W	0000b	Secondary ADC Input Channel Do not select the same channel that is already in use by an audio ADC 0: No Select (default) 1: ch1(L) 2: ch1(R) 3: ch2(L) 4: ch2(R) 5: ch3(L) 6: ch3(R) 7: ch4(L) 8: ch4(R)

13.3.11 Page 0: Register 11 (address = 0x0B) [reset = 0x44]

Figure 86. Page 0: Register 11

7	6	5	4	3	2	1	0
RX_WLEN		RSV	TDM_LRCK_MODE	TX_WLEN		FMT	
R/W-01b		R/W-0	R/W-0b	R/W-01b		R/W-00b	

Table 37. Page 0: Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RX_WLEN	R/W	01b	Receive PCM Word Length 00: 32-bit 01: 24-bit (default) 10: 20-bit 11: 16-bit
5	RSV	R/W	0b	Reserved. Do not access.
4	TDM_LRCK_MODE	R/W	0b	LRCK Duty Cycle in TDM Mode TDM format can support 2 channels, 4 channels, or 6 channels with one device. When BCK to LRCK ratio is 256, FMT must be configured as TDM format. Configure the duty cycle of LRCK when I^2S is configured as TDM mode 0: duty cycle of LRCK is 50% (default) 1: duty cycle of LRCK is 1/256 (similar DSP mode)
3-2	TX_WLEN	R/W	01b	Stereo PCM Word Length 00: 32-bit 01: 24-bit (default) 10: 20-bit 11: 16-bit
1-0	FMT	R/W	00b	Serial Audio Interface Format (TDM/DSP Mode) 0: I^2S (default) 1: Left justified 2: Right justified 3: TDM/DSP (256f_S BCK is required)

13.3.12 Page 0: Register 12 (address = 0x0C) [reset = 0x00]

Figure 87. Page 0: Register 12

7	6	5	4	3	2	1	0
RSV						TDM_OSEL	
R/W-000000b						R/W-00b	

Table 38. Page 0: Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RSV	R/W	000000b	Reserved. Do not access.
1-0	TDM_OSEL	R/W	00b	Select TDM Transmission Data Ch2 data only available on 4-channel device. 00: 2ch TDM (default) DOUT1: ch1[L], ch1[R] DOUT2: ch2[L], ch2[R] 01: 4ch TDM DOUT1: ch1[L], ch1[R], ch2[L], ch2[R] DOUT2: ch1[L], ch1[R], ch2[L], ch2[R] 10: 6ch TDM DOUT1: ch1[L], ch1[R], ch2[L], ch2[R], sec_ADC_LPF, sec_ADC_HPF DOUT2: ch1[L], ch1[R], ch2[L], ch2[R], sec_ADC_LPF, sec_ADC_HPF 11: RESERVED

13.3.13 Page 0: Register 13 (address = 0x0D) [reset = 0x00]

Figure 88. Page 0: Register 13

7	6	5	4	3	2	1	0
TX_TDM_OFFSET							
R/W-0000 0000b							

Table 39. Page 0: Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_TDM_OFFSET	R/W	0000 0000b	Set Offset Position in Serial Audio Data Frame This setting is enabled when 0x0B FMT[1:0] is set to DSP format. 0: 0 (default) 1: 1 BCK (same as I^2S) 2: 2 BCK 3: 3 BCK : 255: 255 BCK

13.3.14 Page 0: Register 14 (address = 0x0E) [reset = 0x00]

Figure 89. Page 0: Register 14

7	6	5	4	3	2	1	0
RX_TDM_OFFSET							
R/W-0000 0000b							

Table 40. Page 0: Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_TDM_OFFSET	R/W	0000 0000b	Set Offset Position in a Serial Audio Data Frame This setting is enabled when I2S_RX_FMT is set to DSP format. Offset position in a serial audio data frame. 0: 0 (default) 1: 1 BCK (same as I^2S, only if LRCK is configured as 50% duty cycle) 2: 2 BCK 3: 3 BCK : 255: 255 BCK

13.3.15 Page 0: Register 15 (address = 0x0F) [reset = 0x00]

Figure 90. Page 0: Register 15

7	6	5	4	3	2	1	0
DPGA_VAL_CH1_L							
R/W-0000 0000b							

Table 41. Page 0: Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPGA_VAL_CH1_L	R/W	0000 0000b	Gain Setting for Digital PGA Channel 1 Left 4-channel PCM186x-Q1 only when is used in following scenarios: i. Analog PGA gain and digital PGA are set separately. ii. Digital microphone Interface is used (when manual gain mapping is enabled in register 0x19). Specify two's complement value with 7.1 format. 0x28 to 0x3F in 0.5-dB steps Others: Reserved

13.3.16 Page 0: Register 16 (address = 0x10) [reset = 0x01]

Figure 91. Page 0: Register 16

7	6	5	4	3	2	1	0
GPIO1_POL	GPIO1_FUNC			GPIO0_POL	GPIO0_FUNC		
R/W-0b	R/W-000b			R/W-0b	R/W-001b		

Table 42. Page 0: Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_POL	R/W	0b	GPIO1 Polarity Control 0: Normal (default) 1: Invert
6-4	GPIO1_FUNC	R/W	000b	Function select, GPIO1 000: GPIO1(default) 001: Digital mic input 1(In) 010: INT 011: Internal SCK (Out) 100: Digital mute (In) 101: DOUT2 (Out) 110: DIN (In) 111: Reserved
3	GPIO0_POL	R/W	0b	GPIO0 Polarity Control 0: Normal (default) 1: Invert
2-0	GPIO0_FUNC	R/W	001b	Function select, GPIO0 000: GPIO0 001: Digital mic input 0 (In, default) 010: SPI MISO (Ou) 011: Internal SCK (Out) 100: Digital mute (In) 101: DOUT2 (Out) 110: DIN (In) 111: Reserved

13.3.17 Page 0: Register 17 (address = 0x11) [reset = 0x20]

Figure 92. Page 0: Register 17

7	6	5	4	3	2	1	0
GPIO3_POL	GPIO3_FUNC			GPIO2_POL	GPIO2_FUNC		
R/W-0b	R/W-010b			R/W-0b	R/W-000b		

Table 43. Page 0: Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO3_POL	R/W	0b	GPIO3 Polarity Control 0: Normal (default) 1: Invert
6-4	GPIO3_FUNC	R/W	010b	Function select, GPIO1 000: GPIO3 001: Reserved 010: INT (default) 011: Internal SCK (Out) 100: Digital mute (In) 101: DOUT2 (Out) 110: DIN (In) 111: Reserved
3	GPIO2_POL	R/W	0b	GPIO2 Polarity Control 0: Normal (default) 1: Invert
2-0	GPIO2_FUNC	R/W	000b	Function select, GPIO2 000: GPIO2 (default) 001: Digital mic clock output 0 (Out) 010: INT 011: Internal SCK (Out) 100: Digital mute (In) 101: DOUT2 (Out) 110: DIN (In) 111: Reserved

13.3.18 Page 0: Register 18 (address = 0x12) [reset = 0x00]

Figure 93. Page 0: Register 18

7	6	5	4	3	2	1	0
RSV	GPIO1_DIR			RSV	GPIO0_DIR		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 44. Page 0: Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Do not access.
6-4	GPIO1_DIR	R/W	000b	Direction Control of GPIO1 When Configured as GPIO Function 000: Input (default) 001: Input with *sticky* bit 010: Input with toggle detection 011: Raw input (not deglictched) 100: Output 101: Open drain 110: Reserved 111: Reserved
3	RSV	R/W	0b	Reserved. Do not access.
2-0	GPIO0_DIR	R/W	000b	Direction Control of GPIO0 When Configured as GPIO Function 000: Input (default) 001: Input with *sticky* bit 010: Input with toggle detection 011: Raw input (not deglictched) 100: Output 101: Open drain 110: Reserved 111: Reserved

13.3.19 Page 0: Register 19 (address = 0x13) [reset = 0x00]

Figure 94. Page 0: Register 19

7	6	5	4	3	2	1	0
RSV	GPIO3_DIR			RSV	GPIO2_DIR		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 45. Page 0: Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Do not access.
6-4	GPIO3_DIR	R/W	000b	Direction Control of GPIO3 When Configured as GPIO Function 000: Input (default) 001: Input with *sticky* bit 010: Input with toggle detection 011: Raw input (not deglictched) 100: Output 101: Open drain 110: Reserved 111: Reserved
3	RSV	R/W	0b	Reserved. Do not access.
2-0	GPIO2_DIR	R/W	000b	Direction Control of GPIO2 When Configured as GPIO Function 000: Input (default) 001: Input with *sticky* bit 010: Input with toggle detection 011: Raw input (not deglictched) 100: Output 101: Open drain 110: Reserved 111: Reserved

13.3.20 Page 0: Register 20 (address = 0x14) [reset = 0x00]

Figure 95. Page 0: Register 20

7	6	5	4	3	2	1	0
GPIO3_OUT	GPIO2_OUT	GPIO1_OUT	GPIO0_OUT	GPIO3_IN	GPIO2_IN	GPIO1_IN	GPIO0_IN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R-0b	R-0b	R-0b

Table 46. Page 0: Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO3_OUT	R/W	0b	GPIO3 Output Status
6	GPIO2_OUT	R/W	0b	GPIO2 Output Status
5	GPIO1_OUT	R/W	0b	GPIO1Output Status
4	GPIO0_OUT	R/W	0b	GPIO0 Output Status
3	GPIO3_IN	R/W	0b	GPIO3 Input Status or Toggle Status The sticky flag is cleared when this register is read.
2	GPIO2_IN	R/W	0b	GPIO2 Input Status or Toggle Status The sticky flag is cleared when this register is read.
1	GPIO1_IN	R/W	0b	GPIO1 Input Status or Toggle Status The sticky flag is cleared when this register is read.
0	GPIO0_IN	R/W	0b	GPIO0 Input Status or Toggle Status The sticky flag is cleared when this register is read.

13.3.21 Page 0: Register 21 (address = 0x15) [reset = 0x00]

Figure 96. Page 0: Register 21

7	6	5	4	3	2	1	0
PULL_DOWN_DIS[3]	PULL_DOWN_DIS[2]	PULL_DOWN_DIS[1]	PULL_DOWN_DIS[0]	RSV			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0000b			

Table 47. Page 0: Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
7	PULL_DOWN_DIS[3]	R/W	0b	Enable or Disable the Pull-Down Resistor of GPIO3 0: Enable the pull down of GPIO3, IntC (pin 19) 1: Disable the pull down
6	PULL_DOWN_DIS[2]	R/W	0b	Enable or Disable the Pull-Down Resistor of GPIO2 0: Enable the pull down of GPIO2, IntB (pin 20)
5	PULL_DOWN_DIS[1]	R/W	0b	Enable or Disable the Pull-Down Resistor of GPIO1 0: Enable the pull down of GPIO1 (pin 21) 1: Disable the pull down
4	PULL_DOWN_DIS[0]	R/W	0b	Enable or Disable the Pull-Down Resistor of GPIO0 0: Enable the pull down of GPIO0 (pin 22) 1: Disable the pull down
3-0	RSV	R/W	0b	Reserved. Do not access.

13.3.22 Page 0: Register 22 (address = 0x16) [reset = 0x00]

Figure 97. Page 0: Register 22

7	6	5	4	3	2	1	0
DPGA_VAL_CH1_R							
R/W-0000 0000b							

Table 48. Page 0: Register 22 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPGA_VAL_CH1_R	R/W	0000 0000b	Gain Setting for Digital PGA Channel 1 Right 4-channel PCM186x-Q1 only when is used in following scenarios: i. Analog PGA gain and digital PGA are set separately ii. Digital microphone Interface is used (\when manual gain mapping is enabled in register 0x19) Specify two's complement value with 7.1 format. 0010 1000: 0.0 dB 0010 1001: 0.5 dB 0010 1010: 1.0 dB 0010 1011: 1.5 dB : 0011 1111: 7.5 dB (max) Others: Reserved

13.3.23 Page 0: Register 23 (address = 0x17) [reset = 0x00]

Figure 98. Page 0: Register 23

7	6	5	4	3	2	1	0
DPGA_VAL_CH2_L							
R/W-0000 0000b							

Table 49. Page 0: Register 23 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPGA_VAL_CH2_L	R/W	0000 0000b	Gain Setting for Digital PGA Channel 2 Left 4-channel PCM186x-Q1 only. See Page 0, Reg 0x16 description

13.3.24 Page 0: Register 24 (address = 0x18) [reset = 0x00]

Figure 99. Page 0: Register 24

7	6	5	4	3	2	1	0
DPGA_VAL_CH2_R							
R/W-0000 0000b							

Table 50. Page 0: Register 24 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPGA_VAL_CH2_R	R/W	0000 0000b	Gain Setting for Digital PGA channel 2 Right 4-channel PCM186x-Q1 only. See Page 0, Reg 0x16 description

13.3.25 Page 0: Register 25 (address = 0x19) [reset = 0x00]

Figure 100. Page 0: Register 25

7	6	5	4	3	2	1	0
DPGA_CH2_R	DPGA_CH2_L	DPGA_CH1_R	DPGA_CH1_L	APGA_CH2_R	APGA_CH2_L	APGA_CH1_R	APGA_CH1_L
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 51. Page 0: Register 25 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPGA_CH2_R	R/W	0b	DPGA Control Mapping (4-channel PCM186x-Q1 only) CH2_R channel (Note: Using manual gain mapping in the 2-channel device sets the digital gain to 0dB.) 0: Auto gain mapping (default) 1: Manual gain mapping
6	DPGA_CH2_L	R/W	0b	DPGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for digital PGA of CH2_L channel 0: Auto gain mapping (default) 1: Manual gain mapping
5	DPGA_CH1_R	R/W	0b	DPGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for digital PGA of CH1_R channel 0: Auto gain mapping (default) 1: Manual gain mapping
4	DPGA_CH1_L	R/W	0b	DPGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for digital PGA of CH1_L channel 0: Auto gain mapping (default) 1: Manual gain mapping
3	APGA_CH2_R	R/W	0b	APGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for analog PGA of CH2_R channel 0: Auto gain mapping (default) 1: Manual gain mapping
2	APGA_CH2_L	R/W	0b	APGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for analog PGA of CH2_L channel 0: Auto gain mapping (default) 1: Manual gain mapping
1	APGA_CH1_R	R/W	0b	APGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for analog PGA of CH1_R channel 0: Auto gain mapping (default) 1: Manual gain mapping
0	APGA_CH1_L	R/W	0b	APGA Control Mapping (4-channel PCM186x-Q1 only) Gain control mode for analogPGA of CH1_L channel 0: Auto gain mapping (default) 1: Manual gain mapping

13.3.26 Page 0: Register 26 (address = 0x1A) [reset = 0x00]

Figure 101. Page 0: Register 26

7	6	5	4	3	2	1	0
DIGMIC_IN1_SEL		DIGMIC_IN0_SEL		RSV		DIGMIC_4CH	DIGMIC_EN
R/W-00b		R/W-00b		R/W-00b		R/W-0b	R/W-0b

Table 52. Page 0: Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIGMIC_IN1_SEL	R/W	00b	Digital Mic Data Input Selection for MIC1 Interface (4-channel devices only) 00: GPIO0 (default) 01: GPIO1 10: Invalid 11: Invalid
5-4	DIGMIC_IN0_SEL	R/W	00b	Digital Mic Data Input Selection for MIC0 Interface 00: GPIO0 (default) 01: GPIO1 10: Invalid 11: Invalid
3-2	RSV	R/W	00b	Reserved. Do not access.
1	DIGMIC_4CH	R/W	0b	Second Pair of Filters Selection for Digital Microphone as Signal Processing (4-channel device only) 0: configured for analog ADC signal processing (default) 1: configured for digital MIC signal processing
0	DIGMIC_EN	R/W	0b	First Pair of Filters Selection for Digital Microphone as Signal Processing 0: configured as analog ADC signal processing (default) 1: configured as digital MIC signal processing

13.3.27 Page 0: Register 27 (address = 0x1B) [reset = 0x00]

Figure 102. Page 0: Register 27

7	6	5	4	3	2	1	0
RSV						DIN_RESAMP	
R/W-00 0000b						R/W-00b	

Table 53. Page 0: Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RSV	R/W	00 0000b	Reserved. Do not access.
1-0	DIN_RESAMP	R/W	00b	Resample DIN with Internal BCK to Avoid Internal Timing Issue 00: No resample (default) 01: resample DIN with rising edge of BCK 10: resample DIN with falling edge of BCK 11: Not supported

13.3.28 Page 0: Register 32 (address = 0x20) [reset = 0x01]

Figure 103. Page 0: Register 32

7	6	5	4	3	2	1	0
SCK_XI_SEL		MST_SCK_SRC	MST_MODE	ADC_CLK_SRC	DSP2_CLK_SRC	DSP1_CLK_SRC	CLKDET_EN
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b

Table 54. Page 0: Register 32 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SCK_XI_SEL	R/W	00b	SCK or XTAL Selection 00: SCK or XTAL (default) 01: SCK 10: XTAL 11: Reserved
5	MST_SCK_SRC	R/W	0b	Master-Mode SCK Source Selection 0: SCK or XI (default) 1: PLL (as in BCK PLL mode)
4	MST_MODE	R/W	0b	Master or Slave Selection 0: Slave (default) 1: Master
3	ADC_CLK_SRC	R/W	0b	ADC Clock Source Selection (ignored if CLKDET_EN = 1) 0: SCK (default) 1: PLL
2	DSP2_CLK_SRC	R/W	0b	DSP2 Clock Source Selection (ignored if CLKDET_EN = 1) 0: SCK (default) 1: PLL
1	DSP1_CLK_SRC	R/W	0b	DSP1 Clock Source Selection (ignored if CLKDET_EN = 1) 0: SCK (default) 1: PLL
0	CLKDET_EN	R/W	1b	Enable Auto Clock Detector Configuration 0: Disable 1: Enable (default)

13.3.29 Page 0: Register 33 (address = 0x21) [reset = 0x00]

Figure 104. Page 0: Register 33

7	6	5	4	3	2	1	0
RSV	DIV_NUM						
R/W-0b	R/W-000 0000b						

Table 55. Page 0: Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Do not access.
6-0	DIV_NUM	R/W	000 0000b	Set DSP1 Clock Divider Value Ignored if CLKDET_EN = 1 0: 1 (default) 1: 1/2 2: 1/3 3: 1/4 : 127: 1/128

13.3.30 Page 0: Register 34 (address = 0x22) [reset = 0x01]

Figure 105. Page 0: Register 34

7	6	5	4	3	2	1	0
RSV	DIV_NUM						
R/W-0b	R/W-000 0001b						

Table 56. Page 0: Register 34 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Do not access.
6-0	DIV_NUM	R/W	000 0001b	Set DSP2 Clock Divider Value Ignored if CLKDET_EN = 1 0: 1 1: 1/2 (default) 2: 1/3 3: 1/4 : 127: 1/128

13.3.31 Page 0: Register 35 (address = 0x23) [reset = 0x03]

Figure 106. Page 0: Register 35

7	6	5	4	3	2	1	0
RSV	DIV_NUM						
R/W-0b	R/W-000 0011b						

Table 57. Page 0: Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0	Reserved. Do not access.
6-0	DIV_NUM	R/W	000 0011b	Set ADC Clock Divider Value Ignored if CLKDET_EN = 1 0: 1 1: 1/2 2: 1/3 3: 1/4 (default) : 127: 1/128

13.3.32 Page 0: Register 37 (address = 0x25) [reset = 0x07]

CLK_DIV_PLL_SCK is the alternate name for this register.

Figure 107. Page 0: Register 37

7	6	5	4	3	2	1	0
RSV	DIVNUM						
R/W-0b	R/W-000 0111b						

Table 58. Page 0: Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0	Reserved. Do not access.
6-0	DIV_NUM	R/W	000 0111b	Set PLL SCK Clock Output Divider for SCK Out (when enabled) Used in BCK slave mode or master mode where PLL-ed SCK Out is required. Requires MST_SCK_SRC (0x20) to be enabled. Divider value: 0: 1 1: 1/2 2: 1/3 3: 1/4 : 7: 1/8 (default) : 127: 1/128

13.3.33 Page 0: Register 38 (address = 0x26) [reset = 0x03]

CLK_DIV_SCK_BCK is the alternate name for this register.

Figure 108. Page 0: Register 38

7	6	5	4	3	2	1	0
RSV	DIVNUM						
R/W-0b	R/W-000 0011b						

Table 59. Page 0: Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0	Reserved. Do not access.
6-0	DIV_NUM	R/W	000 0011b	Set Master Clock (SCK) to BCK Divider Value Ratio of master clock (SCK) to bit clock (BCK) in master mode Divider value: 0: 1 1: 1/2 2: 1/3 3: 1/4 (default) : 7: 1/8 : 127: 1/128

13.3.34 Page 0: Register 39 (address = 0x27) [reset = 0x3F]

CLK_DIV_BCK_LRCK is the alternate name for this register.

Figure 109. Page 0: Register 39

7	6	5	4	3	2	1	0
DIV_NUM							
R/W-0011 1111b							

Table 60. Page 0: Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIV_NUM	R/W	0011 1111b	Set the Master SCK Clock Value SCK to LRCK ratio in master mode Divider value: 0: 1 1: 1/2 2: 1/3 3: 1/4 : 63: 1/64 (default) : 127: 1/128 : 255: 1/256

13.3.35 Page 0: Register 40 (address = 0x28) [reset = 0x01]

Figure 110. Page 0: Register 40

7	6	5	4	3	2	1	0
RSV			LOCK	RSV		PLL_REF_SEL	PLL_EN
R/W-000b			R/W-0b	R/W-00b		R/W-0b	R/W-1b

Table 61. Page 0: Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R/W	000b	Reserved. Do not access.
4	LOCK	R/W	0b	PLL Lock Status 0: Not locked (default) 1: Locked
3-2	RSV	R/W	00b	Reserved. Do not access.
1	PLL_REF_SEL	R/W	0b	PLL Reference Clock Selection Ignored if CLKDET_EN = 1 0: SCK (default) 1: BCK
0	PLL_EN	R/W	1b	PLL Enable Ignored if CLKDET_EN = 1 0: Disable 1: Enable (default)

13.3.36 Page 0: Register 41 (address = 0x29) [reset = 0x00]

Figure 111. Page 0: Register 41

7	6	5	4	3	2	1	0
RSV	P						
R/W-0b	R/W-000 0000b						

Table 62. Page 0: Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Do not access.
6-0		R/W	000 0000b	PLL P Divider Value Ignored if CLKDET_EN = 1 0: 1 (default) 1: 1/2 2: 1/3 3: 1/4 : 127: 1/128

13.3.37 Page 0: Register 42 (address = 0x2A) [reset = 0x00]

Figure 112. Page 0: Register 42

7	6	5	4	3	2	1	0
RSV				R			
R/W-0000b				R/W-0000b			

Table 63. Page 0: Register 42 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSV	R/W	0000b	Reserved. Do not access.
3-0	R	R/W	0000b	PLL R Multiplier Value Ignored if CLKDET_EN = 1 0: 1 (default) 1: 2 2: 3 3: 4 : 15 16

13.3.38 Page 0: Register 43 (address = 0x2B) [reset = 0x01]

Figure 113. Page 0: Register 43

7	6	5	4	3	2	1	0
RSV	J						
R/W-0b	R/W-000 0001b						

Table 64. Page 0: Register 43 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Do not access.
6-0	J	R/W	000 0001b	Integer Part of PLL J.D Multiplier Value Ignored if CLKDET_EN = 1 0: (Prohibit) 1: 1 (default) 2: 2 : 63: 63

13.3.39 Page 0: Register 44 (address = 0x2C) [reset = 0x00]

Figure 114. Page 0: Register 44

7	6	5	4	3	2	1	0
D_LSB							
R/W-0000 0000b							

Table 65. Page 0: Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	D_LSB	R/W	0000 0000b	Fractional Part of PLL J.D-Multiplier Value (least significant bits) Ignored if CLKDET_EN = 1 0: 0 (default) 1: 1 2: 2 : 9999: 9999 (0x270F for both registers combined)

13.3.40 Page 0: Register 45 (address = 0x2D) [reset = 0x00]

Figure 115. Page 0: Register 45

7	6	5	4	3	2	1	0
RSV		D_MSB					
R/W-00b		R/W-00 0000b					

Table 66. Page 0: Register 45 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSV	R/W	00b	Reserved. Do not access.
5-0	D_MSB	R/W	00 0000b	Fractional Part of PLL J.D Multiplier Value. (most significant bits, [13:8]) Ignored if CLKDET_EN = 1 0: 0 (default) 1: 1 2: 2 : 9999: 9999 (0x270F for both registers combined)

13.3.41 Page 0: Register 48 (address = 0x30) [reset = 0x00]

SIGDET_CH_MODE is the alternate name for this register.

Figure 116. Page 0: Register 48

7	6	5	4	3	2	1	0
CH4R	CH4L	CH3R	CH3L	CH2R	CH2L	CH1R	CH1L
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 67. Page 0: Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4R	R/W	0b	Signal Detection Mode for Channel 4 Right Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
6	CH4L	R/W	0b	Signal Detection Mode for Channel 4 Left Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
5	CH3R	R/W	0b	Signal Detection Mode for Channel 3 Right Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
4	CH3L	R/W	0b	Signal Detection Mode for Channel 3 Left Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
3	CH2R	R/W	0b	Signal Detection Mode for Channel 2 Right Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
2	CH2L	R/W	0b	Signal Detection Mode for Channel 2 Left Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
1	CH1R	R/W	0b	Signal Detection Mode for Channel 1 Right Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection
0	CH1L	R/W	0b	Signal Detection Mode for Channel 1 Left Select the signal detection mode for each channel in SLEEP mode 0: Audio signal detection (default) 1: DC level-change detection

13.3.42 Page 0: Register 49 (address = 0x31) [reset = 0x00]

SIGDET_TRIG_MASK is the alternate name for this register.

Figure 117. Page 0: Register 49

7	6	5	4	3	2	1	0
CH4R	CH4L	CH3R	CH3L	CH2R	CH2L	CH1R	CH1L
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 68. Page 0: Register 49 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4R	R/W	0b	Mask Bits of Interrupt Trigger for Channel 4 Right All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
6	CH4L	R/W	0b	Mask Bits of Interrupt Trigger for Channel 4 Left All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
5	CH3R	R/W	0b	Mask Bits of Interrupt Trigger for Channel 3 Right All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
4	CH3L	R/W	0b	Mask Bits of Interrupt Trigger for Channel 3 Left All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
3	CH2R	R/W	0b	Mask Bits of Interrupt Trigger for Channel 2 Right All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
2	CH2L	R/W	0b	Mask Bits of Interrupt Trigger for Channel 2 Left All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
1	CH1R	R/W	0b	Mask Bits of Interrupt Trigger for Channel 1 Right All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask
0	CH1L	R/W	0b	Mask Bits of Interrupt Trigger for Channel 1 Left All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register 0: No mask (default) 1: Mask

13.3.43 Page 0: Register 50 (address = 0x32) [reset = 0x00]

SIGDET_STAT is the alternate name for this register.

Figure 118. Page 0: Register 50

7	6	5	4	3	2	1	0
CH4R	CH4L	CH3R	CH3L	CH2R	CH2L	CH1R	CH1L
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 69. Page 0: Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4R	R/W	0b	Status of Signal Level Detection in Both *Energysense* and *Controlsense* Modes (read only). *Field* column indicates respective channel. A) In audio signal detection mode: a) In the active or run state: 0: Signal active 1: Signal lost b) In the sleep mode 0: Signal lost 1: Signal active In automatic clipping suppression mode: 0: No change 1: changed DC level
6	CH4L	R/W	0b	
5	CH3R	R/W	0b	
4	CH3L	R/W	0b	
3	CH2R	R/W	0b	
2	CH2L	R/W	0b	
1	CH1R	R/W	0b	
0	CH1L	R/W	0b	

13.3.44 Page 0: Register 51 (address = 0x33) [reset = 0x00]

SIGDET_LOSS_TIME is the alternate name for this register.

Figure 119. Page 0: Register 51

7	6	5	4	3	2	1	0
RSV			TIME				
R/W-000b			R/W-0 0001b				

Table 70. Page 0: Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R/W	000	Reserved. Do not access.
4-0	TIME	R/W	0 0001b	If the signal drops below the threshold on the current audio input for this set amount of time, the device generates an interrupt 0: Prohibit 1: 1 minute (default) 2: 2 minutes 3: 3 minutes : 30: 30 minutes (Max)

13.3.45 Page 0: Register 52 (address = 0x34) [reset = 0x00]

SIGDET_SCAN_TIME is the alternate name for this register.

Figure 120. Page 0: Register 52

7	6	5	4	3	2	1	0
RSV					TIME		
R/W-0 0000b					R/W-000b		

Table 71. Page 0: Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
7-33	RSV	R/W	0 0000	Reserved. Do not access.
2-1	TIME	R/W	000	Configures the scan time for each channel in the SLEEP state 000: 160 ms (default) 001: 80 ms 010: 40 ms 011: 20 ms 100: 10 ms Others: Invalid

13.3.46 Page 0: Register 54 (address = 0x36) [reset = 0x01]

SIGDET_INT_INTVL is the alternate for this register.

Figure 121. Page 0: Register 54

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	INT_INTVL		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b

Table 72. Page 0: Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RSV	R/W	0 0000	Reserved. Do not access.
2-0	INT_INTVL	R/W	001b	Interval time of the signal detector interrupt when there is signal detection. This time value is used for *energysense* wakeup from sleep interrupt and from *controlsense* interrupts Interval time of the signal-resume interrupt 000: No repeat 001: 1 sec (default) 010: 2 sec 011: 3 sec 100: 4 sec Others: Invalid

13.3.47 Page 0: Register 64 (address = 0x40) [reset =0x80]

SIGDET_DC_REF_CH1_L is the alternate name for this register.

Figure 122. Page 0: Register 64

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 73. Page 0: Register 64 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.48 Page 0: Register 65 (address = 0x41) [reset = 0x7F]

SIGDET_DC_DIFF_CH1_L is the alternate name for this register.

Figure 123. Page 0: Register 65

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 74. Page 0: Register 65 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.49 Page 0: Register 66 (address = 0x42) [reset = 0x00]

SIGDET_DC_LEVEL_CH1_L is the alternate name for this register.

Figure 124. Page 0: Register 66

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 75. Page 0: Register 66 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.50 Page 0: Register 67 (address = 0x43) [reset = 0x80]

SIGDET_DC_REF_CH1_R is the alternate name for this register.

Figure 125. Page 0: Register 67

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 76. Page 0: Register 67 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.51 Page 0: Register 68 (address = 0x44) [reset = 0x7F]

SIGDET_DC_DIFF_CH1_R is the alternate name for this register.

Figure 126. Page 0: Register 68

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 77. Page 0: Register 68 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.52 Page 0: Register 69 (address = 0x45) [reset = 0x00]

SIGDET_DC_LEVEL_CH 1_R is the alternate name for this register.

Figure 127. Page 0: Register 69

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 78. Page 0: Register 69 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.53 Page 0: Register 70 (address = 0x46) [reset = 0x80]

SIGDET_DC_REF_CH2_L is the alternate name for this register.

Figure 128. Page 0: Register 70

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 79. Page 0: Register 70 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.54 Page 0: Register 71 (address = 0x47) [reset = 0x7F]

SIGDET_DC_DIFF_CH2_L is the alternate name for this register.

Figure 129. Page 0: Register 71

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 80. Page 0: Register 71 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.55 Page 0: Register 72 (address = 0x48) [reset = 0x00]

SIGDET_DC_LEVEL_CH2_L is the alternate name for this register.

Figure 130. Page 0: Register 72

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 81. Page 0: Register 72 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.56 Page 0: Register 73 (address = 0x49) [reset = 0x80]

SIGDET_DC_REF_CH2_R is the alternate name for this register.

Figure 131. Page 0: Register 73

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 82. Page 0: Register 73 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.57 Page 0: Register 74 (address = 0x4A) [reset = 0x7F]

SIGDET_DC_DIFF_CH2_R is the alternate name for this register.

Figure 132. Page 0: Register 74

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 83. Page 0: Register 74 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.58 Page 0: Register 75 (address = 0x4B) [reset = 0x00]

SIGDET_DC_LEVEL_CH 2_R is the alternate name for this register.

Figure 133. Page 0: Register 75

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 84. Page 0: Register 75 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.59 Page 0: Register 76 (address = 0x4C) [reset = 0x80]

SIGDET_DC_REF_CH3_L is the alternate name for this register.

Figure 134. Page 0: Register 76

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 85. Page 0: Register 76 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.60 Page 0: Register 77 (address = 0x4D) [reset = 0x7F]

SIGDET_DC_DIFF_CH3_L is the alternate name for this register.

Figure 135. Page 0: Register 77

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 86. Page 0: Register 77 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.61 Page 0: Register 78 (address = 0x4E) [reset = 0x00]

SIGDET_DC_LEVEL_CH3_L is the alternate name for this register.

Figure 136. Page 0: Register 78

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 87. Page 0: Register 78 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.62 Page 0: Register 79 (address = 0x4F) [reset = 0x80]

SIGDET_DC_REF_CH3_R is the alternate name for this register.

Figure 137. Page 0: Register 79

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 88. Page 0: Register 79 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.63 Page 0: Register 80 (address = 0x50) [reset = 0x7F]

SIGDET_DC_DIFF_CH3_R is the alternate name for this register.

Figure 138. Page 0: Register 80

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 89. Page 0: Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.64 Page 0: Register 81 (address = 0x51) [reset = 0x00]

SIGDET_DC_LEVEL_CH3_R is the alternate name for this register.

Figure 139. Page 0: Register 81

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 90. Page 0: Register 81 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.65 Page 0: Register 82 (address = 0x52) [reset = 0x80]

SIGDET_DC_REF_CH4_L is the alternate name for this register.

Figure 140. Page 0: Register 82

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 91. Page 0: Register 82 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.66 Page 0: Register 83 (address = 0x53) [reset = 0x7F]

SIGDET_DC_DIFF_CH4_L is the alternate name for this register.

Figure 141. Page 0: Register 83

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 92. Page 0: Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.67 Page 0: Register 84 (address = 0x54) [reset = 0x00]

SIGDET_DC_LEVEL_CH4_L is the alternate name for this register.

Figure 142. Page 0: Register 84

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 93. Page 0: Register 84 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.68 Page 0: Register 85 (address = 0x55) [reset = 0x80]

SIGDET_DC_REF_CH4_R is the alternate name for this register.

Figure 143. Page 0: Register 82

7	6	5	4	3	2	1	0
REF							
R/W-1000 0000b							

Table 94. Page 0: Register 85 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REF	R/W	1000 0000b	Reference Level of *Controlsense* Detection

13.3.69 Page 0: Register 86 (address = 0x56) [reset = 0x7F]

SIGDET_DC_DIFF_CH4_R is the alternate name for this register.

Figure 144. Page 0: Register 86

7	6	5	4	3	2	1	0
DIFF							
R/W-0111 1111b							

Table 95. Page 0: Register 86 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIFF	R/W	0111 1111b	Difference Level of *Controlsense* Detection

13.3.70 Page 0: Register 87 (address = 0x57) [reset = 0x00]

Figure 145. Page 0: Register 84

7	6	5	4	3	2	1	0
LEVEL							
R-0000 0000b							

Table 96. Page 0: Register 87 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LEVEL	R	0000 0000b	Current DC Level

13.3.71 Page 0: Register 88 (address = 0x58) [reset = 0x00]

AUXADC_DATA_CTRL is the alternate name for this register.

Figure 146. Page 0: Register 88

7	6	5	4	3	2	1	0
DC_NOLATCH	AUXADC_RDY	DC_RDY	AUXADC_LATCH	AUXADC_DATA_TYPE	DC_CH		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-000b		

Table 97. Page 0: Register 88 Field Descriptions

Bit	Field	Type	Reset	Description
7	DC_NOLATCH	R/W	0b	Read Without Latch Read directly without latch operation (from secondary ADC) 0: With latch operation (default) 1: Without latch operation when read dc value
6	AUXADC_RDY	R/W	0b	AUXADC Ready Indicate latch operation is finished and AUXADC value is ready for read operation. 0: Latch operation is running (default) 1: AUXADC value is ready for read operation
5	DC_RDY	R/W	0b	DC Ready Indicate latch operation is finished and dc value is ready. 0: Latch operation is running (default) 1: DC value is ready for read operation
4	AUXADC_LATCH	R/W	0b	AUXADC Latch Trigger to latch 16-bit AUXADC value for read operation: rising edge is the trigger signal 0: Idle (default) 1: Latch the value for read operation
3	AUXADC_DATA_TYPE	R/W	0b	Data to be Read From Control Interface 0: read LPF data (default) 1: read HPF data
2-0	DC_CH[2:0]	R/W	000b	DC-Value Channel Select Select dc-value channel to be latched for control-interface read operation 000: CH1_L (default) 001: CH1_R 010: CH2_L 011: CH2_R 100: CH3_L 101: CH3_R 110: CH4_L 111: CH4_R

13.3.72 Page 0: Register 89 (address = 0x59) [reset = 0x00]

Figure 147. Page 0: Register 89

7	6	5	4	3	2	1	0
AUXADC_DATA_LSB							
R-0000 0000b							

Table 98. Page 0: Register 89 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUXADC_DATA_LSB	R	0000 0000b	Low Byte of Secondary ADC Output The data depends on AUXADC_DATA_TYPE setting AUXADC_DATA_TYPE = 0: reading LPF of secondary ADC AUXADC_DATA_TYPE = 1: reading HPF of secondary ADC

13.3.73 Page 0: Register 90 (address = 0x5A) [reset = 0x00]

Figure 148. Page 0: Register 90

7	6	5	4	3	2	1	0
AUXADC_DATA_MSB							
R-0000 0000b							

Table 99. Page 0: Register 90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUXADC_DATA_MSB	R	0000 0000b	High Byte of Secondary ADC Output [15:8] The data depends on AUXADC_DATA_TYPE setting AUXADC_DATA_TYPE = 0: reading LPF of secondary ADC AUXADC_DATA_TYPE = 1: reading HPF of secondary ADC

13.3.74 Page 0: Register 96 (address = 0x60) [reset = 0x01]

Figure 149. Page 0: Register 96

7	6	5	4	3	2	1	0
RSV			POSTPGA_CP	RSV	DC_CHANG	DIN_TOGGLE	ENGSTR
R/W-000b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b

Table 100. Page 0: Register 96 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R/W	000b	Reserved. Always write 000b.
4	POSTPGA_CP	R/W	0b	Enable the Post-PGA Clipping Interrupt Write 0 to clear interrupts, all bits in this register 0: Disable (default) 1: Enable
3	RSV	R/W	0b	Reserved. Always write 0b.
2	DC_CHANG	R/W	0b	Enable the DC Level Change Interrupt 0: Disable (default) 1: Enable
1	DIN_TOGGLE	R/W	0b	Enable I2S RX DIN toggle Interrupt 0: Disable (default) 1: Enable
0	ENGSTR	R/W	1b	Enable the *energysense* Interrupt 0: Disable 1: Enable (default)

13.3.75 Page 0: Register 97 (address = 0x61) [reset = 0x00]

Figure 150. Page 0: Register 97

7	6	5	4	3	2	1	0
RSV			POSTPGA_CP	RSV	DC_CHANG	DIN_TOGGLE	ENGSTR
R-000b			R-0b	R-0b	R-0b	R-0b	R-0b

Table 101. Page 0: Register 97 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R	000b	Reserved. Always write 000b.
4	POSTPGA_CP	R	0b	Status of Post-PGA Clipping Interrupt Write 0 to register 0x60 clear interrupts, all bits in this register 0: None 1: Interrupt occurred
3	RSV	R	0b	Reserved. Always write 0b.
2	DC_CHANG	R	0b	Status of the DC Level Change Interrupt 0: None 1: Interrupt occurred
1	DIN_TOGGLE	R	0b	Status of I2S RX DIN toggle Interrupt 0: None 1: Interrupt occurred
0	ENGSTR	R	0b	Status of the *energysense* Interrupt 0: None 1: Interrupt occurred

13.3.76 Page 0: Register 98 (address = 0x62) [reset =0x10]

Figure 151. Page 0: Register 98

7	6	5	4	3	2	1	0
RSV		POL		RSV		WIDTH	
R/W-00b		R/W-01b		R/W-00b		R/W-00b	

Table 102. Page 0: Register 98 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R/W	00b	Reserved. Always write 00b.
5-4	POL	R/W	01b	Polarity of the Interrupt Pulse 00: Low active 01: High active (default) 10: Open drain (L-Active) 11: Reserved
3-2	RSV	R/W	00b	Reserved. Always write 00b.
1-0	WIDTH	R/W	00b	Width of the Interrupt Pulse 00: 1 ms (default) 01: 2 ms 10: 3 ms 11: Infinity for level sense

13.3.77 Page 0: Register 112 (address = 0x70) [reset = 0x70]

Figure 152. Page 0: Register 112

7	6	5	4	3	2	1	0
RSV					PWRDN	SLEEP	STBY
R/W-0 1110b					R/W-0b	R/W-0b	R/W-0b

Table 103. Page 0: Register 112 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RSV	R/w	0 1110b	Reserved. Always write 0 1110b
2	PWRDN	R/W	0b	Enter Analog Power Down State 0: Power Up (default) 1: Power Down
1	SLEEP	R/W	0b	Enter the Device Sleep State After the chip enters SLEEP state, *energysense* application will be triggered. 0: Power Up (default) 1: Sleep
0	STBY	R/W	0b	Enter Digital Standby State 0: Run (default) 1: Standby

13.3.78 Page 0: Register 113 (address = 0x71) [reset = 0x10]

DSP_CTRL is the alternate name for this register.

Figure 153. Page 0: Register 113

7	6	5	4	3	2	1	0
2CH	RSV	FLT	HPF_EN	MUTE_CH2_R	MUTE_CH2_L	MUTE_CH1_R	MUTE_CH1_L
R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 104. Page 0: Register 113 Field Descriptions

Bit	Field	Type	Reset	Description
7	2CH	R/W	0b	Processing Mode Selection Select the processing mode for 4-channel device only. This configuration CANNOT be changed *on the fly* in RUN state. 0: 4 channels (default) 1: 2 channels
6	RSV	R/W	0b	Reserved. Always write 0b.
5	FLT	R/W	0b	Select Decimation Filter Type 0: Normal (default) 1: Short latency
4	HPF_EN	R/W	1b	Enable High-Pass Filter 0: Disable 1: Enable (default)
3	MUTE_CH2_R	R/W	0b	Mute Ch2(R) 0: Unmute (default) 1: Mute
2	MUTE_CH2_L	R/W	0b	Mute Ch2(L) 0: Unmute (default) 1: Mute
1	MUTE_CH1_R	R/W	0b	Mute Ch1(R) 0: Unmute (default) 1: Mute
0	MUTE_CH1_L	R/W	0b	Mute Ch1(L) 0: Unmute (default) 1: Mute

13.3.79 Page 0: Register 114 (address = 0x72) [reset = 0x00]

Figure 154. Page 0: Register 114

7	6	5	4	3	2	1	0
RSV				STATE			
R-0000b				R-0000b			

Table 105. Page 0: Register 114 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSV	R	0000b	Reserved. Always write 0000b.
3-0	STATE	R	0000b	Device Current Status 0000: Power down (default) 0001: Wait clock stable 0010: Release reset 0011: Stand-by 0100: Fade IN 0101: Fade OUT 0110: Reserved 0111: Reserved 1000: Reserved 1001: Sleep 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Run

13.3.80 Page 0: Register 115 (address = 0x73) [reset = 0x00]

Figure 155. Page 0: Register 115

7	6	5	4	3	2	1	0
RSV					INFO		
R-0 0000b					R-000b		

Table 106. Page 0: Register 115 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RSV	R	0 0000b	Reserved. Always write 0 0000b.
2-0	INFO	R	000b	Current Sampling Frequency 000: Out of range (Low) or LRCK Halt (default) 001: 8 kHz 010: 16 kHz 011: 32 khz to 48 kHz 100: 88.2 kHz to 96 kHz 101: 176.4 kHz to 192 kHz 110: Out of range (High) 111: Invalid f_S

13.3.81 Page 0: Register 116 (address = 0x74) [reset = 0x00]

Figure 156. Page 0: Register 116

7	6	5	4	3	2	1	0
RSV	BCK_RATIO			RSV	SCK_RATIO		
R-0b	R-000b			R-0b	R-000b		

Table 107. Page 0: Register 116 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R	0b	Reserved. Always write 0 0000b.
6-4	BCK_RATIO	R	000b	Current Receiving BCK Ratio Default value: 000 (default) 000: Out of range (L) or BCK Halt 001: 32 010: 48 011: 64 100: 256 101: (Not assigned) 110: Out of range (H) 111: Invalid BCK ratio or LRCK Halt
3	RSV	R	0b	Reserved. Always write 0 0000b.
2-0	SCK_RATIO	R	000b	Current SCK Ratio 000: Out of range (L) or SCK Halt (default) 001: 128 010: 256 011: 384 100: 512 101: 768 110: Out of range (H) 111: Invalid SCK ratio or LRCK Halt

13.3.82 Page 0: Register 117 (address = 0x75) [reset = 0x00]

CLK_ERR_STAT is the alternate name for this register.

Figure 157. Page 0: Register 117

7	6	5	4	3	2	1	0
RSV	LRCKHLT	BCKHLT	SCKHTL	RSV	LRCKERR	BCKERR	SCKERR
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 108. Page 0: Register 117 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R	0b	Reserved. Always write 0b.
6	LRCKHLT	R	0b	LRCK Halt Status 0: No Error (default) 1: Halt
5	BCKHLT	R	0b	BCK Halt Status 0: No Error (default) 1: Halt
4	SCKHTL	R	0b	SCK Halt Status 0: No Error (default) 1: Halt
3	RSV	R	0b	Reserved. Always write 0b.
2	LRCKERR	R	0b	LRCK Error Status 0: No Error (default) 1: Error
1	BCKERR	R	0b	BCK Error Status 0: No Error (default) 1: Error
0	SCKERR	R	0b	SCK Error Status 0: No Error (default) 1: Error

13.3.83 Page 0: Register 120 (address = 0x78) [reset = 0x00]

Figure 158. Page 0: Register 120

7	6	5	4	3	2	1	0
RSV					DVDD	AVDD	LDO
R/W-0b					R/W-0b	R/W-0b	R/W-0b

Table 109. Page 0: Register 120 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RSV	R	0 0000b	Reserved. Always write 0 0000b.
2	DVDD	R	0b	DVDD Status 0:Bad or Missing (default) 1:Good
1	AVDD	R	0b	AVDD Status 0:Bad or issing (default) 1:Good
0	LDO	R	0b	Digital LDO Status 0:Bad or Missing (default) 1:Good

13.4 Page 1 Registers

13.4.1 Page 1: Register 1 (address = 0x01) [reset = 0x00]

Figure 159. Page 1: Register 1

7	6	5	4	3	2	1	0
RSV			DONE	RSV	BUSY	R_REQ	W_REQ
R/W-000b			R-0b	R/W-0b	R-0b	R/W-0b	R/W-0b

Table 110. Page 1: Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R/W	000b	Reserved. Always write 000b.
4	DONE	R	0b	Done Status Flag 1: Write or read operation is done with one cycle as indicator 0: Idle or is busy (default)
3	RSV	R/W	0b	Reserved. Always write 000b.
2	BUSY	R	0b	Busy Status Flag 1: Write or read operation is running and not finished 0: Write or read operation is finished (default)
1	R_REQ	R/W	0b	Memory Mapper Register Access to DSP-2 - READ 1: Request read operation 0: The read operation is done and data is ready to read from I^2C/SPI interface (default)
0	W_REQ	R/W	0b	Memory Mapper Register Access to DSP-2 - WRITE 1: Request write operation 0: The write operation is done and is ready for next write operation command (default)

13.4.2 Page 1: Register 2 (address = 0x02) [reset = 0x00]

Figure 160. Page 1: Register 2

7	6	5	4	3	2	1	0
RSV	MEM_ADDR						
R/W-0b	R/W-000 0000b						

Table 111. Page 1: Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RSV	R/W	0b	Reserved. Always write 0b.
6-0	MEM_ADDR	R/W	000 0000b	Memory Mapped Register Address Status of the memory mapped register access

13.4.3 Page 1: Register 4 (address = 0x04) [reset = 0x00]

Figure 161. Page 1: Register 4

7	6	5	4	3	2	1	0
MEM_WDATA_0							
R/W-0000 0000b							

Table 112. Page 1: Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEM_WDATA_0	R/W	0000 0000b	Write Data to 24-Bit Memory Coefficient [23:16]

13.4.4 Page 1: Register 5 (address = 0x05) [reset = 0x00]

Figure 162. Page 1: Register 5

7	6	5	4	3	2	1	0
MEM_WDATA_1							
R/W-0000 0000b							

Table 113. Page 1: Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEM_WDATA_1	R/W	0000 0000b	Write Data to 24-Bit Memory Coefficient [15:8]

13.4.5 Page 1: Register 6 (address = 0x06) [reset = 0x00]

Figure 163. Page 1: Register 6

7	6	5	4	3	2	1	0
MEM_WDATA_2							
R/W-0000 0000b							

Table 114. Page 1: Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEM_WDATA_2	R/W	0000 0000b	Write Data to 24-Bit Memory Coefficient [7:0]

13.4.6 Page 1: Register 7 (address = 0x07) [reset = 0x00]

Figure 164. Page 1: Register 7

7	6	5	4	3	2	1	0
MEM_WDATA_3	RSV						
R/W-0b	R/W-000 0000b						

Table 115. Page 1: Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
7	MEM_WDATA_2	R/W	0b	Write Data to 24-Bit Memory Reserved
6-0	RSV	R/W	000 0000b	Reserved. Always write 000 0000b.

13.4.7 Page 1: Register 8 (address = 0x08) [reset = 0x00]

Figure 165. Page 1: Register 8

7	6	5	4	3	2	1	0
MEM_RDATA_0							
R-0000 0000b							

Table 116. Page 1: Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEM_RDATA_0	R	0000 0000b	Read Data from 24-Bit Memory Coefficient [23:16]

13.4.8 Page 1: Register 9 (address = 0x09) [reset = 0x00]

Figure 166. Page 1: Register 9

7	6	5	4	3	2	1	0
MEM_RDATA_1							
R-0000 0000b							

Table 117. Page 1: Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEM_RDATA_1	R	0000 0000b	Read Data from 24-Bit Memory Coefficient [15:8]

13.4.9 Page 1: Register 10 (address = 0x0A) [reset = 0x00]

Figure 167. Page 1: Register 10

7	6	5	4	3	2	1	0
MEM_RDATA_2							
R-0000 0000b							

Table 118. Page 1: Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEM_RDATA_2	R	0000 0000b	Read Data from 24-Bit Memory Coefficient [7:0]

13.4.10 Page 1: Register 11 (address = 0x0B) [reset = 0x00]

Figure 168. Page 1: Register 11

7	6	5	4	3	2	1	0
MEM_RDATA_3	RSV						
R/W-0b	R/W-000 0000b						

Table 119. Page 1: Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
7	MEM_RDATA_3	R	0b	Read Data from 24-Bit Memory Reserved
6-0	RSV	R/W	000 0000b	Reserved. Always write 000 0000b.

13.5 Page 3 Registers

13.5.1 Page 3: Register 18 (address = 0x12) [reset =0x40]

Figure 169. Page 3: Register 18

7	6	5	4	3	2	1	0
RSV							PD
R/W-010 0000b							R/W-0b

Table 120. Page 3: Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RSV	R/W	010 0000b	Reserved. Always write 010 0000b
0	PD	R/W	0b	Oscillator Power Down Control 0: Power up (default) 1: Power down

13.5.2 Page 3: Register 21 (address = 0x15) [reset = 0x01]

Figure 170. Page 3: Register 21

7	6	5	4	3	2	1	0
RSV			TERM	RSV			PDZ
R/W-000b			W-0b	R/W-000b			W-1b

Table 121. Page 3: Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSV	R/W	000b	Reserved. Always write 000b.
4	TERM	W	0b	Mic Bias Resistor Bypass (Write only) 0: Disable (default) 1: Enable
3-1	RSV	R/W	000b	Reserved. Always write 000b.
0	PDZ	W	0b	Mic Bias Control (Write only) 0: Power down 1: Power up (default)

13.6 Page 253 Registers

13.6.1 Page 253: Register 20 (address = 0x14) [reset = 0x00]

Figure 171. Page 253: Register 20

7	6	5	4	3	2	1	0
PGA_ICI		REF_ICI		RSV			
R/W-00b		R/W-00b		R/W-0000b			

Table 122. Page 253: Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGA_ICI	R/W	00b	PGA Bias Current Trim 00: 100% (default) 01: Reserved 10: 75% 11: Reserved
5-4	REF_ICI	R/W	00b	Global bias current trim 00: 100% (default) 01: 75% 10: Reserved 11: Reserved
3-0	RSV	R/W	0000b	Reserved. Always write 0000b.

14 Device and Documentation Support

14.1 Development Support

- PCM186x EVM User's Guide

14.2 Related Links

Table 123 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 123. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
PCM1860-Q1	Click here	Click here	Click here	Click here	Click here
PCM1861-Q1	Click here	Click here	Click here	Click here	Click here
PCM1862-Q1	Click here	Click here	Click here	Click here	Click here
PCM1863-Q1	Click here	Click here	Click here	Click here	Click here
PCM1864-Q1	Click here	Click here	Click here	Click here	Click here
PCM1865-Q1	Click here	Click here	Click here	Click here	Click here

14.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

14.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1860QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1860Q1	Samples
PCM1861QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1861Q1	Samples
PCM1862QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1862Q1	Samples
PCM1863QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1863Q1	Samples
PCM1864QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1864Q1	Samples
PCM1865QDBTRQ1	ACTIVE	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PCM1865Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

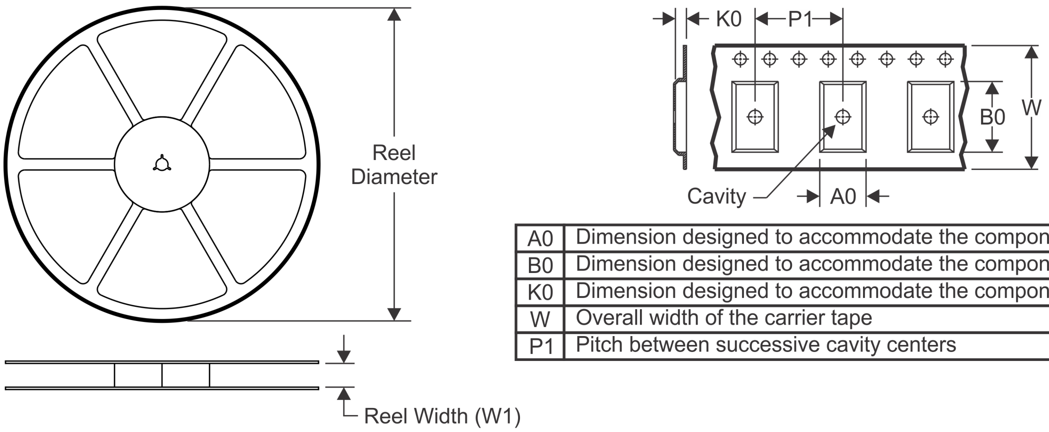
OTHER QUALIFIED VERSIONS OF PCM1860-Q1, PCM1861-Q1, PCM1862-Q1, PCM1863-Q1, PCM1864-Q1, PCM1865-Q1 :

- Catalog: PCM1860, PCM1861, PCM1862, PCM1863, PCM1864, PCM1865

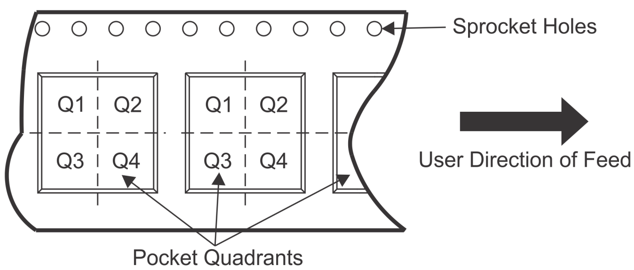
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



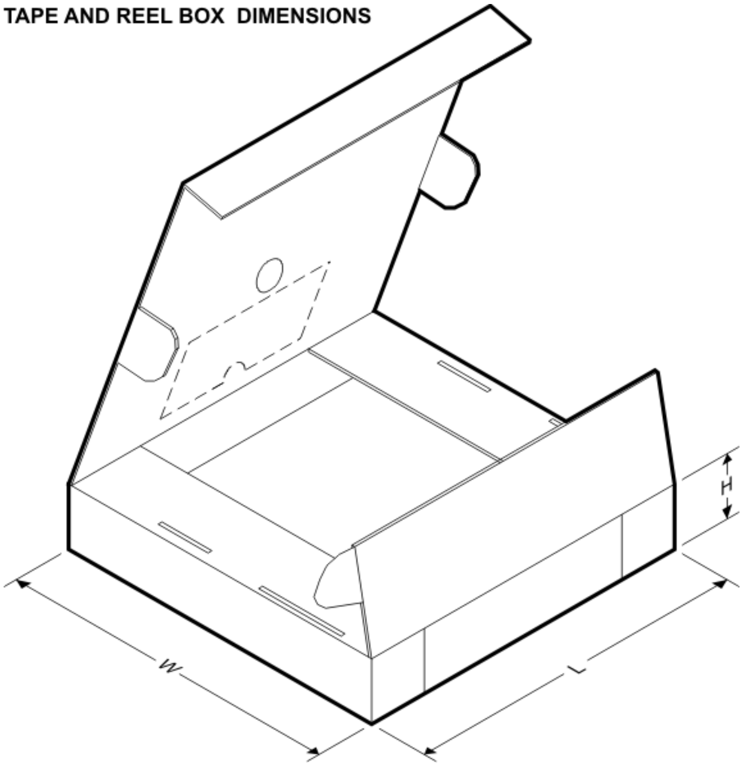
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

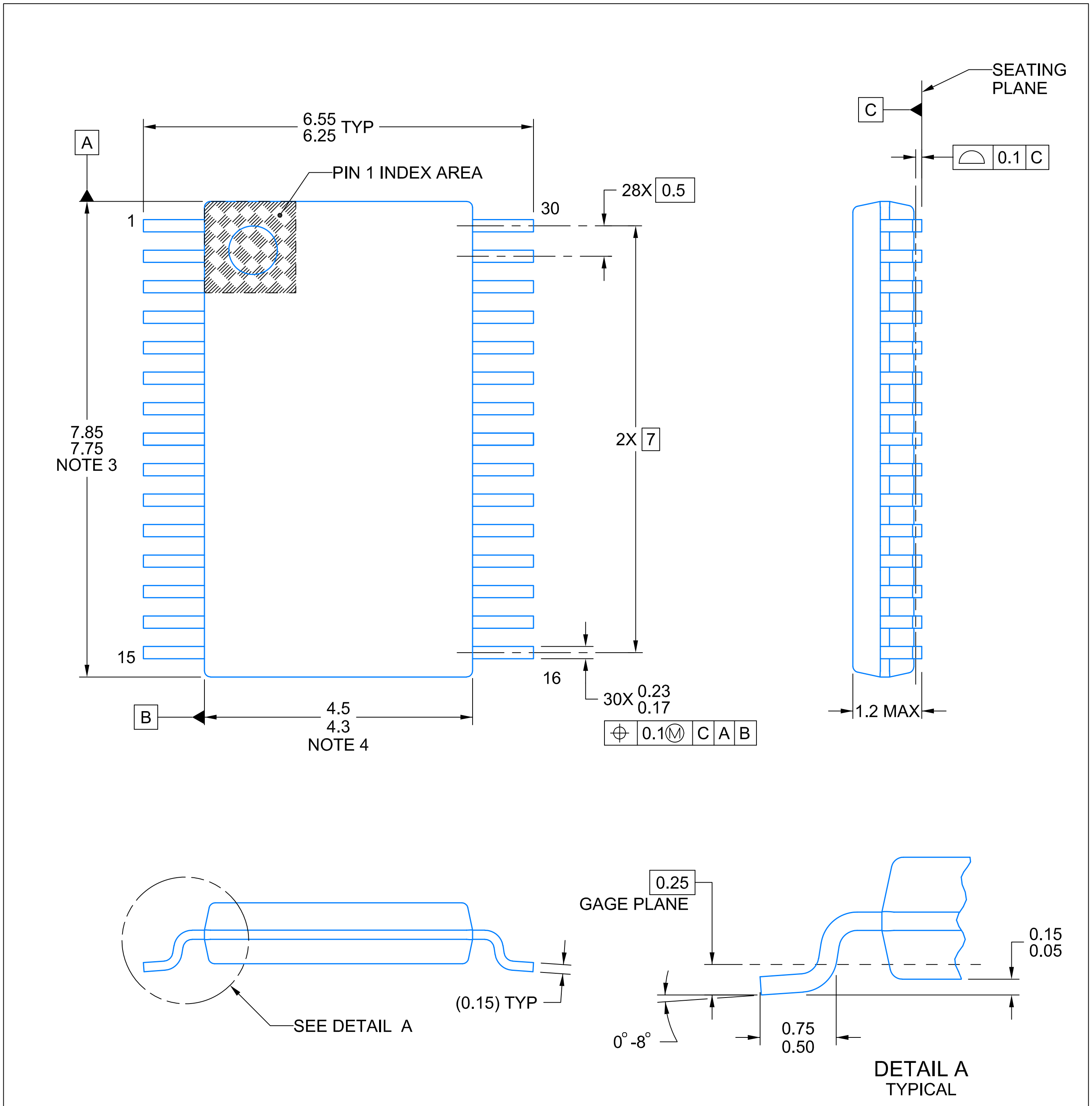
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1860QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCM1861QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCM1862QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCM1863QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCM1864QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCM1865QDBTRQ1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

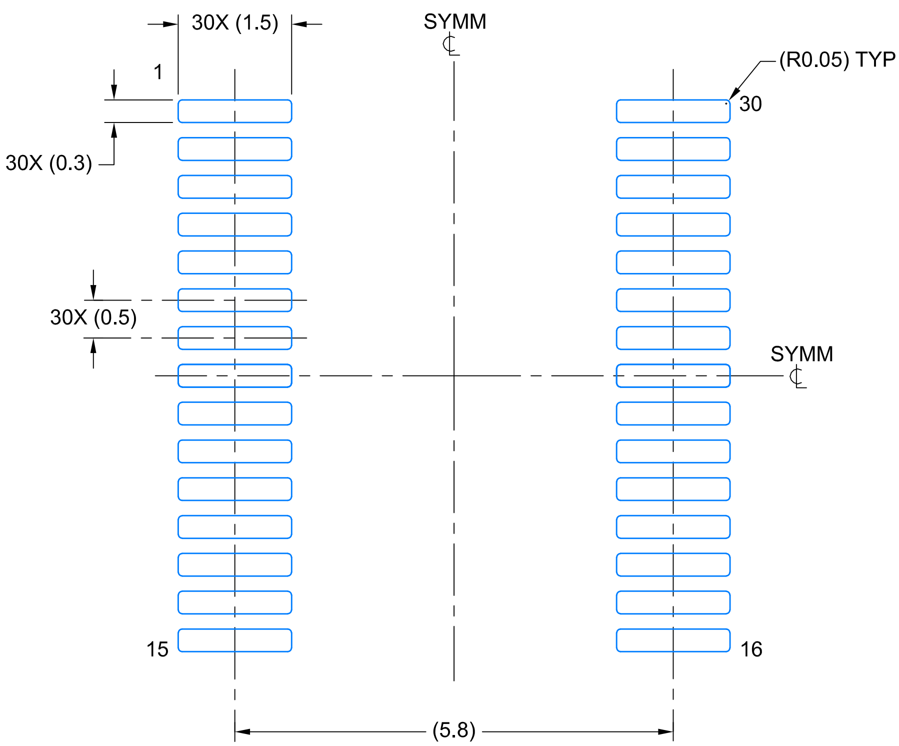
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1860QDBTRQ1	TSSOP	DBT	30	2000	350.0	350.0	43.0
PCM1861QDBTRQ1	TSSOP	DBT	30	2000	350.0	350.0	43.0
PCM1862QDBTRQ1	TSSOP	DBT	30	2000	350.0	350.0	43.0
PCM1863QDBTRQ1	TSSOP	DBT	30	2000	350.0	350.0	43.0
PCM1864QDBTRQ1	TSSOP	DBT	30	2000	350.0	350.0	43.0
PCM1865QDBTRQ1	TSSOP	DBT	30	2000	350.0	350.0	43.0



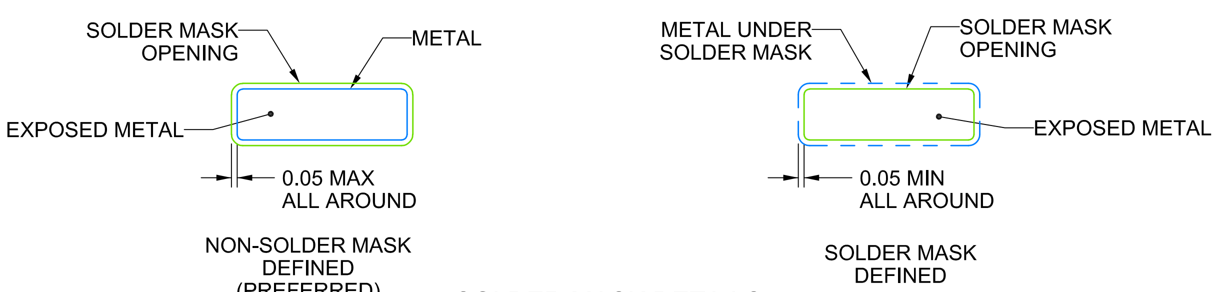
4220214/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

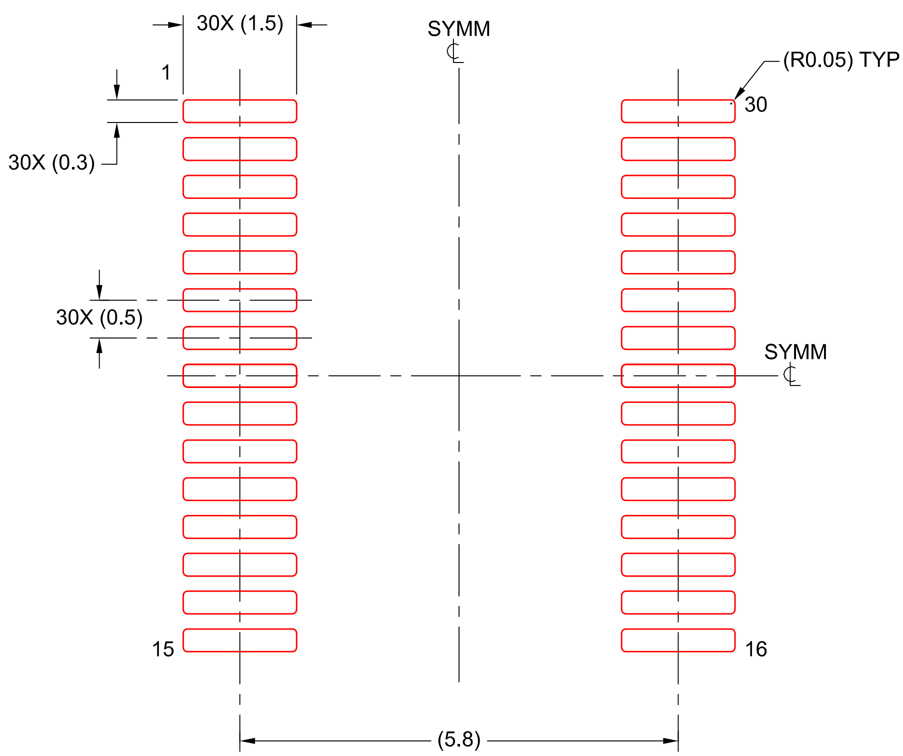


SOLDER MASK DETAILS

4220214/B 09/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220214/B 09/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.