

SN54LV540A, SN74LV540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS409C – APRIL 1998 – REVISED MAY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $>2.3\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV540A devices are octal buffers/drivers designed for 2-V to 5.5-V V_{CC} operation.

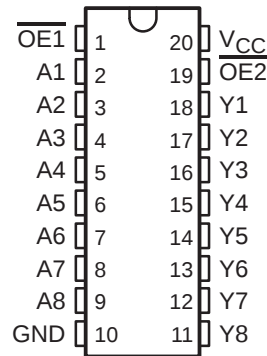
These devices are ideal for driving bus lines or buffer memory address registers. They feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

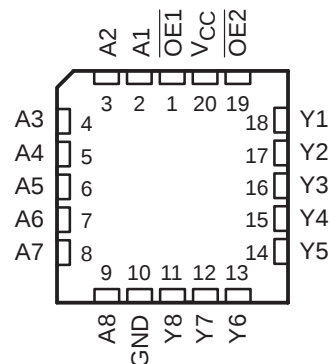
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV540A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV540A is characterized for operation from -40°C to 85°C .

SN54LV540A . . . J OR W PACKAGE
SN74LV540A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV540A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z



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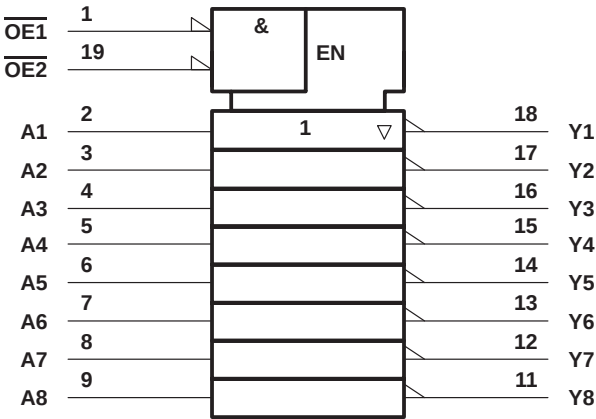
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**TEXAS
INSTRUMENTS**

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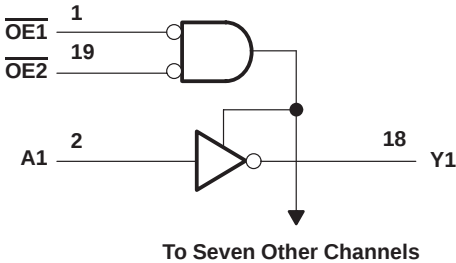
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV540A, SN74LV540A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LV540A		SN74LV540A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		1.5		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5		0.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		–50		–50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		–2		–2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		–8		–8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		–16		–16	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50		50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2		2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		8		8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	200	0	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0	100	0	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV540A			SN74LV540A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –8 mA	3 V	2.48			2.48			
	I _{OH} = –16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	0 V to 5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.5			2.5			pF
		5 V	2.5			2.5			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV540A		SN74LV540A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF	5.6*	12*		1*	14.5*	1	14.5	ns
t _{en}	$\overline{\text{OE}}$	Y		7.8*	17.4*		1*	21*	1	21	
t _{dis}	$\overline{\text{OE}}$	Y		5.7*	16*		1*	19*	1	19	
t _{pd}	A	Y	C _L = 50 pF	7.9	16.8		1	18.5	1	18.5	ns
t _{en}	$\overline{\text{OE}}$	Y		10.1	22.2		1	25.5	1	25.5	
t _{dis}	$\overline{\text{OE}}$	Y		8.1	22.3		1	25.5	1	25.5	
t _{sk(o)}					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV540A		SN74LV540A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF	4.1*	7*		1*	8.5*	1	8.5	ns
t _{en}	$\overline{\text{OE}}$	Y		5.6*	10.5*		1*	12.5*	1	12.5	
t _{dis}	$\overline{\text{OE}}$	Y		4.2*	10.5*		1*	12.5*	1	12.5	
t _{pd}	A	Y	C _L = 50 pF	5.8	10.5		1	12	1	12	ns
t _{en}	$\overline{\text{OE}}$	Y		7.3	14		1	16	1	16	
t _{dis}	$\overline{\text{OE}}$	Y		5.8	15.4		1	17.5	1	17.5	
t _{sk(o)}					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV540A		SN74LV540A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$		3*	5*	1*	6*	1	6	ns
t_{en}	$\overline{OE}$	Y			4.1*	7.2*	1*	8.5*	1	8.5	
t_{dis}	$\overline{OE}$	Y			2.9*	7*	1*	8*	1	8	
t_{pd}	A	Y	$C_L = 50\text{ pF}$		4.2	7	1	8	1	8	ns
t_{en}	$\overline{OE}$	Y			5.3	9.2	1	10.5	1	10.5	
t_{dis}	$\overline{OE}$	Y			3.5	8.8	1	10	1	10	
$t_{sk(o)}$						1				1	

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV540A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage		2.3		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	V

NOTE 5: Characteristics are for surface-mount packages only.

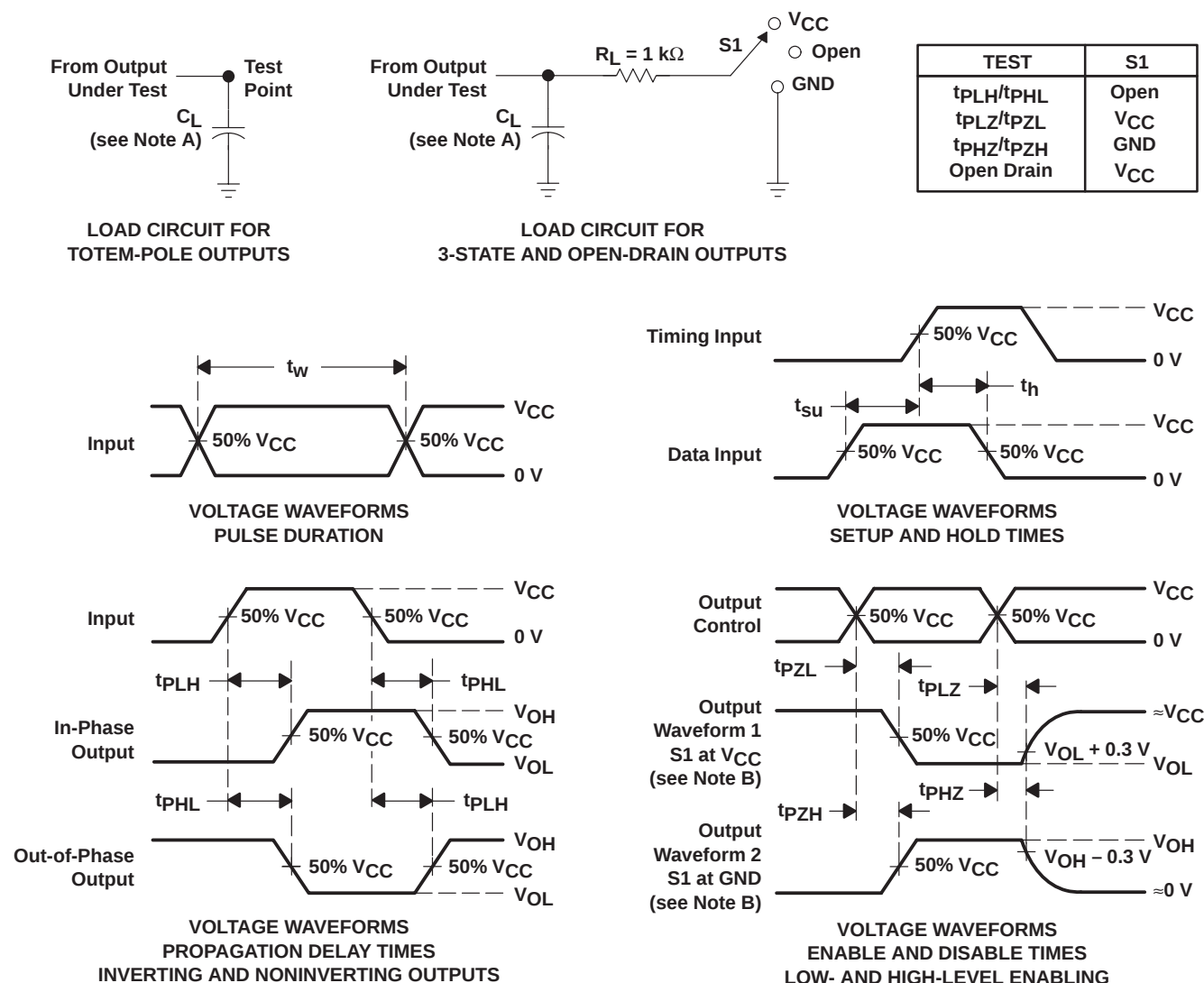
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	10	pF
		Outputs disabled		5 V	11	

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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SN74LV540A, OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Related Documents](#)

Parameter Name	SN74LV540A
Voltage Nodes (V)	5, 3.3, 2.5
Vcc range (V)	2.0 to 5.5
Input Level	LVTTL
Output Level	LVTTL
No. of Outputs	8
Output Drive (mA)	-8/8
tpd(max) (ns)	8.5
Static Current	0.02
Logic	Inv

Description

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- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
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Datasheets

Full datasheet in Acrobat PDF: [scls409c.pdf](#) (123 KB)

Full datasheet in Zipped PostScript: [scls409c.psz](#) (127 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN74LV540ADBR	DB	20	-40 TO 85	ACTIVE	0.40	2000	Check stock or order
SN74LV540ADGVR	DGV	20	-40 TO 85	ACTIVE	0.57	2000	Check stock or order
SN74LV540ADW	DW	20	-40 TO 85	ACTIVE	0.48	25	Check stock or order
SN74LV540ADWR	DW	20	-40 TO 85	ACTIVE	0.40	2000	Check stock or order
SN74LV540APWR	PW	20	-40 TO 85	ACTIVE	0.40	2000	Check stock or order

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- [LIVE INSERTION](#) (SDYA012 - Updated: 02/05/1999)
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