

<u>Device Type</u>	<u>Generic Number</u>
01	MAX358M(x)/883B
02	MAX359M(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
JE	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
FE	CDFP4-F16	16 LEAD Flatpack	F16
LP	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V⁻

V ⁺ to V ⁻	44V
V ⁺ to GND	+22V
V ⁻ to GND	-22V
Digital Inputs, Overvoltage	
V _{EN} , V _A to V ⁺	+4V
V _{EN} , V _A to V ⁻	-4V
Analog Input Overvoltage with Multiplexer Power On:	
V _S to V ⁺	+20V
V _S to V ⁻	-20V
Analog Input Overvoltage with Multiplexer Power Off:	
V _S to V ⁺	+35V
V _S to V ⁻	-35V
Continuous Current, S or D	20mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)	40mA
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C
Continuous Power Dissipation	
16 lead CERDIP(derate 10.0mW/°C above +70°C)	800mW
16 lead Flatpack(derate 6.06mW/°C above +70°C)	485mW
20 lead LCC (derate 9.1mW/°C above +70°C)	727mW
Junction Temperature T _J	+150°C
Thermal Resistance, Junction to Case, θ_{JC} :	
Case Outline 16 lead CERDIP	50°C/W
Case Outline 16 lead Flatpack	65°C/W
Case Outline 20 lead LCC	20°C/W
Thermal Resistance, Junction to Ambient, θ_{JA} :	
Case Outline 16 lead CERDIP	100°C/W
Case Outline 16 lead Flatpack	165°C/W
Case Outline 20 lead LCC	110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T _A)	-55°C to +125°C
Positive Supply Voltage (V ⁺)	+15V
Negative Supply Voltage (V ⁻)	-15V
Logic Low Level Address Input Voltage (V _{IL})	0V to 0.8V
Logic High Level Address Input Voltage (V _{IH})	2.4V to (V ⁺)-0.7V
Enable Voltage (V _{EN})	2.4V to (V ⁺)-0.7V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $V^+ = +15\text{V}$, $V^- = -15\text{V}$, $V_{AH} = +2.4\text{V}$, $V_{AL} = +0.8\text{V}$ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC							
ON Resistance	$r_{DS(ON)}$	$V_D = \pm 10\text{V}$, $I_S = 100\mu\text{A}$	1 2,3	All		1.5 1.8	k Ω
OFF Input Leakage Current	$I_{S(OFF)}$	$V_S = +/-10\text{V}$, $V_D = -/+10\text{V}$, $V_{EN} = 0.8\text{V}$	1 2,3	All		0.5 50	nA
OFF Output Leakage Current	$I_{D(OFF)}$	$V_S = +/-10\text{V}$, $V_D = -/+10\text{V}$, $V_{EN} = 0.8\text{V}$	1 2,3 2,3	All 01 02		1.0 200 100	nA
ON Channel Leakage Current	$I_{D(ON)}$	$V_{S(ALL)} = V_D = \pm 10\text{V}$, NOTE 2 $V_{AH} = V_{EN} = 2.4\text{V}$ $V_{AL} = 0.8\text{V}$	1 2,3 2,3	All 01 02		2.0 200 100	nA
Analog Signal Range	V_{AN}	NOTE 1	1,2,3	All	-15	+15	V
Differential, OFF Output Leakage Current	I_{DIFF}		1,2,3	02		50	nA
FAULT							
Output Leakage Current (with Overvoltage)	$I_{D(OFF)}$	$V_D = 0\text{V}$, NOTE 2 Analog Overvoltage = $\pm 33\text{V}$	2,3	All		2.0	μA
Input Leakage Current (with Overvoltage)	$I_{S(OFF)}$	$V_{IN} = \pm 25\text{V}$, $V_O = \pm 10\text{V}$ NOTE 2	1	All		5.0	μA
Input Leakage Current (with Power Supplies Off)	$I_{S(OFF)}$	$V_{IN} = \pm 25\text{V}$, $V_{EN} = V_O = 0\text{V}$ $A_0 = A_1 = A_2 = 0\text{V}$ or 5V	1	All		2.0	μA
INPUT							
Input Low Threshold	V_{AL}		1,2,3	All		0.8	V
Input High Threshold	V_{AH}		1,2,3	All	2.4		V
Input Leakage Current (High or Low)	I_A	$V_A = 4\text{V}$ or 0V , NOTE 4	1,2,3	All		1.0	μA
DYNAMIC							
Access Time	t_A	Figure 1 in Commercial Datasheet	1	All		1.0	μs
Break-Before-Make Delay	$t_{ON} - t_{OFF}$	$V_{EN} = +5\text{V}$, $V_{IN} = \pm 10\text{V}$ A_0 , A_1 , A_2 Strobed Figure 2 in Commercial Datasheet	1	All	25		ns
Enable Delay (ON)	$t_{ON(EN)}$	Figure 3 in Commercial Datasheet	1 2,3	All		500 1000	ns
Enable Delay (OFF)	$t_{OFF(EN)}$	Figure 3 in Commercial Datasheet	1 2,3	All		500 1000	ns
“OFF Isolation”	$OFF_{(ISO)}$	$V_{EN} = 0.8\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 15\text{pF}$, $V = 7V_{RMS}$, $f = 100\text{kHz}$.	1	All	50		dB

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125 °C V ⁺ = +15V, V ⁻ = -15V, V _{AH} = +2.4V, V _{AL} = +0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SUPPLY							
Positive Supply Current	I ⁺	V _{EN} = 0.8 or 2.4V, All V _A = 0V or 5V	1 2,3	All		0.6 0.7	mA
Negative Supply Current	I ⁻	V _{EN} = 0.8 or 2.4V, All V _A = 0V or 5V	1 2,3	All		0.1 0.2	mA
Power Supply Range for Continuous Operation	V _{OP}	NOTE 3	1	All	±4.5	±18	V

NOTE 1: When the analog signal exceeds +13.5V or -12V the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.

NOTE 2: The value shown is the steady state value. The transient leakage is typically 10μA. See detailed description in Commercial datasheet.

NOTE 3: Electrical Characteristics (such as on resistance) will change when power supplies other than ±15V are used.

NOTE 4: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

FIGURE 1: ACCESS TIME VS. LOGIC LEVEL (HIGH): See Commercial Datasheet.

FIGURE 2: BREAK-BEFORE-MAKE DELAY (t_{OPEN}): See Commercial Datasheet.

FIGURE 3: ENABLE DELAY (t_{ON(EN)}, t_{OFF(EN)}): See Commercial Datasheet.

TRUTH TABLE

TERMINAL CONNECTION

A ₂	A ₁	A ₀	EN	MAX358 ON SWITCH	TERMINAL NUMBER	01 MAX358	02 MAX359	01 MAX358	02 MAX359
X	X	X	0	None		J16, R16 & F16	J16, R16 & F16	L20	L20
0	0	0	1	1	1	A0	A0	NC	NC
0	0	1	1	2	2	EN	EN	A0	A0
0	1	0	1	3	3	V-	V-	EN	EN
0	1	1	1	4	4	IN1	IN1A	V-	V-
1	0	0	1	5	5	IN2	IN2A	IN1	IN1A
1	0	1	1	6	6	IN3	IN3A	NC	NC
1	1	0	1	7	7	IN4	IN4A	IN2	IN2A
1	1	1	1	8	8	OUT	OUTA	IN3	IN3A
					9	IN8	OUTB	IN4	IN4A
				MAX359	10	IN7	IN4B	OUT	OUTA
	A ₁	A ₀	EN	ON SWITCH	11	IN6	IN3B	NC	NC
	X	X	0	None	12	IN5	IN2B	IN8	OUTB
	0	0	1	1	13	V+	IN1B	IN7	IN4B
	0	1	1	2	14	GND	V+	IN6	IN3B
	1	0	1	3	15	A2	GND	IN5	IN2B
	1	1	1	4	16	A1	A1	NC	NC
					17			V+	IN1B
					18			GND	V+
					19			A2	GND
					20			A1	A1

ORDERING INFORMATION:					
01	MAX358MJE/883B	16 CDIP	02	MAX359MJE/883B	16 CDIP
01	MAX358MFE/883B	16 FLATPACK	02	MAX359MFE/883B	16 FLATPACK
01	MAX358MLP/883B	20 LCC	02	MAX359MLP/883B	20 LCC

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table I.