

SN54HC09, SN74HC09 QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-DRAIN OUTPUTS

D2804, MARCH 1984 — REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

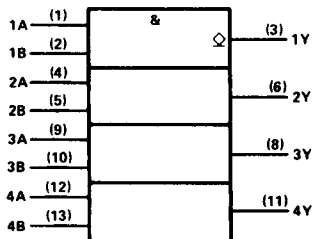
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC09 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC09 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

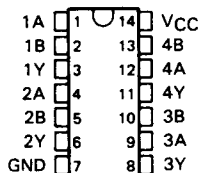
logic symbol†



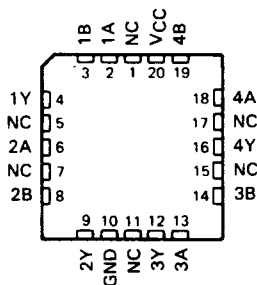
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC09 . . . J PACKAGE
SN74HC09 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC09 . . . FK PACKAGE
(TOP VIEW)



NC--No internal connection

logic diagram (positive logic)



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HCMOS Devices

SN54HC09, SN74HC09

QUADRUPLE 2-INPUT POSITIVE-AND GATES

WITH OPEN-DRAIN OUTPUTS

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, $I_{IK}(V_I < 0 \text{ or } V_I > V_{CC})$	± 20 mA
Output clamp current, $I_{OK}(V_O < 0 \text{ or } V_O > V_{CC})$	± 20 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC09			SN74HC09			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0	0.3	0	0.3	V	
		$V_{CC} = 4.5$ V	0	0.9	0	0.9		
		$V_{CC} = 6$ V	0	1.2	0	1.2		
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V		
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V		
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000	0	1000	ns	
		$V_{CC} = 4.5$ V	0	500	0	500		
		$V_{CC} = 6$ V	0	400	0	400		
T_A	Operating free-air temperature	-55	125	-40	85	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC09		SN74HC09		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH} \text{ or } V_{IL}, V_O = V_{CC}$	6 V	0.01	0.5	10		.5		μA	
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 20 \mu\text{A}$	2 V	0.002	0.1	0.1		0.1		V	
		4.5 V	0.001	0.1	0.1		0.1			
		6 V	0.001	0.1	0.1		0.1			
	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 4 \text{ mA}$	4.5 V	0.17	0.26	0.4		0.33			
	$V_I = V_{IH} \text{ or } V_{IL}, I_{OL} = 5.2 \text{ mA}$	6 V	0.15	0.26	0.4		0.33			
I_I	$V_I = V_{CC} \text{ or } 0$	6 V	± 0.1	± 100	± 1000		± 1000	nA		
I_{CC}	$V_I = V_{CC} \text{ or } 0, I_O = 0$	6 V		2	40		20	μA		
C_i		2 to 6 V	3	10	10		10	pF		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $R_L = 1\text{ k}\Omega$, $C_L = 50\text{ pF}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC09		SN74HC09		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V	60	105	155	131	ns			
			4.5 V	13	25	36	31				
			6 V	10	23	31	27				
t_{PHL}	A or B	Y	2 V	50	100	150	125	ns			
			4.5 V	10	20	30	25				
			6 V	8	17	25	21				
t_f		Y	2 V	38	75	110	95	ns			
			4.5 V	8	15	22	19				
			6 V	6	13	19	16				

C_{pd}	Power dissipation capacitance per gate	No load, $T_A = 25^\circ\text{C}$	20 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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