

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

1-of-8 Decoder/Demultiplexer with Address Latch

High-Performance Silicon-Gate CMOS

The MC74HC237 is identical in pinout to the LS137, but has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

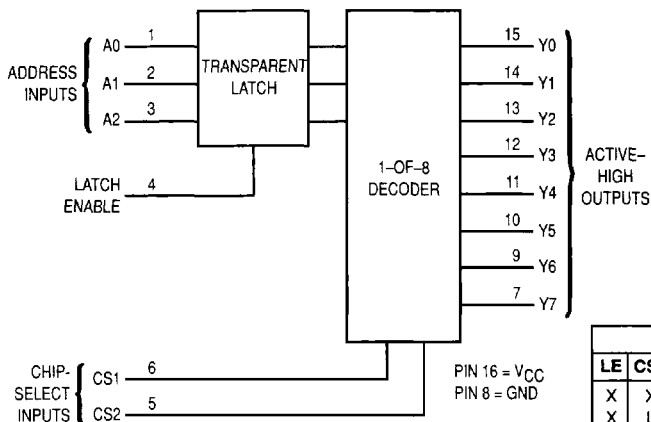
The HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

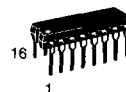
The HC237 is the noninverting version of the HC137.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 156 FETs or 39 Equivalent Gates

LOGIC DIAGRAM



MC74HC237



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC74HCXXN Plastic
MC74HCXXD SOIC

PIN ASSIGNMENT

A0	1	16	V _{CC}
A1	2	15	Y0
A2	3	14	Y1
LATCH ENABLE	4	13	Y2
CS2	5	12	Y3
CS1	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

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FUNCTION TABLE

Inputs						Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	*							

* = Depends upon the Address previously applied while LE was at a low level.



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	235	295	355	ns
		4.5	47	59	71	
		6.0	40	50	60	
t _{PHL}		2.0	185	230	280	
		4.5	37	46	56	
		6.0	31	39	48	
t _{PLH}	Maximum Propagation Delay, CS2 to Output Y (Figures 2 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t _{PHL}		2.0	145	180	220	
		4.5	29	36	44	
		6.0	25	31	38	
t _{PLH}	Maximum Propagation Delay, CS1 to Output Y (Figures 3 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t _{PHL}		2.0	160	200	240	
		4.5	32	40	48	
		6.0	27	34	41	
t _{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t _{PHL}		2.0	190	240	285	
		4.5	38	48	57	
		6.0	32	41	48	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		100	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2.

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PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

CONTROL INPUTS

CS1, CS2 (Pins 6, 5)

Chip select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the data inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a low level.

Latch Enable (Pin 4)

Latch Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the Address (CS1 = H and CS2 = L).

OUTPUTS

Y0–Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)

Active-high outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the Address inputs correspond to that particular output. The selected output is at a high level while all others remain at a low level.

SWITCHING WAVEFORMS

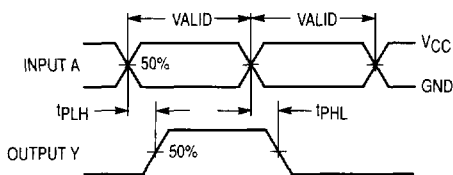


Figure 1.

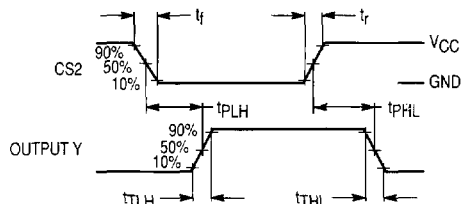


Figure 2.

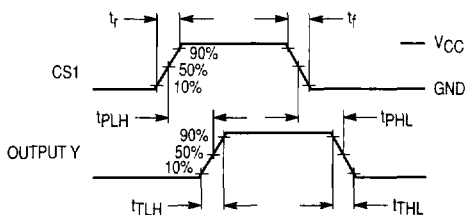


Figure 3.

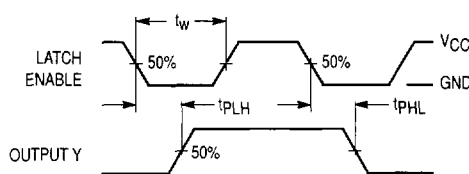


Figure 4.

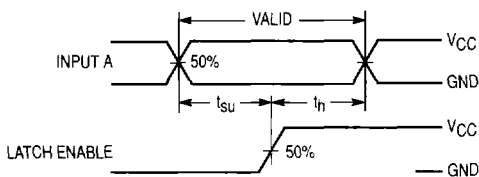
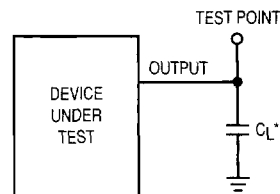


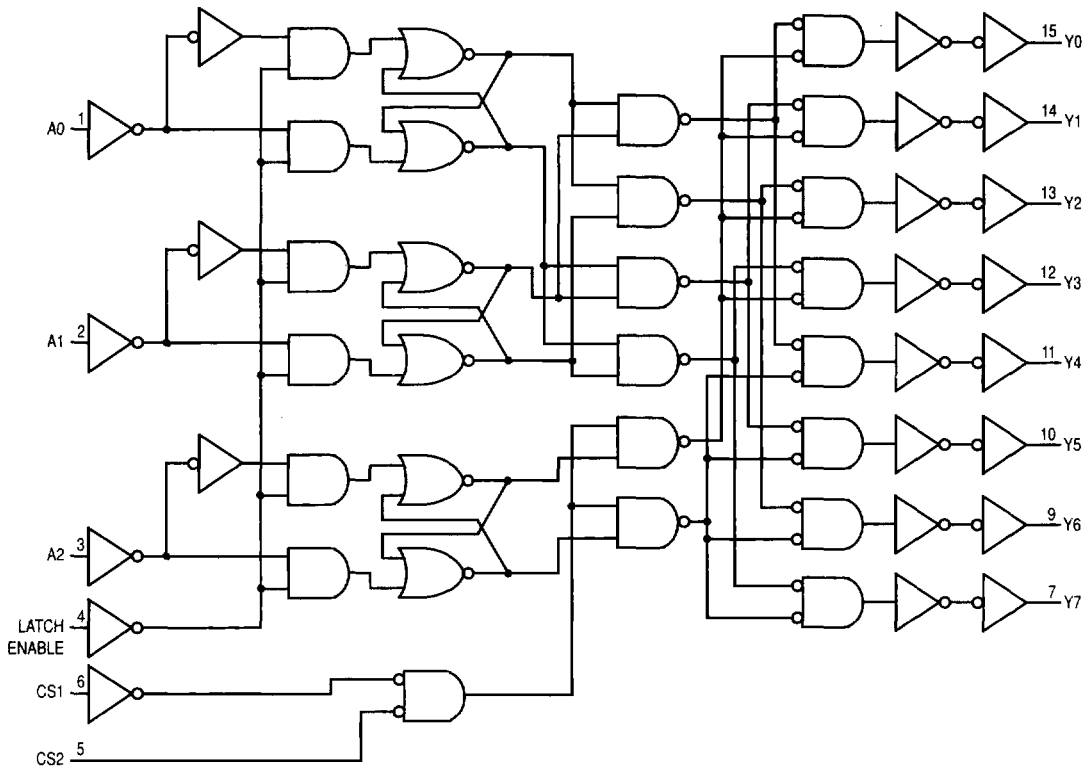
Figure 5.



* Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



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