

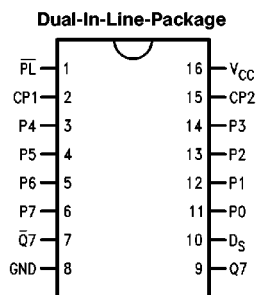
## 54165/DM74165 8-Bit Parallel-to-Serial Converter

### General Description

The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load ( $\overline{PL}$ ) input is LOW. With  $\overline{PL}$  HIGH, serial shifting occurs on

the rising edge of the clock; new data enters via the Serial Data ( $D_S$ ) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

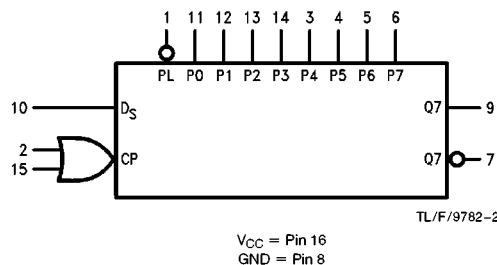
### Connection Diagram



TL/F/9782-1

Order Number 54165DMQB, 54165FMQB or DM74165N  
See NS Package Number J16A, N16E or W16A

### Logic Symbol



Pin Names	Description
CP1, CP2	Clock Pulse Inputs (Active Rising Edge)
$D_S$	Serial Data Input
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0-P7	Parallel Data Inputs
Q7	Serial Output from Last Stage
$\overline{Q7}$	Complementary Output

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	-55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	54165			DM74165			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			-0.8			-0.8	mA
I <sub>OL</sub>	Low Level Output Current			16			16	mA
T <sub>A</sub>	Free Air Operating Temperature	-55		125	0		70	°C
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW P <sub>n</sub> to $\overline{PL}$	10 10			10 10			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW P <sub>n</sub> to PL	10 10			0 0			ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>S</sub> to CP <sub>n</sub>	20 20			20 20			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>S</sub> to CP <sub>n</sub>	0 0			0 0			ns
t <sub>s</sub> (H)	Setup Time HIGH CP1 to CP2 or CP2 to CP1	30			30			ns
t <sub>w</sub> (H)	CP <sub>n</sub> Pulse Width HIGH	25			25			ns
t <sub>w</sub> (L)	$\overline{PL}$ Pulse Width LOW	15			15			ns
t <sub>rec</sub>	Recovery Time, $\overline{PL}$ to CP <sub>n</sub>	45			45			ns

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -12 mA			-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	2.4	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, V <sub>IH</sub> = Min		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V	$\overline{PL}$		80	μA
			Inputs		40	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V	$\overline{PL}$		-3.2	mA
			Inputs		-1.6	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	54	-20	-55	mA
			DM74	-18	-55	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max, $\overline{PL}$ = $\overline{PL}$ P <sub>n</sub> = $\overline{PL}$ , CP <sub>1</sub> , CP <sub>2</sub> = 4.5V			63	mA

## Switching Characteristics

$V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$  (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15\text{ pF}$ $R_L = 400\Omega$		Units
		Min	Max	
$f_{max}$	Maximum Clock Frequency	20		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{P}L$ to Q7 or $\overline{Q}7$		31 40	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP1 to Q7 or $\overline{Q}7$		24 31	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay P7 to Q7		17 36	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay P7 to $\overline{Q}7$		27 27	ns

**Note 1:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

**Note 2:** Not more than one output should be shorted at a time.

## Functional Description

The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the  $\overline{P}L$  signal is LOW. The parallel data can change while  $\overline{P}L$  is LOW provided that the recommended setup and hold times are observed.

For clocked operation,  $\overline{P}L$  must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit

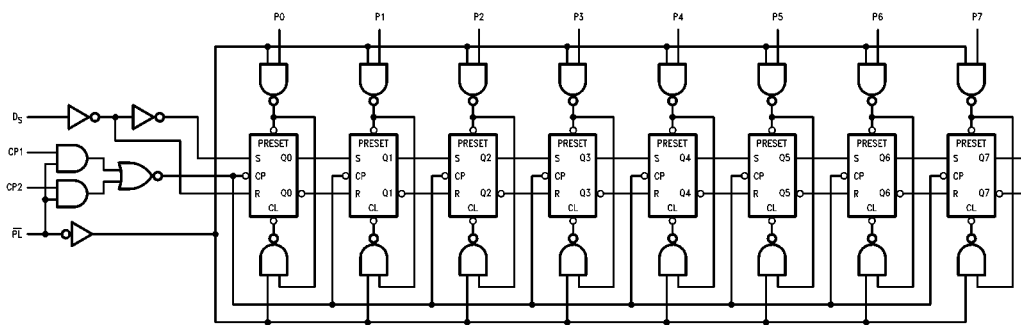
by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

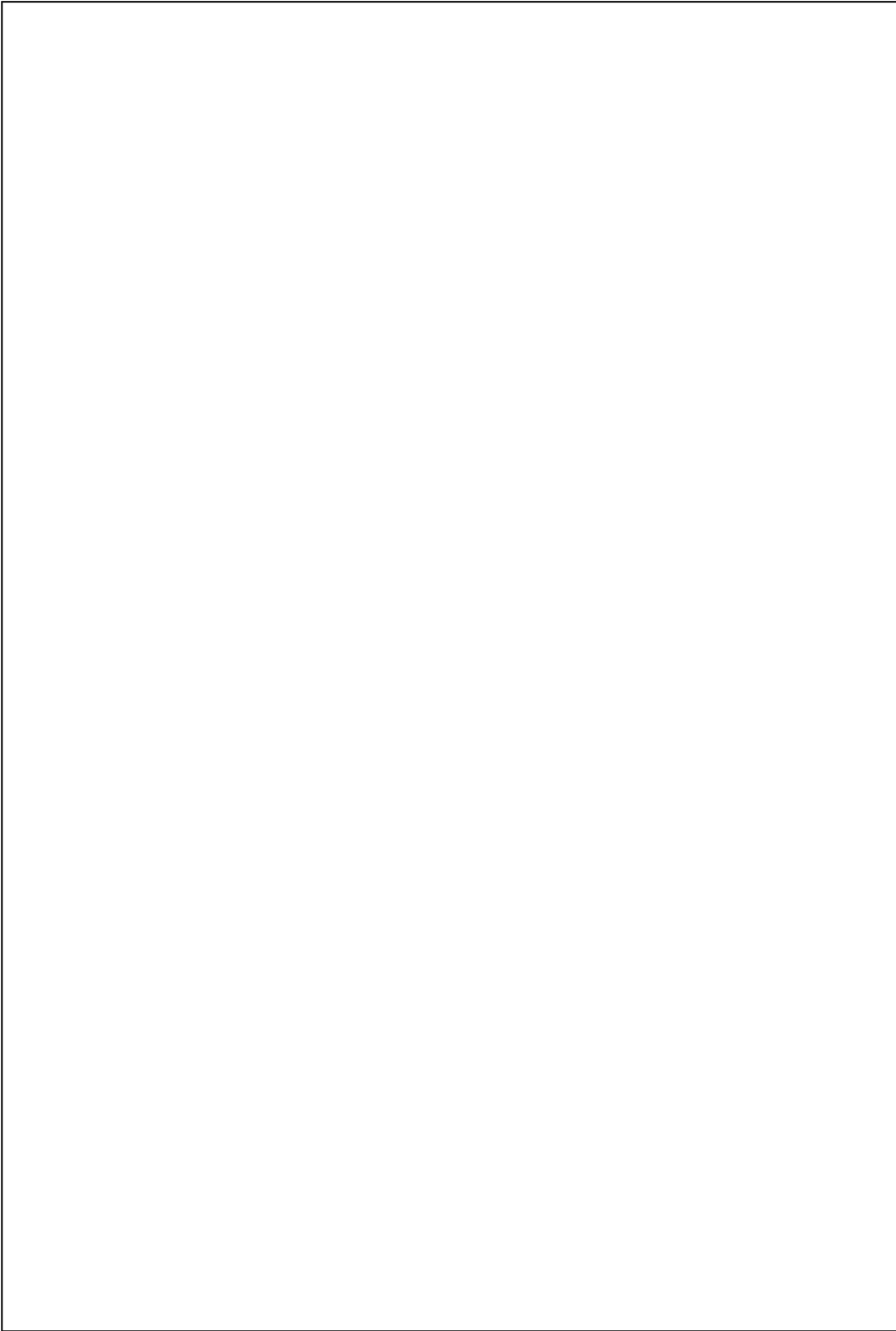
## Truth Table

$\overline{P}L$	CP		Contents								Response
	1	2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	X	X	P0	P1	P2	P3	P4	P5	P6	P7	Parallel Entry
H	L	↗	$D_S$	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Right Shift
H	H	↗	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	No Change
H	↗	L	$D_S$	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Right Shift
H	↗	H	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	No Change

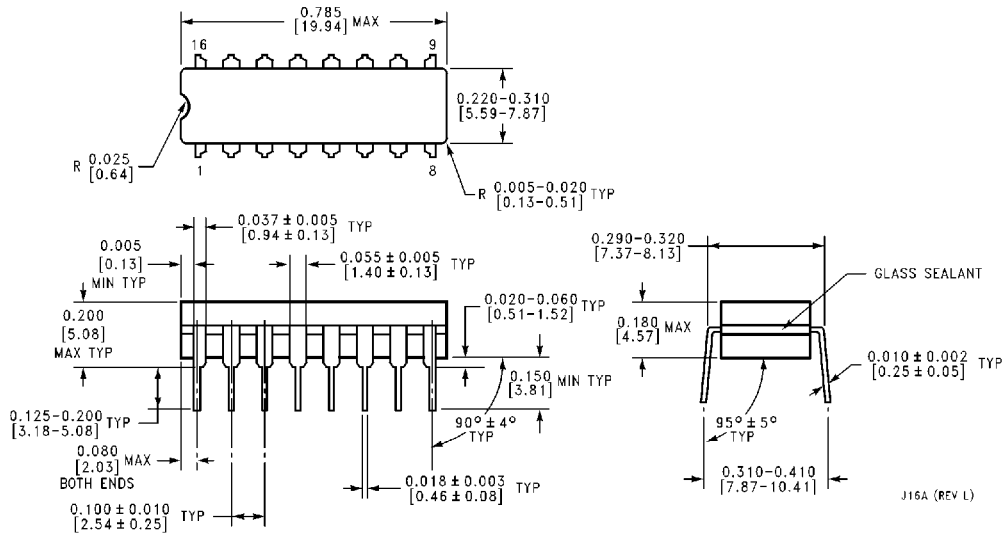
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = Positive Rising Edge

## Logic Diagram

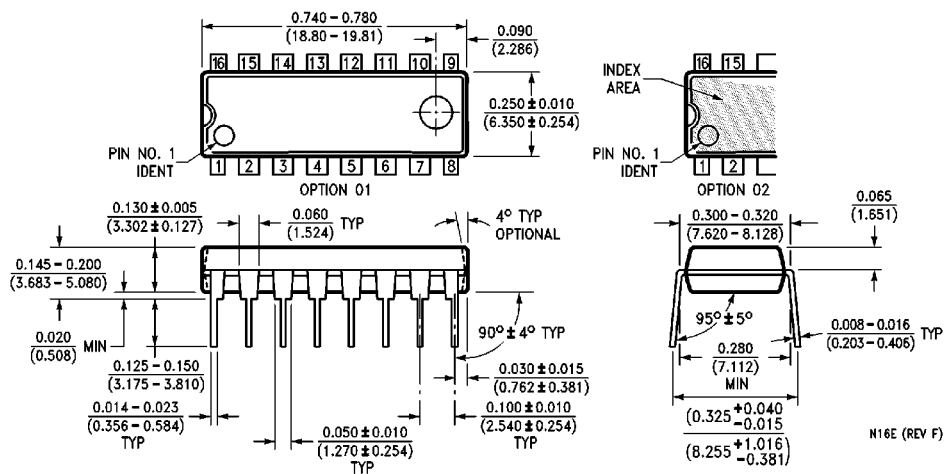




**Physical Dimensions** inches (millimeters)

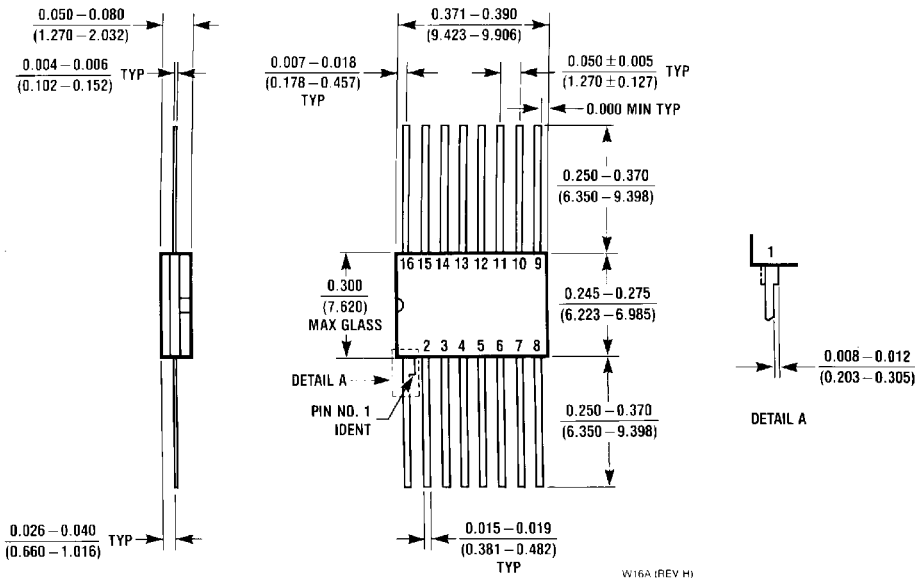


**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54165DMQB**  
**NS Package Number J16A**



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74165N**  
**NS Package Number N16E**

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Ceramic Flat Package (W)  
Order Number 54165FMQB  
NS Package Number W16A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
1111 West Bardin Road  
Arlington, TX 76017  
Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018

**National Semiconductor Europe**  
Fax: (+49) 0-180-530 85 86  
Email: cnjwge@tevm2.nsc.com  
Deutsch Tel: (+49) 0-180-530 85 85  
English Tel: (+49) 0-180-532 78 32  
Français Tel: (+49) 0-180-532 93 58  
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.