

SN74ALVC162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

SCAS278 – OCTOBER 1993 – REVISED MARCH 1994

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments **Widebus™** Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Output Ports Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required.
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 10-bit flip-flop is designed specifically for low-voltage (3.3-V) V_{CC} operation

The flip-flops of the SN74ALVC162820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 26- Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC162820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC162820 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OE}$	1	56	CLK
1Q1	2	55	D1
1Q2	3	54	NC
GND	4	53	GND
2Q1	5	52	D2
2Q2	6	51	NC
V_{CC}	7	50	V_{CC}
3Q1	8	49	D3
3Q2	9	48	NC
4Q1	10	47	D4
GND	11	46	GND
4Q2	12	45	NC
5Q1	13	44	D5
5Q2	14	43	NC
6Q1	15	42	D6
6Q2	16	41	NC
7Q1	17	40	D7
GND	18	39	GND
7Q2	19	38	NC
8Q1	20	37	D8
8Q2	21	36	NC
V_{CC}	22	35	V_{CC}
9Q1	23	34	D9
9Q2	24	33	NC
GND	25	32	GND
10Q1	26	31	D10
10Q2	27	30	NC
2OE	28	29	NC

PRODUCT PREVIEW

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3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

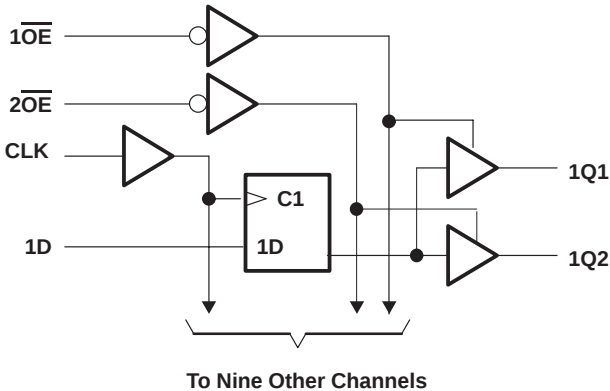
AND SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

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FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input voltage range, V_I (I/O ports) (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$		–8	mA
		$V_{CC} = 3\text{ V}$		–12†	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$		8	mA
		$V_{CC} = 3\text{ V}$		12†	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

† Current duty cycle $\leq 50\%$, $f \geq 1\text{ kHz}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}^\ddagger$	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18\text{ mA}$	2.7 V			–1.2	V
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	MIN to MAX	$V_{CC}-0.2$			V
	$I_{OH} = -8\text{ mA}$	2.7 V	2			
	$I_{OH} = -12\text{ mA}$	3 V	2			
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 8\text{ mA}$	2.7 V			0.8	
	$I_{OL} = 12\text{ mA}$	3 V			0.8	
I_I	$V_I = V_{CC}\text{ or GND}$	3.6 V			± 5	μA
$I_{I(\text{hold})}$	$V_I = 0.8\text{ V}$	3 V	75			μA
	$V_I = 2\text{ V}$	3 V	–75			μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V			± 10	μA
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V			40	μA
ΔI_{CC}	$V_{CC} = 3\text{ V to }3.6\text{ V,}$ One input at $V_{CC} - 0.6\text{ V,}$ Other inputs at $V_{CC}\text{ or GND}$				750	μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V				pF
C_o	$V_O = V_{CC}\text{ or GND}$	3.3 V				pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW



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