

## 600 MHz Dual Integrated DCL with PPMU, VHH Drive Capability, Level Setting DACs, and On-Chip Calibration Engine

### FEATURES

- ▶ 600 MHz/1200 Mbps data rate
- ▶ 3-level driver with high-Z and reflection clamps
- ▶ Window and differential comparators
- ▶  $\pm 25$  mA active load
- ▶ Per pin PPMU with  $-2.0$  V to  $+6.5$  V range
- ▶ Low leakage mode (typically 4 nA)
- ▶ Integrated 16-bit DACs with offset and gain correction
- ▶ High speed operating voltage range:  $-1.5$  V to  $+6.5$  V
- ▶ Dedicated VHH output pin range:  $0.0$  V to  $13.5$  V
- ▶ 1.1 W power dissipation per channel
- ▶ Driver
  - ▶ 3-level voltage range:  $-1.5$  V to  $+6.5$  V
  - ▶ Precision trimmed output resistance
  - ▶ Unterminated swing: 200 mV minimum to 8 V maximum
  - ▶ 725 ps minimum pulse width,  $V_{IH} - V_{IL} = 2.0$  V
- ▶ Comparator
  - ▶ Differential and single-ended window modes
  - ▶  $>1.2$  GHz input equivalent bandwidth
- ▶ Load
  - ▶  $\pm 25$  mA current range
- ▶ Per pin PPMU (PPMU)
  - ▶ Force voltage/compliance range:  $-2.0$  V to  $+6.5$  V
  - ▶ 5 current ranges: 40 mA, 1 mA, 100  $\mu$ A, 10  $\mu$ A, 2  $\mu$ A
  - ▶ External sense input for system PMU
  - ▶ Go/no-go comparators
- ▶ Levels
  - ▶ Fully integrated 16-bit DACs
  - ▶ On-chip gain and offset calibration registers and add/multiply engine
- ▶ 84-lead 10 mm  $\times$  10 mm LFCSP (0.4 mm pitch) package

### APPLICATIONS

- ▶ Automatic test equipment
- ▶ Semiconductor test systems
- ▶ Board test systems
- ▶ Instrumentation and characterization equipment

### GENERAL DESCRIPTION

The ADATE318 is a complete, single-chip ATE solution that performs the pin electronics functions of a driver, comparator, and active load (DCL), and a four quadrant per pin parametric measurement unit (PPMU). It has VHH drive capability per chip to support flash memory testing applications and integrated 16-bit DACs with an on-chip calibration engine to provide all necessary dc levels for operation of the part.

The driver features three active states: data high, data low, and terminate mode, as well as a high impedance inhibit state. The inhibit state, in conjunction with the integrated dynamic clamps, facilitates the implementation of a high speed active termination. The output voltage capability is  $-1.5$  V to  $+6.5$  V to accommodate a wide range of ATE and instrumentation applications.

The ADATE318 can be used as a dual, single-ended drive/receive channel or as a single differential drive/receive channel. Each channel of the ADATE318 features a high speed window comparator as well as a programmable threshold differential comparator for differential ATE applications. A four quadrant PPMU is also provided per channel.

All dc levels for DCL and PPMU functions are generated by 24 on-chip 16-bit DACs. To facilitate accurate levels programming, the ADATE318 contains an integrated calibration function to correct gain and offset errors for each functional block. Correction coefficients can be stored on chip, and any values written to the DACs are automatically adjusted using the appropriate correction factors.

The ADATE318 uses a serial programmable interface (SPI) bus to program all functional blocks, DACs, and on-chip calibration constants. It also has an on-chip temperature sensor and over/undervoltage fault clamps for monitoring and reporting the device temperature and any output pin or PPMU voltage faults that may occur during operation.

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## REVISION HISTORY

## 8/2022—Rev. B to Rev. C

|                                                                                                                                                                    |    |
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| Added Electrical Specifications Section.....                                                                                                                       | 4  |
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FUNCTIONAL BLOCK DIAGRAM

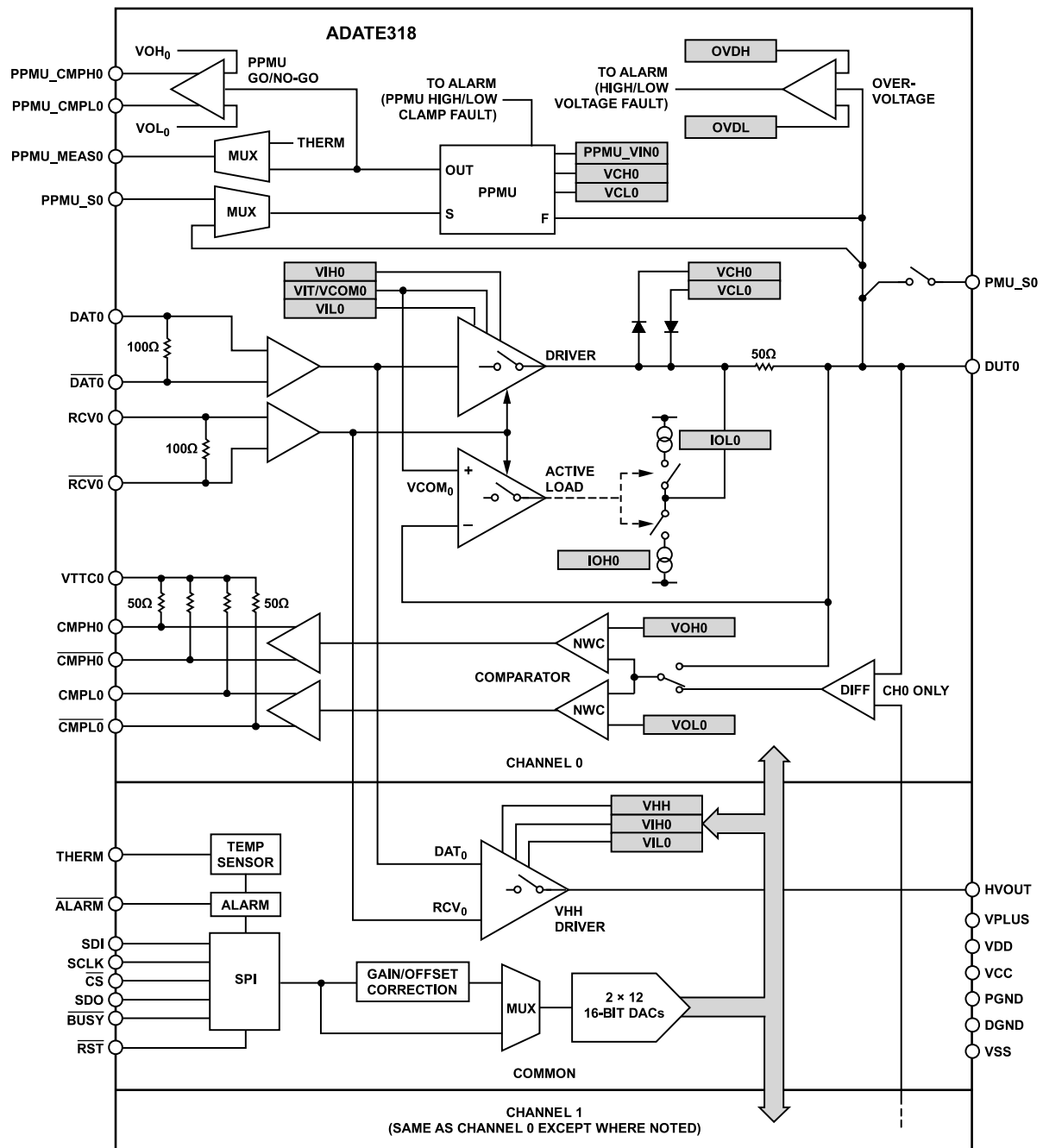


Figure 1.

## SPECIFICATIONS

VDD = +10.0 V, VCC = +2.5 V, VSS = -6.0 V, VPLUS = +16.75 V, VTTCx = +1.2 V, VREF = 5.000 V, VREFGND = 0.000 V. All test conditions are as defined in Table 32. All specified values are at  $T_J = 50^\circ\text{C}$ , where  $T_J$  corresponds to the internal temperature sensor reading (THERM pin), unless otherwise noted. Temperature coefficients are measured around  $T_J = 50^\circ \pm 20^\circ\text{C}$ , unless otherwise noted. Typical values are based on statistical mean of design, simulation analyses, and/or limited bench evaluation data. Typical values are neither tested nor guaranteed. See Table 16 for an explanation of test levels.

## ELECTRICAL SPECIFICATIONS

Table 1.

| Parameter                                           | Min   | Typ   | Max   | Unit | Test Level     | Test Conditions/Comments                                                                                            |
|-----------------------------------------------------|-------|-------|-------|------|----------------|---------------------------------------------------------------------------------------------------------------------|
| TOTAL FUNCTION                                      |       |       |       |      |                |                                                                                                                     |
| Output Leakage Current, DCL Disable<br>PPMU Range E | -10.0 | ±4.0  | +10.0 | nA   | P              | -2.0 V < VDUTx < +6.5 V, PPMU and DCL disabled, PPMU Range E, VCL = -2.5 V, VCH = +7.5 V                            |
| PPMU Range A, Range B, Range C, and Range D         |       | ±4.0  |       | nA   | C <sub>T</sub> | -2.0 V < VDUTx < +6.5 V, PPMU and DCL disabled, PPMU Range A, Range B, Range C, Range D, VCL = -2.5 V, VCH = +7.5 V |
| Output Leakage Current, Driver High-Z Mode          | -2    |       | +2    | µA   | P              | -2.0 V < VDUTx < +7.0 V, PPMU disabled and DCL enabled, RCVx active, VCL = -2.5 V, VCH = +7.5 V                     |
| DUTx Pin Capacitance                                |       | 1.2   |       | pF   | S              | Drive VIT = 0.0 V                                                                                                   |
| DUTx Pin Voltage Range                              | -2.0  |       | +7.0  | V    | D              |                                                                                                                     |
| POWER SUPPLIES                                      |       |       |       |      |                |                                                                                                                     |
| Total Supply Range, VPLUS to VSS                    |       | 22.75 | 23.55 | V    | D              |                                                                                                                     |
| VPLUS Supply, VPLUS                                 | 15.90 | 16.75 | 17.60 | V    | D              | Defines dc PSR conditions                                                                                           |
| Positive Supply, VDD                                | 9.5   | 10.0  | 10.5  | V    | D              | Defines dc PSR conditions                                                                                           |
| Negative Supply, VSS                                | -6.3  | -6.0  | -5.7  | V    | D              | Defines dc PSR conditions                                                                                           |
| Logic Supply, VCC                                   | 2.3   | 2.5   | 3.5   | V    | D              | Defines dc PSR conditions                                                                                           |
| Comparator Output Termination, VTTCx                | 0.5   | 1.2   | 3.3   | V    | D              |                                                                                                                     |
| VPLUS Supply Current, VPLUS                         |       | 1.1   | 2.5   | mA   | P              | VHH pin disabled                                                                                                    |
|                                                     | 4.75  | 13.28 | 16.25 | mA   | P              | VHH pin enabled, RCVx active, no load, VHH programmed level = 13.0 V                                                |
| Logic Supply Current, VCC                           | -125  | +1    | +125  | µA   | P              | Quiescent (SPI is static); VCC = 2.5 V                                                                              |
|                                                     |       | 7.5   |       | mA   | S              | Current drawn during clocked portion of device reset sequence                                                       |
| Termination Supply Current, VTTCx                   | 30    | 45    | 50    | mA   | P              |                                                                                                                     |
| Positive Supply Current, VDD                        | 90    | 99    | 115   | mA   | P              | Load power-down (IOH = IOL = 0 mA)                                                                                  |
| Negative Supply Current, VSS                        | 155   | 172   | 185   | mA   | P              | Load power-down (IOH = IOL = 0 mA)                                                                                  |
| Total Power Dissipation                             | 1.9   | 2.1   | 2.3   | W    | P              | Load power-down (IOH = IOL = 0 mA)                                                                                  |
| Positive Supply Current, VDD                        | 145   | 174   | 210   | mA   | P              | Load active off (IOH = IOL = 25 mA)                                                                                 |
| Negative Supply Current, VSS                        | 210   | 246   | 280   | mA   | P              | Load active off (IOH = IOL = 25 mA)                                                                                 |
| Total Power Dissipation                             | 3.0   | 3.3   | 3.6   | W    | P              | Load active off (IOH = IOL = 25 mA)                                                                                 |
| Positive Supply Current, VDD                        |       | 167   |       | mA   | C <sub>T</sub> | Load active off (IOH = IOL = 25 mA), calibrated                                                                     |
| Negative Supply Current, VSS                        |       | 238   |       | mA   | C <sub>T</sub> | Load active off (IOH = IOL = 25 mA), calibrated                                                                     |
| Total Power Dissipation                             |       | 3.2   |       | W    | C <sub>T</sub> | Load active off (IOH = IOL = 25 mA), calibrated                                                                     |
| Positive Supply Current, VDD                        |       | 109   |       | mA   | C <sub>T</sub> | Load power-down, PPMU standby                                                                                       |
| Negative Supply Current, VSS                        |       | 183   |       | mA   | C <sub>T</sub> | Load power-down, PPMU standby                                                                                       |
| Total Power Dissipation                             |       | 2.3   |       | W    | C <sub>T</sub> | Load power-down, PPMU standby                                                                                       |
| TEMPERATURE MONITOR                                 |       |       |       |      |                |                                                                                                                     |
| Temperature Sensor Gain                             |       | 10    |       | mV/K | D              |                                                                                                                     |
| Temperature Sensor Accuracy over Temperature Range  |       | ±6    |       | K    | C <sub>T</sub> |                                                                                                                     |
| VREF INPUT REFERENCE                                |       |       |       |      |                |                                                                                                                     |
| DAC Reference Input Voltage Range (VREF Pin)        | 4.950 | 5.000 | 5.050 | V    | D              | Provided externally:<br>VREF pin = +5.000 V                                                                         |

## SPECIFICATIONS

Table 1.

| Parameter                               | Min  | Typ | Max  | Unit | Test Level | Test Conditions/Comments                                                                      |
|-----------------------------------------|------|-----|------|------|------------|-----------------------------------------------------------------------------------------------|
| Input Bias Current                      |      |     | 100  | μA   | P          | VREFGND pin = 0.000 V (not referenced to V <sub>DUTGND</sub> )<br>Tested with 5.000 V applied |
| DUTGND INPUT                            |      |     |      |      |            |                                                                                               |
| Input Voltage Range, Referenced to AGND | -0.1 |     | +0.1 | V    | D          |                                                                                               |
| Input Bias Current                      | -100 |     | +100 | μA   | P          | Tested at -100 mV and +100 mV                                                                 |

## DRIVER SPECIFICATIONS

VIH – VIL ≥ 100 mV to meet dc and ac performance specifications.

Table 2.

| Parameter                                           | Min  | Typ  | Max  | Unit   | Test Level     | Test Conditions/Comments                                                                                                                                                                                           |
|-----------------------------------------------------|------|------|------|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DC SPECIFICATIONS                                   |      |      |      |        |                |                                                                                                                                                                                                                    |
| High-Speed Differential Input Characteristics       |      |      |      |        |                |                                                                                                                                                                                                                    |
| High Speed Input Termination Resistance: DATx, RCVx | 92   | 100  | 108  | Ω      | P              | Impedance between each pair of DATx and RCVx pins; push 4 mA into positive pin, force 0.8 V on negative pin, measure voltage between pins; calculate resistance ( $\Delta V/\Delta I$ )                            |
| Input Voltage Differential: DATx, RCVx              | 0.2  | 0.4  | 1.0  | V      | D              | $0.2\text{ V} < V_{DM} < 1.0\text{ V}$                                                                                                                                                                             |
| Input Voltage Range: DATx, RCVx                     | 0.0  |      | 3.3  | V      | D              | $0.0\text{ V} < (V_{CM} \pm V_{DM}/2) < 3.3\text{ V}$                                                                                                                                                              |
| Output Characteristics                              |      |      |      |        |                |                                                                                                                                                                                                                    |
| Output High Range, VIH                              | -1.4 |      | +6.5 | V      | D              |                                                                                                                                                                                                                    |
| Output Low Range, VIL                               | -1.5 |      | +6.4 | V      | D              |                                                                                                                                                                                                                    |
| Output Term Range, VIT                              | -1.5 |      | +6.5 | V      | D              |                                                                                                                                                                                                                    |
| Functional Amplitude (VIH – VIL)                    | 0.0  | 8.0  |      | V      | D              |                                                                                                                                                                                                                    |
| DC Output Current Limit Source                      | 75   |      | 130  | mA     | P              | Drive high, VIH = +6.5 V, short DUTx pin to -1.5 V, measure current                                                                                                                                                |
| DC Output Current Limit Sink                        | -130 |      | -75  | mA     | P              | Drive low, VIL = -1.5 V, short DUTx pin to +6.5 V, measure current                                                                                                                                                 |
| Output Resistance, ±40 mA                           | 46   | 48.6 | 51   | Ω      | P              | $\Delta V_{DUT}/\Delta I_{DUT}$ ; source: VIH = 3.0 V, IDUT = +1 mA, +40 mA; sink: VIL = 0.0 V, IDUT = -1 mA, -40 mA                                                                                               |
| DC ACCURACY                                         |      |      |      |        |                |                                                                                                                                                                                                                    |
| VIH, VIL, VIT Offset Error                          | -500 |      | +500 | mV     | P              | VIH tests with VIL = -2.5 V, VIT = -2.5 V<br>VIL tests with VIH = +7.5 V, VIT = +7.5 V<br>VIT tests with VIL = -2.5 V, VIH = +7.5 V, unless otherwise specified<br>Measured at DAC Code 0x4000 (0 V), uncalibrated |
| VIH, VIL, VIT Offset Tempco                         |      | ±625 |      | μV/°C  | C <sub>T</sub> |                                                                                                                                                                                                                    |
| VIH, VIL, VIT Gain                                  | 1.0  |      | 1.1  | V/V    | P              | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer functions (see Table 21)                                                                            |
| VIH, VIL, VIT Gain Tempco                           |      | ±40  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                                                    |
| VIH, VIL, VIT DNL                                   |      | ±1   |      | mV     | C <sub>T</sub> | After two point gain/offset calibration; calibration points at 0x4000 (0 V) output; 0xC000 (+5 V) output; measured over full specified output range                                                                |
| VIH, VIL, VIT INL                                   | -7   |      | +7   | mV     | P              | After two point gain/offset calibration; applies to nominal VDD = +10.0 V supply case only                                                                                                                         |
| VIH, VIL, VIT Resolution                            |      | 153  |      | μV     | D              |                                                                                                                                                                                                                    |
| DUTGND Voltage Accuracy                             | -7   | ±2   | +7   | mV     | P              | Over ±0.1 V range; measured at end points of VIH, VIL, and VIT functional range                                                                                                                                    |
| DC Levels Interaction                               |      |      |      |        |                | DC interaction on VIL, VIH, and VIT output level while other driver DAC levels are varied                                                                                                                          |
| VIH vs. VIL                                         |      | ±0.2 |      | mV     | C <sub>T</sub> | Monitor interaction on VIH = +6.5 V; sweep VIL = -1.5 V to +6.4 V, VIT = +1.0 V                                                                                                                                    |

## SPECIFICATIONS

Table 2.

| Parameter                                 | Min | Typ  | Max | Unit | Test Level     | Test Conditions/Comments                                                                               |
|-------------------------------------------|-----|------|-----|------|----------------|--------------------------------------------------------------------------------------------------------|
| VIH vs. VIT                               |     | ±1   |     | mV   | C <sub>T</sub> | Monitor interaction on VIH = +6.5 V; sweep VIT = -1.5 V to +6.5 V, VIL = 0.0 V                         |
| VIL vs. VIH                               |     | ±0.2 |     | mV   | C <sub>T</sub> | Monitor interaction on VIL = -1.5 V; sweep VIH = -1.4 V to +6.5 V, VIT = +1.0 V                        |
| VIL vs. VIT                               |     | ±1   |     | mV   | C <sub>T</sub> | Monitor interaction on VIL = -1.5 V; sweep VIT = -1.5 V to +6.5 V, VIH = +2.0 V                        |
| VIT vs. VIH                               |     | ±1   |     | mV   | C <sub>T</sub> | Monitor interaction on VIT = +1.0 V; sweep VIH = -1.4 V to +6.5 V, VIL = -1.5 V                        |
| VIT vs. VIL                               |     | ±1   |     | mV   | C <sub>T</sub> | Monitor interaction on VIT = +1.0 V; sweep VIL = -1.5 V to +6.4 V, VIH = +6.5 V                        |
| Overall Voltage Accuracy                  |     | ±8   |     | mV   | C <sub>T</sub> | VIH - VIL ≥ 100 mV; sum of INL, dc interaction, DUTGND, and tempco errors over ±5°C, after calibration |
| VIH, VIL, VIT DC PSRR                     |     | ±10  |     | mV/V | C <sub>T</sub> | Measured at calibration points                                                                         |
| AC SPECIFICATIONS                         |     |      |     |      |                |                                                                                                        |
| Rise/Fall Times                           |     |      |     |      |                | All ac specifications performed after calibration<br>Toggle DATx                                       |
| 0.2 V Programmed Swing, T <sub>RISE</sub> |     | 215  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 0.2 V, VIL = 0.0 V, terminated                                                       |
| 0.2 V Programmed Swing, T <sub>FALL</sub> |     | 277  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 0.2 V, VIL = 0.0 V, terminated                                                       |
| 0.5 V Programmed Swing, T <sub>RISE</sub> |     | 218  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 0.5 V, VIL = 0.0 V, terminated                                                       |
| 0.5 V Programmed Swing, T <sub>FALL</sub> |     | 274  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 0.5 V, VIL = 0.0 V, terminated                                                       |
| 1.0 V Programmed Swing, T <sub>RISE</sub> | 150 | 222  | 320 | ps   | P              | 20% to 80%, VIH = 1.0 V, VIL = 0.0 V, terminated                                                       |
| 1.0 V Programmed Swing, T <sub>FALL</sub> | 150 | 283  | 320 | ps   | P              | 20% to 80%, VIH = 1.0 V, VIL = 0.0 V, terminated                                                       |
| 2.0 V Programmed Swing, T <sub>RISE</sub> |     | 297  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 2.0 V, VIL = 0.0 V, terminated                                                       |
| 2.0 V Programmed Swing, T <sub>FALL</sub> |     | 322  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 2.0 V, VIL = 0.0 V, terminated                                                       |
| 3.0 V Programmed Swing, T <sub>RISE</sub> |     | 447  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 3.0 V, VIL = 0.0 V, terminated                                                       |
| 3.0 V Programmed Swing, T <sub>FALL</sub> |     | 397  |     | ps   | C <sub>B</sub> | 20% to 80%, VIH = 3.0 V, VIL = 0.0 V, terminated                                                       |
| 5.0 V Programmed Swing, T <sub>RISE</sub> |     | 1117 |     | ps   | C <sub>B</sub> | 10% to 90%, VIH = 5.0 V, VIL = 0.0 V, unterminated                                                     |
| 5.0 V Programmed Swing, T <sub>FALL</sub> |     | 798  |     | ps   | C <sub>B</sub> | 10% to 90%, VIH = 5.0 V, VIL = 0.0 V, unterminated                                                     |
| Rise to Fall Matching                     |     | -25  |     | ps   | C <sub>B</sub> | Rise to fall within one channel, VIH = 2.0 V, VIL = 0.0 V, terminated                                  |
|                                           |     | -61  |     | ps   | C <sub>B</sub> | Rise to fall within one channel; VIH = 1.0 V, VIL = 0.0 V, terminated                                  |
| Minimum Pulse Width                       |     |      |     |      |                | Toggle DATx                                                                                            |
| 0.5 V Programmed Swing                    |     | 725  |     | ps   | C <sub>B</sub> | VIH = 0.5 V, VIL = 0.0 V, terminated, timing error less than +69/-33 ps                                |
|                                           |     | 725  |     | ps   | C <sub>B</sub> | VIH = 0.5 V, VIL = 0.0 V, terminated, less than 10% amplitude loss                                     |
| Maximum Toggle Rate                       |     | 2040 |     | Mbps | C <sub>B</sub> | VIH = 0.5 V, VIL = 0.0 V, terminated, less than 10% loss at 50% duty                                   |
| 1.0 V Programmed Swing                    |     | 725  |     | ps   | C <sub>B</sub> | VIH = 1.0 V, VIL = 0.0 V, terminated, timing error less than +58/-35 ps                                |
|                                           |     | 725  |     | ps   | C <sub>B</sub> | VIH = 1.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss                                     |
| Maximum Toggle Rate                       |     | 2040 |     | Mbps | C <sub>B</sub> | VIH = 1.0 V, VIL = 0.0 V, terminated, less than 10% loss at 50% duty                                   |
| 2.0 V Programmed Swing                    |     | 725  |     | ps   | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, timing error less than +80/-48 ps                                |
|                                           |     | 725  |     | ps   | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss                                     |
| Maximum Toggle Rate                       |     | 1400 |     | Mbps | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, less than 10% loss at 50% duty                                   |
| 3.0 V Programmed Swing                    |     | 900  |     | ps   | C <sub>B</sub> | VIH = 3.0 V, VIL = 0.0 V, terminated, timing error less than +50/-83 ps                                |
|                                           |     | 900  |     | ps   | C <sub>B</sub> | VIH = 3.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss                                     |
| Maximum Toggle Rate                       |     | 1100 |     | Mbps | C <sub>B</sub> | VIH = 3.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss at 50% duty cycle                   |
| Dynamic Performance, Drive (VIH to VIL)   |     |      |     |      |                | Toggle DATx                                                                                            |

## SPECIFICATIONS

Table 2.

| Parameter                                                 | Min | Typ  | Max | Unit     | Test Level     | Test Conditions/Comments                                                                         |
|-----------------------------------------------------------|-----|------|-----|----------|----------------|--------------------------------------------------------------------------------------------------|
| Propagation Delay Time                                    |     | 1.26 |     | ns       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated                                                             |
| Propagation Delay Tempco                                  |     | 1.4  |     | ps/°C    | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated                                                             |
| Delay Matching, Edge to Edge                              |     | 43   |     | ps       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, rising vs. falling                                         |
| Delay Matching, Channel to Channel                        |     | 32   |     | ps       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, rising vs. rising, falling vs. falling                     |
| Delay Change vs. Duty Cycle                               |     | -28  |     | ps       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, 5% to 95% duty cycle                                       |
| Overshoot and Undershoot                                  |     | -116 |     | mV       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, driver CLC set to 0                                        |
| Settling Time (VIH to VIL)                                |     |      |     |          |                | Toggle DATx                                                                                      |
| To Within 3% of Final Value                               |     | 1.7  |     | ns       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated                                                             |
| To Within 1% of Final Value                               |     | 45   |     | ns       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated                                                             |
| Dynamic Performance, VTerm (VIH or VIL to/from VIT)       |     |      |     |          |                | Toggle RCVx                                                                                      |
| Propagation Delay Time                                    |     | 1.39 |     | ns       | C <sub>B</sub> | VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated                                                |
| Propagation Delay Tempco                                  |     | 2.3  |     | ps/°C    | C <sub>B</sub> | VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated                                                |
| Transition Time, Active to VIT                            |     | 310  |     | ps       | C <sub>B</sub> | 20% to 80%, VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated                                    |
| Transition Time, VIT to Active                            |     | 329  |     | ps       | C <sub>B</sub> | 20% to 80%, VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated                                    |
| Dynamic Performance, Inhibit (VIH or VIL to/from Inhibit) |     |      |     |          |                | Toggle RCVx                                                                                      |
| Transition Time, Inhibit to Active                        |     | 357  |     | ps       | C <sub>B</sub> | 20% to 80%, VIH = +1.0 V, VIL = -1.0 V, terminated                                               |
| Transition Time, Active to Inhibit                        |     | 1.34 |     | ns       | C <sub>B</sub> | 20% to 80%, VIH = +1.0 V, VIL = -1.0 V, terminated                                               |
| Prop Delay, Inhibit to VIH                                |     | 2.6  |     | ns       | C <sub>B</sub> | VIH = +1.0 V, VIL = -1.0 V, terminated; measured from RCVx input crossing to DUTx pin output 50% |
| Prop Delay, Inhibit to VIL                                |     | 2.8  |     | ns       | C <sub>B</sub> | VIH = +1.0 V, VIL = -1.0 V, terminated                                                           |
| Prop Delay Matching, Inhibit to VIL vs. Inhibit to VIH    |     | 52   |     | ps       | C <sub>B</sub> | VIH = +1.0 V, VIL = -1.0 V, terminated                                                           |
| Prop Delay, VIH to Inhibit                                |     | 2.29 |     | ns       | C <sub>B</sub> | VIH = +1.0 V, VIL = -1.0 V, terminated, measured from RCVx input crossing to DUTx pin output 50% |
| Prop Delay, VIL to Inhibit                                |     | 2.02 |     | ns       | C <sub>B</sub> | VIH = +1.0 V, VIL = -1.0 V, terminated                                                           |
| I/O Spike                                                 |     | 24   |     | mV pk-pk | C <sub>B</sub> | VIH = 0.0 V, VIL = 0.0 V, terminated                                                             |
| Driver Pre-Emphasis (CLC)                                 |     |      |     |          |                |                                                                                                  |
| Pre-Emphasis Amplitude Rising                             |     | 35   |     | %        | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 7                                       |
|                                                           |     | 14   |     | %        | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 0                                       |
| Pre-Emphasis Amplitude Falling                            |     | 24   |     | %        | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 7                                       |
|                                                           |     | 16   |     | %        | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 0                                       |
| Pre-Emphasis Resolution                                   |     | 2    |     | %        | D              |                                                                                                  |
| Pre-Emphasis Time Constant                                |     | 0.8  |     | ns       | C <sub>B</sub> | VIH = 2.0 V, VIL = 0.0 V, terminated                                                             |

## REFLECTION CLAMP SPECIFICATIONS

Clamp accuracy specifications apply only when VCH – VCL > 0.8 V.

Table 3.

| Parameter                  | Min  | Typ  | Max  | Unit  | Test Level     | Test Conditions/Comments                                               |
|----------------------------|------|------|------|-------|----------------|------------------------------------------------------------------------|
| VCH/VCL PROGRAMMABLE RANGE | -2.5 |      | +7.5 | V     | D              | DC specifications apply over full functional range unless noted        |
| VCH                        |      |      |      |       |                |                                                                        |
| VCH Functional Range       | -1.2 |      | +7.0 | V     | D              |                                                                        |
| VCH Offset Error           | -300 |      | +300 | mV    | P              | Driver high-Z, sinking 1 mA, measured at DAC Code 0x4000, uncalibrated |
| VCH Offset Tempco          |      | ±0.5 |      | mV/°C | C <sub>T</sub> |                                                                        |

## SPECIFICATIONS

Table 3.

| Parameter                   | Min  | Typ  | Max  | Unit   | Test Level     | Test Conditions/Comments                                                                                                                                                          |
|-----------------------------|------|------|------|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCH Gain                    | 1.0  |      | 1.1  | V/V    | P              | Driver high-Z, sinking 1 mA, gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V), based on ideal DAC transfer function (see Table 21)               |
| VCH Gain Tempco             |      | ±30  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                   |
| VCH Resolution              |      | 153  |      | μV     | D              |                                                                                                                                                                                   |
| VCH DNL                     |      | ±1   |      | mV     | C <sub>T</sub> | Driver high-Z, sinking 1 mA, after two point gain/offset calibration; calibration points at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V), measured over functional clamp range |
| VCH INL                     | -20  |      | +20  | mV     | P              | Driver high-Z, sinking 1 mA, after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (5 V), measured over functional clamp range                   |
| VCL                         |      |      |      |        |                |                                                                                                                                                                                   |
| VCL Functional Range        | -2   |      | +6.2 | V      | D              |                                                                                                                                                                                   |
| VCL Offset Error            | -300 |      | +300 | mV     | P              | Driver high-Z, sourcing 1 mA, measured at DAC Code 0x4000, uncalibrated                                                                                                           |
| VCL Offset Tempco           |      | ±0.5 |      | mV/°C  | C <sub>T</sub> |                                                                                                                                                                                   |
| VCL Gain                    | 1.0  |      | 1.1  | V/V    | P              | Drive high-Z, sourcing 1 mA, gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V), based on ideal DAC transfer function (see Table 21)               |
| VCL Gain Tempco             |      | ±30  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                   |
| VCL Resolution              |      | 153  |      | μV     | D              |                                                                                                                                                                                   |
| VCL DNL                     |      | ±1   |      | mV     | C <sub>T</sub> | Driver high-Z, sourcing 1 mA, after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (+5 V), measured over functional clamp range                 |
| VCL INL                     | -20  |      | +20  | mV     | P              | Driver high-Z, sourcing 1 mA, after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (+5 V), measured over functional clamp range                 |
| DC Clamp Current Limit, VCH | -120 |      | -75  | mA     | P              | Driver high-Z, VCH = 0 V, VCL = -2.0 V, VDUTx = +5.0 V                                                                                                                            |
| DC Clamp Current Limit, VCL | +75  |      | +120 | mA     | P              | Driver high-Z, VCH = +6.0 V, VCL = +5.0 V, VDUTx = 0.0 V                                                                                                                          |
| DUTGND Voltage Accuracy     | -7   | ±2   | +7   | mV     | P              | Over ±0.1 V range, measured at end points of VCH and VCL functional range                                                                                                         |

## NORMAL WINDOW COMPARATOR (NWC) SPECIFICATIONS

VOH tests at VOL = -1.5 V, VOL tests at VOH = +6.5 V, specifications apply to both comparators, unless otherwise specified.

Table 4.

| Parameter                       | Min  | Typ  | Max  | Unit   | Test Level     | Test Conditions/Comments                                                                                                               |
|---------------------------------|------|------|------|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------|
| DC SPECIFICATIONS               |      |      |      |        |                |                                                                                                                                        |
| Input Voltage Range             | -1.5 |      | +6.5 | V      | D              |                                                                                                                                        |
| Differential Voltage Range      | ±0.1 |      | ±8.0 | V      | D              |                                                                                                                                        |
| Comparator Input Offset Voltage | -250 |      | +250 | mV     | P              | Measured at DAC Code 0x4000 (0V), uncalibrated                                                                                         |
| Input Offset Voltage Tempco     |      | ±100 |      | μV/°C  | C <sub>T</sub> |                                                                                                                                        |
| Gain                            | 1.0  |      | 1.1  | V/V    | P              | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21) |
| Gain Tempco                     |      | ±25  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                        |
| Threshold Resolution            |      | 153  |      | μV     | D              |                                                                                                                                        |

## SPECIFICATIONS

Table 4.

| Parameter                                                    | Min        | Typ        | Max  | Unit  | Test Level     | Test Conditions/Comments                                                                                                                                                                                                |
|--------------------------------------------------------------|------------|------------|------|-------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Threshold DNL                                                |            | ±1         |      | mV    | C <sub>T</sub> | Measured over –1.5 V to +6.5 V functional range after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (5 V)                                                                            |
| Threshold INL                                                | –7         |            | +7   | mV    | P              | Measured over –1.5 V to +6.5 V functional range after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (5 V)                                                                            |
| DUTGND Voltage Accuracy                                      | –7         | ±2         | +7   | mV    | P              | Over ±0.1 V range; measured at end points of VOH and VOL functional range                                                                                                                                               |
| Uncertainty Band                                             |            | 5          |      | mV    | C <sub>B</sub> | VDUTx = 0 V, sweep comparator threshold to determine the uncertainty band                                                                                                                                               |
| Maximum Programmable Hysteresis                              |            | 96         |      | mV    | C <sub>B</sub> |                                                                                                                                                                                                                         |
| Hysteresis Resolution                                        |            | 5          |      | mV    | D              | Calculated over hysteresis control Code 10 to Code 31                                                                                                                                                                   |
| DC PSRR                                                      |            | ±5         |      | mV/V  | C <sub>T</sub> | Measured at calibration points                                                                                                                                                                                          |
| Digital Output Characteristics                               |            |            |      |       |                |                                                                                                                                                                                                                         |
| Internal Pull-Up Resistance to Comparator, VTTC              | 46         | 50         | 54   | Ω     | P              | Pull 1 mA and 10 mA from Logic 1 leg and measure ΔV to calculate resistance; measured ΔV/9 mA; done for both comparator logic states                                                                                    |
| Comparator Termination Voltage, VTTC                         | 0.5        | 1.2        | 3.3  | V     | D              |                                                                                                                                                                                                                         |
| Common Mode Voltage                                          |            | VTTC – 0.3 |      | V     | C <sub>T</sub> | Measured with 100 Ω differential termination                                                                                                                                                                            |
|                                                              | VTTC – 0.5 |            | VTTC | V     | P              | Measured with no external termination                                                                                                                                                                                   |
| Differential Voltage                                         |            | 250        |      | mV    | C <sub>T</sub> | Measured with 100 Ω differential termination                                                                                                                                                                            |
|                                                              | 450        | 500        | 550  | mV    | P              | Measured with no external termination                                                                                                                                                                                   |
| Rise/Fall Times, 20% to 80%                                  |            | 166        |      | ps    | C <sub>B</sub> | Measured with 50 Ω to external termination voltage (VTTC)                                                                                                                                                               |
| AC SPECIFICATIONS                                            |            |            |      |       |                |                                                                                                                                                                                                                         |
|                                                              |            |            |      |       |                | All ac specifications performed after dc level calibration, input transition time of ~200 ps, 20% to 80%, measured with 50 Ω to external termination voltage (VTTC); peaking set to CLC = 2, unless otherwise specified |
| Propagation Delay, Input to Output                           |            | 0.93       |      | ns    | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V                                                                                                                                  |
| Propagation Delay Tempco                                     |            | 1.6        |      | ps/°C | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V                                                                                                                                  |
| Propagation Delay Matching High Transition to Low Transition |            | 7          |      | ps    | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V                                                                                                                                  |
| Propagation Delay Matching High to Low Comparator            |            | 7          |      | ps    | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V                                                                                                                                  |
| Propagation Delay Dispersion                                 |            |            |      |       |                |                                                                                                                                                                                                                         |
| Slew Rate                                                    |            | 19         |      | ps    | C <sub>B</sub> | VDUTx: 0 V to 0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.25 V                                                                                                                                 |
| 400 ps vs. 1 ns (20% to 80%)                                 |            |            |      |       |                |                                                                                                                                                                                                                         |
| Overdrive                                                    |            | 40         |      | ps    | C <sub>B</sub> | For 250 mV, VDUTx: 0 V to 0.5 V swing; for 1.0 V, VDUTx: 0 V to 1.25 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.25 V                                                                              |
| 250 mV vs. 1.0 V                                             |            |            |      |       |                |                                                                                                                                                                                                                         |
| 1 V Pulse Width                                              |            | +2/– 17    |      | ps    | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing at ~32.0 MHz; driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V                                                                                                                     |
| 0.7 ns, 1 ns, 5 ns, 10 ns                                    |            |            |      |       |                |                                                                                                                                                                                                                         |
| 0.5 V Pulse Width                                            |            | +3/– 24    |      | ps    | C <sub>B</sub> | VDUTx: 0 V to 0.5 V swing at ~32.0 MHz, driver term mode, VIT = 0.0 V; comparator threshold = 0.25 V                                                                                                                    |
| 0.6 ns, 1 ns, 5 ns, 10 ns                                    |            |            |      |       |                |                                                                                                                                                                                                                         |
| Duty Cycle                                                   |            | 21         |      | ps    | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing at ~32.0 MHz; driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V                                                                                                                     |
| 5% to 95%                                                    |            |            |      |       |                |                                                                                                                                                                                                                         |

## SPECIFICATIONS

Table 4.

| Parameter                              | Min | Typ  | Max | Unit      | Test Level     | Test Conditions/Comments                                                                                                                                              |
|----------------------------------------|-----|------|-----|-----------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Minimum Detectable Pulse Width         |     | 0.5  |     | ns        | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing at 32.0 MHz, driver term mode, VIT = 0.0 V; greater than 50% output differential amplitude                                                  |
| Input Equivalent Bandwidth, Terminated |     | 1520 |     | MHz       | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing; driver term mode, VIT = 0.0 V, CLC = 2; as measured by shmoo plot; $f_{\text{EQUIV}} = 0.22/\sqrt{(t_{\text{MEAS}}^2 - t_{\text{DUT}}^2)}$ |
| ERT High-Z Mode, 3 V, 20% to 80%       |     | 721  |     | ps        | C <sub>B</sub> | VDUTx: 0 V to 3.0 V swing, driver high-Z as measured by shmoo plot; $f_{\text{EQUIV}} = 0.22/\sqrt{(t_{\text{MEAS}}^2 - t_{\text{DUT}}^2)}$                           |
| Comparator Pre-Emphasis (CLC)          |     |      |     |           |                |                                                                                                                                                                       |
| CLC Amplitude Range                    |     | 16   |     | %         | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator pre-emphasis set to maximum                                                                      |
| CLC Resolution                         |     | 2.3  |     | % per bit | C <sub>B</sub> | 3-bit amplitude control                                                                                                                                               |
| Pre-Emphasis Time Constant             |     | 4.3  |     | ns        | C <sub>B</sub> | VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator pre-emphasis set to maximum                                                                      |

## DIFFERENTIAL MODE COMPARATOR (DMC) SPECIFICATIONS

VOH tests at VOL = -1.1 V, VOL tests at VOH = +1.1 V, unless otherwise specified.

Table 5.

| Parameter                       | Min   | Typ  | Max  | Unit   | Test Level     | Test Conditions/Comments                                                                                                                                                                                                           |
|---------------------------------|-------|------|------|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DC SPECIFICATIONS               |       |      |      |        |                |                                                                                                                                                                                                                                    |
| Input Voltage Range             | -1.5  |      | +6.5 | V      | D              |                                                                                                                                                                                                                                    |
| Functional Differential Range   | ±0.05 |      | ±1.1 | V      | D              |                                                                                                                                                                                                                                    |
| Maximum Differential Input      |       |      | ±8   | V      | D              |                                                                                                                                                                                                                                    |
| Input Offset Voltage            | -250  |      | +250 | mV     | P              | Offset extrapolated from measurements at DAC Code 0x2666 (-1 V) and DAC Code 0x599A (+1 V), with V <sub>CM</sub> = 0 V                                                                                                             |
| Offset Voltage Tempco           |       | ±150 |      | μV/°C  | C <sub>T</sub> |                                                                                                                                                                                                                                    |
| Gain                            | 1.0   |      | 1.1  | V/V    | P              | Gain derived from measurements at DAC Code 0x2666 (-1 V) and DAC Code 0x599A (+1 V), based on ideal DAC transfer function (see Table 21)                                                                                           |
| Gain Tempco                     |       | ±25  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                                                                    |
| VOH, VOL Resolution             |       | 153  |      | μV     | D              |                                                                                                                                                                                                                                    |
| VOH, VOL DNL                    |       | ±1   |      | mV     | C <sub>T</sub> | After two point gain/offset calibration, V <sub>CM</sub> = 0.0 V, calibration points at 0x2666 (-1 V) and 0x599A (+1 V)                                                                                                            |
| VOH, VOL INL                    | -7    |      | +7   | mV     | P              | After two point gain/offset calibration, measured over VOH/VOL range of -1.1 V to +1.1 V, V <sub>CM</sub> = 0.0 V; calibration points at 0x2666 (-1 V) and 0x599A (+1 V)                                                           |
| Uncertainty Band                |       | 7    |      | mV     | C <sub>B</sub> | VDUTx = 0 V; sweep comparator threshold to determine the uncertainty band                                                                                                                                                          |
| Maximum Programmable Hysteresis |       | 117  |      | mV     | C <sub>B</sub> |                                                                                                                                                                                                                                    |
| Hysteresis Resolution           |       | 5.6  |      | mV     | D              | Calculated over hysteresis control Code 10 to Code 31                                                                                                                                                                              |
| CMRR                            | -1    |      | +1   | mV/V   | P              | Offset measured at V <sub>CM</sub> = -1.5 V and +6.5 V with V <sub>DM</sub> = 0.0 V, offset error change                                                                                                                           |
| DC PSRR                         |       | ±5   |      | mV/V   | C <sub>T</sub> | Measured at calibration points                                                                                                                                                                                                     |
| AC SPECIFICATIONS               |       |      |      |        |                |                                                                                                                                                                                                                                    |
|                                 |       |      |      |        |                | All ac specifications performed after dc level calibration, unless noted; input transition time ~200 ps, 20% to 80%, measured with 50 Ω to external termination voltage (VTTC), peaking set to CLC = 2, unless otherwise specified |

## SPECIFICATIONS

Table 5.

| Parameter                                                     | Min | Typ    | Max | Unit      | Test Level     | Test Conditions/Comments                                                                                                                                                                                                 |
|---------------------------------------------------------------|-----|--------|-----|-----------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Propagation Delay, Input to Output                            |     | 0.83   |     | ns        | C <sub>B</sub> | VDUT0 = 0 V, VDUT1: -0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel                                                                                        |
| Propagation Delay Tempco                                      |     | 2.6    |     | ps/°C     | C <sub>B</sub> | VDUT0 = 0 V, VDUT1: -0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel                                                                                        |
| Propagation Delay Matching, High Transition to Low Transition |     | 15     |     | ps        | C <sub>B</sub> | VDUT0 = 0 V, VDUT1: -0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel                                                                                        |
| Propagation Delay Matching, High to Low Comparator            |     | 17     |     | ps        | C <sub>B</sub> | VDUT0 = 0 V, VDUT1: -0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel                                                                                        |
| Propagation Delay Change (Dispersion) With Respect To         |     |        |     |           |                |                                                                                                                                                                                                                          |
| Slew Rate:                                                    |     | 31     |     | ps        | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.5 V to +0.5 V swing; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V, repeat for other channel                                                                                      |
| 400 ps and 1 ns (20% to 80%)                                  |     |        |     |           |                |                                                                                                                                                                                                                          |
| Overdrive:                                                    |     | 32     |     | ps        | C <sub>B</sub> | VDUT0 = 0.0 V; for 250 mV: VDUT1: 0 V to 0.5 V swing; for 750 mV: VDUT1: 0 V to 1.0 V swing; driver term mode, VIT = 0.0 V; comparator threshold = -0.25 V; repeat for other channel with comparator threshold = +0.25 V |
| 250 mV and 750 mV                                             |     |        |     |           |                |                                                                                                                                                                                                                          |
| 1 V Pulse Width:                                              |     | +1/-21 |     | ps        | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.5 V to +0.5 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; repeat for other channel                                                                            |
| 0.7 ns, 1 ns, 5 ns, 10 ns                                     |     |        |     |           |                |                                                                                                                                                                                                                          |
| 0.5 V Pulse Width:                                            |     | +1/-31 |     | ps        | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.25 V to +0.25 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; repeat for other channel                                                                          |
| 0.6 ns, 1 ns, 5 ns, 10 ns                                     |     |        |     |           |                |                                                                                                                                                                                                                          |
| Duty Cycle:                                                   |     | 18     |     | ps        | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.5 V to +0.5 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; repeat for other channel                                                                            |
| 5% to 95%                                                     |     |        |     |           |                |                                                                                                                                                                                                                          |
| Minimum Detectable Pulse Width                                |     | 0.5    |     | ns        | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.5 V to +0.5 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; greater than 50% output differential amplitude; repeat for other channel                            |
| Input Equivalent Bandwidth, Terminated                        |     | 1038   |     | MHz       | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.5 V to +0.5 V swing; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V, CLC = 2 as measured by shmoo; repeat for other channel                                                        |
| Comparator Pre-Emphasis (CLC)                                 |     |        |     |           |                |                                                                                                                                                                                                                          |
| CLC Amplitude Range                                           |     | 11     |     | %         | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.8 V to +0.8 V swing, driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; comparator CLC set to maximum; repeat for other channel                                                       |
| CLC Resolution                                                |     | 1.6    |     | % per bit | C <sub>B</sub> | 3-bit amplitude control                                                                                                                                                                                                  |
| Pre-Emphasis Time Constant                                    |     | 4.8    |     | ns        | C <sub>B</sub> | VDUT0 = 0.0 V; VDUT1: -0.8 V to +0.8 V swing, driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; comparator CLC set to maximum; repeat for other channel                                                       |

## SPECIFICATIONS

## ACTIVE LOAD SPECIFICATIONS

Table 6.

| Parameter                                           | Min  | Typ      | Max  | Unit                         | Test Level     | Test Conditions/Comments                                                                                                                                                                                                                          |
|-----------------------------------------------------|------|----------|------|------------------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DC SPECIFICATIONS                                   |      |          |      |                              |                |                                                                                                                                                                                                                                                   |
| Load active on, RCVx active, unless otherwise noted |      |          |      |                              |                |                                                                                                                                                                                                                                                   |
| Input Characteristics                               |      |          |      |                              |                |                                                                                                                                                                                                                                                   |
| VCOM Voltage Range                                  | -1.5 |          | +6.5 | V                            | D              | $ I_{OL} \text{ and } I_{OH}  \leq 1 \text{ mA}$                                                                                                                                                                                                  |
|                                                     | -1.0 |          | +5.5 | V                            | D              | $ I_{OL} \text{ and } I_{OH}  \leq 25 \text{ mA}$                                                                                                                                                                                                 |
| VCOM Offset                                         | -200 |          | +200 | mV                           | P              | Measured at DAC Code 0x4000, uncalibrated                                                                                                                                                                                                         |
| VCOM Offset Tempco                                  |      | $\pm 25$ |      | $\mu\text{V}/^\circ\text{C}$ | C <sub>T</sub> |                                                                                                                                                                                                                                                   |
| VCOM Gain                                           | 1.0  |          | 1.1  | V/V                          | P              | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (+5 V), based on ideal DAC transfer function (see <a href="#">Table 21</a> )                                                                                          |
| VCOM Gain Tempco                                    |      | $\pm 25$ |      | ppm/ $^\circ\text{C}$        | C <sub>T</sub> |                                                                                                                                                                                                                                                   |
| VCOM Resolution                                     |      | 153      |      | $\mu\text{V}$                | D              |                                                                                                                                                                                                                                                   |
| VCOM DNL                                            |      | $\pm 1$  |      | mV                           | C <sub>T</sub> | $I_{OH} = I_{OL} = 12.5 \text{ mA}$ ; after two point gain/offset calibration; measured over VCOM range of -1.5 V to +6.5 V; calibration points at 0x4000 (0 V) and 0xC000 (+5 V)                                                                 |
| VCOM INL                                            | -7   |          | +7   | mV                           | P              | $I_{OH} = I_{OL} = 12.5 \text{ mA}$ ; after two point gain/offset calibration; measured at end points of VCOM functional range                                                                                                                    |
| DUTGND Voltage Accuracy                             | -7   | $\pm 2$  | +7   | mV                           | P              | Over $\pm 0.1 \text{ V}$ range                                                                                                                                                                                                                    |
| Output Characteristics                              |      |          |      |                              |                |                                                                                                                                                                                                                                                   |
| Maximum Source Current                              | 25   |          |      | mA                           | D              | -1.5 V to +5.5 V DUT range                                                                                                                                                                                                                        |
| IOL Offset                                          | -600 |          | +600 | $\mu\text{A}$                | P              | $I_{OH} = -2.5 \text{ mA}$ , VCOM = 1.5 V, VDUTx = 0.0 V; offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)                                                                                             |
| IOL Offset Tempco                                   |      | $\pm 1$  |      | $\mu\text{A}/^\circ\text{C}$ | C <sub>T</sub> |                                                                                                                                                                                                                                                   |
| IOL Gain Error                                      | 0    |          | 25   | %                            | P              | $I_{OH} = -2.5 \text{ mA}$ , VCOM = 1.5 V, VDUTx = 0.0 V; gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on ideal DAC transfer function (see <a href="#">Table 21</a> and <a href="#">Table 22</a> ) |
| IOL Gain Tempco                                     |      | $\pm 25$ |      | ppm/ $^\circ\text{C}$        | C <sub>T</sub> |                                                                                                                                                                                                                                                   |
| IOL Resolution                                      |      | 763      |      | nA                           | D              |                                                                                                                                                                                                                                                   |
| IOL DNL                                             |      | $\pm 4$  |      | $\mu\text{A}$                | C <sub>T</sub> | $I_{OH} = -2.5 \text{ mA}$ , VCOM = 1.5 V, VDUTx = 0.0 V; after two point gain/offset calibration; measured over IOL range, 0 mA to 25 mA; calibrated at Code 0x451F (1 mA) and Code 0xA666 (20 mA)                                               |
| IOL INL                                             | -100 | $\pm 20$ | +100 | $\mu\text{A}$                | P              | $I_{OH} = -2.5 \text{ mA}$ , VCOM = 1.5 V, VDUTx = 0.0 V; after two point gain/offset calibration                                                                                                                                                 |
| IOL 90% Commutation Voltage                         |      | 0.25     | 0.4  | V                            | P              | $I_{OH} = I_{OL} = 25 \text{ mA}$ , VCOM = 2.0 V; measure IOL reference at VDUTx = -1.0 V; measure IOL current at VDUTx = 1.6 V; check >90% of reference current                                                                                  |
| IOL 90% Commutation Voltage                         |      | 0.1      |      | V                            | C <sub>T</sub> | $I_{OH} = I_{OL} = 1 \text{ mA}$ , VCOM = 2.0 V; measure IOL reference at VDUTx = -1.0 V; measure IOL current at VDUTx = 1.9 V; check >90% of reference current                                                                                   |
| Maximum Sink Current                                | 25   |          |      | mA                           | D              | -1.0 V to +6.5 V output range                                                                                                                                                                                                                     |
| IOH Offset                                          | -600 |          | +600 | $\mu\text{A}$                | P              | $I_{OL} = -2.5 \text{ mA}$ , VCOM = 1.5 V, VDUTx = 3.0 V; offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)                                                                                             |
| IOH Offset Tempco                                   |      | $\pm 1$  |      | $\mu\text{A}/^\circ\text{C}$ | C <sub>T</sub> |                                                                                                                                                                                                                                                   |

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Table 6.

| Parameter                                                      | Min  | Typ  | Max  | Unit     | Test Level     | Test Conditions/Comments                                                                                                                                                                                                                      |
|----------------------------------------------------------------|------|------|------|----------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IOH Gain Error                                                 | 0    |      | 25   | %        | P              | IOL = -2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on ideal DAC transfer function (see Table 21 and Table 22)                                            |
| IOH Gain Tempco                                                |      | ±25  |      | ppm/°C   | C <sub>T</sub> |                                                                                                                                                                                                                                               |
| IOH Resolution                                                 |      | 763  |      | nA       | D              |                                                                                                                                                                                                                                               |
| IOH DNL                                                        |      | ±4   |      | μA       | C <sub>T</sub> | IOL = -2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; after two point gain/offset calibration; measured over IOH range, 0 mA to 25 mA; calibrated at Code 0x451F (1 mA) and Code 0xA666 (20 mA)                                                         |
| IOH INL                                                        | -100 | ±25  | +100 | μA       | P              | IOL = -2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; after two point gain/offset calibration                                                                                                                                                           |
| IOH 90% Commutation Voltage                                    |      | 0.25 | 0.4  | V        | P              | IOH = IOL = 25 mA, VCOM = 2.0 V; measure IOH reference at VDUTx = 5.0 V; measure IOH current at VDUTx = 2.4 V; ensure >90% of reference current                                                                                               |
|                                                                |      | 0.1  |      | V        | C <sub>T</sub> | IOH = IOL = 1 mA, VCOM = 2.0 V; measure IOH reference at VDUTx = 5.0 V; measure IOH current at VDUTx = 2.1 V; ensure >90% of reference current                                                                                                |
| AC SPECIFICATIONS                                              |      |      |      |          |                |                                                                                                                                                                                                                                               |
| Dynamic Performance                                            |      |      |      |          |                | All ac specifications performed after dc level calibration unless noted; load active on                                                                                                                                                       |
| Propagation Delay, Load Active On to Load Active Off; 50%, 90% |      | 3.1  |      | ns       | C <sub>B</sub> | Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and -1.5 V for IOH; measured from 50% point of RCVx - $\overline{RCVx}$ to 90% point of final output; repeat for drive low and drive high |
| Propagation Delay, Load Active Off to Load Active On; 50%, 90% |      | 4.1  |      | ns       | C <sub>B</sub> | Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and -1.5 V for IOH; measured from 50% point of RCVx - $\overline{RCVx}$ to 90% point of final output; repeat for drive low and drive high |
| Propagation Delay Matching                                     |      | 1.0  |      | ns       | C <sub>B</sub> | Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and -1.5 V for IOH; active on vs. active off; repeat for drive low and drive high                                                         |
| Load Spike                                                     |      | 106  |      | mV pk-pk | C <sub>B</sub> | Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 0 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and -1.5 V for IOH; repeat for drive low and drive high                                                                                    |
| Settling Time to 90%                                           |      | 1.6  |      | ns       | C <sub>B</sub> | Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and -1.5 V for IOH; measured at 90% of final value                                                                                        |

## PPMU SPECIFICATIONS

PPMU enabled in FV, DCL disabled.

Table 7.

| Parameter       | Min  | Typ | Max  | Unit | Test Level | Test Conditions/Comments |
|-----------------|------|-----|------|------|------------|--------------------------|
| FORCE VOLTAGE   |      |     |      |      |            |                          |
| Current Range A | -40  |     | +40  | mA   | D          |                          |
| Current Range B | -1   |     | +1   | mA   | D          |                          |
| Current Range C | -100 |     | +100 | μA   | D          |                          |
| Current Range D | -10  |     | +10  | μA   | D          |                          |
| Current Range E | -2   |     | +2   | μA   | D          |                          |

## SPECIFICATIONS

Table 7.

| Parameter                                 | Min  | Typ      | Max   | Unit                         | Test Level     | Test Conditions/Comments                                                                                                                                                                      |
|-------------------------------------------|------|----------|-------|------------------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Voltage Range at Output                   |      |          |       |                              |                |                                                                                                                                                                                               |
| Range A                                   | -2.0 |          | +5.75 | V                            | D              | Output range for full-scale source and sink                                                                                                                                                   |
|                                           | -2.0 |          | +6    | V                            | D              | Output range for $\pm 25$ mA                                                                                                                                                                  |
| Range B, Range C, Range D, and Range E    | -2.0 |          | +6.5  | V                            | D              | Output range for full-scale source and sink                                                                                                                                                   |
| Offset                                    |      |          |       |                              |                |                                                                                                                                                                                               |
| Range C                                   | -100 |          | +100  | mV                           | P              | Measured at DAC Code 0x4000 (0 V)                                                                                                                                                             |
| All Ranges                                |      | $\pm 10$ |       | mV                           | C <sub>T</sub> | Measured at DAC Code 0x4000 (0 V)                                                                                                                                                             |
| Offset Tempco, All Ranges                 |      | $\pm 25$ |       | $\mu\text{V}/^\circ\text{C}$ | C <sub>T</sub> |                                                                                                                                                                                               |
| Gain                                      |      |          |       |                              |                |                                                                                                                                                                                               |
| Range C                                   | 1.0  |          | 1.1   | V/V                          | P              | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21 and Table 23)                                           |
| All Ranges                                |      | 1.05     |       | V/V                          | C <sub>T</sub> | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21 and Table 23)                                           |
| Gain Tempco, All Ranges                   |      | $\pm 25$ |       | ppm/ $^\circ\text{C}$        | C <sub>T</sub> | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); calibration point 0x4000 (0 V) and 0xC000 (+5 V) output                                                    |
| INL                                       |      |          |       |                              |                |                                                                                                                                                                                               |
| Range A                                   |      | $\pm 1$  |       | mV                           | CT             | After two point gain/offset calibration, output range of -2.0 V to +5.75 V, PPMU Current Range A only                                                                                         |
| Range C                                   | -1.7 |          | +1.7  | mV                           | P              | After two point gain/offset calibration; output range of -2.0 V to +6.5 V                                                                                                                     |
| Range B, Range D, and Range E             |      | $\pm 1$  |       | mV                           | C <sub>T</sub> | After two point gain/offset calibration, output range of -2.0 V to +6.5 V                                                                                                                     |
| Compliance vs. Current Load               |      |          |       |                              |                |                                                                                                                                                                                               |
| Range A                                   |      | $\pm 40$ |       | mV                           | C <sub>T</sub> | Force -2.0 V; measure voltage while sinking zero and full-scale current; measure $\Delta V$ ; force +5.75 V; measure voltage while sourcing zero and full-scale current; measure $\Delta V$ . |
|                                           |      | $\pm 25$ |       | mV                           | C <sub>T</sub> | Force -2.0 V; measure voltage while sinking zero and 25 mA current; measure $\Delta V$ ; force +6 V; measure voltage while sourcing zero and 25 mA current; measure $\Delta V$ .              |
| Range B, Range C, Range D, and Range E    |      | $\pm 1$  |       | mV                           | C <sub>T</sub> | Force -2.0 V; measure voltage while sinking zero and full-scale current; measure $\Delta V$ ; force +6.5 V; measure voltage while sourcing zero and full-scale current; measure $\Delta V$ .  |
| Current Limit, Source and Sink All Ranges | 120  | 140      | 180   | %FS                          | P              | Sink: force -2.0 V, short DUTx to +6.5 V; source: force +6.5 V, short DUTx to -2.0 V; repeat for each current range; example: Range A<br>FS = 40 mA,<br>120% FS = 48 mA<br>180% FS = 72 mA    |
| DUTGND Voltage Accuracy                   | -7   | $\pm 2$  | +7    | mV                           | P              | Over $\pm 0.1$ V range; measured at endpoints of PPMU_VIN <sub>FS</sub> functional range (see Figure 135)                                                                                     |

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Table 7.

| Parameter                                                                      | Min   | Typ          | Max   | Unit               | Test Level     | Test Conditions/Comments                                                                                                                                                                                                                                       |
|--------------------------------------------------------------------------------|-------|--------------|-------|--------------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MEASURE CURRENT                                                                |       |              |       |                    |                | PPMU enabled in FIMI, DCL disabled                                                                                                                                                                                                                             |
| DUTx Pin Voltage Range at Full Current                                         |       |              |       |                    |                |                                                                                                                                                                                                                                                                |
| Range A                                                                        | -2.0  |              | +5.75 | V                  | D              |                                                                                                                                                                                                                                                                |
| Range B, Range C, Range D, and Range E                                         | -2.0  |              | +6.5  | V                  | D              |                                                                                                                                                                                                                                                                |
| Zero-Current Offset, Range B                                                   | -2    |              | +2    | %FSR               | P              | Interpolated from measurements sourcing and sinking 80% FSR current each range; FSR = 80 mA for Range A, 2 mA for Range B, 200 $\mu$ A for Range C, 20 $\mu$ A for Range D, 4 $\mu$ A for Range E (see <a href="#">Table 21</a> and <a href="#">Table 23</a> ) |
| All Ranges                                                                     |       | $\pm 0.5$    |       | %FSR               | C <sub>T</sub> | See <a href="#">Table 21</a> and <a href="#">Table 23</a>                                                                                                                                                                                                      |
| Zero-Current Offset Tempco, Range A                                            |       | $\pm 0.001$  |       | %FSR/ $^{\circ}$ C | C <sub>T</sub> | See <a href="#">Table 21</a> and <a href="#">Table 23</a>                                                                                                                                                                                                      |
| Range B, Range C, and Range D                                                  |       | $\pm 0.001$  |       | %FSR/ $^{\circ}$ C | C <sub>T</sub> |                                                                                                                                                                                                                                                                |
| Range E                                                                        |       | $\pm 0.002$  |       | %FSR/ $^{\circ}$ C | C <sub>T</sub> |                                                                                                                                                                                                                                                                |
| Gain Error                                                                     |       |              |       |                    |                |                                                                                                                                                                                                                                                                |
| Range B                                                                        | -30   |              | +5    | %                  | P              | Based on measurements sourcing and sinking, 80% FSR current                                                                                                                                                                                                    |
| All Ranges                                                                     |       | -10          |       | %                  | C <sub>T</sub> | Based on measurements sourcing and sinking, 80% FSR current                                                                                                                                                                                                    |
| Gain Tempco                                                                    |       |              |       |                    |                |                                                                                                                                                                                                                                                                |
| Range A                                                                        |       | $\pm 50$     |       | ppm/ $^{\circ}$ C  | C <sub>T</sub> |                                                                                                                                                                                                                                                                |
| Range B, Range C, Range D, and Range E                                         |       | $\pm 25$     |       | ppm/ $^{\circ}$ C  | C <sub>T</sub> |                                                                                                                                                                                                                                                                |
| INL                                                                            |       |              |       |                    |                |                                                                                                                                                                                                                                                                |
| Range A                                                                        |       | $\pm 0.0125$ |       | %FSR               | C <sub>T</sub> | Range A, after two point gain/offset calibration at $\pm 80\%$ FSR current; measured over FSR output of -40 mA to +40 mA                                                                                                                                       |
| Range B                                                                        | -0.03 |              | +0.03 | %FSR               | P              | After two point gain/offset calibration at $\pm 80\%$ FSR current; measured over FSR output of -1 mA to +1 mA                                                                                                                                                  |
| Range C, Range D, and Range E                                                  |       | $\pm 0.01$   |       | %FSR               | C <sub>T</sub> | After two point gain/offset calibration at $\pm 80\%$ FSR current; measured over each FSR output for Range C, Range D, and Range E                                                                                                                             |
| DUTx Pin Voltage Rejection                                                     | -1.2  |              | +1.2  | $\mu$ A            | P              | Range B, FVMI, force -1 V and +5 V into load of 0.5 mA, measure $\Delta I$ reported at PPMU_MEASx pin                                                                                                                                                          |
| DUTGND Voltage Accuracy                                                        | -7    | $\pm 2$      | +7    | mV                 | P              | Over $\pm 0.1$ V range (see <a href="#">Figure 135</a> )                                                                                                                                                                                                       |
| FORCE CURRENT                                                                  |       |              |       |                    |                | PPMU enabled in FIMI, DCL disabled                                                                                                                                                                                                                             |
| DUTx Pin Voltage Range in Range A                                              | -2.0  |              | +5.75 | V                  | D              | At full-scale source and sink current                                                                                                                                                                                                                          |
|                                                                                | -2.0  |              | +6    | V                  | D              | At 25 mA source and sink current                                                                                                                                                                                                                               |
| DUTx Pin Voltage Range at Full Current, Range B, Range C, Range D, and Range E | -2.0  |              | +6.5  | V                  | D              |                                                                                                                                                                                                                                                                |
| Zero-Current Offset, All Ranges                                                | -14.5 |              | +14.5 | %FSR               | P              | Extrapolated from measurements at Code 0x4CCC and Code 0xB333 for each range (see <a href="#">Table 21</a> and <a href="#">Table 23</a> )                                                                                                                      |
| Zero-Current Offset Tempco                                                     |       | $\pm 0.002$  |       | %FSR/ $^{\circ}$ C | C <sub>T</sub> |                                                                                                                                                                                                                                                                |

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Table 7.

| Parameter                                 | Min    | Typ   | Max    | Unit   | Test Level     | Test Conditions/Comments                                                                                                                                                                                       |
|-------------------------------------------|--------|-------|--------|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Gain Error, All Ranges                    | -5     |       | +25    | %      | P              | Derived from measurements at Code 0x4CCC and Code 0xB333 for each range (see Table 21 and Table 23)                                                                                                            |
| Gain Tempco                               |        |       |        |        |                |                                                                                                                                                                                                                |
| Range A                                   |        | ±50   |        | ppm/°C | C <sub>T</sub> | Significant PPMU self-heating effects in Range A can influence gain drift/tempco measurements                                                                                                                  |
| Range B, Range C, Range D, and Range E    |        | ±25   |        | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                                                |
| INL                                       |        |       |        |        |                |                                                                                                                                                                                                                |
| Range A                                   | -0.12  | ±0.02 | +0.12  | %FSR   | P              | After two point gain/offset calibration; measured over FSR output of -40 mA to +40 mA                                                                                                                          |
| Range B, Range C, and Range D             | -0.03  |       | +0.03  | %FSR   | P              | After two point gain/offset calibration; measured over FSR output; repeat for Range B, Range C, and Range D                                                                                                    |
| Range E                                   | -0.045 |       | +0.045 | %FSR   | P              | After two point gain/offset calibration; measured over FSR output                                                                                                                                              |
| Force Current Compliance vs. Voltage Load |        |       |        |        |                |                                                                                                                                                                                                                |
| Range A                                   | -0.3   |       | +0.3   | %FSR   | P              | Force positive full-scale current driving -2.0 V and +5.75 V; measure ΔI at DUTx pin; force negative full-scale current driving -2.0 V and +5.75 V; measure ΔI at DUTx pin                                     |
|                                           | -0.3   |       | +0.3   | %FSR   | P              | Force +25 mA driving -2.0 V and +6.0 V; measure ΔI at DUTx pin; force -25 mA driving -2.0 V and +6.0 V; measure ΔI at DUTx pin                                                                                 |
|                                           | -0.06  |       | +0.06  | %FSR   | P              | Force positive full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin                                         |
| Range B and Range C                       | -0.3   |       | +0.3   | %FSR   | P              | Force positive full-scale current driving -2.0 V and +6.5 V; measure ΔI at DUTx pin; force negative full-scale current driving -2.0 V and +6.5 V; measure ΔI at DUTx pin                                       |
|                                           | -0.06  |       | +0.06  | %FSR   | P              | Force positive full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin                                         |
| Range D                                   | -0.3   |       | +0.3   | %FSR   | P              | Force positive full-scale current driving -2.0 V and +6.5 V; measure ΔI at DUTx pin; force negative full-scale current driving -2.0 V and +6.5 V; measure ΔI at DUTx pin; allows for 10 nA of DUTx pin leakage |
| Range E                                   | -0.85  |       | +0.85  | %FSR   | P              | Force positive full-scale current driving -2.0 V and +6.5 V; measure ΔI at DUTx pin; force negative full-scale current driving -2.0 V and +6.5 V; measure ΔI at DUTx pin; allows for 10 nA of DUTx pin leakage |
| MEASURE VOLTAGE                           |        |       |        |        |                | PPMU enabled, FVMV, DCL disabled                                                                                                                                                                               |
| Voltage Range                             | -2.0   |       | +6.5   | V      | D              |                                                                                                                                                                                                                |
| Offset                                    | -25    |       | +25    | mV     | P              | Range B, VDUTx = 0 V; offset = (PPMU_MEAS - VDUTx)                                                                                                                                                             |
| Offset Tempco                             |        | ±10   |        | μV/°C  | C <sub>T</sub> |                                                                                                                                                                                                                |

## SPECIFICATIONS

Table 7.

| Parameter                             | Min  | Typ  | Max  | Unit   | Test Level     | Test Conditions/Comments                                                                                                                                                                                                                                                               |
|---------------------------------------|------|------|------|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Gain                                  | 0.98 |      | 1.02 | V/V    | P              | Range B, gain derived from measurements at VDUTx = 0.0 V and +5.0 V                                                                                                                                                                                                                    |
| Gain Tempco                           |      | ±1   |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                                                                                                                        |
| INL                                   | -1.7 |      | +1.7 | mV     | P              | Range B, measured over -2.0 V to +6.5 V                                                                                                                                                                                                                                                |
| Measure Pin DC Characteristics        |      |      |      |        |                |                                                                                                                                                                                                                                                                                        |
| Output Range                          | -2.0 |      | +6.5 | V      | D              |                                                                                                                                                                                                                                                                                        |
| DC Output Current                     |      |      | 4    | mA     | D              |                                                                                                                                                                                                                                                                                        |
| Output Impedance                      |      |      | 200  | Ω      | P              | PPMU enabled in FVMV, DCL disabled;<br>Source resistance:<br>PPMU force +6.5 V with 0 mA, +4 mA load<br>Sink resistance:<br>PPMU force -2.0 V with 0 mA, -4 mA load<br>Resistance = $\Delta V/\Delta I$ at PPMU_MEAS pin<br>Tested at -2.0 V and +6.5 V                                |
| Output Leakage Current When Tristated | -1   |      | +1   | μA     | P              |                                                                                                                                                                                                                                                                                        |
| Output Short-Circuit Current          | -25  |      | +25  | mA     | P              | PPMU enabled in FVMV, DCL disabled;<br>Source:<br>PPMU force +6.5 V, PPMU_MEAS to -2.0 V<br>Sink:<br>PPMU force -2.0 V, PPMU_MEAS to +6.5 V                                                                                                                                            |
| PPMU_MEASx Pin, Output Capacitance    |      | 2    |      | pF     | S              |                                                                                                                                                                                                                                                                                        |
| PPMU_MEASx Pin, Load Capacitance      |      | 100  |      | pF     | S              | Maximum load capacitance                                                                                                                                                                                                                                                               |
| VOLTAGE CLAMPS                        |      |      |      |        |                | PPMU enabled in FIMI, DCL disabled, PPMU clamps enabled; clamp accuracy specifications apply only when VCH > VCL                                                                                                                                                                       |
| Low Clamp Range (VCL)                 | -2.0 |      | +4.0 | V      | D              |                                                                                                                                                                                                                                                                                        |
| High Clamp Range (VCH)                | 0.0  |      | +6.5 | V      | D              |                                                                                                                                                                                                                                                                                        |
| Positive Clamp Voltage Droop          | -300 | ±1   | +300 | mV     | P              | $\Delta V$ seen at DUTx pin, Range A, VCH = +5.0 V, VCL = -1 V; PPMU force 5 mA and 40 mA into open                                                                                                                                                                                    |
| Negative Clamp Voltage Droop          | -300 | ±1   | +300 | mV     | P              | $\Delta V$ seen at DUTx pin, Range A, VCH = +5.0 V, VCL = -1 V; PPMU force -5 mA and +40 mA into open                                                                                                                                                                                  |
| Offset, PPMU Clamp VCH/VCL            | -300 |      | +300 | mV     | P              | Range B, PPMU force ±0.5 mA into open; VCH measured at DAC Code 0x4000 (0 V) with VCL at Code 0x0000 (-2.5 V); VCL measured at DAC Code 0x4000 (0 V) with VCH at 0xFFFF (+7.5 V)                                                                                                       |
| Offset Tempco, PPMU Clamp VCH/VCL     |      | ±0.5 |      | mV/°C  | C <sub>T</sub> |                                                                                                                                                                                                                                                                                        |
| Gain, PPMU Clamp VCH/VCL              | 1.0  |      | 1.2  | V/V    | P              | Range B, PPMU force ±0.5 mA into open; VCH gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (+5.0 V) with VCL at Code 0x0000 (-2.5 V); VCL gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xA666 (+4.0 V) with VCH at 0xFFFF (+7.5 V) |
| Gain Tempco, PPMU Clamp VCH/VCL       |      | ±25  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                                                                                                                                        |
| INL, PPMU Clamp VCH/VCL               | -20  |      | +20  | mV     | P              | Range B, PPMU force ±0.5 mA into open, after two point gain/offset calibration; measured over PPMU clamp functional range                                                                                                                                                              |

## SPECIFICATIONS

Table 7.

| Parameter                                          | Min | Typ   | Max | Unit | Test Level     | Test Conditions/Comments                                                                                                                                                                                            |
|----------------------------------------------------|-----|-------|-----|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DUTGND Voltage Accuracy                            | -7  | ±2    | +7  | mV   | P              | Over ±0.1 V range; measured at end points of clamp functional range                                                                                                                                                 |
| SETTLING/SWITCHING TIMES                           |     |       |     |      |                |                                                                                                                                                                                                                     |
| Force Voltage Settling Time to 0.1% of Final Value |     |       |     |      |                |                                                                                                                                                                                                                     |
| Range A,<br>200 pF and 2000 pF Load                |     | 10    |     | μs   | S              | PPMU enabled in FV, Range A, DCL disabled; program VIN steps from 0 V to 0.5 V and 5.0 V                                                                                                                            |
| Range B,<br>200 pF and 2000 pF Load                |     | 12    |     | μs   | S              | PPMU enabled in FV, Range B, DCL disabled; program VIN steps from 0 V to 0.5 V and 5.0 V                                                                                                                            |
| Range C,<br>200 pF and 2000 pF Load                |     | 32    |     | μs   | S              | PPMU enabled in FV, Range C, DCL disabled; program VIN steps from 0 V to 0.5 V and 5.0 V                                                                                                                            |
| Force Voltage Settling Time to 1.0% of Final Value |     |       |     |      |                |                                                                                                                                                                                                                     |
| Range A,<br>200 pF and 2000 pF Load                |     | 8.1   |     | μs   | C <sub>B</sub> | PPMU enabled in FV, Range A, DCL disabled; program VIN steps from 0 V to 5.0 V                                                                                                                                      |
| Range B,<br>200 pF and 2000 pF Load                |     | 8.1   |     | μs   | C <sub>B</sub> | PPMU enabled in FV, Range B, DCL disabled; program VIN steps from 0 V to 5.0 V                                                                                                                                      |
| Range C,<br>200 pF and 2000 pF Load                |     | 8.1   |     | μs   | C <sub>B</sub> | PPMU enabled in FV, Range C, DCL disabled; program VIN steps from 0 V to 5.0 V                                                                                                                                      |
| Range A,<br>200 pF and 2000 pF Load                |     | 2.5   |     | μs   | C <sub>B</sub> | PPMU enabled in FV, Range A, DCL disabled; program VIN steps from 0 V to 0.5 V                                                                                                                                      |
| Range B,<br>200 pF and 2000 pF Load                |     | 6.3   |     | μs   | C <sub>B</sub> | PPMU enabled in FV, Range B, DCL disabled; program VIN steps from 0 V to 0.5 V                                                                                                                                      |
| Range C,<br>200 pF and 2000 pF Load                |     | 8.1   |     | μs   | C <sub>B</sub> | PPMU enabled in FV, Range C, DCL disabled; program VIN steps from 0 V to 0.5 V                                                                                                                                      |
| Force Current Settling Time to 0.1% of Final Value |     |       |     |      |                |                                                                                                                                                                                                                     |
| Range A,<br>200 pF in Parallel with 120 Ω          |     | 16    |     | μs   | S              | PPMU enabled in FI, Range A, DCL disabled; program VIN step of 0 mA to 40 mA                                                                                                                                        |
| Range B,<br>200 pF in Parallel with 1.5 kΩ         |     | 10    |     | μs   | S              | PPMU enabled in FI, Range B, DCL disabled; program VIN step of 0 mA to 1 mA                                                                                                                                         |
| Range C,<br>200 pF in Parallel with 15.0 kΩ        |     | 40    |     | μs   | S              | PPMU enabled in FI, Range C, DCL disabled; program VIN step of 0 mA to 100 μA                                                                                                                                       |
| Force Current Settling Time to 1.0% of Final Value |     |       |     |      |                |                                                                                                                                                                                                                     |
| Range A,<br>200 pF in Parallel with 120 Ω          |     | 8.1   |     | μs   | C <sub>B</sub> | PPMU enabled in FI, Range A, DCL disabled; program VIN step of 0 mA to 40 mA                                                                                                                                        |
| Range B,<br>200 pF in Parallel with 1.5 kΩ         |     | 7.5   |     | μs   | C <sub>B</sub> | PPMU enabled in FI, Range B, DCL disabled; program VIN step of 0 mA to 1 mA                                                                                                                                         |
| Range C,<br>200 pF in Parallel with 15.0 kΩ        |     | 8.1   |     | μs   | C <sub>B</sub> | PPMU enabled in FI, Range C, DCL disabled; program VIN step of 0 mA to 100 μA                                                                                                                                       |
| INTERACTION and CROSSTALK                          |     |       |     |      |                |                                                                                                                                                                                                                     |
| Measure Voltage Channel-to-Channel Crosstalk       |     | ±0.01 |     | %FSR | C <sub>T</sub> | 0.01% × 8.5 V = 0.85 mV, PPMU enabled in FIMV, DCL disabled; CHx under test: Range B, forcing 0 mA into 0 V load; other channel: Range A, sweep 0 mA to 40 mA into 0 V load; report ΔV of PPMU_MEASx pin under test |

## SPECIFICATIONS

Table 7.

| Parameter                                    | Min | Typ   | Max | Unit | Test Level     | Test Conditions/Comments                                                                                                                                                                                                               |
|----------------------------------------------|-----|-------|-----|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Measure Current Channel-to-Channel Crosstalk |     | ±0.01 |     | %FSR | C <sub>T</sub> | 0.01% × 5.0 V = 0.5 mV, PPMU enabled in FVMI, DCL disabled; CHx under test: Range E, forcing 0 V into 0 mA current load; other channel: Range E, sweep -2.0 V to +6.5 V into 0 mA current load; report ΔV of PPMU_MEASx pin under test |

## PPMU\_GO/NO-GO COMPARATORS SPECIFICATIONS

Table 8.

| Parameter                       | Min         | Typ | Max         | Unit   | Test Level     | Test Conditions/Comments                                                                                                                    |
|---------------------------------|-------------|-----|-------------|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| DC SPECIFICATIONS               |             |     |             |        |                |                                                                                                                                             |
| Compare Voltage Range           | -2.0        |     | +6.5        | V      | D              | Measured at DAC Code 0x4000 (0 V)                                                                                                           |
| Input Offset Voltage            | -250        |     | +250        | mV     | P              |                                                                                                                                             |
| Input Offset Voltage Tempco     |             | ±50 |             | μV/°C  | C <sub>T</sub> |                                                                                                                                             |
| Gain                            | 1.0         |     | 1.1         | V/V    | P              | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (+5.0 V)                                                        |
| Gain Tempco                     |             | ±25 |             | ppm/°C | C <sub>T</sub> | Applies at m = 1.0 and c = 0.0                                                                                                              |
| Comparator Threshold Resolution |             | 153 |             | μV     | D              | After two point gain/offset calibration; measured over VOH/VOL range -2.0 V to +6.5 V; calibration points at 0x4000 (0 V) and 0xC000 (+5 V) |
| Comparator Threshold DNL        |             | ±1  |             | mV     | C <sub>T</sub> |                                                                                                                                             |
| Comparator Threshold INL        | -7          |     | +7          | mV     | P              |                                                                                                                                             |
| DUTGND Voltage Accuracy         | -7          | ±2  | +7          | mV     | P              | Over ±0.1 V range                                                                                                                           |
| Comparator Uncertainty Band     |             | 1.6 |             | mV     | C <sub>B</sub> | Sweep comparator threshold to determine uncertainty (oscillation) band                                                                      |
| DC Hysteresis                   |             | <1  |             | mV     | C <sub>B</sub> | Sweep comparator threshold                                                                                                                  |
| COMPARATOR OUTPUTS              |             |     |             |        |                |                                                                                                                                             |
| Output Logic High               | VDD/4 - 0.5 |     | VDD/4 + 0.5 | V      | P <sub>F</sub> | PPMU_CMPHx, PPMU_CMPLx<br>Sourcing 100 μA                                                                                                   |
| Output Logic Low                | 0           |     | 0.5         | V      | P <sub>F</sub> | Sinking 100 μA                                                                                                                              |

## PPMU\_SENSE PIN SPECIFICATIONS

Table 9.

| Parameter                                         | Min  | Typ | Max  | Unit | Test Level | Test Conditions/Comments                                                               |
|---------------------------------------------------|------|-----|------|------|------------|----------------------------------------------------------------------------------------|
| PMU_Sx (SYSTEM PMU) SENSE PIN CHARACTERISTICS     |      |     |      |      |            |                                                                                        |
| Voltage Range                                     | -2.0 |     | +7.0 | V    | D          | DCL high-Z compliance range is -2.0 V to +7.0 V                                        |
| Ext Sense Switch R <sub>ON</sub>                  |      |     | 2.5  | kΩ   | P          | Push 0.5 mA into PMU_Sx with switch closed and DUTx pin at 0 V; calculate R = V/0.0005 |
| Leakage                                           | -2   |     | +2   | nA   | P          | Tested at -2.0 V and +7.0 V, switch open                                               |
| Pin Capacitance (PMU_Sx)                          |      | 0.5 |      | pF   | S          | Switch open                                                                            |
| PPMU_Sx (INTERNAL PPMU) SENSE PIN CHARACTERISTICS |      |     |      |      |            |                                                                                        |
| Voltage Range                                     | -2.0 |     | +6.5 | V    | D          | PPMU input select in all states                                                        |
| Leakage                                           | -2   |     | +2   | nA   | P          | Tested at -2.0 V and +6.5 V                                                            |
| Max Load Capacitance                              |      | 2   |      | nF   | S          |                                                                                        |

## SPECIFICATIONS

SERIAL PROGRAMMABLE INTERFACE (SPI) (SDI,  $\overline{\text{RST}}$ ,  $\overline{\text{CS}}$ , SCLK, SDO,  $\overline{\text{BUSY}}$ ) SPECIFICATIONS

Table 10.

| Parameter                                | Min       | Typ | Max | Unit | Test Level     | Test Conditions/Comments                                                                                     |
|------------------------------------------|-----------|-----|-----|------|----------------|--------------------------------------------------------------------------------------------------------------|
| Input Logic High                         | 1.8       |     | VCC | V    | P <sub>F</sub> | SDI, $\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SCLK                                                 |
| Input Logic Low                          | 0         |     | 0.7 | V    | P <sub>F</sub> |                                                                                                              |
| Input Bias Current                       | -10       | ±1  | +10 | μA   | P              | Tested at 0.0 V and VCC volts                                                                                |
| SCLK Clock Rate                          | 0.5       |     | 50  | MHz  | D              |                                                                                                              |
| SCLK Pulse Width, Minimum                |           | 9   |     | ns   | C <sub>T</sub> |                                                                                                              |
| SCLK Crosstalk on DUTx Pin               |           | 30  |     | mV   | C <sub>B</sub> | DCL disabled; PPMU FV enabled and forcing 0.0 V                                                              |
| Serial Output Logic High                 | VCC - 0.5 |     | VCC | V    | P <sub>F</sub> | SDO; sourcing 2 mA                                                                                           |
| Serial Output Logic Low                  | 0         |     | 0.5 | V    | P <sub>F</sub> | Sinking 2 mA                                                                                                 |
| $\overline{\text{BUSY}}$ Pull-Up Voltage | 2.3       | 2.5 | 3.5 | V    | D              | $\overline{\text{BUSY}}$ is an open drain output that pulls low when the SPI requires additional SCLK cycles |
| $\overline{\text{BUSY}}$ Active Voltage  |           | 0.2 | 0.8 | V    | P <sub>F</sub> | $\overline{\text{BUSY}}$ active, sinking 2 mA                                                                |

## VHH DRIVER SPECIFICATIONS

VHH mode enabled, RCV active.

Table 11.

| Parameter                              | Min  | Typ  | Max  | Unit   | Test Level     | Conditions                                                                                                                                                       |
|----------------------------------------|------|------|------|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VHH BUFFER                             |      |      |      |        |                | VHH mode enabled, RCVx active                                                                                                                                    |
| Voltage Range                          | 0.0  |      | 13.5 | V      | D              |                                                                                                                                                                  |
| Output High                            | 13.5 |      |      | V      | P              | VHH level = full scale, sourcing 15 mA                                                                                                                           |
| Output Low                             |      |      | 5.9  | V      | P              | VHH level = zero-scale, sinking 15 mA                                                                                                                            |
| Extrapolated Offset                    | -500 |      | +500 | mV     | P              | Extrapolated from measurements at DAC Code 0x8000 (+7 V) and DAC Code 0xC000 (+12 V)                                                                             |
| Extrapolated Offset Tempco             |      | ±0.5 |      | mV/°C  | C <sub>T</sub> |                                                                                                                                                                  |
| Gain                                   | 2    |      | 2.2  | V/V    | P              | Gain derived from measurements at DAC Code 0x8000 (+7 V) and DAC Code 0xC000 (+12 V); based on ideal DAC transfer function (see Table 21)                        |
| Gain Tempco                            |      | ±25  |      | ppm/°C | C <sub>T</sub> |                                                                                                                                                                  |
| Resolution                             |      | 305  |      | μV     | D              |                                                                                                                                                                  |
| INL                                    | -25  |      | +25  | mV     | P              | VHH mode enabled, RCVx active; after two point gain/offset calibration; measured over +5.9 V to +13.5 V; calibrate at Code 0x8000 (+7 V) and Code 0xC000 (+12 V) |
| DUTGND Voltage Accuracy                |      | ±4   |      | mV     | C <sub>T</sub> | Over ±0.1 V range; measured at end points of VHH functional range                                                                                                |
| Output Resistance                      |      |      | 10   | Ω      | P              | ΔV/ΔI; VHH mode enabled, RCVx active;<br>Source: VHH = +10.0 V, I = 0 mA, +15 mA<br>Sink: VHH = +6.5 V, I = 0 mA, -15 mA                                         |
| DC Output Current Limit Source         | +60  |      | +100 | mA     | P              | VHH mode enabled, RCVx active; VHH = +13.5 V, short HVOUT pin to +5.9 V, measure current                                                                         |
| DC Output Current Limit Sink           | -100 |      | -60  | mA     | P              | VHH mode enabled, RCVx active, VHH = 5.9 V, short HVOUT pin to 13.5 V, measure current                                                                           |
| VHH Rise Time (from VIL or VIH to VHH) |      | 163  |      | ns     | C <sub>B</sub> | 20% to 80%, VHH mode enabled, toggle RCVx: VHH = 13.5 V, VIL = 0.0 V, VIH = 3.0 V, DATx = high; VHH = 13.5 V, VIL = 3.0 V, VIH = 4.0 V, DATx = low               |

## SPECIFICATIONS

Table 11.

| Parameter                              | Min  | Typ   | Max  | Unit   | Test Level     | Conditions                                                                                                                                                        |
|----------------------------------------|------|-------|------|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VHH Fall Time (from VHH to VIL or VIH) |      | 30    |      | ns     | C <sub>B</sub> | 20% to 80%, VHH mode enabled, toggle RCVx; VHH = 13.5 V, VIL = 0.0 V, VIH = 3.0 V, DATx = high; VHH = 13.5 V, VIL = 3.0 V, VIH = 4.0 V, DATx = low                |
| Preshoot, Overshoot, and Undershoot    |      | ±40.0 |      | mV     | C <sub>B</sub> | VHH mode enabled, toggle RCVx; VHH = 13.5 V, VIL = 0.0 V, VIH = 3.0 V, DATx = high; VHH = 13.5 V, VIL = 3.0 V, VIH = 4.0 V, DATx = low                            |
| VIL/VIH DRIVE FUNCTION                 |      |       |      |        |                |                                                                                                                                                                   |
| Voltage Range                          | -0.1 |       | +6.5 | V      | D              | Measured at DAC Code 0x4000 (0 V), for DATx = high and DATx = low                                                                                                 |
| Offset Voltage                         | -500 |       | +500 | mV     | P              |                                                                                                                                                                   |
| Offset Voltage Tempco                  |      | 1     |      | mV/°C  | C <sub>T</sub> |                                                                                                                                                                   |
| Gain                                   | 1.0  |       | 1.1  | V/V    | P              | Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21)                            |
| Gain Tempco                            |      | ±75   |      | ppm/°C | C <sub>T</sub> | VHH mode enabled, RCVx inactive; after two point gain/offset calibration; measured over -0.1 V to +6.0 V; calibrate at Code 0x4000 (0 V) and Code 0xC000 (+5.0 V) |
| Resolution                             |      | 153   |      | μV     | D              |                                                                                                                                                                   |
| INL                                    | -20  |       | +20  | mV     | P              |                                                                                                                                                                   |
| DUTGND Voltage Accuracy                |      | ±2    |      | mV     | C <sub>T</sub> | Over ±0.1 V range; measured at end points of VIH and VIL functional range                                                                                         |
| Output Resistance                      | 46   | 48    | 50   | Ω      | P              | ΔV/ΔI; VHH mode enabled, RCVx inactive; Source: VIH = +3.0 V, I = +1 mA, +50 mA; Sink: VIL = +2.0 V; I = -1 mA, -50 mA                                            |
| DC Output Current Limit Source         | 60   |       | 100  | mA     | P              | VHH mode enabled, RCVx inactive, VIH = +6.0 V, short HVOUT pin to -0.1 V, DATx high, measure current                                                              |
| DC Output Current Limit Sink           | -100 |       | -60  | mA     | P              | VHH mode enabled, RCVx inactive, VIL = -0.1 V, short HVOUT pin to +6.0 V, DATx low, measure current                                                               |
| Rise Time, VIL to VIH                  |      | 6.4   |      | ns     | C <sub>B</sub> | 20% to 80%, VHH mode enabled, RCVx inactive, VIL = 0.0 V, VIH = 3.0 V, R <sub>LOAD</sub> > 500 Ω, toggle DATx                                                     |
| Fall Time, VIH to VIL                  |      | 7.3   |      | ns     | C <sub>B</sub> | 20% to 80%, VHH mode enabled, RCVx inactive, VIL = 0.0 V, VIH = 3.0 V, R <sub>LOAD</sub> > 500 Ω, toggle DATx                                                     |
| Preshoot, Overshoot, and Undershoot    |      | ±30   |      | mV     | C <sub>B</sub> | VHH mode enabled, RCVx inactive, VIL = 0.0 V, VIH = 3.0 V, R <sub>LOAD</sub> > 500 Ω, toggle DATx                                                                 |

## ALARM FUNCTIONS SPECIFICATIONS

Table 12.

| Parameter                    | Min  | Typ | Max  | Unit | Test Level | Test Conditions/Comments                                                                                                                         |
|------------------------------|------|-----|------|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| DC CHARACTERISTICS           |      |     |      |      |            |                                                                                                                                                  |
| Overshoot Detect (OVD)       |      |     |      |      |            | See Figure 136                                                                                                                                   |
| Programmable Voltage Range   | -2.5 |     | +7.5 | V    | D          | Measured at DAC Code 0x0CCC (-2.0 V); OVD comparators not guaranteed to function as specified if VDUTx is outside absolute maximum voltage range |
| Uncalibrated Error at -2.0 V | -200 |     | +200 | mV   | P          |                                                                                                                                                  |
| Uncalibrated Error at +7.0 V | -450 |     | +450 | mV   | P          | Measured at DAC Code 0xF333 (+7.0 V)                                                                                                             |

## SPECIFICATIONS

Table 12.

| Parameter                           | Min | Typ   | Max | Unit    | Test Level     | Test Conditions/Comments                                                                                                                           |
|-------------------------------------|-----|-------|-----|---------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Offset Voltage Tempco               |     | ±0.5  |     | mV/°C   | C <sub>T</sub> | Gain derived from measurements at DAC Code 0x4000 and DAC Code 0xC000                                                                              |
| Gain                                |     | 1.045 |     | V/V     | C <sub>T</sub> |                                                                                                                                                    |
| Hysteresis                          |     | 125   |     | mV      | C <sub>T</sub> |                                                                                                                                                    |
| Thermal Alarm                       |     |       |     |         |                | See Figure 136                                                                                                                                     |
| Setpoint Error                      |     | ±10   |     | °C      | C <sub>T</sub> | Relative to default value, 100°C                                                                                                                   |
| Thermal Hysteresis                  |     | -15   |     | °C      | C <sub>T</sub> |                                                                                                                                                    |
| PPMU Clamp Alarm                    |     |       |     |         |                | See Figure 136 and Table 29 for electrical characteristics                                                                                         |
| <b>ALARM Output Characteristics</b> |     |       |     |         |                |                                                                                                                                                    |
| Off State Leakage                   |     | 10    | 500 | nA      | P              | Disable alarm, apply 2.5 V to $\overline{\text{ALARM}}$ pin, measure leakage current                                                               |
| Max On Voltage at 100 $\mu$ A       |     | 0.1   | 0.7 | V       | P              | Activate alarm, force 100 $\mu$ A into $\overline{\text{ALARM}}$ pin, measure active alarm voltage                                                 |
| Propagation Delay                   |     | 1.5   |     | $\mu$ s | C <sub>B</sub> | For OVD_HI:<br>VDUTx: 0 V to 6 V swing,<br>OVDH = +3.0 V, OVDL = -1.0 V<br>For OVD_LO:<br>VDUTx: 0 V to 6 V swing,<br>OVDH = +7.0 V, OVDL = +3.0 V |

## SPI TIMING DETAILS

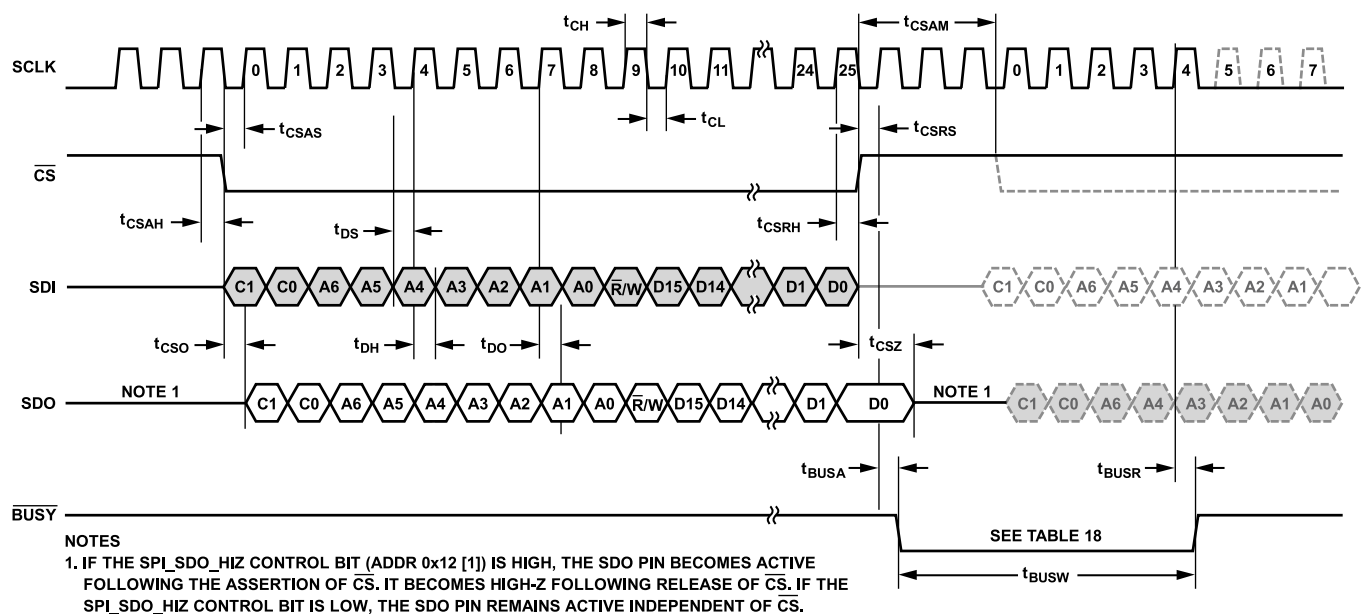


Figure 2. SPI Detailed Read/Write Timing Diagram

SPECIFICATIONS

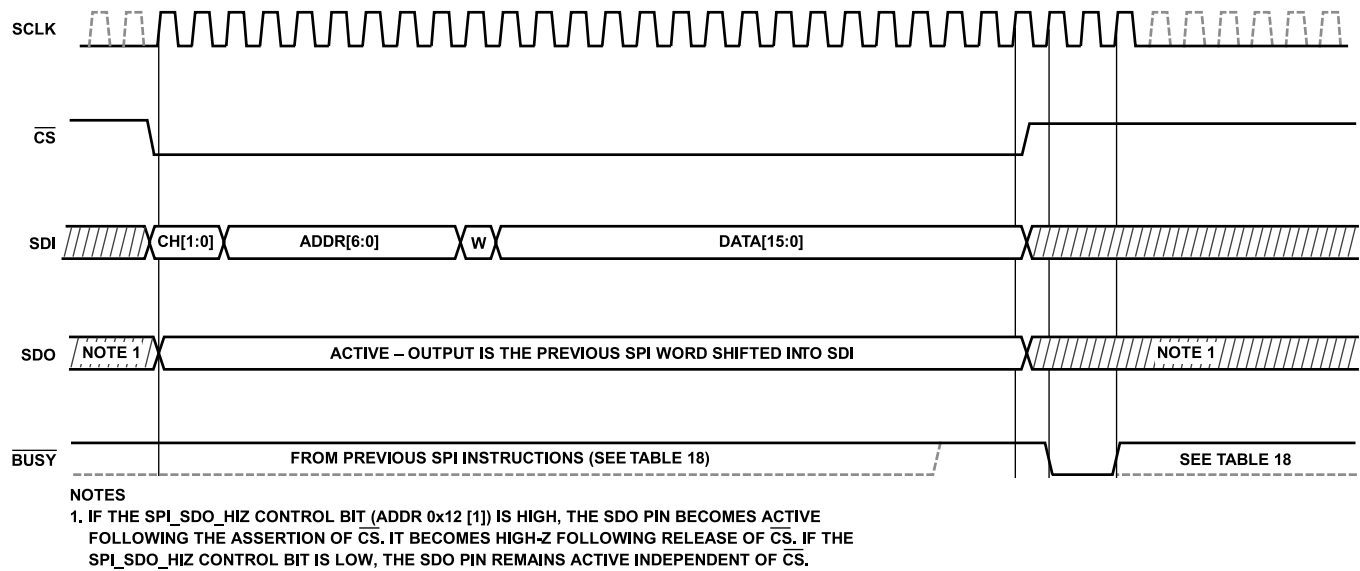


Figure 3. SPI Write Instruction

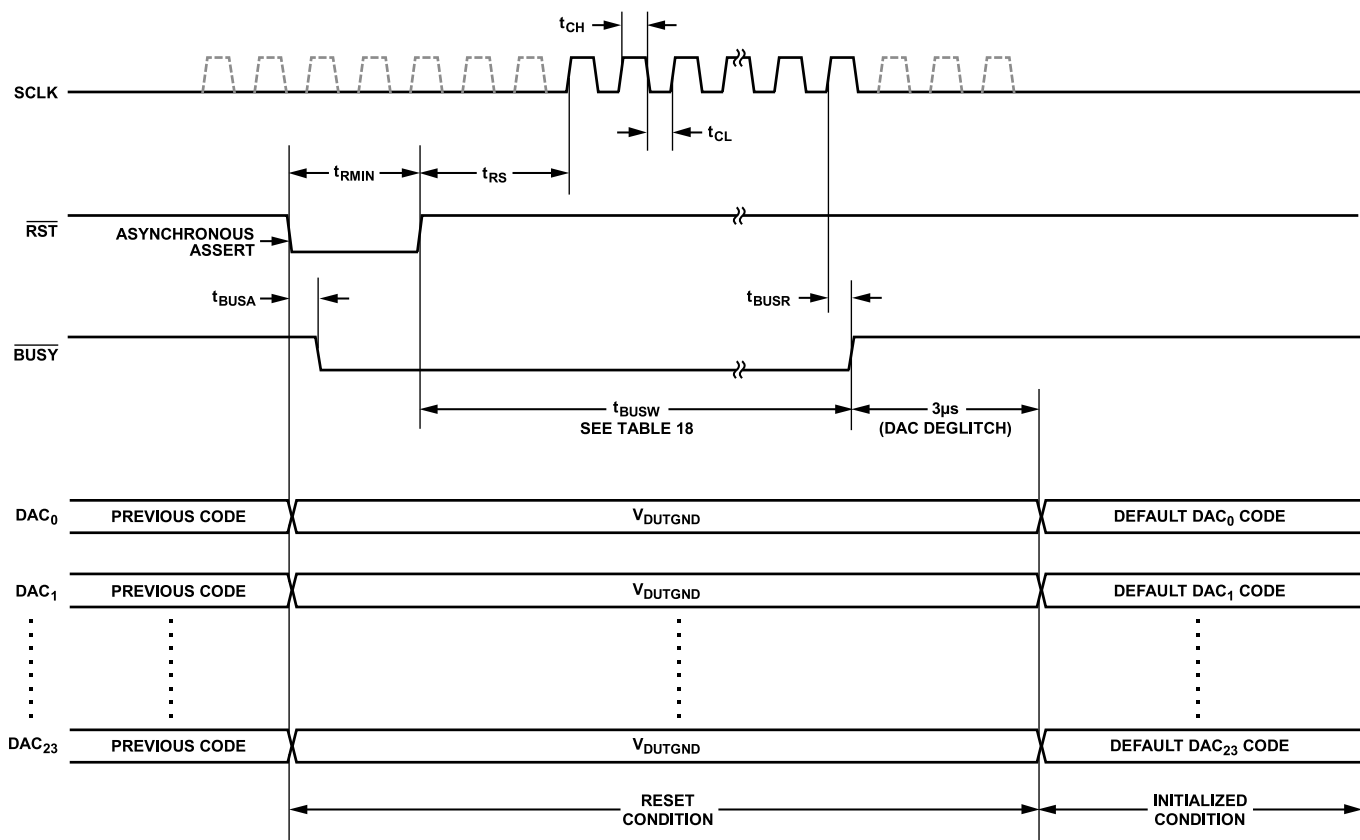
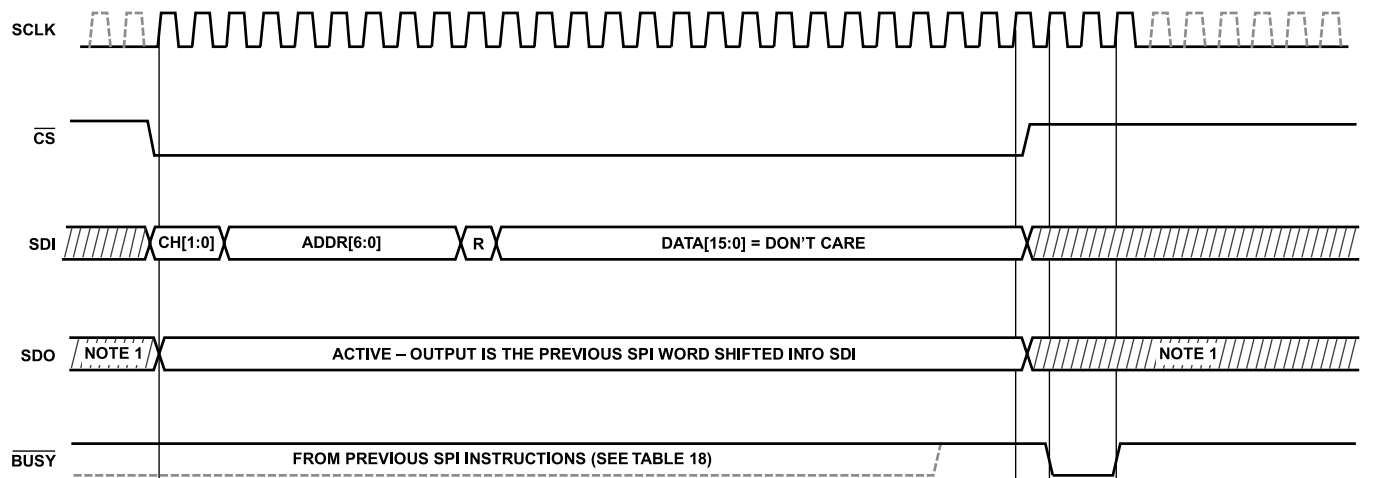
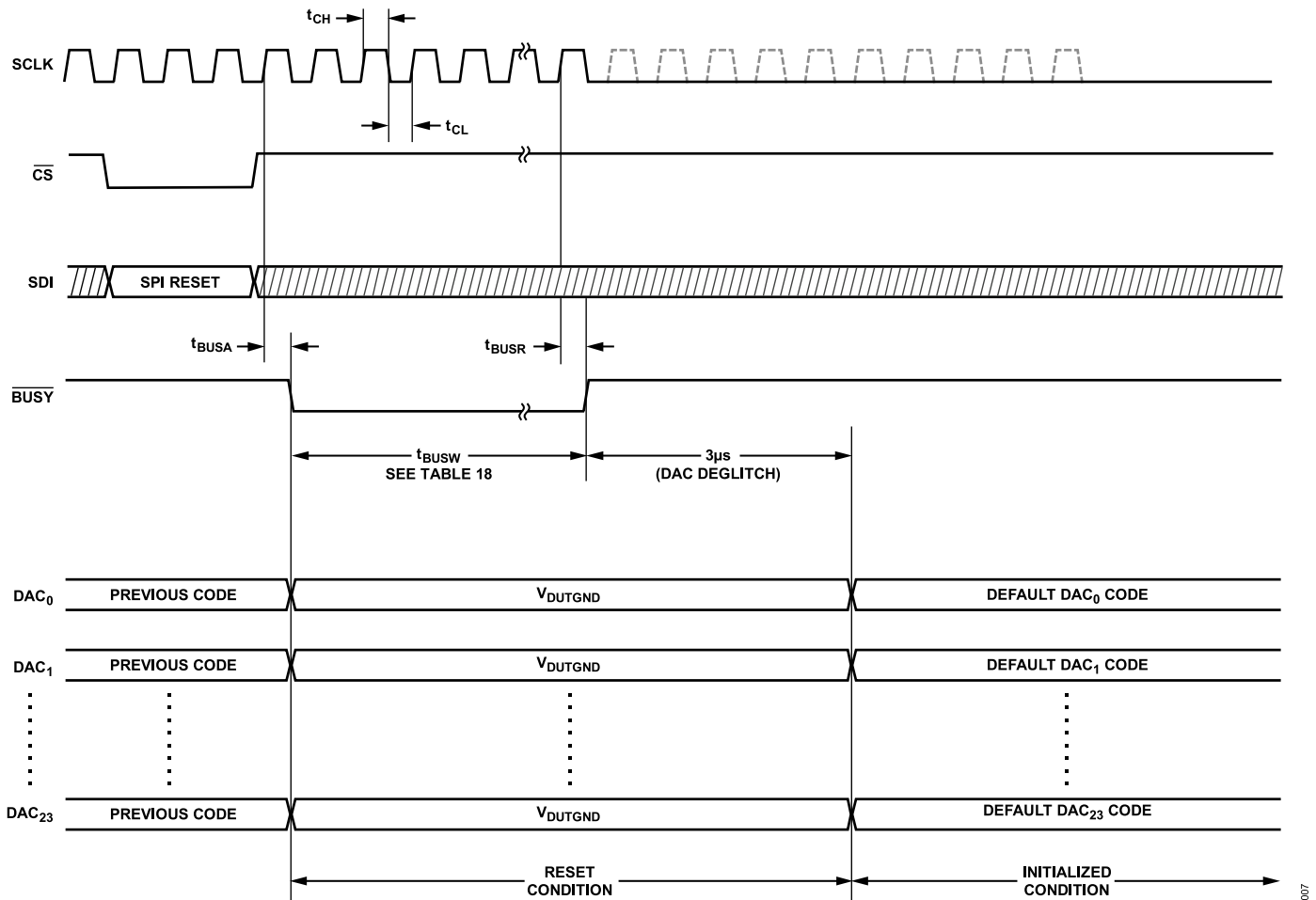


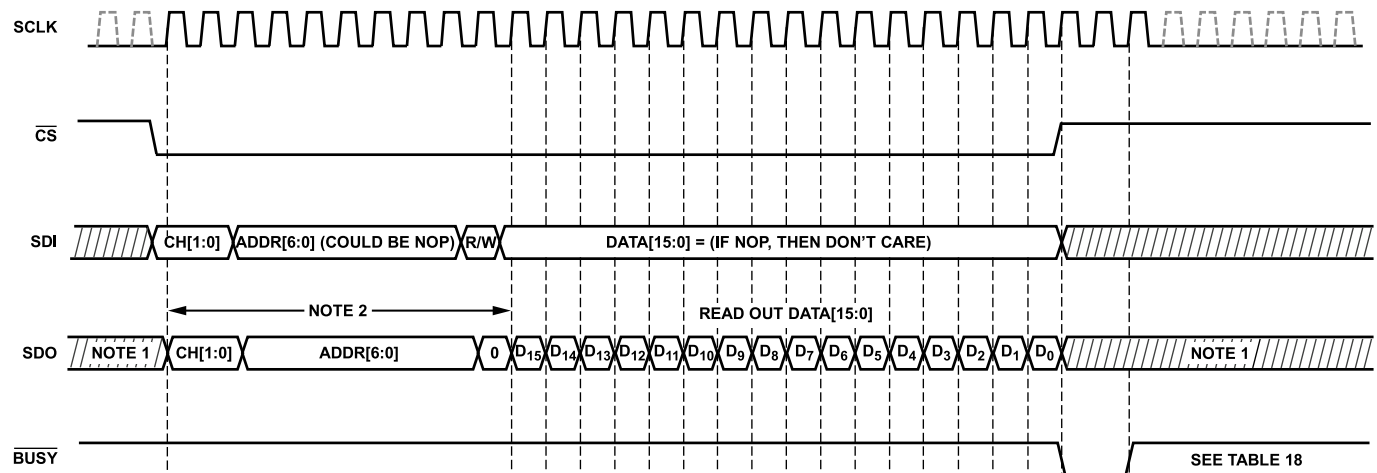
Figure 4. SPI Detailed Hardware Reset Timing Diagram

SPECIFICATIONS



NOTES  
1. IF THE SPI\_SDO\_HIZ CONTROL BIT (ADDR 0x12 [1]) IS HIGH, THE SDO PIN BECOMES ACTIVE FOLLOWING THE ASSERTION OF CS. IT BECOMES HIGH-Z FOLLOWING RELEASE OF CS. IF THE SPI\_SDO\_HIZ CONTROL BIT IS LOW, THE SDO PIN ALWAYS REMAINS ACTIVE INDEPENDENT OF CS.

## SPECIFICATIONS



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1. IF THE SPI\_SDO\_HIZ CONTROL BIT (ADDR 0x12 {1}) IS HIGH, THE SDO PIN BECOMES ACTIVE FOLLOWING THE ASSERTION OF CS. IT BECOMES HIGH-Z FOLLOWING RELEASE OF CS. IF THE SPI\_SDO\_HIZ CONTROL BIT IS LOW, THE SDO PIN REMAINS ACTIVE INDEPENDENT OF CS.
2. THE FIRST 10 BITS OF SDO FOLLOWING A READ REQUEST ECHO ADDRESS AND CHANNEL BITS OF THE PRECEDING REQUEST. THE R/W BIT POSITION IS SET LOW. THE FOLLOWING 16-BITS CONTAIN DATA FROM THE REQUESTED ADDRESS AND CHANNEL.

Figure 7. SPI Readout Instruction (Subsequent to Read Request)

Table 13. SPI Detailed Timing Requirements

| Parameter         | Min | Max | Unit   | Test Level     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|-----|-----|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| f <sub>CLK</sub>  | 0.5 | 50  | MHz    | C <sub>T</sub> | SCLK operating frequency.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| t <sub>CH</sub>   | 9   |     | ns     | C <sub>T</sub> | SCLK high time.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| t <sub>CL</sub>   | 9   |     | ns     | C <sub>T</sub> | SCLK low time.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| t <sub>CSAS</sub> | 3   |     | ns     | C <sub>T</sub> | Setup of $\overline{CS}$ to rising SCLK at assert.                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| t <sub>CSAH</sub> | 3   |     | ns     | C <sub>T</sub> | Hold of $\overline{CS}$ to rising SCLK at assert.                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| t <sub>CSRS</sub> | 3   |     | ns     | C <sub>T</sub> | Setup of $\overline{CS}$ to rising SCLK at release.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| t <sub>CSRH</sub> | 3   |     | ns     | C <sub>T</sub> | Hold of $\overline{CS}$ to rising SCLK at release.                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                   | 4   |     | ns     | C <sub>T</sub> | Hold of $\overline{CS}$ release prior to rising SCLK. This parameter is critical only if the number of SCLK cycles from the previous release of $\overline{CS}$ is the minimum specified by the t <sub>CSAM</sub> parameter.                                                                                                                                                                                                                                                                                   |
| t <sub>CSO</sub>  |     | 6   | ns     | C <sub>T</sub> | Delay from $\overline{CS}$ assert to SDO active.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| t <sub>CSZ</sub>  |     | 10  | ns     | C <sub>T</sub> | Delay from $\overline{CS}$ release to SDO high-Z, depends greatly on external pin loading.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| t <sub>CSAM</sub> | 3   |     | Cycles | C <sub>T</sub> | Width of $\overline{CS}$ release between consecutive assertions of $\overline{CS}$ . This parameter is specified in units of SCLK cycles, more specifically in terms of rising edges of the SCLK input.                                                                                                                                                                                                                                                                                                        |
| t <sub>DS</sub>   | 3   |     | ns     | C <sub>T</sub> | Setup of SDI data prior to rising SCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| t <sub>DH</sub>   | 4   |     | ns     | C <sub>T</sub> | Hold of SDI data following rising SCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| t <sub>DO</sub>   |     | 12  | ns     | C <sub>T</sub> | Delay of SDO data from rising SCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| t <sub>BUSA</sub> |     | 12  | ns     | C <sub>T</sub> | Delay of $\overline{BUSY}$ assert from first rising SCLK following a valid $\overline{CS}$ release or an asynchronous $\overline{RSTb}$ release.                                                                                                                                                                                                                                                                                                                                                               |
| t <sub>BUSW</sub> | 3   | 26  | Cycles | C <sub>T</sub> | Width of $\overline{BUSY}$ assert. To ensure proper SPI operation, the SCLK must be provided for as long as $\overline{BUSY}$ remains asserted. Note that the number of SCLK cycles within any $\overline{BUSY}$ period is variable but deterministic and is based on the previous SPI write instruction type. See the <a href="#">Use of the SPI BUSY Pin</a> section and <a href="#">Figure 2</a> , <a href="#">Figure 4</a> , <a href="#">Figure 5</a> , and <a href="#">Table 18</a> for more information. |
| t <sub>BUSR</sub> |     | 12  | ns     | C <sub>T</sub> | Delay of $\overline{BUSY}$ release from first rising SCLK, satisfying the requirements detailed in the <a href="#">Use of the SPI BUSY Pin</a> section.                                                                                                                                                                                                                                                                                                                                                        |
| t <sub>RMIN</sub> | 10  |     | ns     | C <sub>T</sub> | Width of asynchronous $\overline{RST}$ assert.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| t <sub>RS</sub>   | 3   |     | ns     | C <sub>T</sub> | Setup of $\overline{RST}$ to rising SCLK at release.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

## SPECIFICATIONS

Table 13. SPI Detailed Timing Requirements

| Parameter        | Min | Max | Unit          | Test Level     | Description                                                                                                                                                                                                                                                                                                                                                         |
|------------------|-----|-----|---------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $t_{\text{SPI}}$ | 29  |     | Cycles        | C <sub>T</sub> | Number of SCLK rising edge cycles per SPI word write plus the additional $t_{\text{CSAM}}$ requirement.                                                                                                                                                                                                                                                             |
| $t_{\text{DAC}}$ | 5   | 10  | $\mu\text{s}$ | S              | Settling time of analog DAC levels to $\pm 0.5$ LSB relative to the beginning of the DAC deglitch period, which begins x SCLK cycles following the release of $\overline{\text{CS}}$ and four SCLK cycles prior to the release of the $\overline{\text{BUSY}}$ pin. The number of SCLK cycles, x, is defined by Table 18. Also see Figure 126 for more information. |

## ABSOLUTE MAXIMUM RATINGS

Table 14. Absolute Maximum Ratings

| Parameter                                            | Rating                 |
|------------------------------------------------------|------------------------|
| Supply Voltages                                      |                        |
| Positive Supply Voltage (VDD to PGND)                | -0.5 V to +11.0 V      |
| Positive VCC Supply Voltage (VCC to DGND)            | -0.5 V to +4.0 V       |
| Negative Supply Voltage (VSS to PGND)                | -6.5 V to +0.5 V       |
| Supply Voltage Difference (VDD to VSS)               | -1.0 V to +17.0 V      |
| Reference Ground (DUTGND to AGND)                    | -0.5 V to +0.5 V       |
| VPLUS Supply Voltage (VPLUS to PGND)                 | -0.5 V to +19.0 V      |
| Supply Sequence or Dropout Condition <sup>1</sup>    |                        |
| Input/Output Voltages                                |                        |
| Analog Input Common-Mode Voltage                     | VSS to VDD             |
| DUTx Output Short Circuit Voltage <sup>2</sup>       | -3.0 V to +8.0 V       |
| High Speed Input Voltage Absolute Range <sup>3</sup> | -0.5 V to VTTC + 0.5 V |
| High Speed Differential Input Voltage <sup>3</sup>   | -1.0 V to +1.0 V       |
| DUTx I/O Pin Current                                 |                        |
| DCL Maximum Short-Circuit Current <sup>4</sup>       | ±140 mA                |
| Temperature                                          |                        |
| Operating Temperature, Junction                      | 125°C                  |
| Storage Temperature Range                            | -65°C to +150°C        |

<sup>1</sup> No supply should exceed the given ratings.

<sup>2</sup>  $R_{LOAD} = 0\ \Omega$ , VDUTx continuous short-circuit condition ( $V_{IH}$ ,  $V_{IL}$ ,  $V_{IT}$ ), high-Z, VCOM, and clamp modes).

<sup>3</sup> DAT,  $\overline{DAT}$ , RCV,  $\overline{RCV}$ , RSOURCE = 0  $\Omega$ .

<sup>4</sup>  $R_{LOAD} = 0\ \Omega$ , VDUTx = -3 V to +8 V; DCL current limit. Continuous short-circuit condition. ADATE318 current limits and survives a continuous short-circuit fault.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 15. Thermal Resistance

| Package Type | $\theta_{JA}$ |    |    | $\theta_{JC}$ | Unit |
|--------------|---------------|----|----|---------------|------|
| Airflow      | 0             | 1  | 2  |               | m/s  |
| LFCSF        | 45            | 40 | 37 | 1             | °C/W |

Table 16. Explanation of Test Levels

| Test Level     | Description                                 |
|----------------|---------------------------------------------|
| D              | Definition                                  |
| S              | Design verification simulation              |
| P              | 100% production tested                      |
| P <sub>F</sub> | Functionally checked during production test |
| C <sub>T</sub> | Characterized on tester                     |
| C <sub>B</sub> | Characterized on bench                      |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

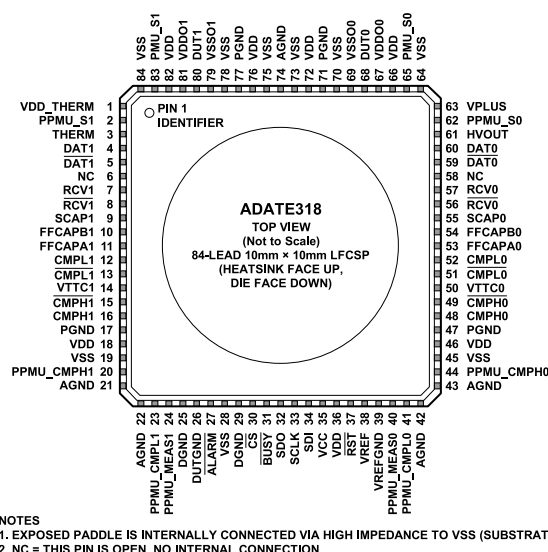


Figure 8. LFCSP Pin Configuration

Table 17. Pin Function Descriptions

| Pin | Mnemonic                  | Description                                                                   |
|-----|---------------------------|-------------------------------------------------------------------------------|
| EP  | Exposed Paddle            | Exposed paddle is internally connected via high impedance to VSS (substrate). |
| 1   | VDD_THERM                 | Temperature Sensor VDD Supply.                                                |
| 2   | PPMU_S1                   | PPMU External Sense Connect, Channel 1.                                       |
| 3   | THERM                     | Temperature Sensor Analog Output.                                             |
| 4   | DAT1                      | High Speed Data Input, Channel 1.                                             |
| 5   | $\overline{\text{DAT1}}$  | High Speed Data Input Complement, Channel 1.                                  |
| 6   | NC                        | This pin is open. No internal connection.                                     |
| 7   | RCV1                      | High Speed Receive Input, Channel 1.                                          |
| 8   | $\overline{\text{RCV1}}$  | High Speed Receive Input Complement, Channel 1.                               |
| 9   | SCAP1                     | PPMU External Compensation Capacitor, Channel 1.                              |
| 10  | FFCAPB1                   | PPMU External Feed Forward Capacitor Pin B, Channel 1.                        |
| 11  | FFCAPA1                   | PPMU External Feed Forward Capacitor Pin A, Channel 1.                        |
| 12  | CMPL1                     | High Speed Comparator Low Output, Channel 1.                                  |
| 13  | $\overline{\text{CMPL1}}$ | High Speed Comparator Low Output Complement, Channel 1.                       |
| 14  | VTTC1                     | Comparator Supply Termination, Channel 1.                                     |
| 15  | $\overline{\text{CMPH1}}$ | High Speed Comparator High Output Complement, Channel 1.                      |
| 16  | CMPH1                     | High Speed Comparator High Output, Channel 1.                                 |
| 17  | PGND                      | Power Ground.                                                                 |
| 18  | VDD                       | VDD Supply.                                                                   |
| 19  | VSS                       | VSS Supply.                                                                   |
| 20  | PPMU_CMPH1                | PPMU Go/No-Go Comparator High Output, Channel 1.                              |
| 21  | AGND                      | Analog Ground.                                                                |
| 22  | AGND                      | Analog Ground.                                                                |
| 23  | PPMU_CMPL1                | PPMU Go/No-Go Comparator Low Output, Channel 1.                               |
| 24  | PPMU_MEAS1                | PPMU Analog Measure Output, Channel 1.                                        |
| 25  | DGND                      | Digital Logic Ground.                                                         |
| 26  | DUTGND                    | DUT Ground Sense Input.                                                       |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

| Pin | Mnemonic           | Description                                                         |
|-----|--------------------|---------------------------------------------------------------------|
| 27  | ALARM              | Fault Alarm Open Drain Output.                                      |
| 28  | VSS                | VSS Supply.                                                         |
| 29  | DGND               | Digital Logic Ground.                                               |
| 30  | $\overline{CS}$    | Serial Programmable Interface (SPI) Chip Select Input (Active Low). |
| 31  | $\overline{BUSY}$  | Serial Programmable Interface (SPI) Busy Output (Active Low).       |
| 32  | SDO                | Serial Programmable Interface (SPI) Serial Data Output.             |
| 33  | SCLK               | Serial Programmable Interface (SPI) Clock Input.                    |
| 34  | SDI                | Serial Programmable Interface (SPI) Serial Data Input.              |
| 35  | VCC                | VCC Supply.                                                         |
| 36  | VDD                | VDD Supply.                                                         |
| 37  | $\overline{RST}$   | Reset Input (Active Low).                                           |
| 38  | VREF               | DAC Precision +5.0 V Reference Input.                               |
| 39  | VREFGND            | DAC Precision +0.0 V Reference Input.                               |
| 40  | PPMU_MEAS0         | PPMU Analog Measure Output, Channel 0.                              |
| 41  | PPMU_CMPL0         | PPMU Go/No-Go Comparator Low Output, Channel 0.                     |
| 42  | AGND               | Analog Ground.                                                      |
| 43  | AGND               | Analog Ground.                                                      |
| 44  | PPMU_CMPH0         | PPMU Go/No-go Comparator High Output, Channel 0.                    |
| 45  | VSS                | VSS Supply.                                                         |
| 46  | VDD                | VDD Supply.                                                         |
| 47  | PGND               | Power Ground.                                                       |
| 48  | CMPH0              | High Speed Comparator High Output, Channel 0.                       |
| 49  | $\overline{CMPH0}$ | High Speed Comparator High Output Complement, Channel 0.            |
| 50  | VTTC0              | Comparator Supply Termination, Channel 0.                           |
| 51  | $\overline{CMPL0}$ | High Speed Comparator Low Output Complement, Channel 0.             |
| 52  | CMPL0              | High Speed Comparator Low Output, Channel 0.                        |
| 53  | FFCAPA0            | PPMU External Feed Forward Capacitor Pin A, Channel 0.              |
| 54  | FFCAPB0            | PPMU External Feed Forward Capacitor Pin B, Channel 0.              |
| 55  | SCAP0              | PPMU External Compensation Capacitor, Channel 0.                    |
| 56  | $\overline{RCV0}$  | High Speed Receive Input Complement, Channel 0.                     |
| 57  | RCV0               | High Speed Receive Input, Channel 0.                                |
| 58  | NC                 | This pin is open. No internal connection.                           |
| 59  | $\overline{DAT0}$  | High Speed Data Input Complement, Channel 0.                        |
| 60  | DAT0               | High Speed Data Input, Channel 0.                                   |
| 61  | HVOUT              | VHH Output Pin.                                                     |
| 62  | PPMU_S0            | PPMU External Sense Connect, Channel 0.                             |
| 63  | VPLUS              | VPLUS Supply.                                                       |
| 64  | VSS                | VSS Supply.                                                         |
| 65  | PMU_S0             | System PMU Sense Input, Channel 0.                                  |
| 66  | VDD                | VDD Supply.                                                         |
| 67  | VDDO0              | VDD Supply, Driver Output Stage, Channel 0.                         |
| 68  | DUT0               | DUT Pin, Channel 0.                                                 |
| 69  | VSSO0              | VSS Supply, Driver Output Stage, Channel 0.                         |
| 70  | VSS                | VSS Supply.                                                         |

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS****Table 17. Pin Function Descriptions**

| Pin | Mnemonic | Description                                 |
|-----|----------|---------------------------------------------|
| 71  | PGND     | Power Ground.                               |
| 72  | VDD      | VDD Supply.                                 |
| 73  | VSS      | VSS Supply.                                 |
| 74  | AGND     | Analog Ground.                              |
| 75  | VSS      | VSS Supply.                                 |
| 76  | VDD      | VDD Supply.                                 |
| 77  | PGND     | Power Ground.                               |
| 78  | VSS      | VSS Supply.                                 |
| 79  | VSS01    | VSS Supply, Driver Output Stage, Channel 1. |
| 80  | DUT1     | DUT Pin, Channel 1.                         |
| 81  | VDD01    | VDD Supply, Driver Output Stage, Channel 1. |
| 82  | VDD      | VDD Supply.                                 |
| 83  | PMU_S1   | System PMU Sense Input, Channel 1.          |
| 84  | VSS      | VSS Supply.                                 |

## TYPICAL PERFORMANCE CHARACTERISTICS

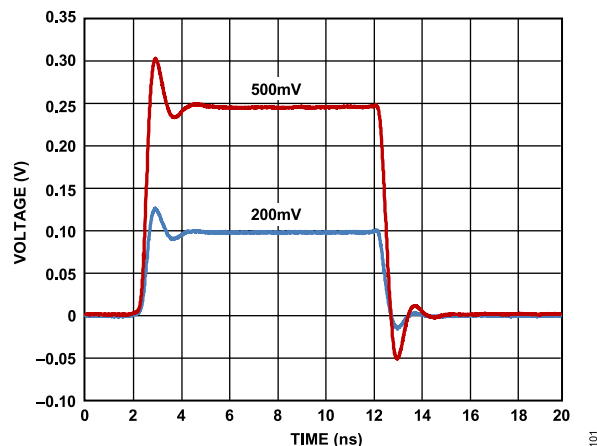


Figure 9. Driver Small Signal Response,  $V_{IH} = 0.2\text{ V}$ ,  $0.5\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

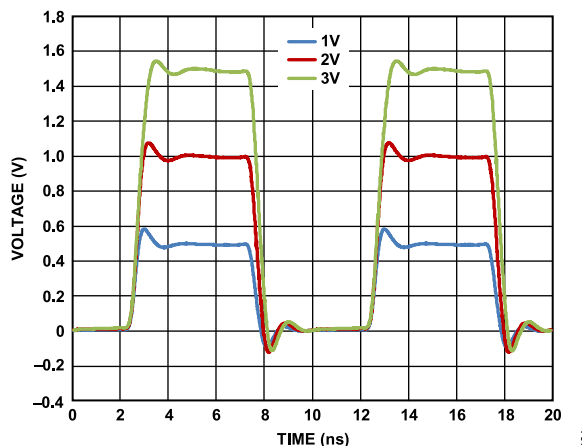


Figure 12. 100 MHz Driver Response,  $V_{IH} = 1.0\text{ V}$ ,  $2.0\text{ V}$ ,  $3.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

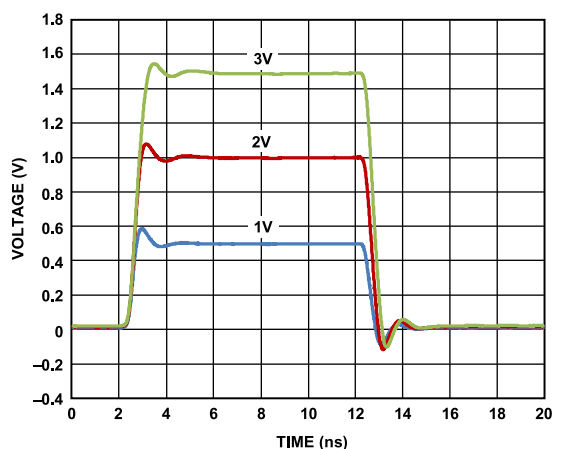


Figure 10. Driver Large Signal Response,  $V_{IH} = 1.0\text{ V}$ ,  $2.0\text{ V}$ ,  $3.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

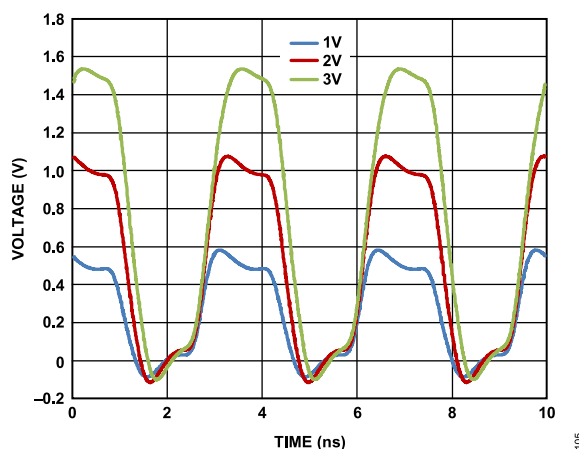


Figure 13. 300 MHz Driver Response,  $V_{IH} = 1.0\text{ V}$ ,  $2.0\text{ V}$ ,  $3.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

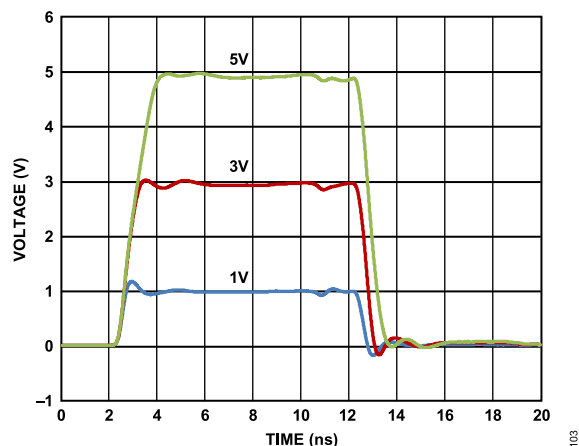


Figure 11. Driver Large Signal Response,  $V_{IH} = 1.0\text{ V}$ ,  $3.0\text{ V}$ ,  $5.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Unterminated

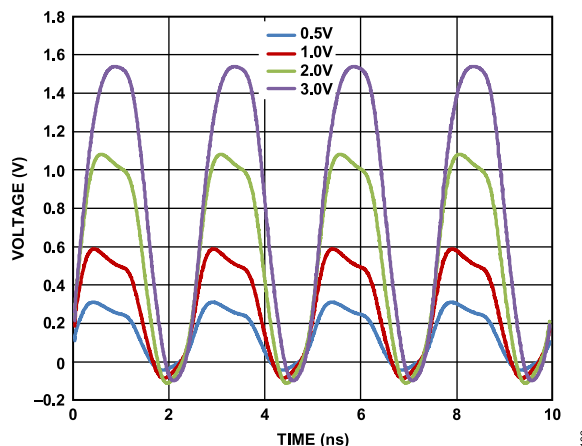


Figure 14. 400 MHz Driver Response,  $V_{IH} = 0.5\text{ V}$ ,  $1.0\text{ V}$ ,  $2.0\text{ V}$ ,  $3.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

## TYPICAL PERFORMANCE CHARACTERISTICS

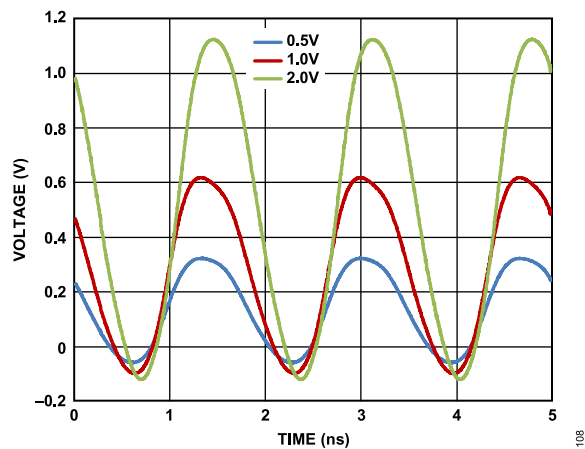


Figure 15. 600 MHz Driver Response,  $V_{IH} = 0.5\text{ V}$ ,  $1.0\text{ V}$ ,  $2.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

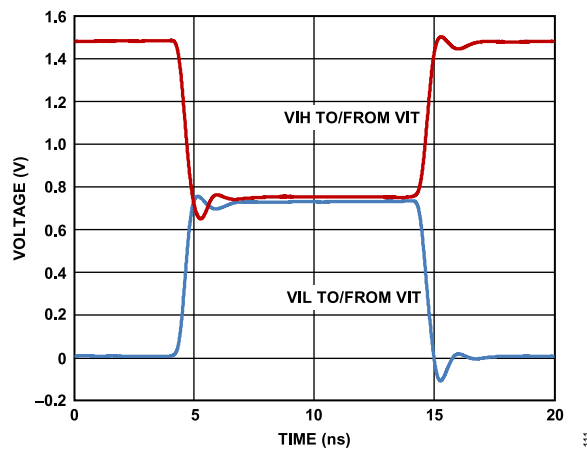


Figure 18. Driver Active ( $V_{IH}/V_{IL}$ ) to/from  $V_{TERM}$  Transition;  $V_{IH} = 3.0\text{ V}$ ,  $V_{IT} = 1.5\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

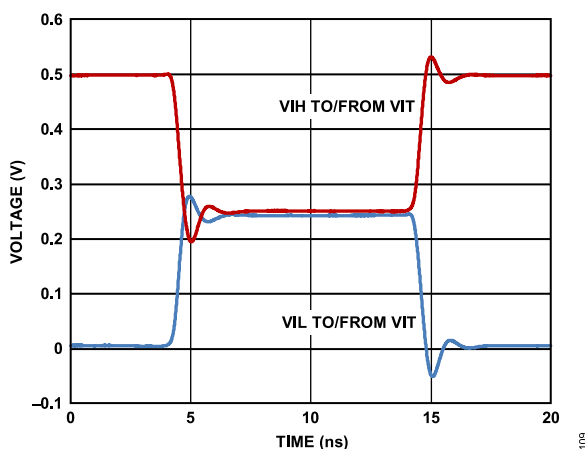


Figure 16. Driver Active ( $V_{IH}/V_{IL}$ ) to/from  $V_{TERM}$  Transition;  $V_{IH} = 1.0\text{ V}$ ,  $V_{IT} = 0.5\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

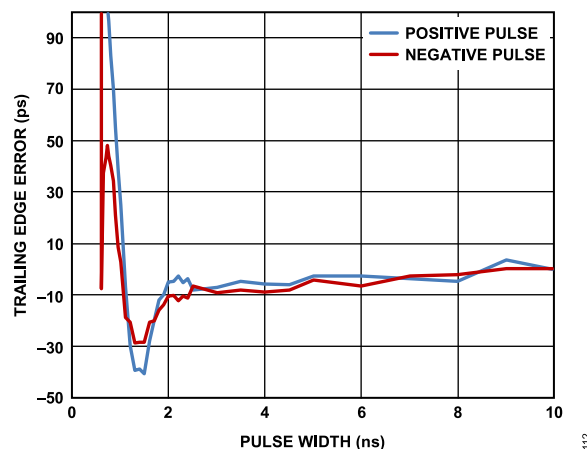


Figure 19. Driver Trailing Edge Timing Error Pulse Width,  $V_{IH} = 0.2\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

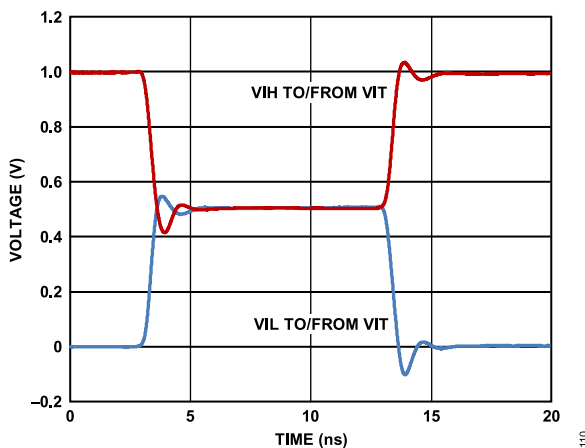


Figure 17. Driver Active ( $V_{IH}/V_{IL}$ ) to/from  $V_{TERM}$  Transition;  $V_{IH} = 2.0\text{ V}$ ,  $V_{IT} = 1.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

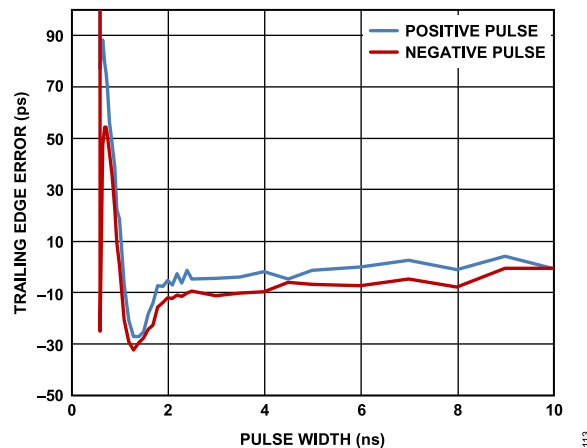


Figure 20. Driver Trailing Edge Timing Error vs. Pulse Width,  $V_{IH} = 0.5\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

## TYPICAL PERFORMANCE CHARACTERISTICS

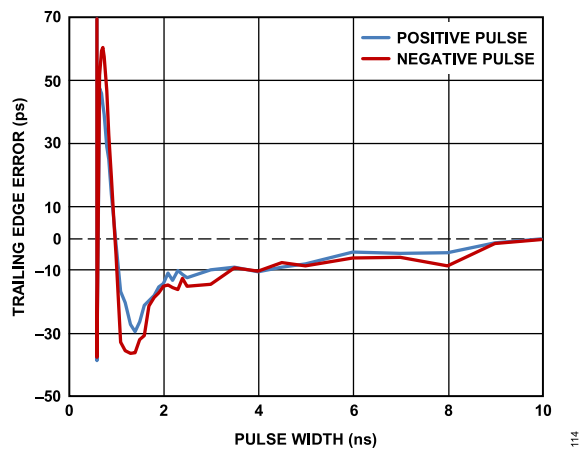


Figure 21. Driver Trailing Edge Timing Error vs. Pulse Width,  $V_{IH} = 1.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

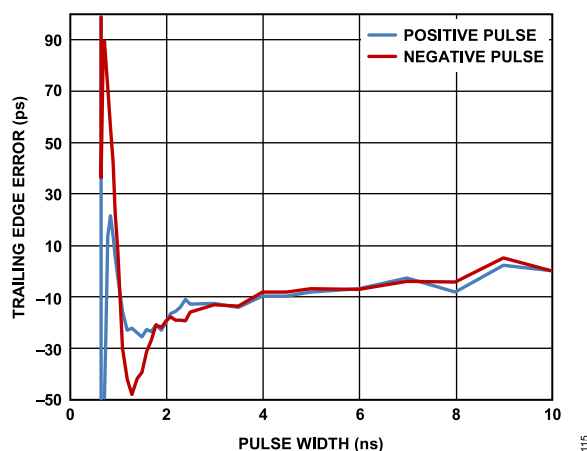


Figure 22. Driver Trailing Edge Timing Error vs. Pulse Width,  $V_{IH} = 2.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

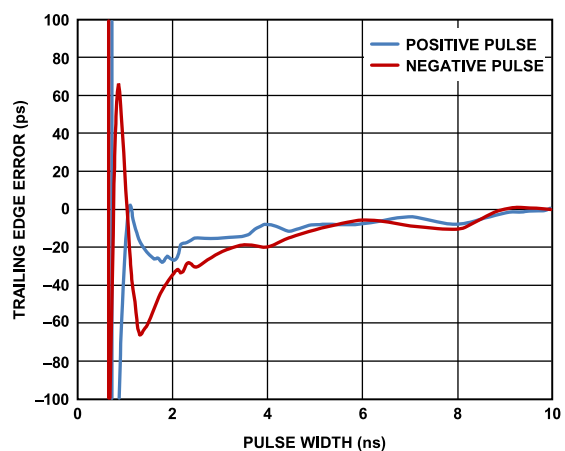


Figure 23. Driver Trailing Edge Timing Error vs. Pulse Width,  $V_{IH} = 3.0\text{ V}$ ;  $V_{IL} = 0.0\text{ V}$ ,  $50\ \Omega$  Termination

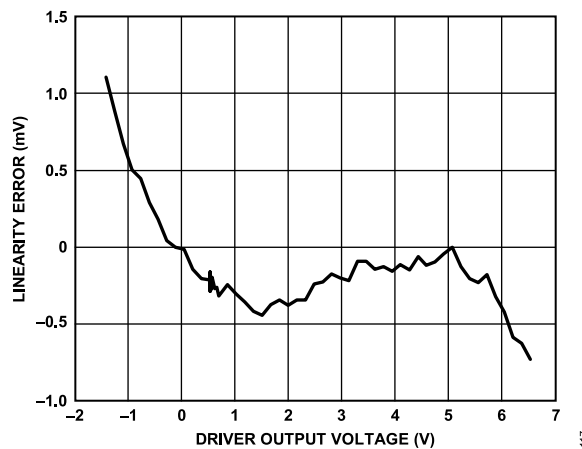


Figure 24. Driver  $V_{IH}$  Linearity Error

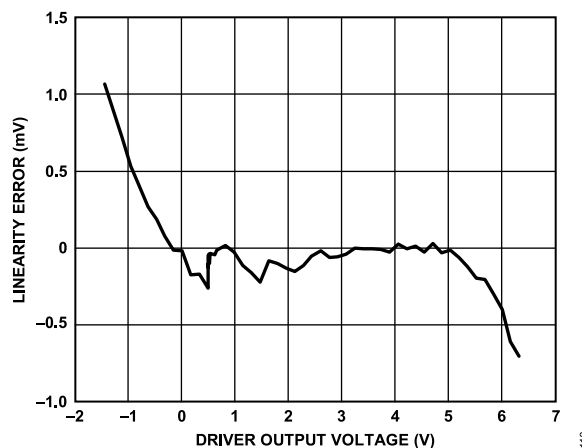


Figure 25. Driver  $V_{IL}$  Linearity Error

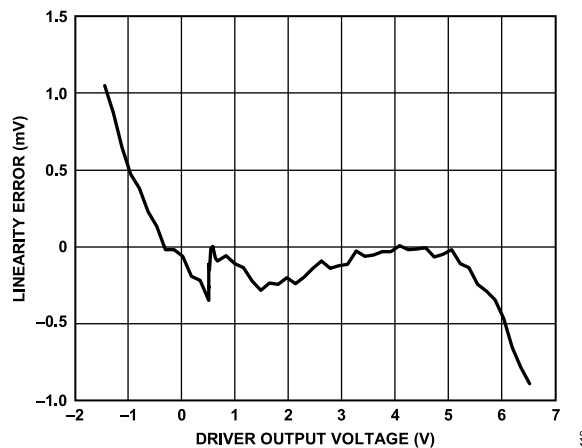


Figure 26. Driver  $V_{IT}$  Linearity Error

## TYPICAL PERFORMANCE CHARACTERISTICS

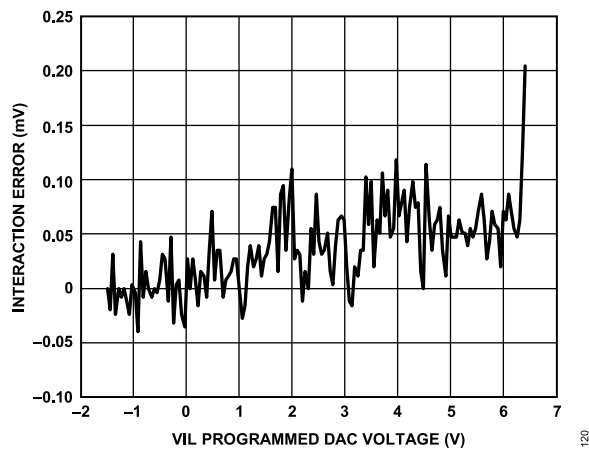


Figure 27. Driver Interaction Error  $V_{IH}$  vs.  $V_{IL}$ ,  $V_{IH} = +6.5$  V,  $V_{IL}$  Swept from  $-1.5$  V to  $+6.5$  V

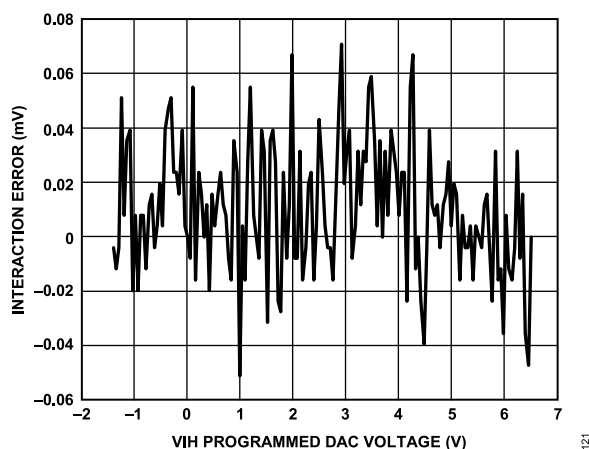


Figure 28. Driver Interaction Error  $V_{IL}$  vs.  $V_{IH}$ ;  $V_{IL} = -1.5$  V,  $V_{IH}$  Swept from  $-1.5$  V to  $+6.5$  V

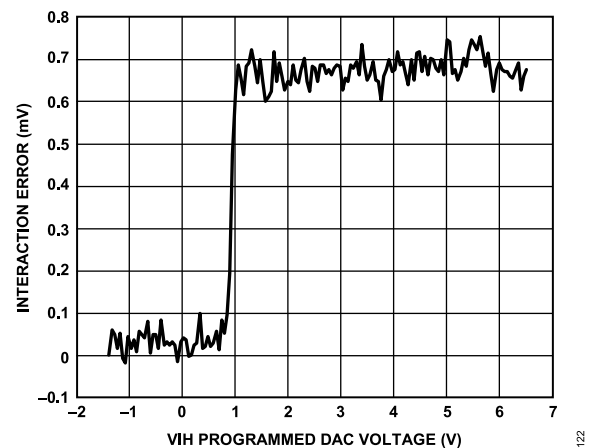


Figure 29. Driver Interaction Error  $V_{IT}$  vs.  $V_{IH}$ ,  $V_{IT} = +1.0$  V,  $V_{IH}$  Swept from  $-1.5$  V to  $+6.5$  V

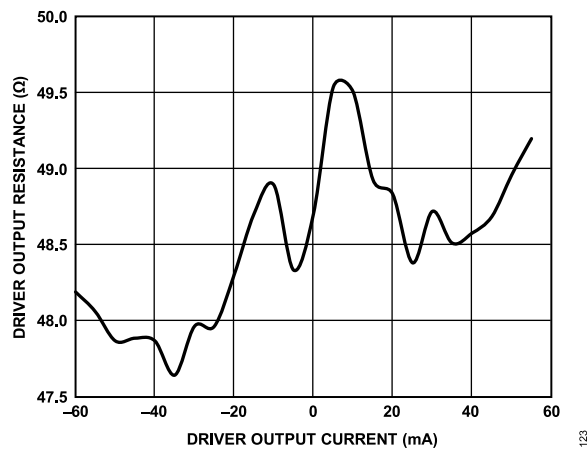


Figure 30. Driver Output Resistance vs. Output Current

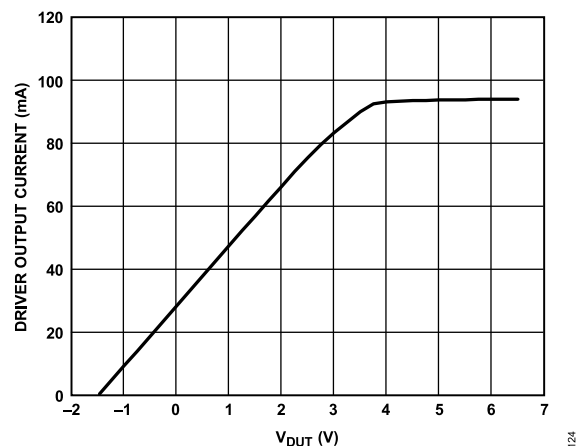


Figure 31. Driver Output Current Limit; Driver Programmed to  $-1.5$  V,  $V_{DUT}$  Swept  $-1.5$  V to  $+6.5$  V

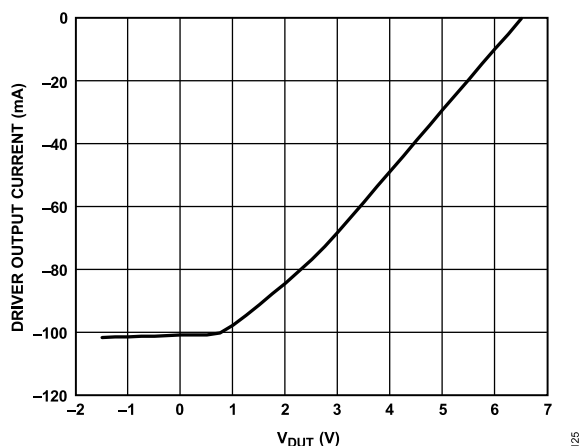


Figure 32. Driver Output Current Limit. Driver Programmed to  $6.5$  V,  $V_{DUT}$  Swept  $-1.5$  V to  $+6.5$  V

## TYPICAL PERFORMANCE CHARACTERISTICS

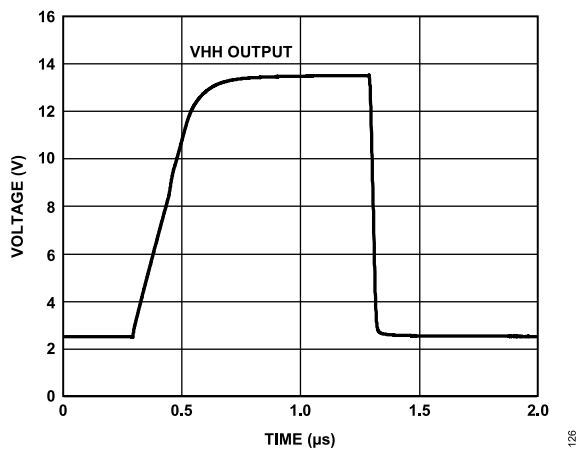


Figure 33. HVOUT Transient Response, VHH = 13.5 V

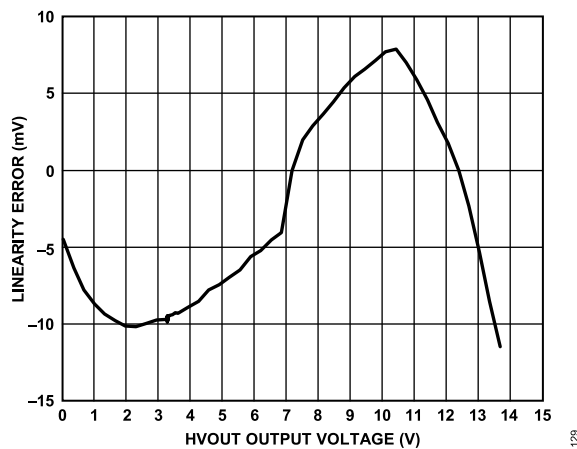


Figure 36. HVOUT VHH Linearity Error

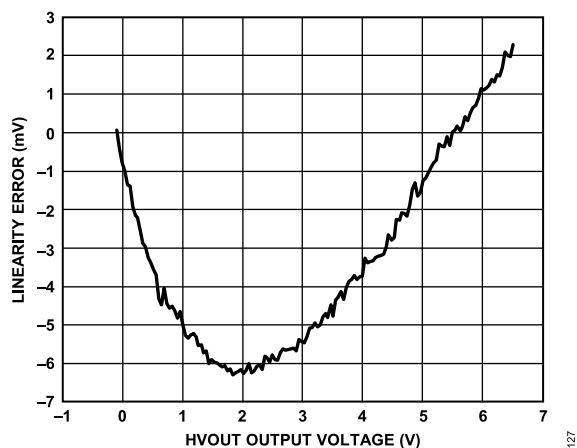


Figure 34. HVOUT VIH Linearity Error

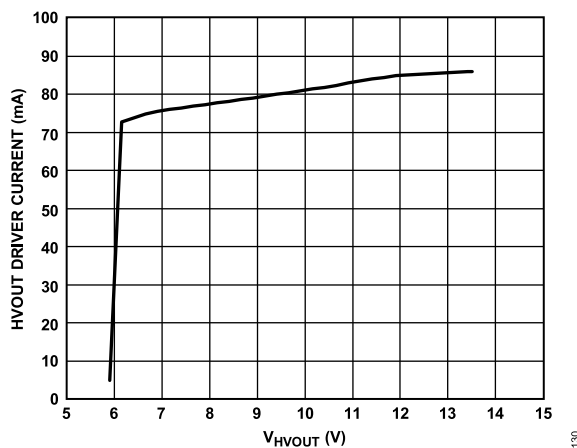


Figure 37. HVOUT VHH Output Current Limit; VHH = 5.9 V, HVOUT Swept 5.9 V to 13.5 V

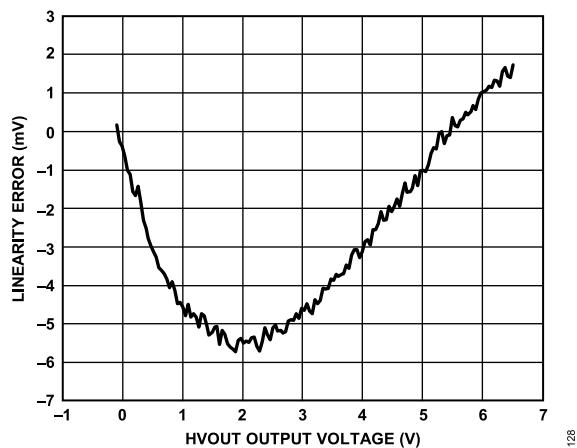


Figure 35. HVOUT VIL Linearity Error

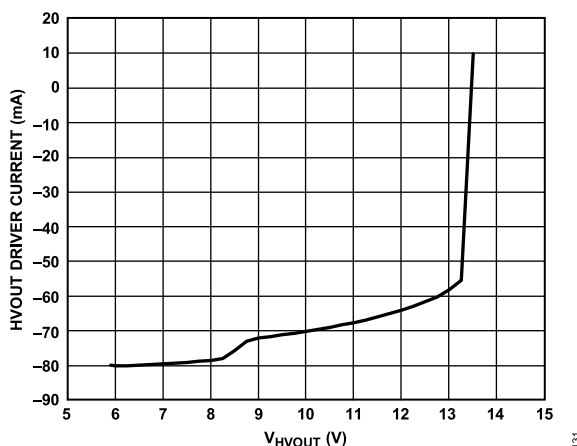


Figure 38. HVOUT VHH Output Current Limit; VHH = 13.5 V, HVOUT Swept 5.9 V to 13.5 V

## TYPICAL PERFORMANCE CHARACTERISTICS

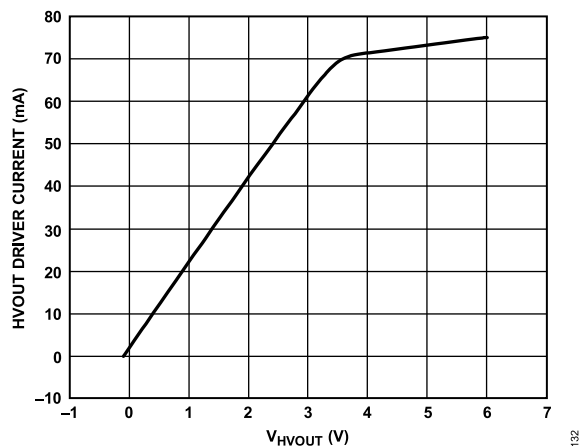


Figure 39. HVOOUT VIL Output Current Limit;  $V_{IL} = -0.1$  V, HVOOUT Swept  $-0.1$  V to 6.0 V

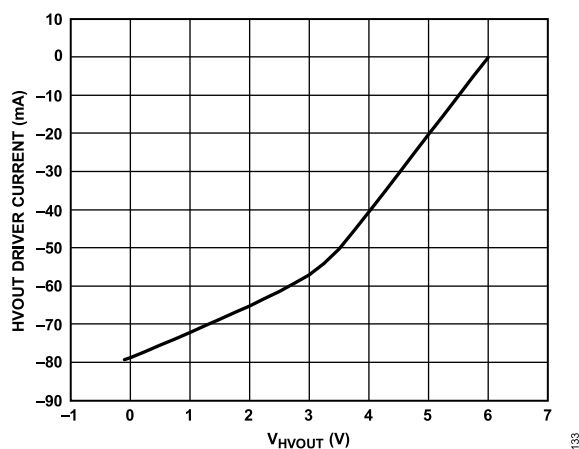


Figure 40. HVOOUT VIH Output Current Limit;  $V_{IH} = 6.0$  V, HVOOUT Swept  $-0.1$  V to 6.0 V

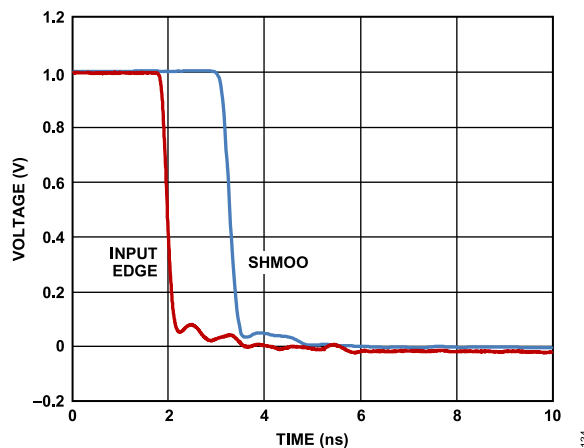


Figure 41. Normal Window Comparator Shmoo 1.0 V Swing; 50  $\Omega$  Termination, 200 ps (20% to 80%)

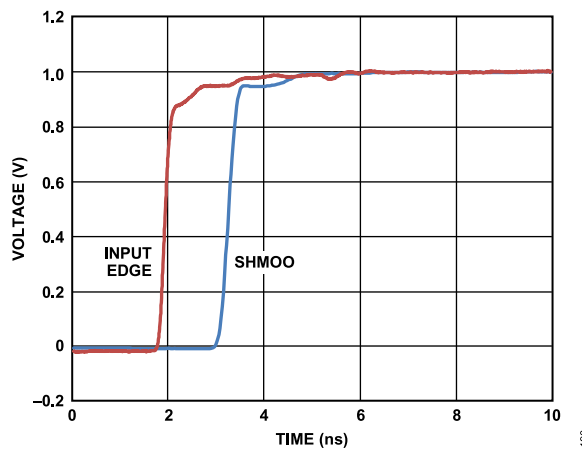


Figure 42. Normal Window Comparator Shmoo; 1.0 V Swing, 50  $\Omega$  Termination, 200 ps (20% to 80%)

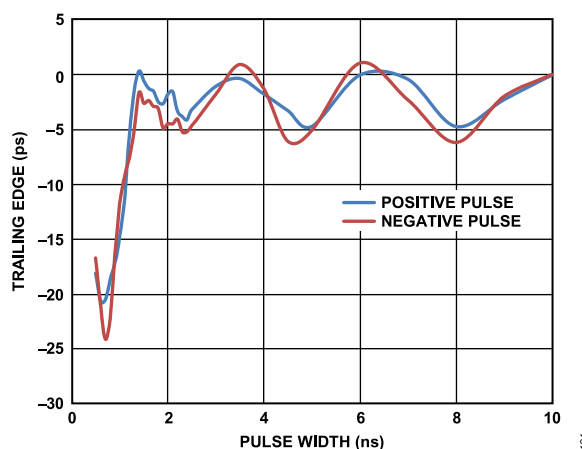


Figure 43. Normal Window Comparator Trailing Edge Timing Error vs. Input Pulse Width; 50  $\Omega$  Termination, 1.0 V Swing, 200 ps (20% to 80%)

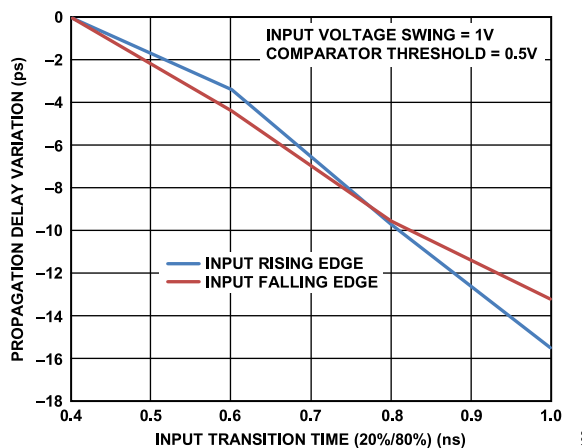


Figure 44. Normal Window Comparator Input Transition Time (20%/80%), 50  $\Omega$  Termination

## TYPICAL PERFORMANCE CHARACTERISTICS

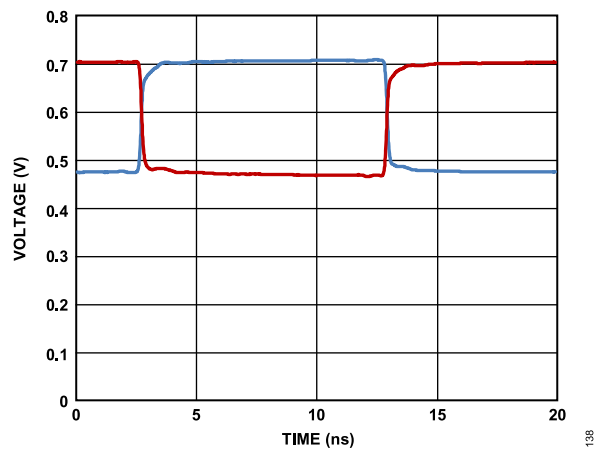


Figure 45. Comparator Output Waveform

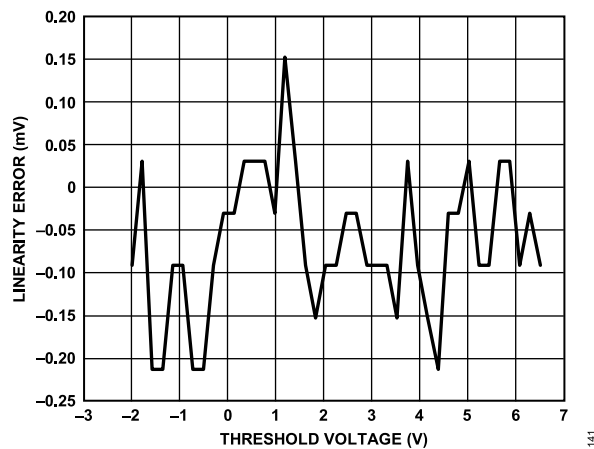


Figure 48. PPMU Go/No-Go Comparator Linearity Error

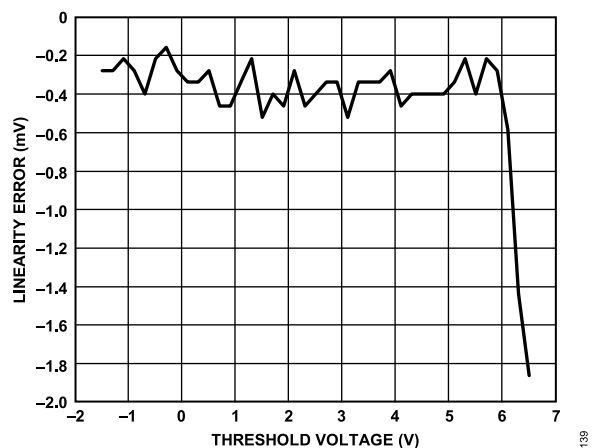


Figure 46. Normal Window Comparator Threshold Linearity Error

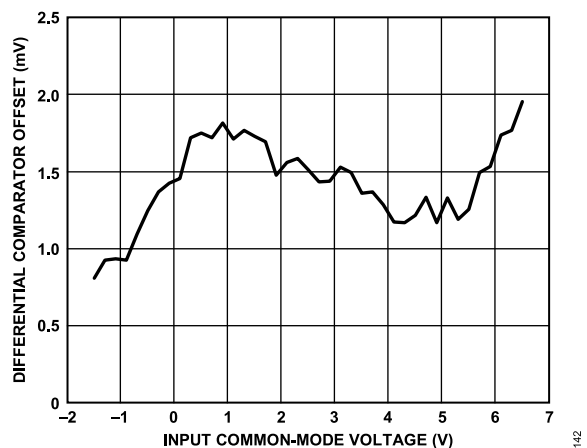


Figure 49. Differential Comparator CMR Error

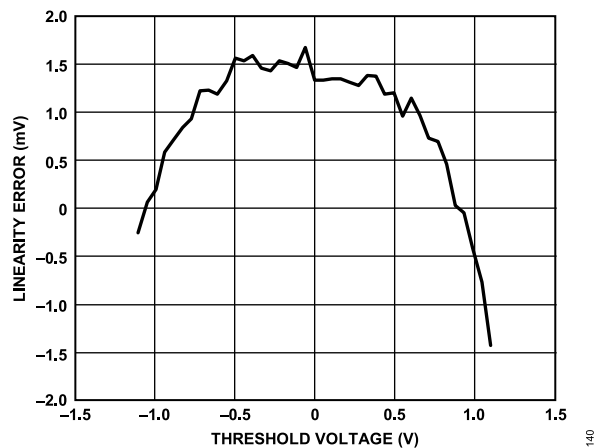
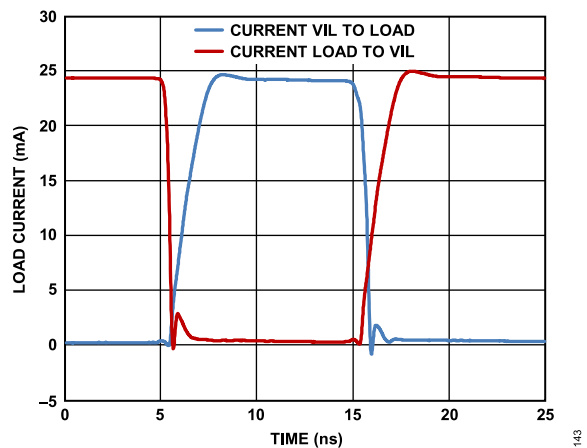


Figure 47. Differential Comparator Threshold Linearity Error

Figure 50. Active Load Response to/from Drive  $V_{IL} = 0\text{ V}$ ,  $50\ \Omega$  Termination,  $I_{OL} = 25\text{ mA}$ ,  $V_{COM} = 2\text{ V}$

## TYPICAL PERFORMANCE CHARACTERISTICS

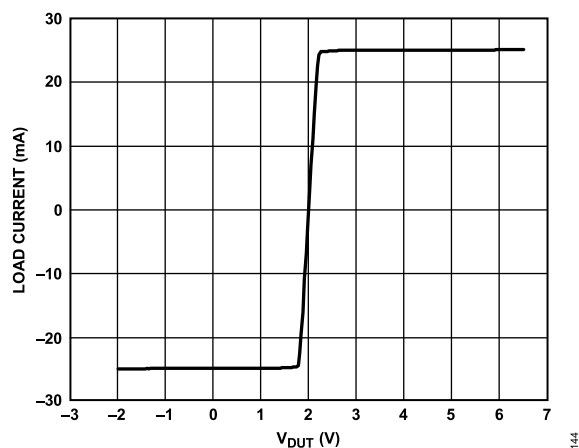


Figure 51. Active Load Commutation Response,  $V_{COM} = 2.0\text{ V}$ ,  $I_{OH} = I_{OL} = 25\text{ mA}$

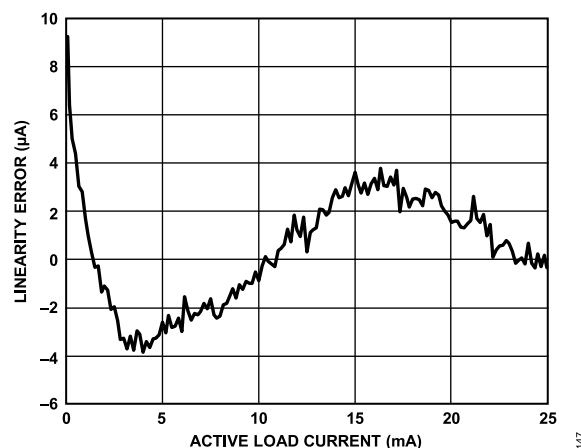


Figure 54. Active Load  $I_{OL}$  Linearity Error

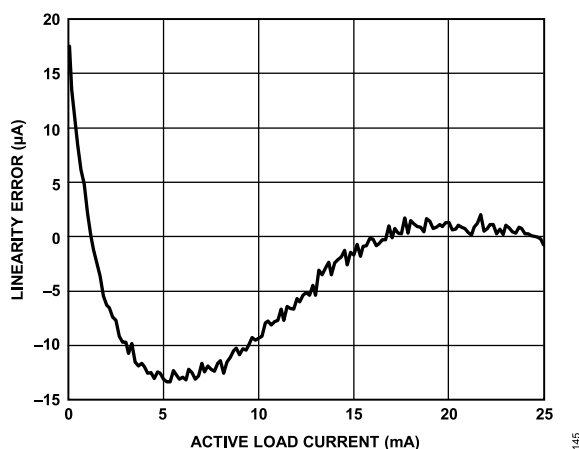


Figure 52. Active Load  $I_{OH}$  Linearity Error

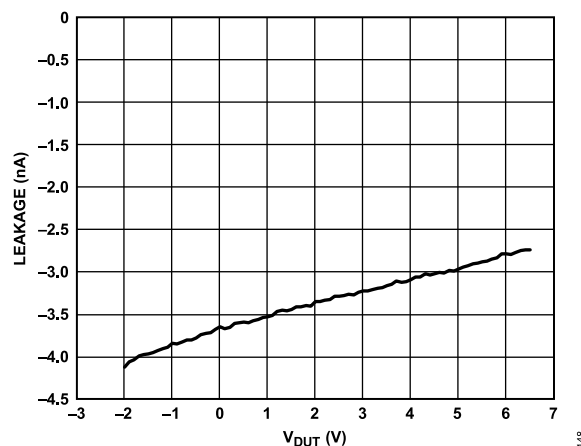


Figure 55. DUTx Pin Leakage in Low Leakage Mode

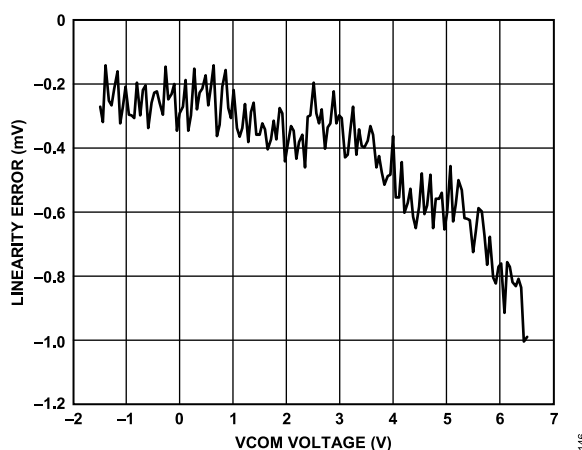


Figure 53. Active Load  $V_{COM}$  Linearity Error

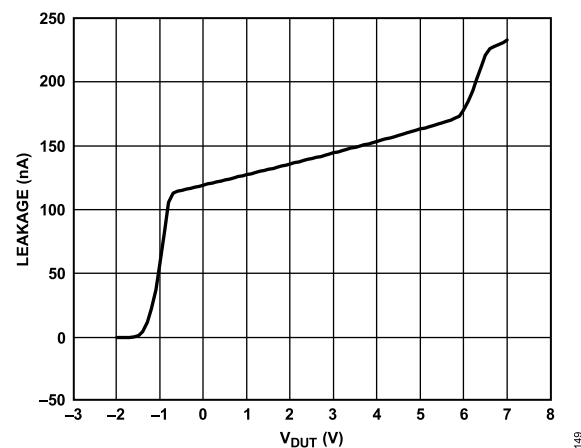


Figure 56. DUTx Pin Leakage in High-Z Mode

## TYPICAL PERFORMANCE CHARACTERISTICS

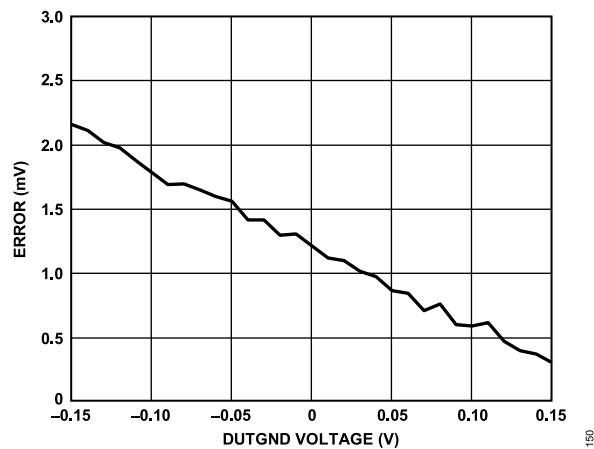


Figure 57. Typical DUTGND Transfer Function Voltage Error, Drive Low VIL = 0 V

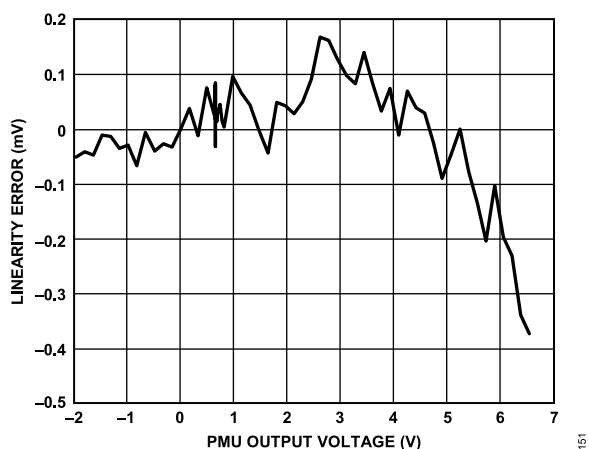


Figure 58. PPMU Force Voltage Linearity Error, All Ranges

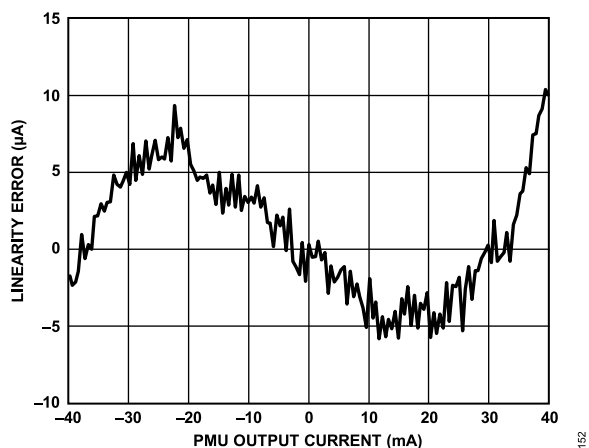


Figure 59. PPMU Range A Force Current Linearity Error

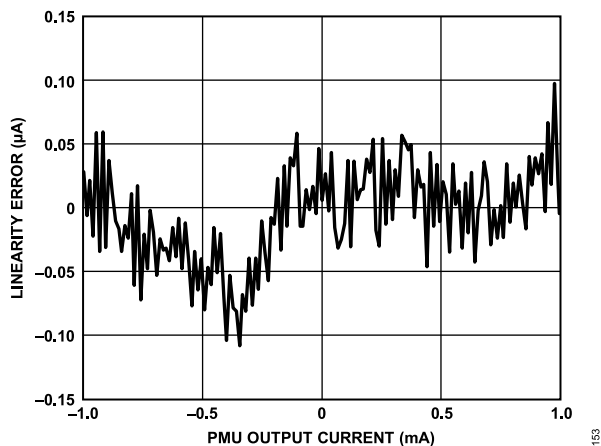


Figure 60. PPMU Range B Force Current Linearity Error

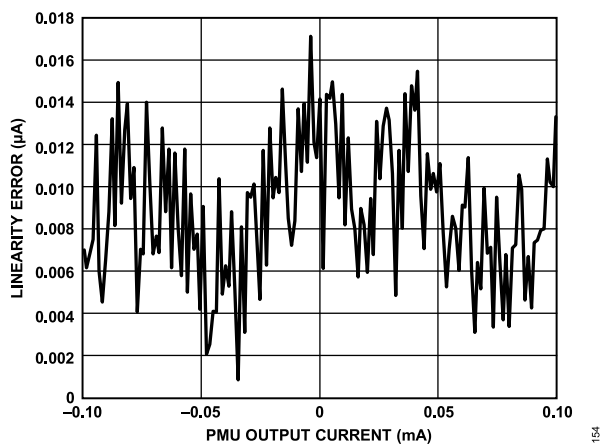


Figure 61. PPMU Range C Force Current Linearity Error

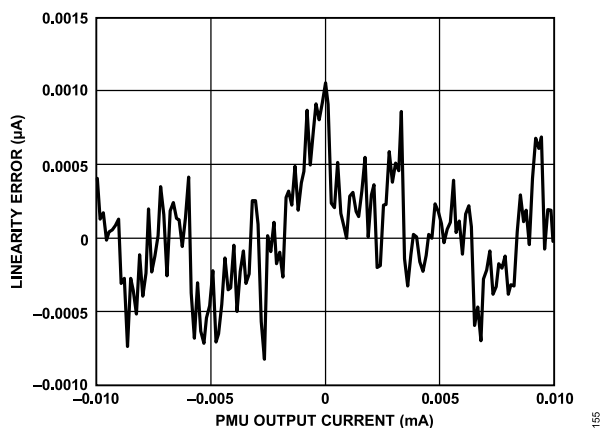


Figure 62. PPMU Range D Force Current Linearity Error

## TYPICAL PERFORMANCE CHARACTERISTICS

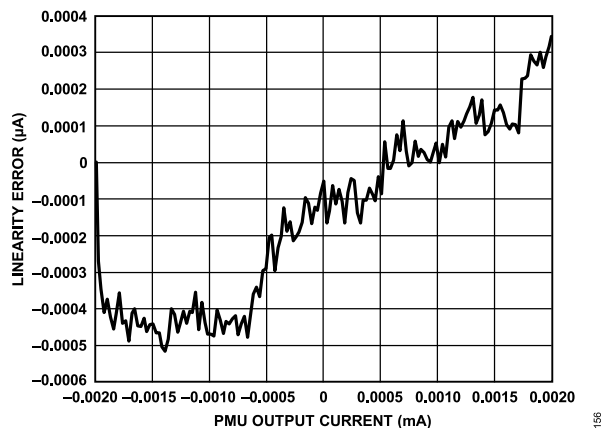


Figure 63. PPMU Range E Force Current Linearity Error

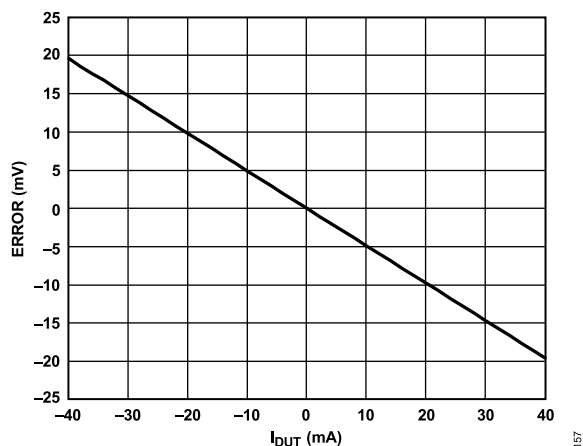


Figure 64. PPMU Force Voltage Range A Compliance Error at -2.0 V vs. Output Current, Internal Sense

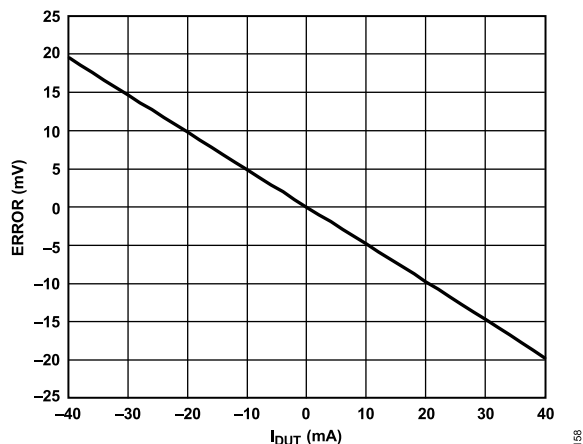


Figure 65. PPMU Force Voltage Range A Compliance Error at +5.75 V vs. Output Current, Internal Sense

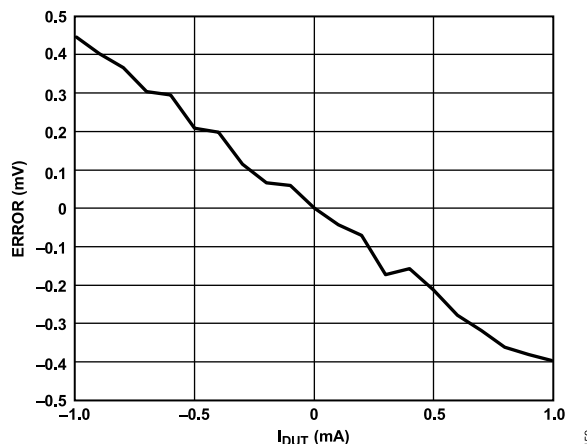


Figure 66. PPMU Force Voltage Range B Compliance Error at -2.0 V vs. Output Current, Internal Sense

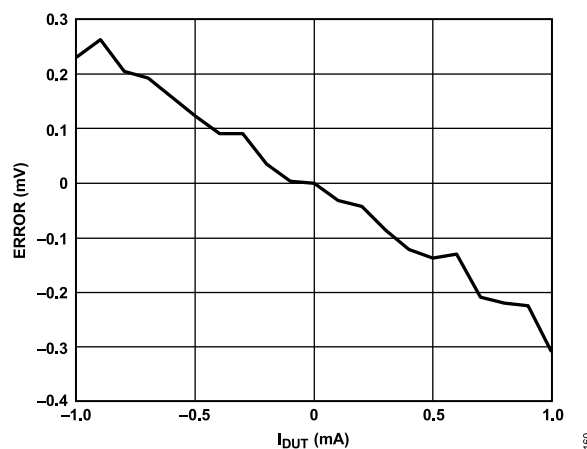


Figure 67. PPMU Force Voltage Range B Compliance Error at +6.5 V vs. Output Current, Internal Sense

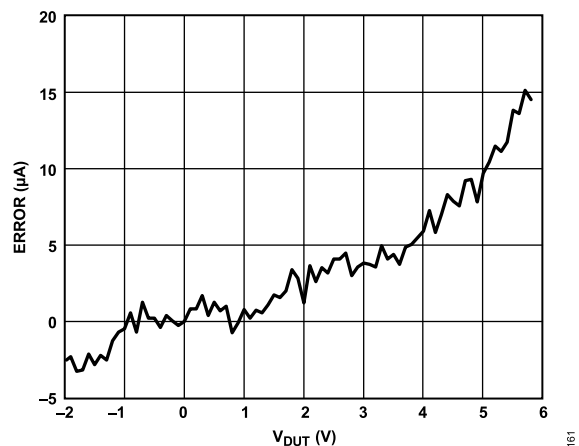


Figure 68. PPMU Force Current Range A Compliance Error at -40 mA vs. Output Voltage

## TYPICAL PERFORMANCE CHARACTERISTICS

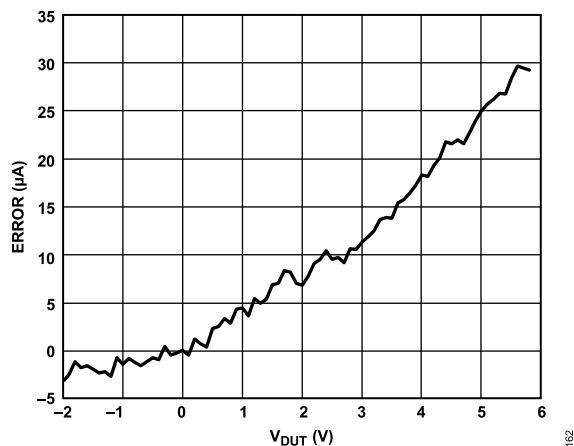


Figure 69. PPMU Force Current Range A Compliance Error at +40 mA vs. Output Voltage

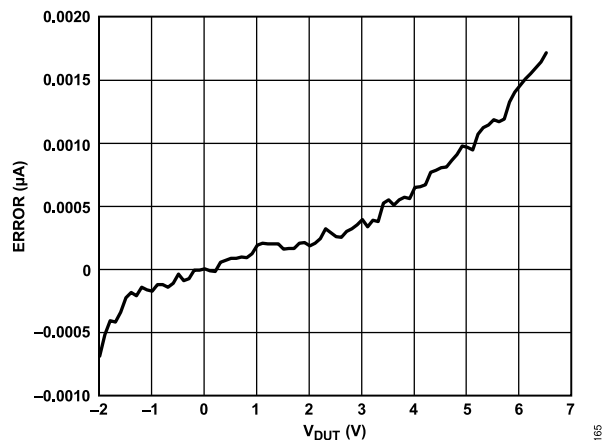


Figure 72. PPMU Force Current Range E Compliance Error at -2 µA vs. Output Voltage

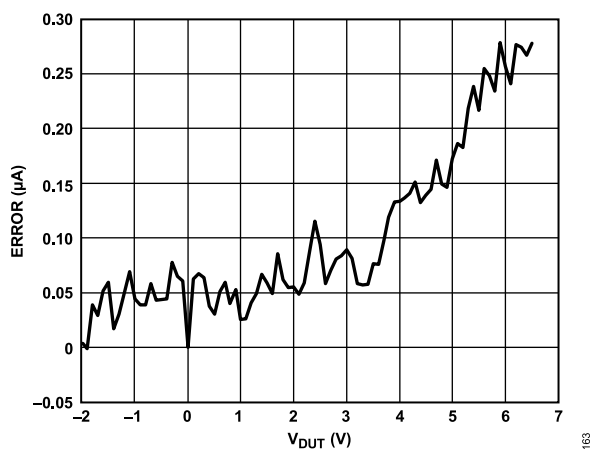


Figure 70. PPMU Force Current Range B Compliance Error at -1 mA vs. Output Voltage

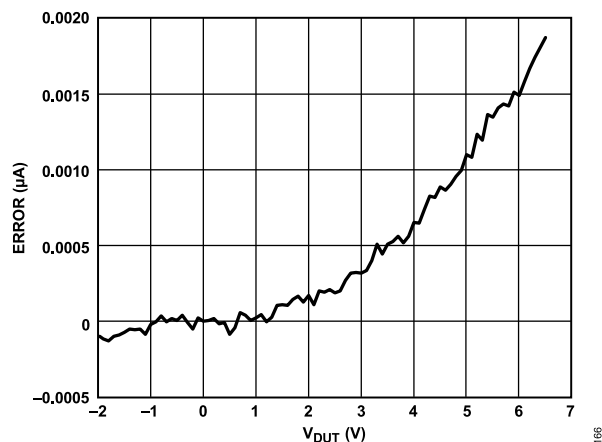


Figure 73. PPMU Force Current Range E Compliance Error at +2 µA vs. Output Voltage

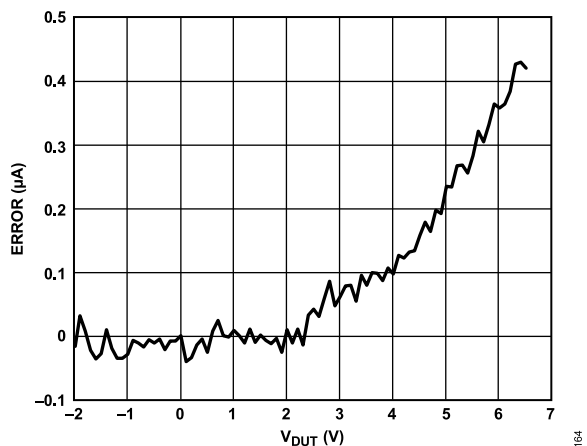


Figure 71. PPMU Force Current Range B Compliance Error at +1 mA vs. Output Voltage

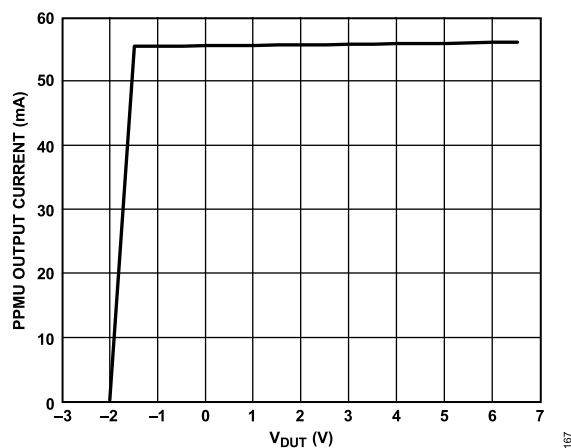


Figure 74. PPMU Force Voltage Output Current Limit Range A, FV = -2.0 V, V<sub>DUT</sub> Swept -2.0 V to +6.5 V

## TYPICAL PERFORMANCE CHARACTERISTICS

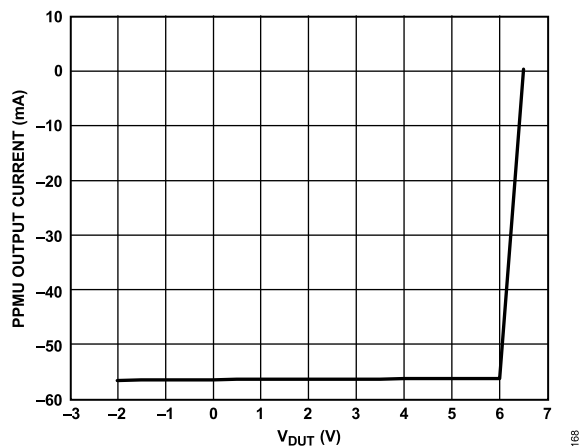


Figure 75. PPMU Force Voltage Output Current Limit Range A, FV = +6.5 V, VDUT Swept -2.0 V to +6.5 V

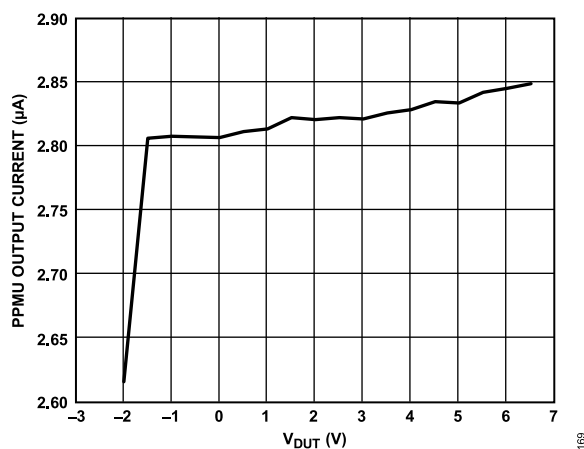


Figure 76. PPMU Force Voltage Output Current Limit Range E, FV = -2.0 V, VDUT Swept -2.0 V to +6.5 V

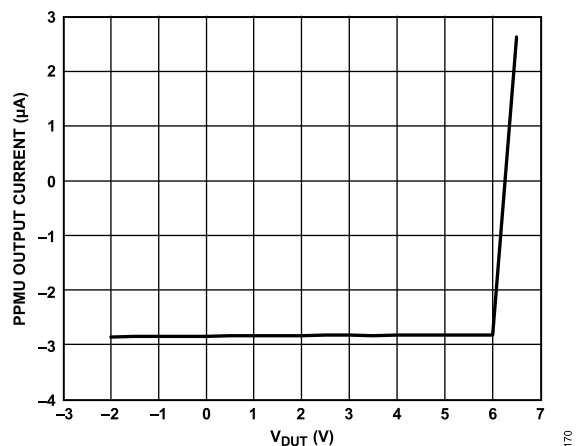


Figure 77. PPMU Force Voltage Output Current Limit Range E, FV = 6.5 V, VDUT Swept -2.0 V to +6.5 V

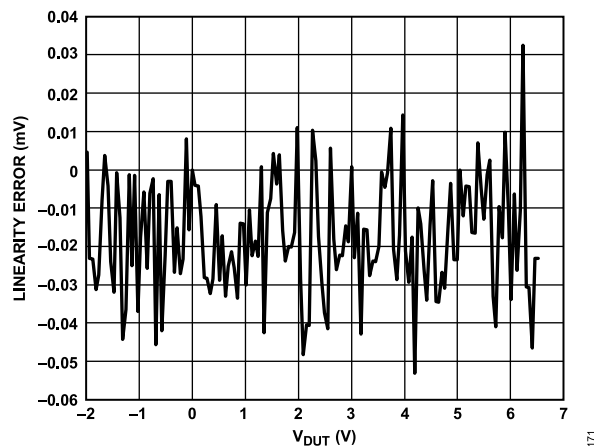


Figure 78. PPMU Range B Measure Voltage Linearity Error

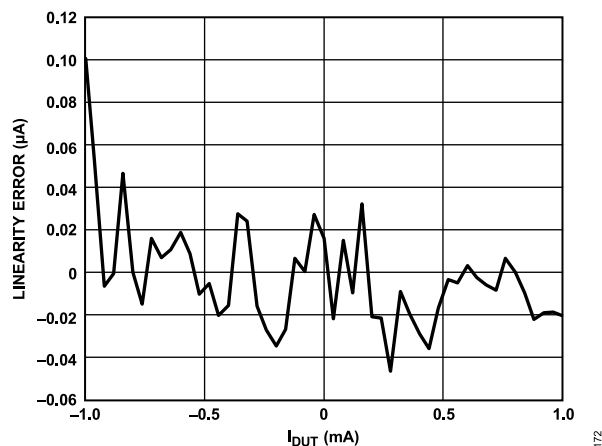


Figure 79. PPMU Range B Measure Current Linearity Error

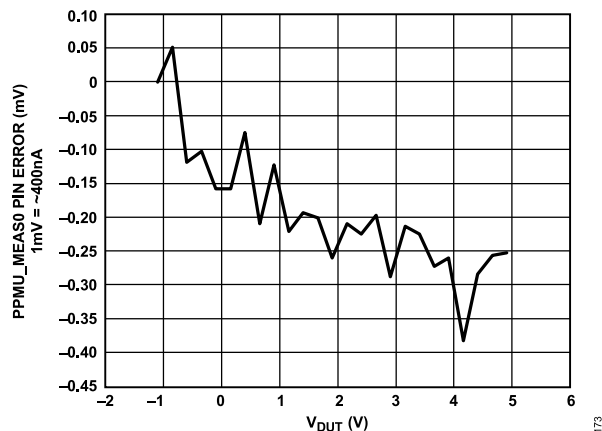


Figure 80. PPMU Measure Current CMR Error, (FVMI), Sourcing 0.5 mA

## TYPICAL PERFORMANCE CHARACTERISTICS

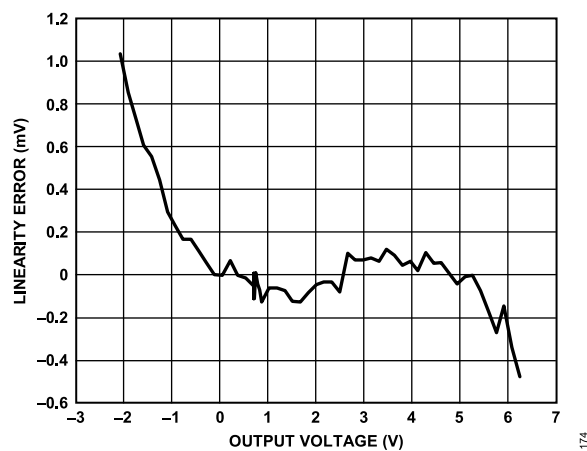


Figure 81. Reflection Clamp VCL Linearity Error

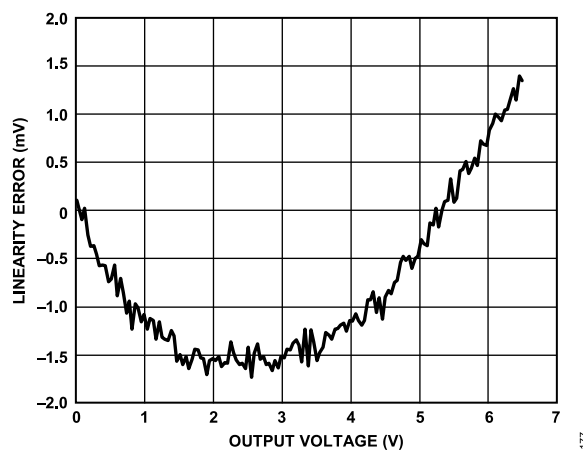


Figure 84. PPMU Voltage Clamp VCH Linearity Error

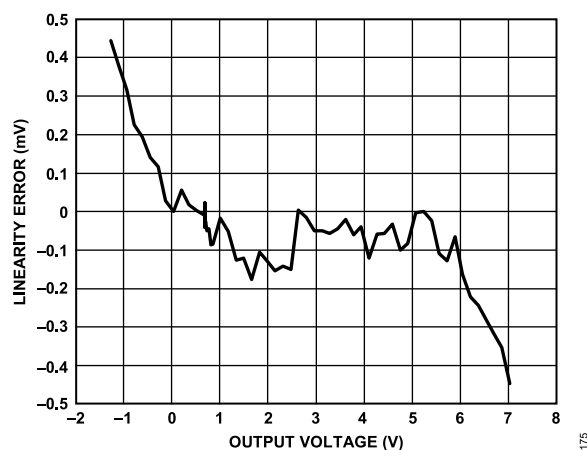


Figure 82. Reflection Clamp VCH Linearity Error

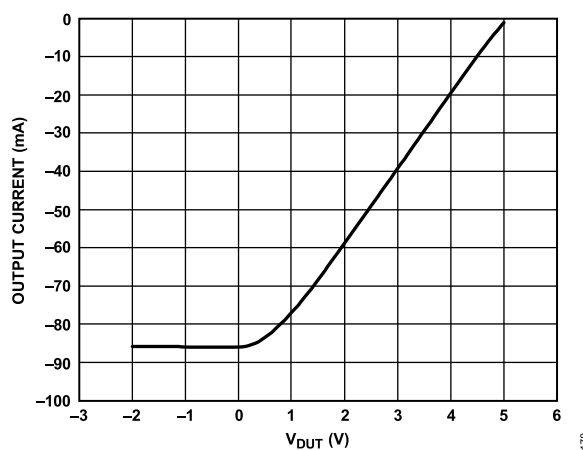


Figure 85. VCL Reflection Clamp Current Limit; VCH = 6 V, VCL = 5 V, VDUT Swept -2.0 V to +5.0 V

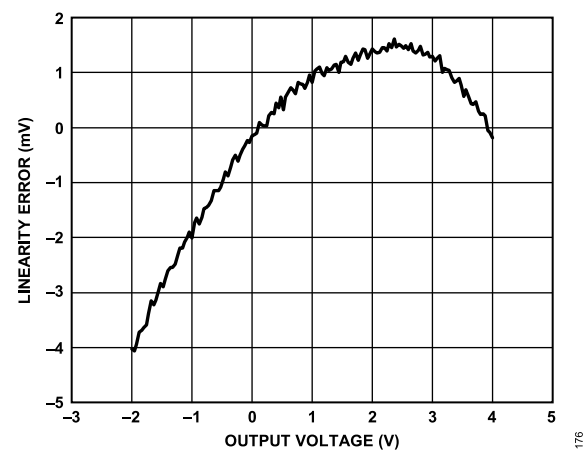


Figure 83. PPMU Voltage Clamp VCL Linearity Error

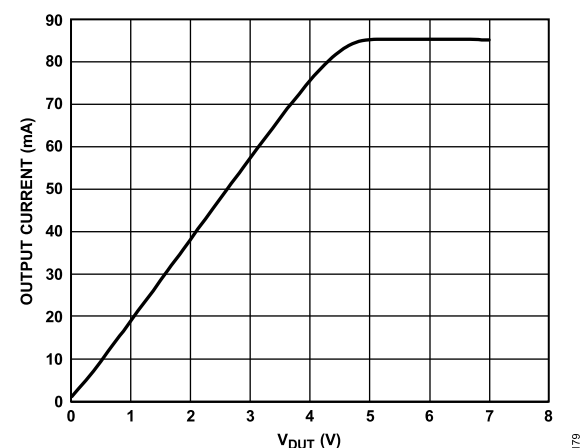


Figure 86. VCH Reflection Clamp Current Limit; VCH = 0 V, VCL = -2 V, VDUT Swept -2.0 V to +5.0 V

## TYPICAL PERFORMANCE CHARACTERISTICS

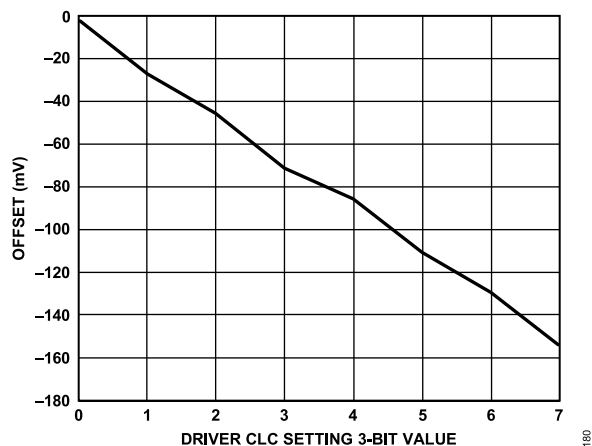


Figure 87. Driver Offset Error vs. Driver CLC Setting

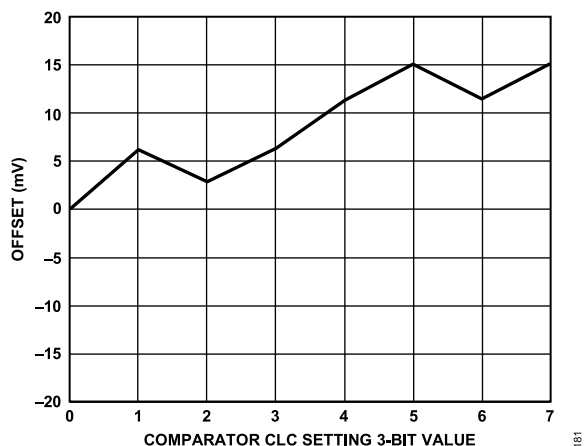


Figure 88. Normal Window Comparator Offset Error vs. CLC Setting

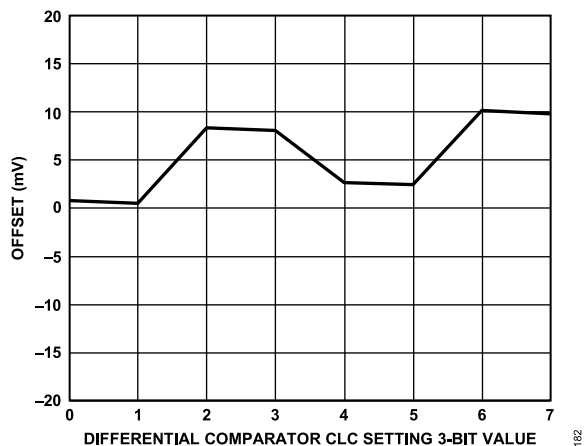


Figure 89. Differential Comparator Offset error vs. CLC Setting

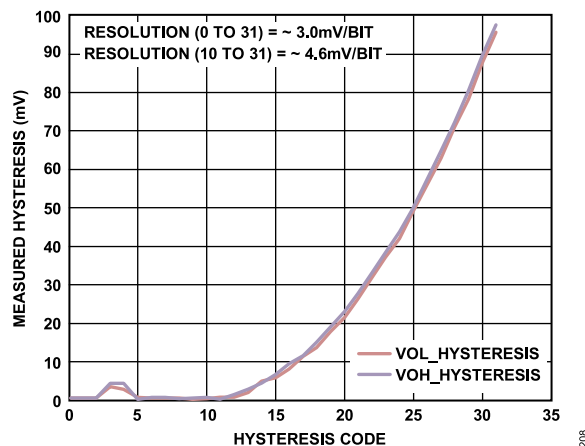


Figure 90. Normal Window Comparator Hysteresis Transfer Function

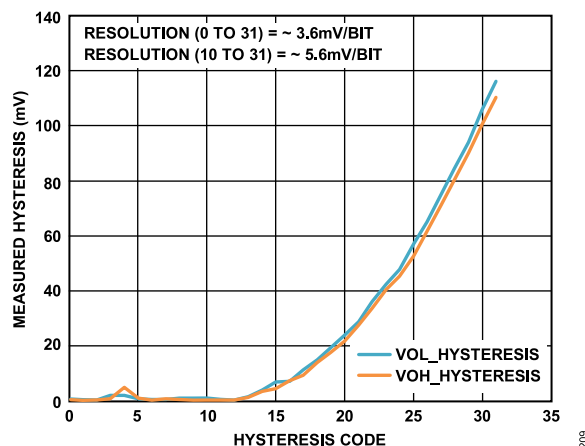
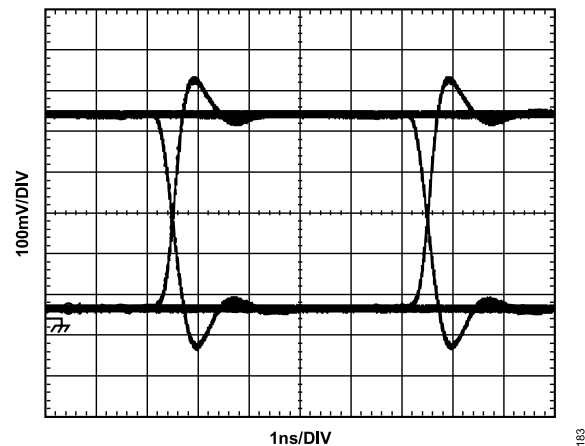
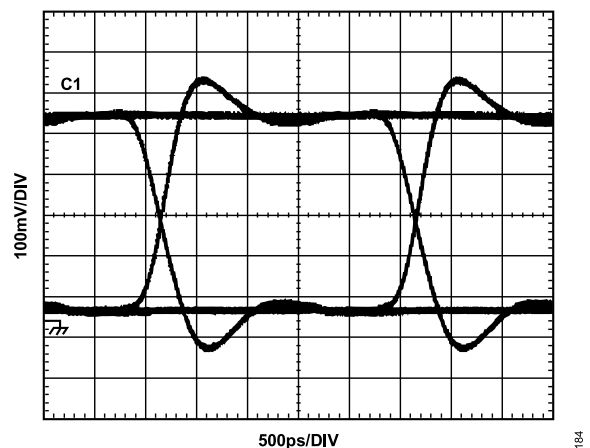
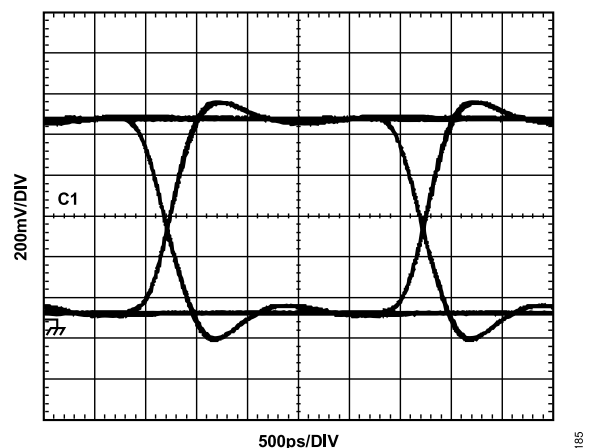
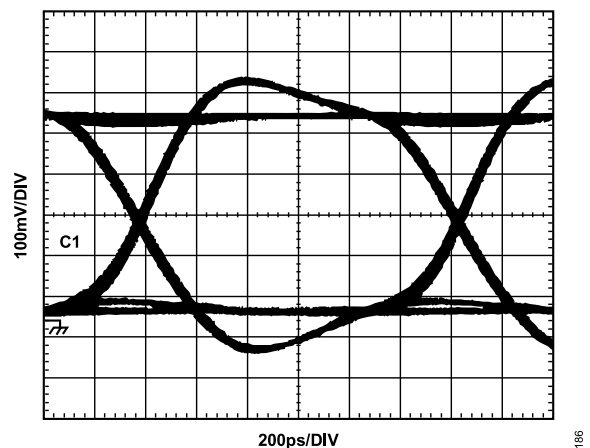
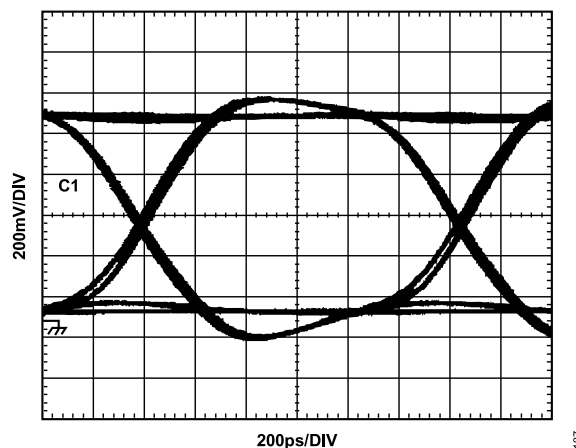
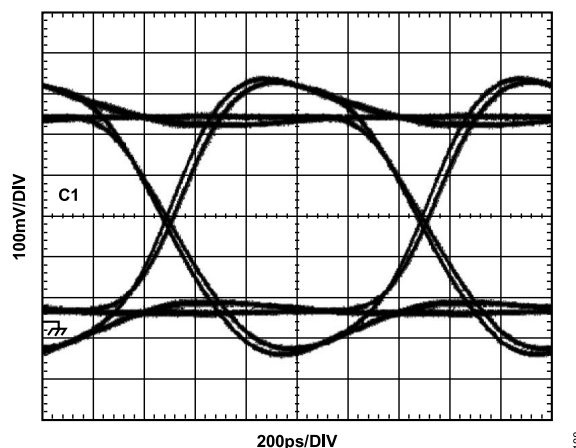
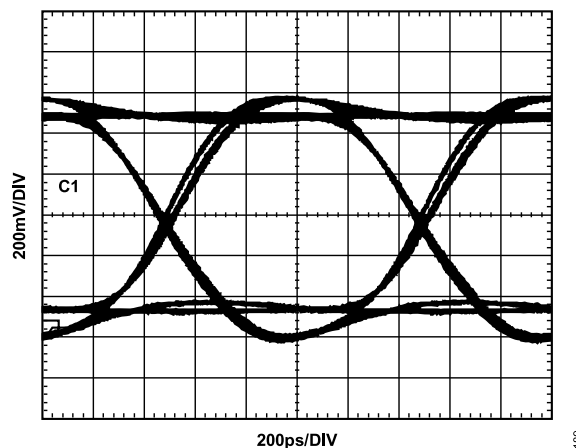


Figure 91. Differential Comparator Hysteresis Transfer Function

Figure 92. Driver Eye Diagram, 400 Mbps, PRBS31;  $V_{IH} = 1\text{ V}$ ,  $V_{IL} = 0\text{ V}$

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 93. Driver Eye Diagram, 800 Mbps, PRBS31;  $V_{IH} = 1\text{ V}$ ,  $V_{IL} = 0\text{ V}$ Figure 94. Driver Eye Diagram, 800 Mbps, PRBS31;  $V_{IH} = 2\text{ V}$ ,  $V_{IL} = 0\text{ V}$ Figure 95. Driver Eye Diagram, 1600 Mbps, PRBS31;  $V_{IH} = 1\text{ V}$ ,  $V_{IL} = 0\text{ V}$ Figure 96. Driver Eye Diagram, 1600 Mbps, PRBS31;  $V_{IH} = 2\text{ V}$ ,  $V_{IL} = 0\text{ V}$ Figure 97. Driver Eye Diagram, 2000 Mbps, PRBS31;  $V_{IH} = 1\text{ V}$ ,  $V_{IL} = 0\text{ V}$ Figure 98. Driver Eye Diagram, 2000 Mbps, PRBS31;  $V_{IH} = 2\text{ V}$ ,  $V_{IL} = 0\text{ V}$

## TYPICAL PERFORMANCE CHARACTERISTICS

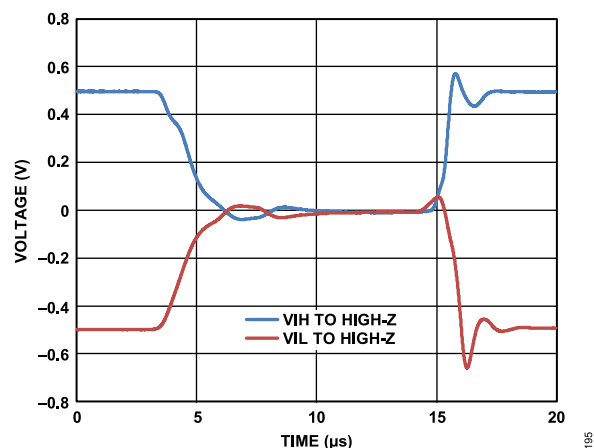


Figure 99. Drive to/from High-Z Transition,  $V_{IH} = 1\text{ V}$ ,  $V_{IL} = -1\text{ V}$ ,  $50\ \Omega$  Termination

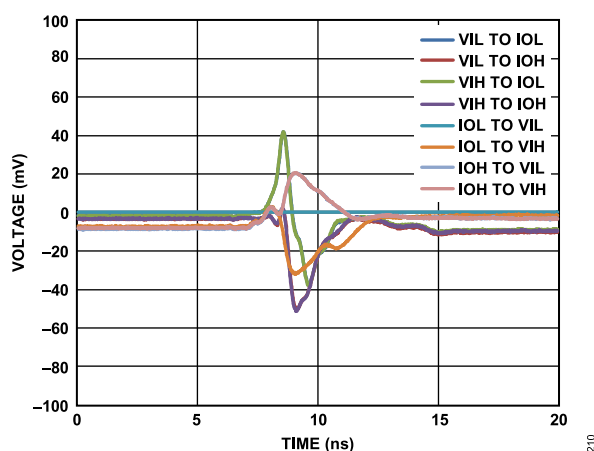


Figure 100. Drive to/from Active Load Transient,  $V_{IL} = V_{IH} = 0\text{ V}$ ,  $IOH = IOL = 0\text{ V}$

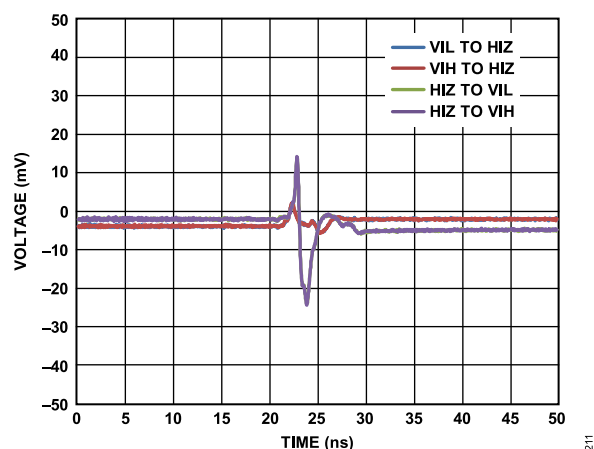


Figure 101. Drive to/from High-Z Transient,  $V_{IL} = V_{IH} = 0\text{ V}$ ,  $50\ \Omega$  Termination

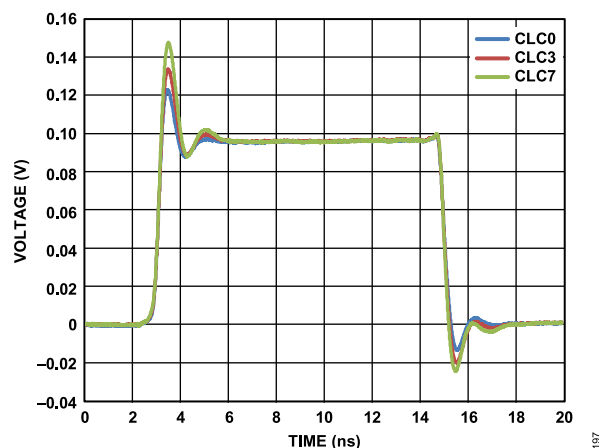


Figure 102. Driver 0.2 V Response vs. CLC Settings

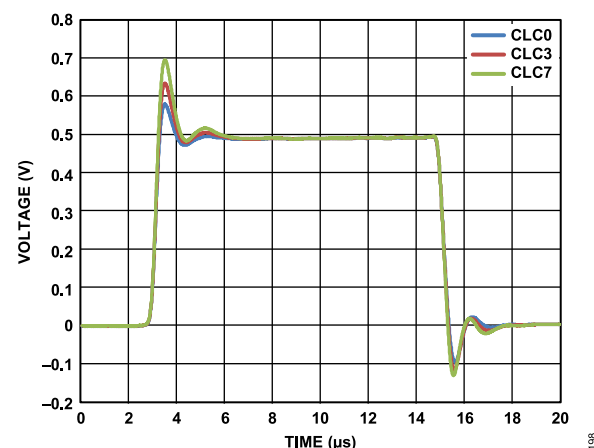


Figure 103. Driver 1 V Response vs. CLC Settings

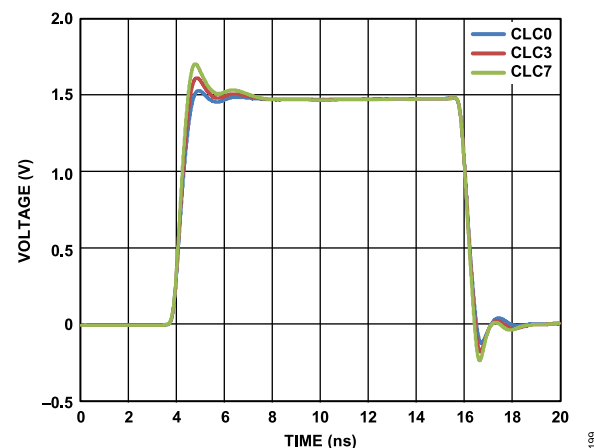


Figure 104. Driver 3 V Response vs. CLC Settings

## TYPICAL PERFORMANCE CHARACTERISTICS

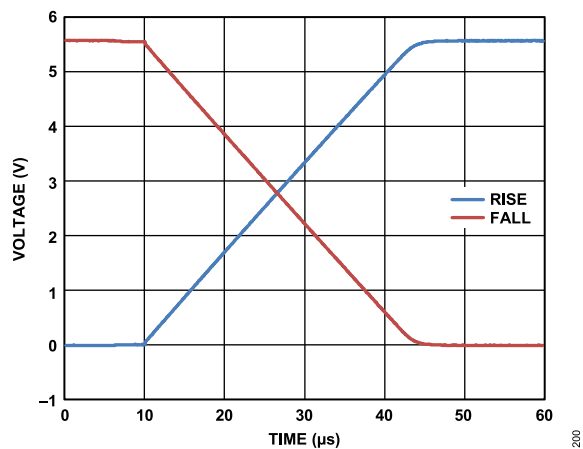


Figure 105. PPMU Transient Response, FI Range A, Full-Scale Transition, Uncalibrated,  $C_{LOAD} = 200\text{ pF}$ ,  $R_{LOAD} = 120\ \Omega$

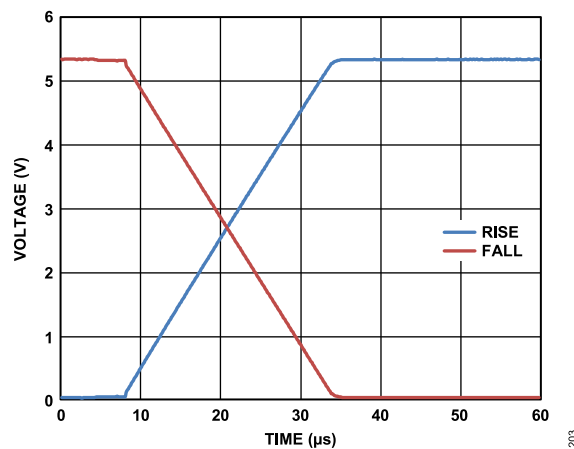


Figure 108. PPMU Transient Response, FV Range A, 0 V to 5 V, Uncalibrated,  $C_{LOAD} = 200\text{ pF}$

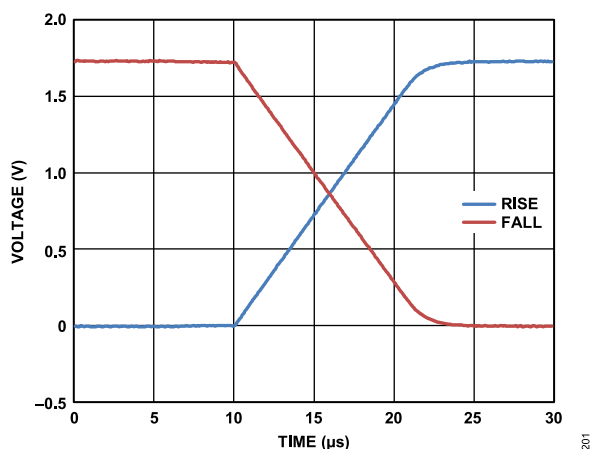


Figure 106. PPMU Transient Response, FI Range B, Full-Scale Transition, Uncalibrated,  $C_{LOAD} = 200\text{ pF}$ ,  $R_{LOAD} = 1.5\text{ k}\Omega$

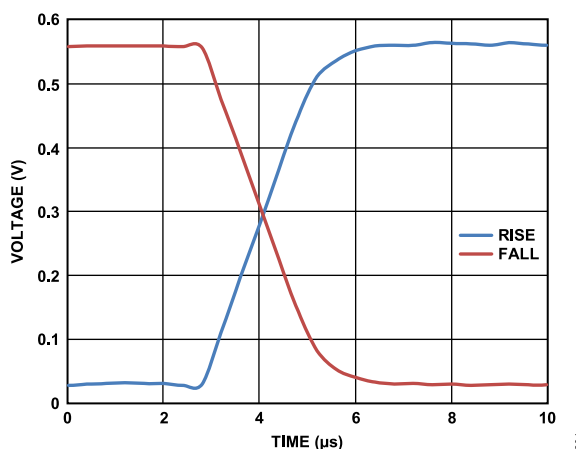


Figure 109. PPMU Transient Response, FV Range A, 0 V to 0.5 V, Uncalibrated,  $C_{LOAD} = 200\text{ pF}$

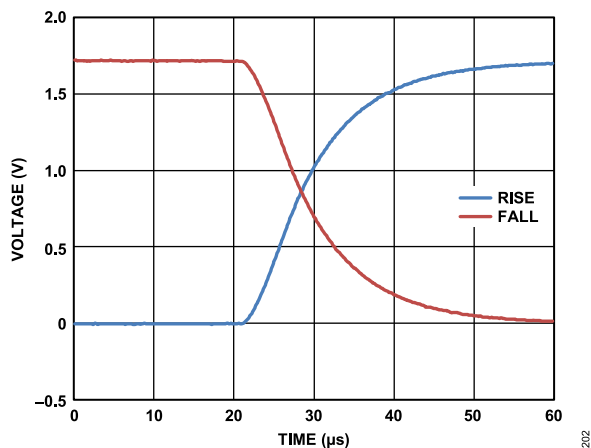


Figure 107. PPMU Transient Response, FI Range C, Full-Scale Transition, Uncalibrated,  $C_{LOAD} = 200\text{ pF}$ ,  $R_{LOAD} = 15\text{ k}\Omega$

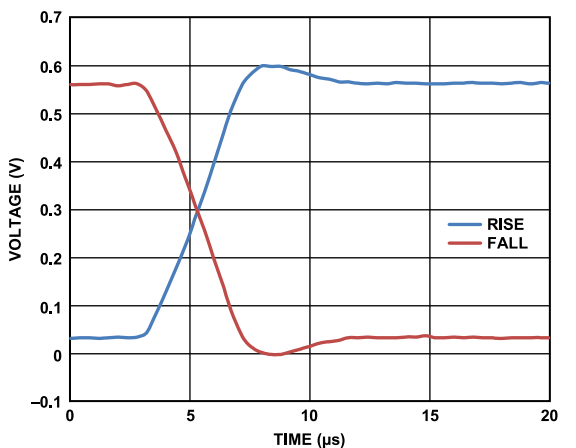


Figure 110. PPMU Transient Response, FV Range C, 0 V to 0.5 V, Uncalibrated,  $C_{LOAD} = 200\text{ pF}$

## TYPICAL PERFORMANCE CHARACTERISTICS

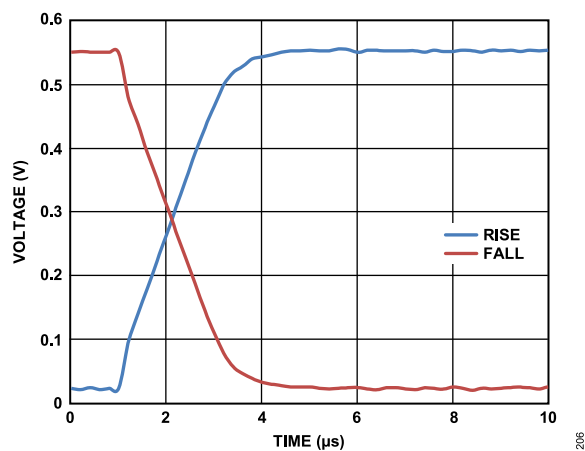


Figure 111. PPMU Transient Response, FV Range A, 0 V to 0.5 V, Uncalibrated,  $C_{LOAD} = 2000$  pF

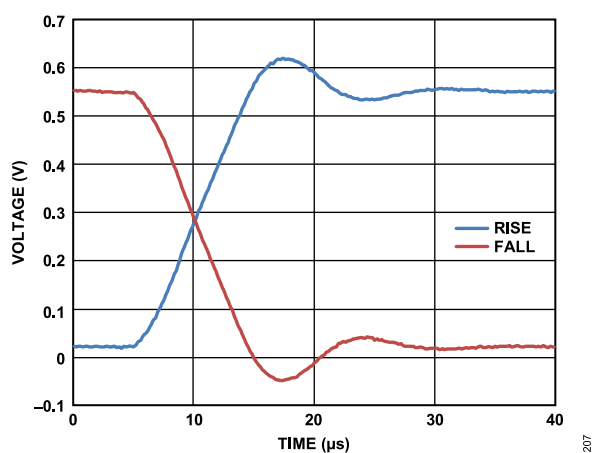


Figure 112. PPMU Transient Response, FV Range C, 0 V to 0.5 V, Uncalibrated,  $C_{LOAD} = 2000$  pF

SPI INTERCONNECT DETAILS

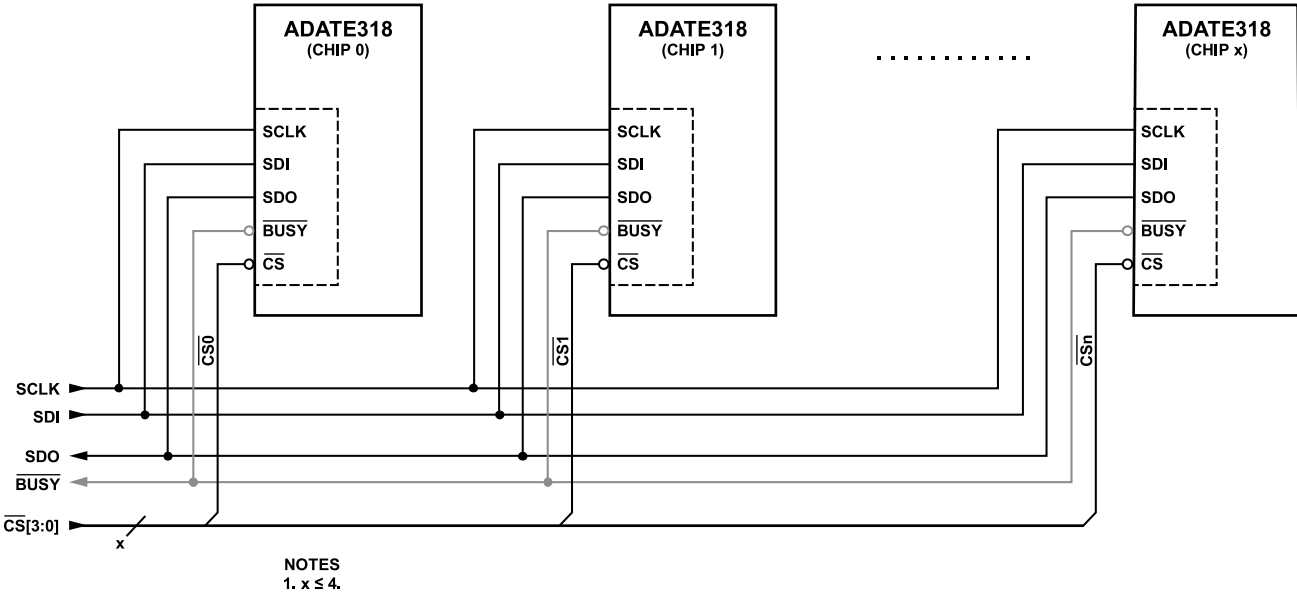


Figure 113. Multiple SPI with Shared SDO Line

003

## USE OF THE SPI $\overline{\text{BUSY}}$ PIN

After any valid SPI instruction is written to the ADATE318, the  $\overline{\text{BUSY}}$  pin becomes asserted to indicate a busy status of the DAC update and calibration engines. The  $\overline{\text{BUSY}}$  pin is an open drain type output capable of sinking a minimum of 5 mA from the VCC supply. Because it is an open drain type output, it can be wire-or'ed in common with many other similar open drain devices. In such cases, it is the user's responsibility either to determine which device is indicating the busy state or, alternatively, to wait until all devices on the shared line become not busy. It is recommended that the  $\overline{\text{BUSY}}$  pin be tied to VCC with an external 1 k $\Omega$  pull-up.

It is not a requirement to wait for release of  $\overline{\text{BUSY}}$  prior to a subsequent assertion of the  $\overline{\text{CS}}$  pin. This is not the purpose of the  $\overline{\text{BUSY}}$  pin. As long as the minimum number of SCLK cycles following the previous release of  $\overline{\text{CS}}$  is met according to the  $t_{\text{CSAM}}$  parameter, the  $\overline{\text{CS}}$  pin can be asserted again for a subsequent SPI operation. With the one exception of recovery from a reset request (either by hardware assertion of the  $\overline{\text{RST}}$  pin or a software setting of the internal SPI\_RESET control bit), there is no scenario in normal operation of the ADATE318 in which the user must wait for release of  $\overline{\text{BUSY}}$  prior to asserting the  $\overline{\text{CS}}$  for another SPI operation. The only requirement on the assertion of  $\overline{\text{CS}}$  is that the  $t_{\text{CSAM}}$  parameter be defined as in [Figure 4](#) and [Table 13](#).

It is very important, however, that the SCLK continue to operate for as long as the  $\overline{\text{BUSY}}$  pin state remains active. This minimum period of time is defined by the  $t_{\text{BUSW}}$  parameter (see [Figure 4](#), [Figure 6](#), [Figure 7](#), and [Table 18](#)). If the SCLK does not remain active for at least the time specified by the  $t_{\text{BUSW}}$  parameter, operations pending to the internal processor may not fully complete or, worse, they may complete in an incorrect fashion. In either case, a temporary malfunction of the ADATE318 may occur.

After the ADATE318 releases the  $\overline{\text{BUSY}}$  pin, the SCLK may again be stopped to prevent unwanted digital noise from coupling into the analog levels during normal operation of the pin electronics functions. In every case (with no exception for reset recovery), it is

the purpose of the  $\overline{\text{BUSY}}$  pin to notify the external test processor that it is again safe to stop the SCLK signal to the ADATE318. Running the SCLK for extra periods when  $\overline{\text{BUSY}}$  is not active is never a problem except for the possibility of adding unwanted digital switching noise to the analog pin electronics circuitry as already noted.

While the length of the  $\overline{\text{BUSY}}$  period ( $t_{\text{BUSW}}$ ) is variable depending on the particular preceding SPI instruction, it is nevertheless deterministic. The parameter  $t_{\text{BUSW}}$  depends only on factors such as whether the previous instruction involved a write to one or more DAC addresses and, if so, then how many channels were involved and whether or not the calibration function was enabled. [Table 18](#) describes the precise length of the  $t_{\text{BUSW}}$  period in units of rising edge SCLK cycles for each possible SPI instruction scenario as well as recovery from a hard  $\overline{\text{RST}}$  reset.

Because  $t_{\text{BUSW}}$  is deterministic, it is therefore possible to predict in advance the minimum number of rising edge SCLK cycles required to complete any given SPI instruction. This makes it possible to operate the ADATE318 without a need to monitor the state of the  $\overline{\text{BUSY}}$  pin. For applications in which it is neither possible nor desirable to monitor the pin, it is acceptable to use the information in [Table 18](#) to guarantee that the minimum number of cycles is provided in lieu of monitoring  $\overline{\text{BUSY}}$  following release of  $\overline{\text{CS}}$  or reset. All DAC addresses have been assigned to the contiguous address block from 0x00 through 0x0F; therefore, it is possible to decode this information within the external test processor to provide a software indication that extra SCLK cycles may be required according to the scenarios listed in [Table 18](#). All other operations not involving these addresses require only the standard number of clock cycles determined by  $t_{\text{CSAM}}$ . As stated above, however, it is extremely important to honor the minimum number of required rising edge SCLK cycles as defined by  $t_{\text{BUSW}}$  following the release of  $\overline{\text{CS}}$  for each of the SPI instruction scenarios listed in [Table 18](#) to ensure proper operation of the ADATE318.

**Table 18.  $\overline{\text{BUSY}}$  Minimum SCLK Cycle Requirements**

| SPI Instruction Type                                                          | Calibration Engine <sup>1</sup> | Maximum $t_{\text{BUSW}}$ (SCLK Cycles) |
|-------------------------------------------------------------------------------|---------------------------------|-----------------------------------------|
| Following the Release of the Asynchronous Reset Pin (Hardware Reset)          | X                               | 64                                      |
| Following Assertion of the SPI_RESET Control Bit (Software Reset)             | X                               | 64                                      |
| No Operation (NOP) Instruction                                                | X                               | 3                                       |
| Read Request to Any Valid ADATE318 Address and/or Channel (0x00 – 0x7F)       | X                               | 3                                       |
| Single/Double Channel Write Request to Any Valid ADATE318 Address $\geq$ 0x10 | X                               | 3                                       |
| Single Channel Write Request to Any DAC (ADDR 0x01 – ADDR 0x0E)               | Disabled                        | 10                                      |
| Double Channel Write Request to Any DAC (ADDR 0x01 – ADDR 0x0E)               | Disabled                        | 16                                      |
| Single Channel Write Request to Any DAC (ADDR 0x01 – ADDR 0x0E)               | Enabled                         | 20                                      |
| Double Channel Write Request to Any DAC (ADDR 0x01 – ADDR 0x0E)               | Enabled                         | 26                                      |

<sup>1</sup> X = don't care.

## RESET SEQUENCE AND THE $\overline{\text{RST}}$ PIN

The internal state of the ADATE318 is indeterminate following power-up. For this reason, it is necessary to perform a complete reset sequence once the power supplies have stabilized. Further, the  $\overline{\text{RST}}$  pin must be held in the asserted state before and during the power-up sequence and released only after all power supplies are known to be stable.

The ADATE318 has an active low pin ( $\overline{\text{RST}}$ ) that asynchronously starts a reset sequence. A soft reset sequence can also be initiated under SPI software control by writing to the SPI\_RESET bit in the SPI Control Register (SPI 0x12[0] (see Figure 13)). In the case of a soft reset, the sequence begins on the first rising edge of SCLK following the release of  $\overline{\text{CS}}$ , subject to the normal setup and hold times. Certain actions take place immediately upon initiation of the reset request, whereas other actions require SCLK.

The following asynchronous actions take place as soon as a reset request is detected, whether or not SCLK is active:

- ▶ Assert  $\overline{\text{BUSY}}$  pin
- ▶ Force all control registers to the default reset state as defined by control register definitions
- ▶ Clear all calibration registers to the default reset state as defined by calibration register definitions
- ▶ Override all DAC output voltages and force analog levels to  $V_{\text{DUTGND}}$
- ▶ Disable DCLs and PPMUs; open system PMU switches

- ▶ Soft connect the DUT0 and DUT1 pins to  $V_{\text{DUTGND}}$  (see Figure 114)

The part remains in this static reset state indefinitely until the clocked portion of the sequence begins with either the first rising edge of SCLK following the release of  $\overline{\text{RST}}$  (asynchronous reset) or the second rising edge of SCLK following the release of  $\overline{\text{CS}}$  (soft reset). No matter how the reset sequence is initiated, the clocked portion of the reset sequence requires 64 SCLK cycles to run to completion, and the  $\overline{\text{BUSY}}$  pin remains asserted until these clock cycles have been received. The following actions take place during the clocked portion of the reset sequence:

- ▶ Complete internal SPI controller initialization
- ▶ Write the appropriate values to specific DAC  $X_2$  registers (see Table 19)
- ▶ Enable the thermal alarm with a 100C threshold; disable PPMU and the overvoltage detect (OVD) alarms

The 64<sup>th</sup> rising edge of SCLK releases  $\overline{\text{BUSY}}$  and starts a self-timed DAC deglitch period of approximately 3  $\mu\text{s}$ . DAC voltages begin to change once the deglitch circuits have timed out, and they then require an additional 10  $\mu\text{s}$  to settle to their final values. Thus, a full reset sequence requires approximately 15  $\mu\text{s}$ , comprising 1.28  $\mu\text{s}$  (64 cycles  $\times$  20 ns) for the reset state machine, 3  $\mu\text{s}$  for DAC deglitch, and another 10  $\mu\text{s}$  for settling.

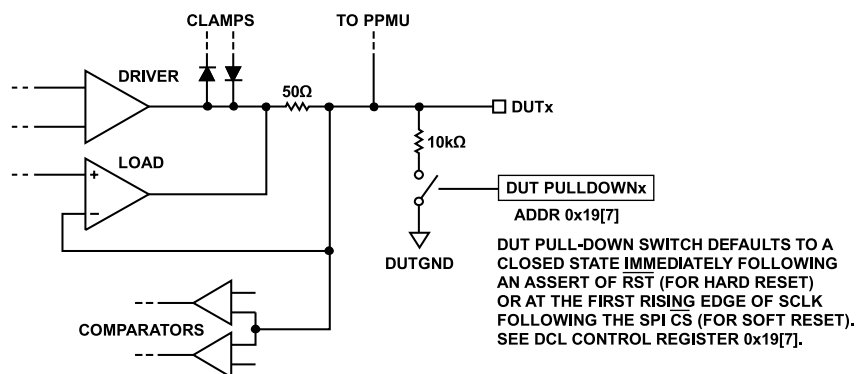


Figure 114. DUTx to  $V_{\text{DUTGND}}$  Soft Connect Detail

## SPI REGISTER DEFINITIONS AND MEMORY MAP

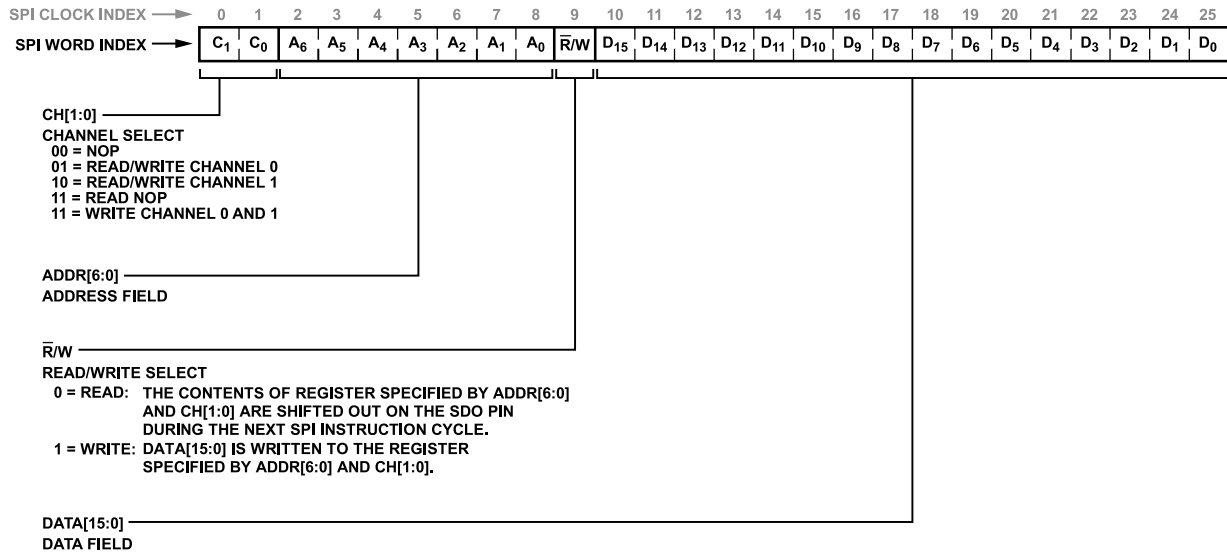


Figure 115. SPI Word Definition

Table 19. SPI Register Memory Map

| CH[1:0] <sup>1,2</sup> | ADDR[6:0]    | R/W <sup>1</sup> | DATA[15:0] <sup>1,3</sup> | Register Description                      | Reset Value <sup>1</sup> |
|------------------------|--------------|------------------|---------------------------|-------------------------------------------|--------------------------|
| XX                     | 0x00         | X                | XXXX                      | No operation (NOP)                        | XXXX                     |
| CC                     | 0x01         | R/W              | DDDD                      | VIH DAC level (reset value = 0.0 V)       | 0x4000                   |
| CC                     | 0x02         | R/W              | DDDD                      | VIT/VCOM DAC level (reset value = 0.0 V)  | 0x4000                   |
| CC                     | 0x03         | R/W              | DDDD                      | VIL DAC level (reset value = 0.0 V)       | 0x4000                   |
| CC                     | 0x04         | R/W              | DDDD                      | VOH DAC level (reset value = +0.5 V)      | 0x4CCC                   |
| CC                     | 0x05         | R/W              | DDDD                      | VOL DAC level (reset value = -0.5 V)      | 0x3333                   |
| CC                     | 0x06         | R/W              | DDDD                      | VCH DAC level (reset value = +7.5 V)      | 0xFFFF                   |
| CC                     | 0x07         | R/W              | DDDD                      | VCL DAC level (reset value = -2.5 V)      | 0x0000                   |
| CC                     | 0x08         | R/W              | DDDD                      | VIOH DAC level (reset value = 50 $\mu$ A) | 0x4040                   |
| CC                     | 0x09         | R/W              | DDDD                      | VIOL DAC level (reset value = 50 $\mu$ A) | 0x4040                   |
| CC                     | 0x0A         | R/W              | DDDD                      | PPMU DAC level (reset value = 0.0 V)      | 0x4000                   |
| 01                     | 0x0B         | R/W              | DDDD                      | VHH DAC level (reset value = 0.0 V)       | 0x2666                   |
| 01                     | 0x0C         | R/W              | DDDD                      | OVDH DAC level (reset value = +7.5 V)     | 0xFFFF                   |
| 01                     | 0x0D         | R/W              | DDDD                      | OVDL DAC level (reset value = -2.5 V)     | 0x0000                   |
| 01                     | 0x0E         | R/W              | DDDD                      | Spare DAC level (reset value = 0.0 V)     | 0x4000                   |
| XX                     | 0x0F         | X                | XXXX                      | Reserved                                  | XXXX                     |
| XX                     | 0x10         | X                | XXXX                      | No operation (NOP)                        | XXXX                     |
| CC                     | 0x11         | R/W              | DDDD                      | DAC control register                      | 0x0000                   |
| 01                     | 0x12         | R/W              | DDDD                      | SPI control register                      | 0x0000                   |
| XX                     | 0x13 to 0x17 | X                | XXXX                      | Reserved                                  | XXXX                     |
| 01                     | 0x18         | R/W              | DDDD                      | VHH control register                      | 0x0000                   |
| CC                     | 0x19         | R/W              | DDDD                      | DCL control register                      | 0x0080                   |
| CC                     | 0x1A         | R/W              | DDDD                      | PPMU control register                     | 0x0000                   |
| CC                     | 0x1B         | R/W              | DDDD                      | PPMU MEAS control register                | 0x0000                   |
| CC                     | 0x1C         | R/W              | DDDD                      | CMP control register                      | 0x07FE                   |
| CC                     | 0x1D         | R/W              | DDDD                      | ALARM mask register                       | 0x0045                   |
| CC                     | 0x1E         | R                | DDDD                      | ALARM state register                      | 0x0000                   |

## SPI REGISTER DEFINITIONS AND MEMORY MAP

Table 19. SPI Register Memory Map

| CH[1:0] <sup>1, 2</sup> | ADDR[6:0] | R/W <sup>1</sup> | DATA[15:0] <sup>1, 3</sup> | Register Description                              | Reset Value <sup>1</sup> |
|-------------------------|-----------|------------------|----------------------------|---------------------------------------------------|--------------------------|
| CC                      | 0x1F      | R/W              | DDDD                       | CLC control register                              | 0x0000                   |
| XX                      | 0x20      | X                | XXXX                       | No operation (NOP)                                | XXXX                     |
| CC                      | 0x21      | R/W              | DDDD                       | VIH (driver) m-coefficient                        | 0xFFFF                   |
| CC                      | 0x22      | R/W              | DDDD                       | VIT (driver) m-coefficient                        | 0xFFFF                   |
| CC                      | 0x23      | R/W              | DDDD                       | VIL (driver) m-coefficient                        | 0xFFFF                   |
| CC                      | 0x24      | R/W              | DDDD                       | VOH (normal window comparator) m-coefficient      | 0xFFFF                   |
| CC                      | 0x25      | R/W              | DDDD                       | VOL (normal window comparator) m-coefficient      | 0xFFFF                   |
| CC                      | 0x26      | R/W              | DDDD                       | VCH (reflection clamp) m-coefficient              | 0xFFFF                   |
| CC                      | 0x27      | R/W              | DDDD                       | VCL (reflection clamp) m-coefficient              | 0xFFFF                   |
| CC                      | 0x28      | R/W              | DDDD                       | VIOH (active load) m-coefficient                  | 0xFFFF                   |
| CC                      | 0x29      | R/W              | DDDD                       | VIOL (active load) m-coefficient                  | 0xFFFF                   |
| CC                      | 0x2A      | R/W              | DDDD                       | PPMU (PPMU force-voltage) m-coefficient           | 0xFFFF                   |
| 01                      | 0x2B      | R/W              | DDDD                       | VHH (HVOUT) m-coefficient                         | 0xFFFF                   |
| 01                      | 0x2C      | R/W              | DDDD                       | OVDH (overvoltage) m-coefficient                  | 0xFFFF                   |
| 01                      | 0x2D      | R/W              | DDDD                       | OVDL (overvoltage) m-coefficient                  | 0xFFFF                   |
| 01                      | 0x2E      | R/W              | DDDD                       | Spare DAC m-coefficient                           | 0xFFFF                   |
| XX                      | 0x2F      | X                | XXXX                       | Reserved                                          | XXXX                     |
| XX                      | 0x30      | X                | XXXX                       | No operation (NOP)                                | XXXX                     |
| CC                      | 0x31      | R/W              | DDDD                       | VIH (driver) c-coefficient                        | 0x8000                   |
| CC                      | 0x32      | R/W              | DDDD                       | VIT (driver) c-coefficient                        | 0x8000                   |
| CC                      | 0x33      | R/W              | DDDD                       | VIL (driver) c-coefficient                        | 0x8000                   |
| CC                      | 0x34      | R/W              | DDDD                       | VOH (normal window comparator) c-coefficient      | 0x8000                   |
| CC                      | 0x35      | R/W              | DDDD                       | VOL (normal window comparator) c-coefficient      | 0x8000                   |
| CC                      | 0x36      | R/W              | DDDD                       | VCH (reflection clamp) c-coefficient              | 0x8000                   |
| CC                      | 0x37      | R/W              | DDDD                       | VCL (reflection clamp) c-coefficient              | 0x8000                   |
| CC                      | 0x38      | R/W              | DDDD                       | VIOH (active load) c-coefficient                  | 0x8000                   |
| CC                      | 0x39      | R/W              | DDDD                       | VIOL (active load) c-coefficient                  | 0x8000                   |
| CC                      | 0x3A      | R/W              | DDDD                       | PPMU (PPMU force voltage) c-coefficient           | 0x8000                   |
| 01                      | 0x3B      | R/W              | DDDD                       | VHH (HVOUT) c-coefficient                         | 0x8000                   |
| 01                      | 0x3C      | R/W              | DDDD                       | OVDH (overvoltage) c-coefficient                  | 0x8000                   |
| 01                      | 0x3D      | R/W              | DDDD                       | OVDL (overvoltage) c-coefficient                  | 0x8000                   |
| 01                      | 0x3E      | R/W              | DDDD                       | Spare DAC c-coefficient                           | 0x8000                   |
| XX                      | 0x3F      | X                | XXXX                       | Reserved                                          | XXXX                     |
| XX                      | 0x40      | X                | XXXX                       | No operation (NOP)                                | XXXX                     |
| 01                      | 0x41      | R/W              | DDDD                       | VIH (HVOUT) m-coefficient                         | 0xFFFF                   |
| CC                      | 0x42      | R/W              | DDDD                       | VCOM (active load) m-coefficient                  | 0xFFFF                   |
| 01                      | 0x43      | R/W              | DDDD                       | VIL (HVOUT) m-coefficient                         | 0xFFFF                   |
| 01                      | 0x44      | R/W              | DDDD                       | VOH (differential comparator) m-coefficient       | 0xFFFF                   |
| CC                      | 0x45      | R/W              | DDDD                       | VOH (PPMU measure voltage) m-coefficient          | 0xFFFF                   |
| CC                      | 0x46      | R/W              | DDDD                       | VOH (PPMU measure current, Range A) m-coefficient | 0xFFFF                   |
| CC                      | 0x47      | R/W              | DDDD                       | VOH (PPMU measure current Range B) m-coefficient  | 0xFFFF                   |
| CC                      | 0x48      | R/W              | DDDD                       | VOH (PPMU measure current, Range C) m-coefficient | 0xFFFF                   |
| CC                      | 0x49      | R/W              | DDDD                       | VOH (PPMU measure current, Range D) m-coefficient | 0xFFFF                   |
| CC                      | 0x4A      | R/W              | DDDD                       | VOH (PPMU measure current, Range E) m-coefficient | 0xFFFF                   |

## SPI REGISTER DEFINITIONS AND MEMORY MAP

Table 19. SPI Register Memory Map

| CH[1:0] <sup>1, 2</sup> | ADDR[6:0]    | R/W <sup>1</sup> | DATA[15:0] <sup>1, 3</sup> | Register Description                              | Reset Value <sup>1</sup> |
|-------------------------|--------------|------------------|----------------------------|---------------------------------------------------|--------------------------|
| 01                      | 0x4B         | R/W              | DDDD                       | VOL (differential comparator) m-coefficient       | 0xFFFF                   |
| CC                      | 0x4C         | R/W              | DDDD                       | VOL (PPMU measure voltage) m-coefficient          | 0xFFFF                   |
| CC                      | 0x4D         | R/W              | DDDD                       | VOL (PPMU measure current, Range A) m-coefficient | 0xFFFF                   |
| CC                      | 0x4E         | R/W              | DDDD                       | VOL (PPMU measure current, Range B) m-coefficient | 0xFFFF                   |
| CC                      | 0x4F         | R/W              | DDDD                       | VOL (PPMU measure current, Range C) m-coefficient | 0xFFFF                   |
| CC                      | 0x50         | R/W              | DDDD                       | VOL (PPMU measure current, Range D) m-coefficient | 0xFFFF                   |
| CC                      | 0x51         | R/W              | DDDD                       | VOL (PPMU measure current, Range E) m-coefficient | 0xFFFF                   |
| CC                      | 0x52         | R/W              | DDDD                       | VCH (PPMU) m-coefficient                          | 0xFFFF                   |
| CC                      | 0x53         | R/W              | DDDD                       | VCL (PPMU) m-coefficient                          | 0xFFFF                   |
| CC                      | 0x54         | R/W              | DDDD                       | PPMU force current, Range A m-coefficient         | 0xFFFF                   |
| CC                      | 0x55         | R/W              | DDDD                       | PPMU force current, Range B m-coefficient         | 0xFFFF                   |
| CC                      | 0x56         | R/W              | DDDD                       | PPMU force current, Range C m-coefficient         | 0xFFFF                   |
| CC                      | 0x57         | R/W              | DDDD                       | PPMU force current Range D m-coefficient          | 0xFFFF                   |
| CC                      | 0x58         | R/W              | DDDD                       | PPMU force current, Range E m-coefficient         | 0xFFFF                   |
| 01                      | 0x59         | R/W              | DDDD                       | VIH (HVOUT) c-coefficient                         | 0x8000                   |
| CC                      | 0x5A         | R/W              | DDDD                       | VCOM (active load) c-coefficient                  | 0x8000                   |
| 01                      | 0x5B         | R/W              | DDDD                       | VIL (HVOUT) c-coefficient                         | 0x8000                   |
| 01                      | 0x5C         | R/W              | DDDD                       | VOH (differential comparator) c-coefficient       | 0x8000                   |
| CC                      | 0x5D         | R/W              | DDDD                       | VOH (PPMU measure voltage) c-coefficient          | 0x8000                   |
| CC                      | 0x5E         | R/W              | DDDD                       | VOH (PPMU measure current) c-coefficient          | 0x8000                   |
| XX                      | 0x5F to 0x62 | X                | XXXX                       | Reserved                                          | XXXX                     |
| 01                      | 0x63         | R/W              | DDDD                       | VOL (differential comparator) c-coefficient       | 0x8000                   |
| CC                      | 0x64         | R/W              | DDDD                       | VOL (PPMU measure voltage) c-coefficient          | 0x8000                   |
| CC                      | 0x65         | R/W              | DDDD                       | VOL (PPMU measure current) c-coefficient          | 0x8000                   |
| XX                      | 0x66 to 0x69 | X                | XXXX                       | Reserved                                          | XXXX                     |
| CC                      | 0x6A         | R/W              | DDDD                       | VCH (PPMU) c-coefficient                          | 0x8000                   |
| CC                      | 0x6B         | R/W              | DDDD                       | VCL (PPMU) c-coefficient                          | 0x8000                   |
| CC                      | 0x6C         | R/W              | DDDD                       | PPMU force current c-coefficient                  | 0x8000                   |
| XX                      | 0x6D to 0x70 | X                | XXXX                       | Reserved                                          | XXXX                     |

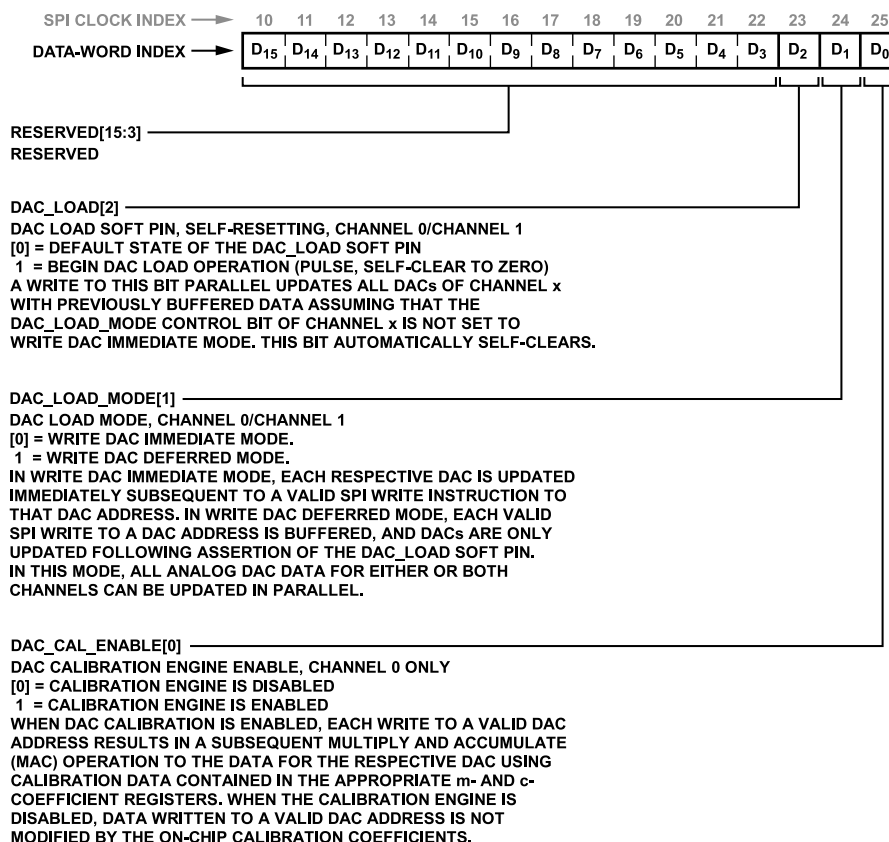
<sup>1</sup> X = don't care.<sup>2</sup> CC corresponds to the channel address bits and indicates that there is dedicated register space for each channel.<sup>3</sup> DDDD stands for data.

## CONTROL REGISTER DETAILS

Reserved bits in any register are undefined. In some cases, a physical (but unused) memory bit may be present, in other cases not. Write operations have no effect. Read operations result in meaningless but deterministic data.

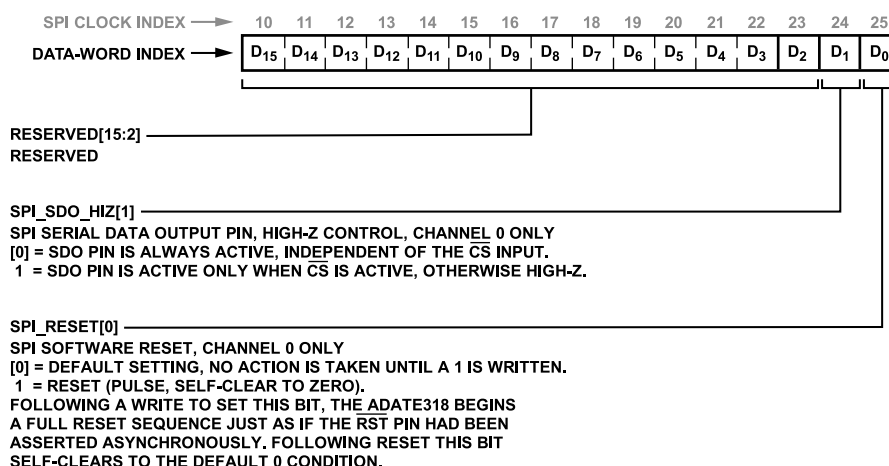
Any SPI read operation from any reserved bit or register results in an unknown but deterministic readback value.

Any SPI write operation to a control bit or control register defined only on Channel 0 must be addressed to at least Channel 0. Any such write that is addressed only to Channel 1 is ignored. Further, any such write that is addressed to both Channel 0 and Channel 1 (as a multichannel write) proceeds as if the write were addressed only to Channel 0. The data addressed to the undefined Channel 1 control bit or control register is ignored.



012

Figure 116. DAC Control Register (ADDR = 0x11)



013

Figure 117. SPI Control Register (ADDR = 0x12)

CONTROL REGISTER DETAILS

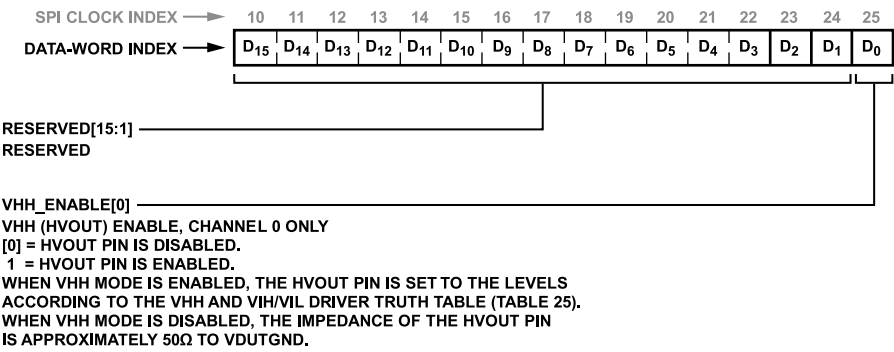


Figure 118. VHH Control Register (ADDR = 0x18) Active Truth Table

## CONTROL REGISTER DETAILS

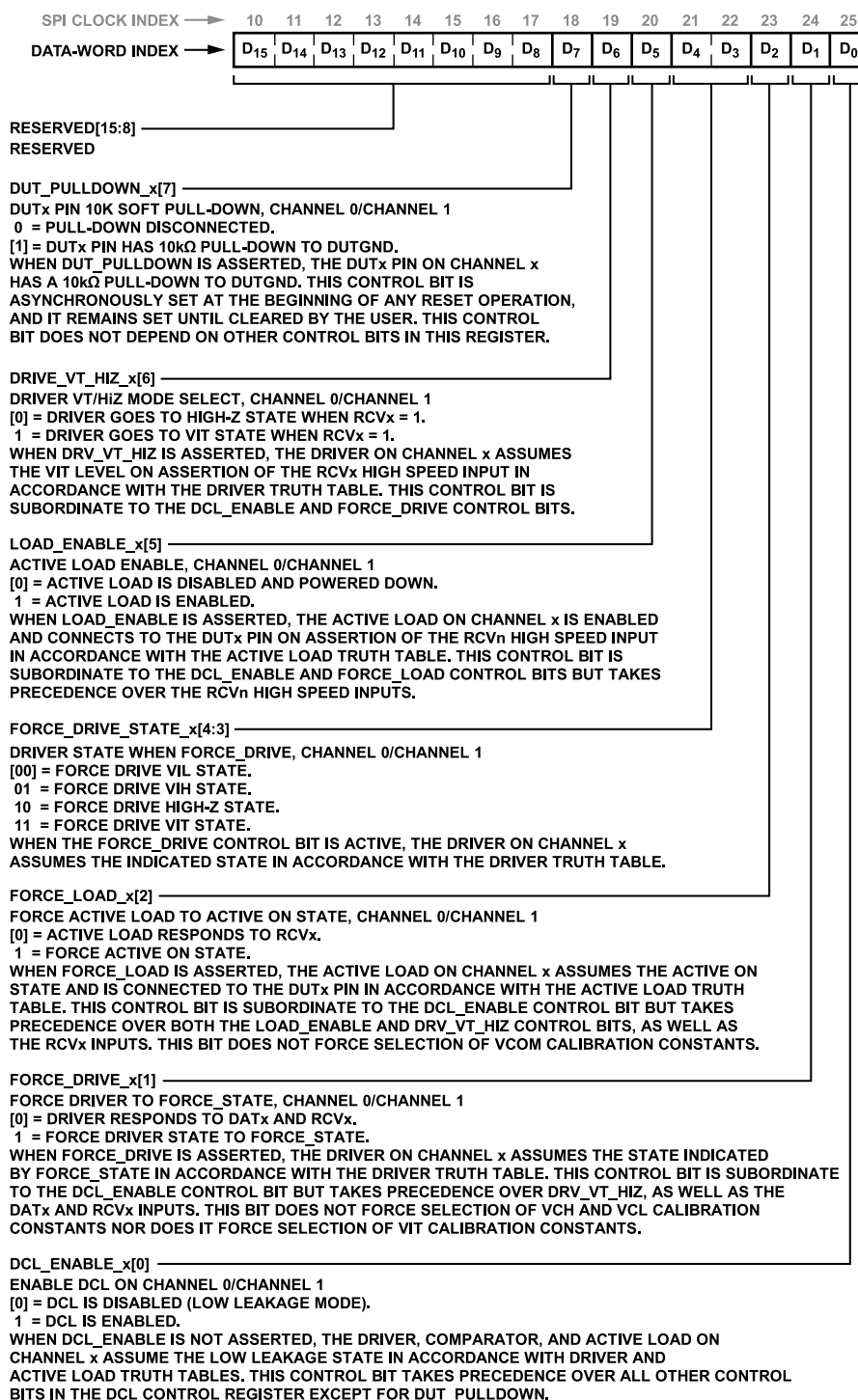


Figure 119. DCL Control Register (ADDR = 0x19)

## CONTROL REGISTER DETAILS

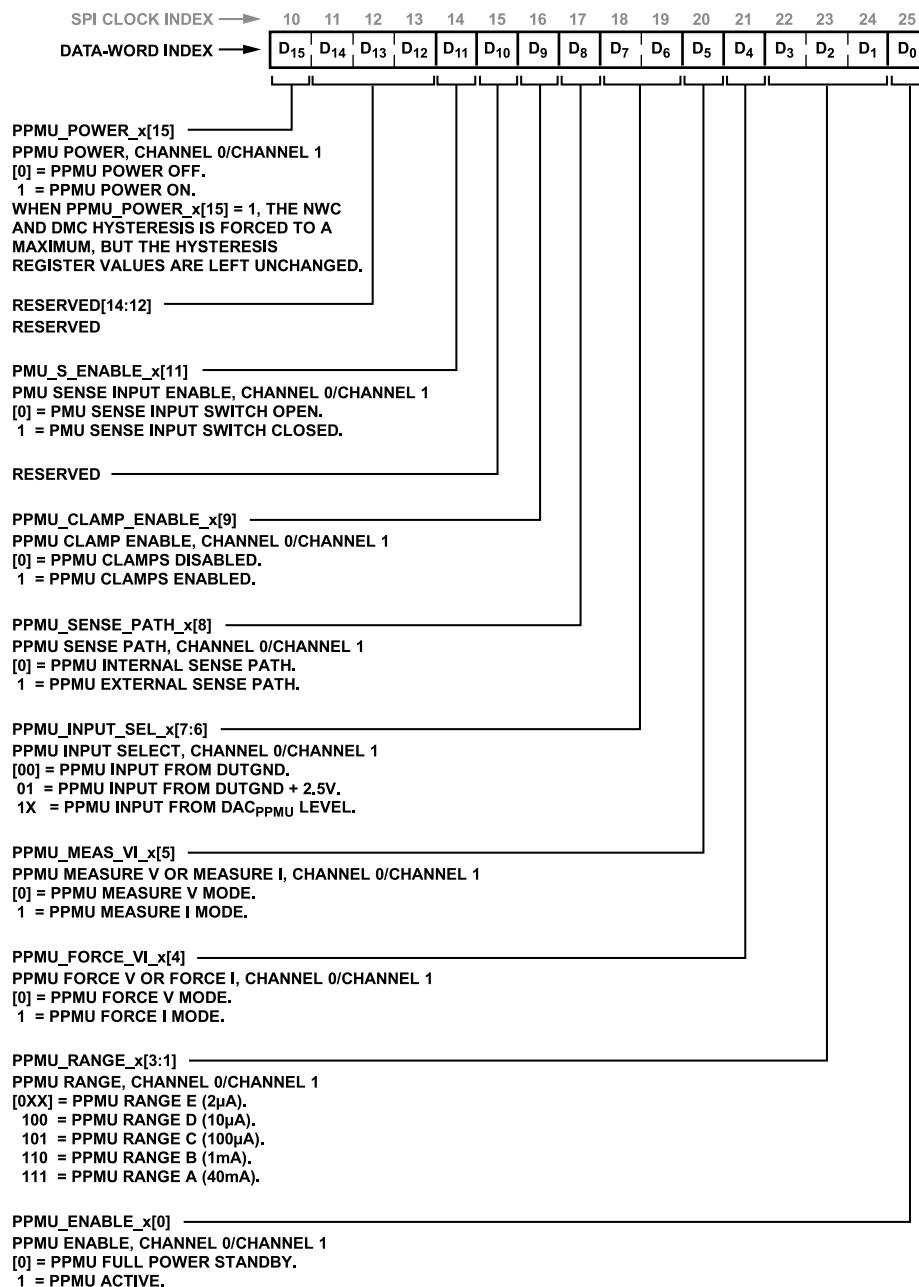
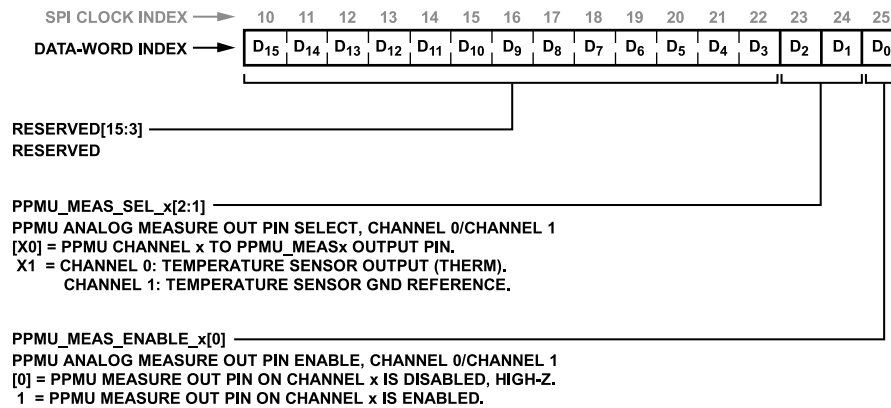


Figure 120. PPMU Control Register (ADDR = 0x1A)

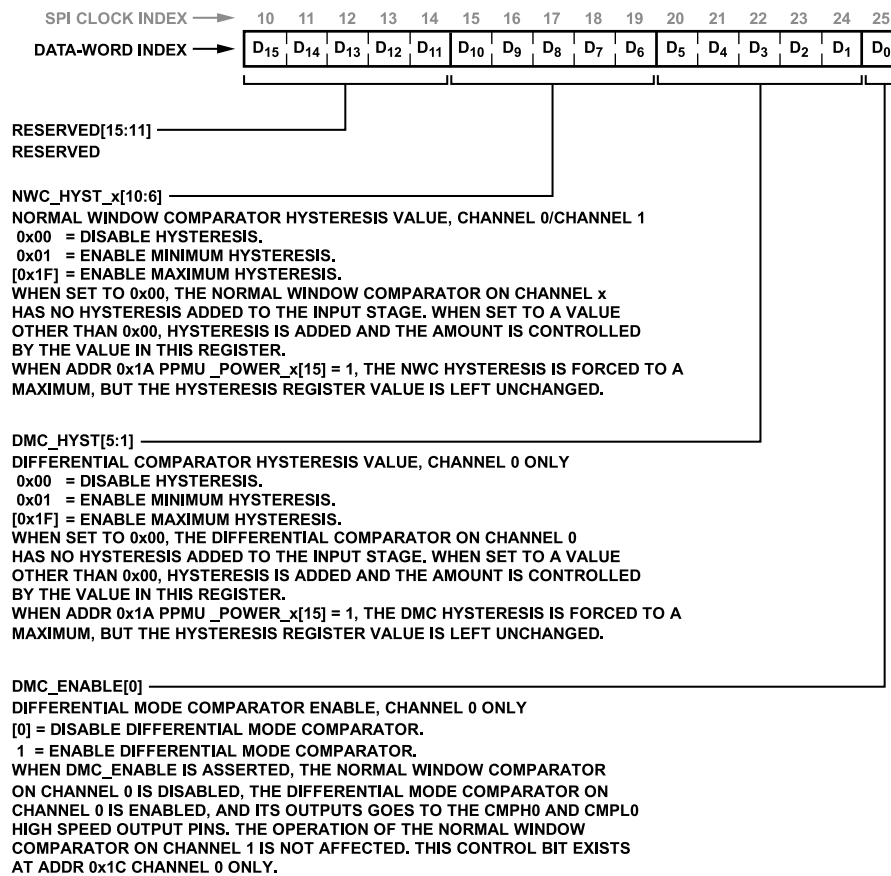
016

## CONTROL REGISTER DETAILS



017

Figure 121. PPMU MEAS Control Register (ADDR = 0x1B)



018

Figure 122. CMP Control Register (ADDR = 0x1C)

CONTROL REGISTER DETAILS

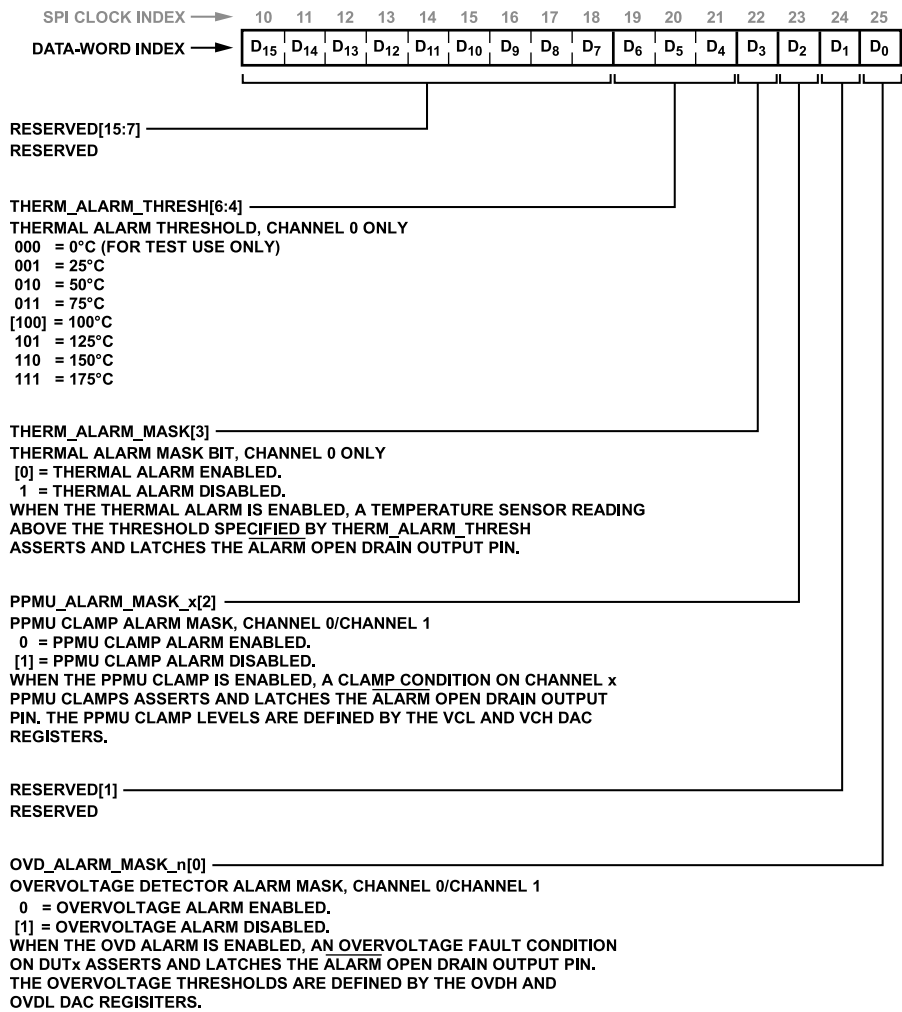


Figure 123. Alarm Mask Register (ADDR = 0x1D)

CONTROL REGISTER DETAILS

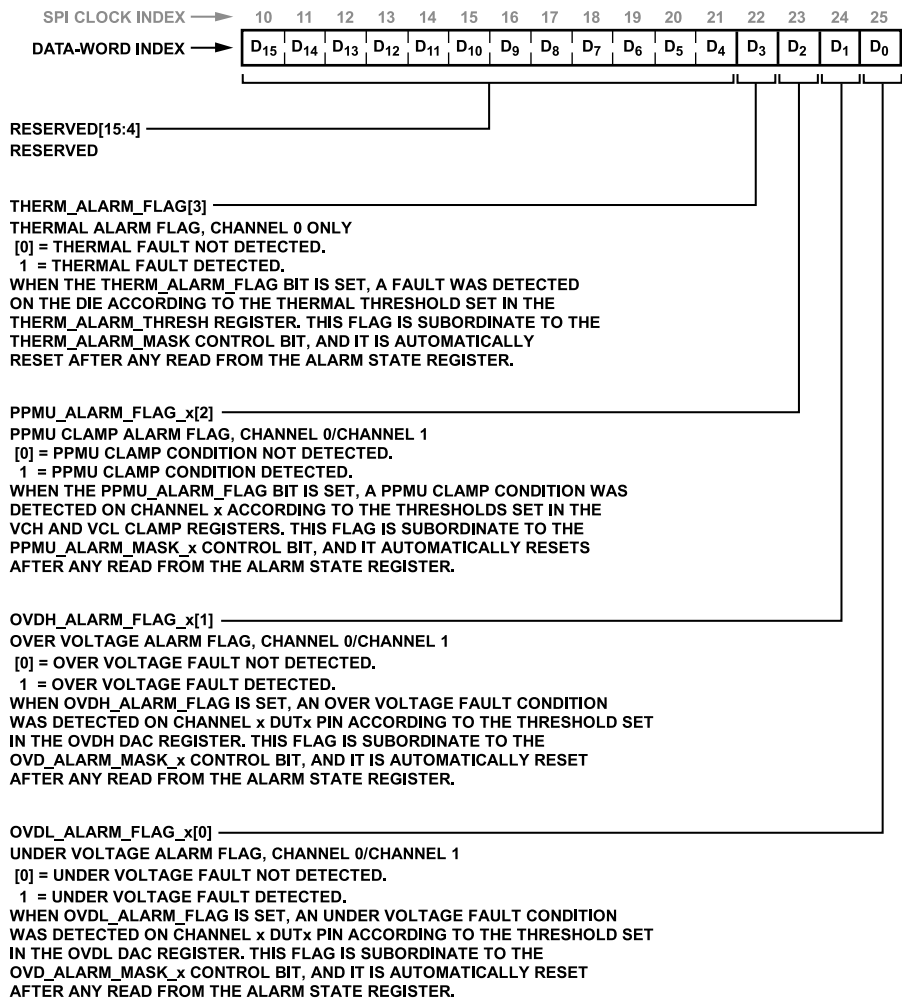
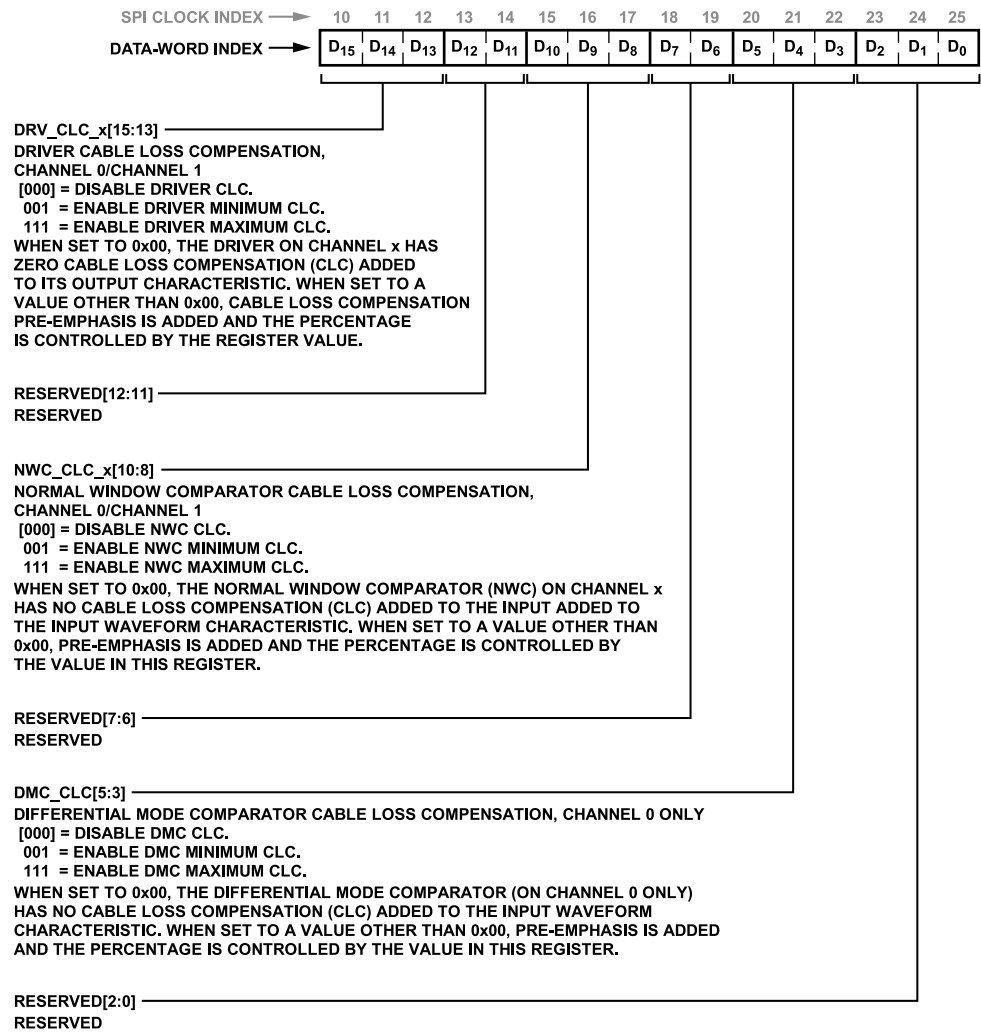


Figure 124. Alarm State Register (ADDR = 0x1E) (Read Only)

CONTROL REGISTER DETAILS



021

Figure 125. CLC Control Register (ADDR = 0x1F)

## LEVEL SETTING DACS

### DAC UPDATE MODES

The ADATE318 provides 24- × 16-bit integrated level setting DACs organized as two channel banks of 12 DACs each. The detailed mapping of the DAC register to pin electronics function is shown in [Table 19](#). Each DAC can be programmed by writing data to the respective SPI register address and channel.

The ADATE318 provides two methods for updating analog DAC levels: DAC immediate update mode and DAC deferred update mode. At release of the  $\overline{CS}$  pin associated with any valid SPI write to a DAC address, the update of analog levels may start immediately, or it can be deferred, depending on the state of the DAC\_LOAD\_MODE control bits in the DAC control register (SPI ADDR 0x11[1] (see [Figure 116](#))). Initiation of the analog level update sequence (and triggering of the on-chip deglitch circuit) actually begins four SCLK cycles following the associated release of the  $\overline{CS}$  pin. For the purpose of this discussion, it is assumed to start coincident with the release of  $\overline{CS}$ . The DAC update mode can be selected independently for each channel bank.

If the DAC\_LOAD\_MODE control bit for a given channel bank is cleared, the DACs assigned to that channel are then in the DAC immediate update mode. Writing to any DAC of that channel causes the corresponding analog level to be updated immediately following the associated release of  $\overline{CS}$ . Because all analog levels are updated on a per-channel basis, any previously pending DAC writes queued to the channel (while in deferred update mode) are also updated at this time. This situation can arise if DAC writes are queued to the channel while in deferred update mode, and the DAC\_LOAD\_MODE bit is subsequently changed to immediate update mode before the analog levels are updated by writing to the respective DAC\_LOAD soft pin. The queued data is not lost. Note that writing to the DAC\_LOAD soft pin has no effect in immediate update mode.

If the DAC\_LOAD\_MODE control bit for a given channel is set, the DACs assigned to that channel are in the deferred update mode. Writing to any DAC of that channel only queues the DAC data into that channel. The analog update of queued DAC levels is deferred until the respective DAC\_LOAD soft pin is set (SPI ADDR 0x11[2] (see [Figure 116](#))). The DAC deferred update mode, in conjunction with the respective DAC\_LOAD soft pin, provides the means to queue all DAC level writes to a given channel bank before synchronously updating the analog levels with a single SPI command.

Certain pin electronics functions, such as VHH, OVDH, OVDL, and the spare DAC, do not fit neatly within a particular channel bank. However, they must be updated as a part of the channel bank to which they are assigned as shown in [Table 19](#).

The ADATE318 provides a feature in which a single SPI write operation can address two channels at one time (see [Figure 115](#)). This

feature makes possible a scenario in which a SPI write operation can address corresponding DACs on both channels at the same time even though the channels may be configured with different DAC update modes. In such a case, the part behaves as expected. For example, if both channels are in immediate update mode, the update of analog levels of both channel banks begins after the associated release of the  $\overline{CS}$  pin. If both channels are in deferred update mode, the update of analog levels is deferred for both channels until the corresponding DAC\_LOAD bits are set. If one channel is in deferred update mode and the other channel is in immediate update mode, the former channel defers analog updates until the corresponding DAC\_LOAD bit is written, and the latter channel begins analog updates immediately after the associated release of the  $\overline{CS}$  pin.

An on-chip deglitch circuit with a period of approximately 3  $\mu$ s is provided to prevent DAC-to-DAC crosstalk whenever an analog update is processed. Only one deglitch circuit is provided per chip, and it must operate over all physical DACs (both channels) at the same time. The deglitch circuit can be retriggered when an analog levels update is initiated before a previous update operation has completed. In the case of a dual-channel immediate mode DAC write using a single SPI command, the deglitch circuit is triggered once after data is loaded into both DAC channels. Analog transitions at the DAC outputs do not begin until the deglitch circuit has timed out, and final settling to full precision requires an additional 7  $\mu$ s beyond the end of the 3  $\mu$ s deglitch interval. Total settling time following release of the associated  $\overline{CS}$  is approximately 10  $\mu$ s. Note that prolonged and consecutive retriggering of the deglitch circuit by one channel may cause the apparent settling time of analog levels on the other channel to be much longer than the specified 10  $\mu$ s.

A typical DAC update sequence is illustrated in [Figure 126](#) in which two immediate mode DAC update commands are written in direct succession. This example illustrates what happens when a DAC update command is written subsequent to a previous update command that has not yet finished its deglitch and settling sequence.

### Recommended Sequence for OVDH DAC Level Addressing

For correct OVDH addressing, first write data to the OVDH DAC level at SPI 0x0C at CH0. If in DAC immediate mode, the OVDH data write must be followed by either a DAC\_LOAD command to SPI 0x11[2] at CH1 or a subsequent write to any other CH1 DAC data address before the OVDH value will be updated. If in DAC deferred mode, the OVDH DAC level write must be followed by a DAC\_LOAD command to SPI 0x11[2] at CH1 (not CH0) before the analog OVDH value will be updated.

## LEVEL SETTING DACS

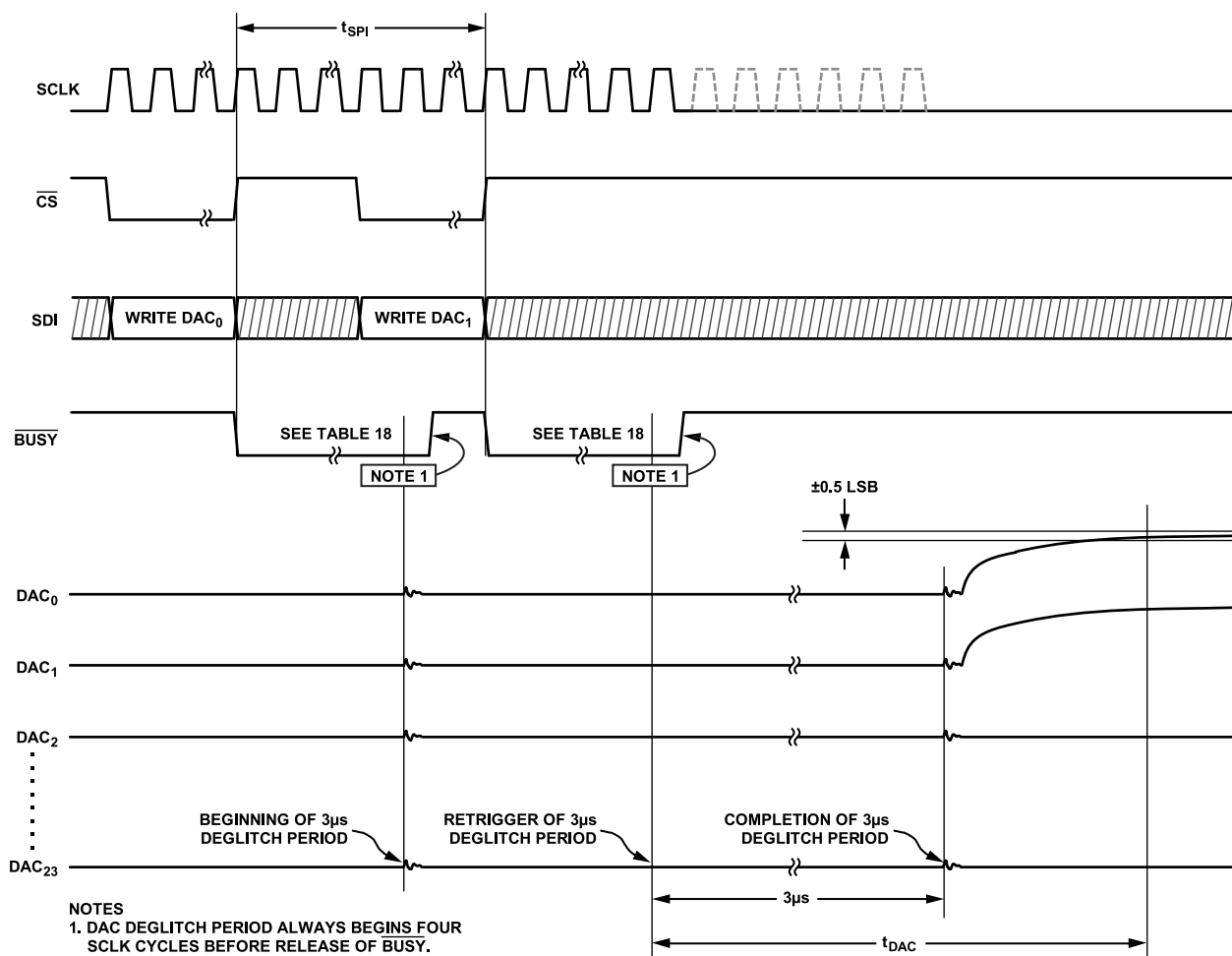


Figure 126. SPI DAC Write and Settling Time

## Addressing M and C Registers

Some DACs have pairs of m/c-coefficients that are controlled depending on other register status. Table 20 details the specific register settings and register addresses for the different pairs (X = don't care).

Table 20. M- and C-Register Mapping

| SPI Address (Channel) | DAC Name | Functional (DAC Usage) Description             | m-register | c-register | VHH_ENABLE 0x18[0] | DMC_ENABLE 0x1C[0] | LOAD_ENABLEx 0x19[5] | PPMU_POWERx 0x1A[15] | PPMU_MEAS_Vlx 0x1A[5] | PPMU_FORCE_Vlx 0x1A[4] | PPMU_RANGEx (0x1A[3:1]) |
|-----------------------|----------|------------------------------------------------|------------|------------|--------------------|--------------------|----------------------|----------------------|-----------------------|------------------------|-------------------------|
| 0x0D[0]               | OVDL     | Overvoltage detect low                         | 0x2D[0]    | 0x3D[0]    | X                  | X                  | X                    | X                    | X                     | X                      | XXX                     |
| 0x04[0]               | VOH0     | NWC high level, Channel 0                      | 0x24[0]    | 0x34[0]    | X                  | 0                  | X                    | 0                    | X                     | X                      | XXX                     |
|                       |          | DMC high level                                 | 0x44[0]    | 0x5C[0]    | X                  | 1                  | X                    | 0                    | X                     | X                      | XXX                     |
|                       |          | PPMU go/no-go MV high level, Channel 0         | 0x45[0]    | 0x5D[0]    | X                  | X                  | X                    | 1                    | 0                     | X                      | XXX                     |
|                       |          | PPMU go/no-go MI Range A high level, Channel 0 | 0x46[0]    | 0x5E[0]    | X                  | X                  | X                    | 1                    | 1                     | X                      | 111                     |

## LEVEL SETTING DACS

Table 20. M- and C-Register Mapping

| SPI<br>Address<br>(Channel) | DAC<br>Name    | Functional (DAC<br>Usage) Description                | m-register | c-register | VHH_<br>ENABLE<br>0x18[0] | DMC_<br>ENABLE<br>0x1C[0] | LOAD_<br>ENABLEx<br>0x19[5] | PPMU_<br>POWERx<br>0x1A[15] | PPMU_<br>MEAS_<br>Vix<br>0x1A[5] | PPMU_FORCE<br>_Vix 0x1A[4] | PPMU_<br>RANGEx<br>(0x1A[3:1]) |
|-----------------------------|----------------|------------------------------------------------------|------------|------------|---------------------------|---------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------|--------------------------------|
|                             |                | PPMU go/no-go MI<br>Range B high level,<br>Channel 0 | 0x47[0]    | 0x5E[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 110                            |
|                             |                | PPMU go/no-go MI<br>Range C high level,<br>Channel 0 | 0x48[0]    | 0x5E[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 101                            |
|                             |                | PPMU go/no-go MI<br>Range D high level,<br>Channel 0 | 0x49[0]    | 0x5E[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 100                            |
|                             |                | PPMU go/no-go MI<br>Range E high level,<br>Channel 0 | 0x4A[0]    | 0x5E[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 0XX                            |
| 0x05[0]                     | VOL0           | NWC low level, Channel<br>0                          | 0x25[0]    | 0x35[0]    | X                         | 0                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |                | DMC low level                                        | 0x4B[0]    | 0x63[0]    | X                         | 1                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |                | PPMU go/no-go MV low<br>level, Channel 0             | 0x4C[0]    | 0x64[0]    | X                         | X                         | X                           | 1                           | 0                                | X                          | XXX                            |
|                             |                | PPMU go/no-go MI<br>Range A low level,<br>Channel 0  | 0x4D[0]    | 0x65[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 111                            |
|                             |                | PPMU go/no-go MI<br>Range B low level,<br>Channel 0  | 0x4E[0]    | 0x65[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 110                            |
|                             |                | PPMU go/no-go MI<br>Range C low level,<br>Channel 0  | 0x4F[0]    | 0x65[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 101                            |
|                             |                | PPMU go/no-go MI<br>Range D low level,<br>Channel 0  | 0x50[0]    | 0x65[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 100                            |
|                             |                | PPMU go/no-go MI<br>Range E low level,<br>Channel 0  | 0x51[0]    | 0x65[0]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 0XX                            |
| 0x08[0]                     | VIOH0          | Load IOH level,<br>Channel 0                         | 0x28[0]    | 0x38[0]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x09[0]                     | VIOL0          | Load IOL level, Channel<br>0                         | 0x29[0]    | 0x39[0]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x02[0]                     | VITO/<br>VCOM0 | Drive term level, Chan-<br>nel 0                     | 0x22[0]    | 0x32[0]    | X                         | X                         | 0                           | X                           | X                                | X                          | XXX                            |
|                             |                | Load commutation volt-<br>age, Channel 0             | 0x42[0]    | 0x5A[0]    | X                         | X                         | 1                           | X                           | X                                | X                          | XXX                            |
| 0x01[0]                     | VIH0           | Drive high level, Chan-<br>nel 0                     | 0x21[0]    | 0x31[0]    | 0                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
|                             |                | HVOUT drive high level,<br>Channel 0                 | 0x41[0]    | 0x59[0]    | 1                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x03[0]                     | VIL0           | Drive low level, Channel<br>0                        | 0x23[0]    | 0x33[0]    | 0                         | X                         | X                           | X                           | X                                | X                          | XXX                            |

## LEVEL SETTING DACS

Table 20. M- and C-Register Mapping

| SPI<br>Address<br>(Channel) | DAC<br>Name | Functional (DAC<br>Usage) Description                | m-register | c-register | VHH_<br>ENABLE<br>0x18[0] | DMC_<br>ENABLE<br>0x1C[0] | LOAD_<br>ENABLEx<br>0x19[5] | PPMU_<br>POWERx<br>0x1A[15] | PPMU_<br>MEAS_<br>Vlx<br>0x1A[5] | PPMU_FORCE<br>_Vlx 0x1A[4] | PPMU_<br>RANGEx<br>(0x1A[3:1]) |
|-----------------------------|-------------|------------------------------------------------------|------------|------------|---------------------------|---------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------|--------------------------------|
|                             |             | HVOUT drive low level,<br>Channel 0                  | 0x43[0]    | 0x5B[0]    | 1                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x06[0]                     | VCH0        | Ref clamp high level,<br>Channel 0                   | 0x26[0]    | 0x36[0]    | X                         | X                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |             | PPMU clamp high level,<br>Channel 0                  | 0x52[0]    | 0x6A[0]    | X                         | X                         | X                           | 1                           | X                                | X                          | XXX                            |
| 0x07[0]                     | VCL0        | Ref clamp low level,<br>Channel 0                    | 0x27[0]    | 0x37[0]    | X                         | X                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |             | PPMU clamp low level,<br>Channel 0                   | 0x53[0]    | 0x6B[0]    | X                         | X                         | X                           | 1                           | X                                | X                          | XXX                            |
| 0x0A[0]                     | PPMU0       | PPMU VIN FV level,<br>Channel 0                      | 0x2A[0]    | 0x3A[0]    | X                         | X                         | X                           | X                           | X                                | 0                          | XXX                            |
|                             |             | PPMU VIN FI Range A<br>level, Channel 0              | 0x54[0]    | 0x6C[0]    | X                         | X                         | X                           | X                           | X                                | 1                          | 111                            |
|                             |             | PPMU VIN FI Range B<br>level, Channel 0              | 0x55[0]    | 0x6C[0]    | X                         | X                         | X                           | X                           | X                                | 1                          | 110                            |
|                             |             | PPMU VIN FI Range C<br>level, Channel 0              | 0x56[0]    | 0x6C[0]    | X                         | X                         | X                           | X                           | X                                | 1                          | 101                            |
|                             |             | PPMU VIN FI Range D<br>Level, Channel 0              | 0x57[0]    | 0x6C[0]    | X                         | X                         | X                           | X                           | X                                | 1                          | 100                            |
|                             |             | PPMU VIN FI Range E<br>level, Channel 0              | 0x58[0]    | 0x6C[0]    | X                         | X                         | X                           | X                           | X                                | 1                          | 0XX                            |
| 0x0B[0]                     | VHH         | VHH level                                            | 0x2B[0]    | 0x3B[0]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x0C[0]                     | OVDH        | Overvoltage detect high                              | 0x2C[0]    | 0x3C[0]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x04[1]                     | VOH1        | NWC high level, Chan-<br>nel 1                       | 0x24[1]    | 0x34[1]    | X                         | X                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |             | PPMU go/no-go MV<br>high level, Channel 1            | 0x45[1]    | 0x5D[1]    | X                         | X                         | X                           | 1                           | 0                                | X                          | XXX                            |
|                             |             | PPMU go/no-go MI<br>Range A high level,<br>Channel 1 | 0x46[1]    | 0x5E[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 111                            |
|                             |             | PPMU go/no-go MI<br>Range B high level,<br>Channel 1 | 0x47[1]    | 0x5E[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 110                            |
|                             |             | PPMU go/no-go MI<br>Range C high level,<br>Channel 1 | 0x48[1]    | 0x5E[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 101                            |
|                             |             | PPMU go/no-go MI<br>Range D high level,<br>Channel 1 | 0x49[1]    | 0x5E[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 100                            |
|                             |             | PPMU go/no-go MI<br>Range E high level,<br>Channel 1 | 0x4A[1]    | 0x5E[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 0XX                            |
| 0x05[1]                     | VOL1        | NWC low level, Channel<br>1                          | 0x25[1]    | 0x35[1]    | X                         | X                         | X                           | 0                           | X                                | X                          | XXX                            |

## LEVEL SETTING DACS

Table 20. M- and C-Register Mapping

| SPI<br>Address<br>(Channel) | DAC<br>Name    | Functional (DAC<br>Usage) Description         | m-register | c-register | VHH_<br>ENABLE<br>0x18[0] | DMC_<br>ENABLE<br>0x1C[0] | LOAD_<br>ENABLEx<br>0x19[5] | PPMU_<br>POWERx<br>0x1A[15] | PPMU_<br>MEAS_<br>Vix<br>0x1A[5] | PPMU_FORCE<br>_Vix 0x1A[4] | PPMU_<br>RANGEx<br>(0x1A[3:1]) |
|-----------------------------|----------------|-----------------------------------------------|------------|------------|---------------------------|---------------------------|-----------------------------|-----------------------------|----------------------------------|----------------------------|--------------------------------|
|                             |                | PPMU go/no-go MV low level, Channel 1         | 0x4C[1]    | 0x64[1]    | X                         | X                         | X                           | 1                           | 0                                | X                          | XXX                            |
|                             |                | PPMU go/no-go MI Range A low level, Channel 1 | 0x4D[1]    | 0x65[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 111                            |
|                             |                | PPMU go/no-go MI Range B low level, Channel 1 | 0x4E[1]    | 0x65[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 110                            |
|                             |                | PPMU go/no-go MI Range C low level, Channel 1 | 0x4F[1]    | 0x65[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 101                            |
|                             |                | PPMU go/no-go MI Range D low level, Channel 1 | 0x50[1]    | 0x65[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 100                            |
|                             |                | PPMU go/no-go MI Range E low level, Channel 1 | 0x51[1]    | 0x65[1]    | X                         | X                         | X                           | 1                           | 1                                | X                          | 0XX                            |
| 0x08[1]                     | VIOH1          | Load IOH level, Channel 1                     | 0x28[1]    | 0x38[1]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x09[1]                     | VIOL1          | Load IOL level, Channel 1                     | 0x29[1]    | 0x39[1]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x02[1]                     | VIT1/<br>VCOM1 | Drive term level, Channel 0                   | 0x22[1]    | 0x32[1]    | X                         | X                         | 0                           | X                           | X                                | X                          | XXX                            |
|                             |                | Load commutation voltage, Channel 1           | 0x42[1]    | 0x5A[1]    | X                         | X                         | 1                           | X                           | X                                | X                          | XXX                            |
| 0x01[1]                     | VIH1           | Drive high level, Channel 1                   | 0x21[1]    | 0x31[1]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x03[1]                     | VIL1           | Drive low level, Channel 1                    | 0x23[1]    | 0x33[1]    | X                         | X                         | X                           | X                           | X                                | X                          | XXX                            |
| 0x06[1]                     | VCH1           | Ref clamp high level, Channel 1               | 0x26[1]    | 0x36[1]    | X                         | X                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |                | PPMU clamp high level, Channel 1              | 0x52[1]    | 0x6A[1]    | X                         | X                         | X                           | 1                           | X                                | X                          | XXX                            |
| 0x07[1]                     | VCL1           | Ref clamp low level, Channel 1                | 0x27[1]    | 0x37[1]    | X                         | X                         | X                           | 0                           | X                                | X                          | XXX                            |
|                             |                | PPMU clamp low level, Channel 1               | 0x53[1]    | 0x6B[1]    | X                         | X                         | X                           | 1                           | X                                | X                          | XXX                            |
| 0x0A[1]                     | PPMU1          | PPMU VIN FV level, Channel 1                  | 0x2A[1]    | 0x3A[1]    | X                         | X                         | X                           | X                           | X                                | 0                          | XXX                            |
|                             |                | PPMU VIN FI Range A level, Channel 1          | 0x54[1]    | 0x6C[1]    | X                         | X                         | X                           | X                           | X                                | 1                          | 111                            |
|                             |                | PPMU VIN FI Range B level, Channel 1          | 0x55[1]    | 0x6C[1]    | X                         | X                         | X                           | X                           | X                                | 1                          | 110                            |
|                             |                | PPMU VIN FI Range C level, Channel 1          | 0x56[1]    | 0x6C[1]    | X                         | X                         | X                           | X                           | X                                | 1                          | 101                            |

## LEVEL SETTING DACS

Table 20. M- and C-Register Mapping

| SPI Address (Channel) | DAC Name | Functional (DAC Usage) Description   | m-register | c-register | VHH_ENABLE 0x18[0] | DMC_ENABLE 0x1C[0] | LOAD_ENABLEx 0x19[5] | PPMU_POWERx 0x1A[15] | PPMU_MEAS_VIx 0x1A[5] | PPMU_FORCE_VIx 0x1A[4] | PPMU_RANGEx (0x1A[3:1]) |
|-----------------------|----------|--------------------------------------|------------|------------|--------------------|--------------------|----------------------|----------------------|-----------------------|------------------------|-------------------------|
|                       |          | PPMU VIN FI Range D level, Channel 1 | 0x57[1]    | 0x6C[1]    | X                  | X                  | X                    | X                    | X                     | 1                      | 100                     |
|                       |          | PPMU VIN FI Range E level, Channel 1 | 0x58[1]    | 0x6C[1]    | X                  | X                  | X                    | X                    | X                     | 1                      | 0XX                     |
| 0x0E[0]               | Spare    | Spare level                          | 0x2E[0]    | 0x3E[1]    | X                  | X                  | X                    | X                    | X                     | X                      | XXX                     |

## DAC TRANSFER FUNCTIONS

Table 21. Detailed DAC Code to Voltage Level Transfer Functions

| Levels                                                       | Programmable DAC Range, <sup>1</sup> 0x0000 to 0xFFFF | DAC-to-Level and Level-to-DAC Transfer Functions                                                                                                                                                                                                                            |
|--------------------------------------------------------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VIHx, VILx, VITx/VCOMx, VOLx, VOHx, VCHx, VCLx, OVDHx, OVDLx | -2.5 V to +7.5 V                                      | $V_{OUT} = 2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) + V_{DUTGND}$ $DAC = [V_{OUT} - V_{DUTGND} + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$                                                               |
| VHH                                                          | -3.0 V to +17.0 V                                     | $V_{OUT} = 4 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.6 \times (VREF - VREFGND) + V_{DUTGND}$ $DAC = [V_{OUT} - V_{DUTGND} + 0.6 \times (VREF - VREFGND)] \times [2^{16}/(4 \times (VREF - VREFGND))]$                                                               |
| IOHx, IOLx                                                   | -12.5 mA to +37.5 mA                                  | $I_{OUT} = [2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND)] \times (25 \text{ mA}/5)$ $DAC = [(I_{OUT} \times (5/25 \text{ mA})) + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$                                   |
| PPMU_VINx (FV)                                               | -2.5 V to +7.5 V                                      | $V_{OUT} = 2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) + V_{DUTGND}$ $DAC = [V_{OUT} - V_{DUTGND} + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$                                                               |
| PPMU_VINx (FI, Range A)                                      | -80 mA to +80 mA                                      | $I_{OUT} = [2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) - 2.5] \times (80 \text{ mA}/5)$ $DAC = [(I_{OUT} \times (5/80 \text{ mA})) + 2.5 + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$                       |
| PPMU_VINx (FI, Range B)                                      | -2 mA to +2 mA                                        | $I_{OUT} = [2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) - 2.5] \times (2 \text{ mA}/5)$ $DAC = [(I_{OUT} \times (5/2 \text{ mA})) + 2.5 + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$                         |
| PPMU_VINx (FI, Range C)                                      | -200 $\mu$ A to +200 $\mu$ A                          | $I_{OUT} = [2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) - 2.5] \times (200 \text{ } \mu\text{A}/5)$ $DAC = [(I_{OUT} \times (5/200 \text{ } \mu\text{A})) + 2.5 + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$ |
| PPMU_VINx (FI, Range D)                                      | -20 $\mu$ A to +20 $\mu$ A                            | $I_{OUT} = [2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) - 2.5] \times (20 \text{ } \mu\text{A}/5)$ $DAC = [(I_{OUT} \times (5/20 \text{ } \mu\text{A})) + 2.5 + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$   |
| PPMU_VINx (FI, Range E)                                      | -4 $\mu$ A to +4 $\mu$ A                              | $I_{OUT} = [2 \times (VREF - VREFGND) \times (DAC/2^{16}) - 0.5 \times (VREF - VREFGND) - 2.5] \times (4 \text{ } \mu\text{A}/5)$ $DAC = [(I_{OUT} \times (5/4 \text{ } \mu\text{A})) + 2.5 + 0.5 \times (VREF - VREFGND)] \times [2^{16}/(2 \times (VREF - VREFGND))]$     |

<sup>1</sup> Programmable ranges include the margin outside the specified performance range, allowing for offset and gain calibration.

Table 22. Load Transfer Functions

| Load Level | Transfer Functions                               | Notes                                                                                          |
|------------|--------------------------------------------------|------------------------------------------------------------------------------------------------|
| IOLx       | $V_{IOLx}/(VREF - VREFGND) \times 25 \text{ mA}$ | V <sub>IOLx</sub> and V <sub>IOHx</sub> DAC levels are not referenced to V <sub>DUTGND</sub> . |
| IOHx       | $V_{IOHx}/(VREF - VREFGND) \times 25 \text{ mA}$ |                                                                                                |

Table 23. PPMU Transfer Functions

| PPMU Mode | Transfer Functions <sup>1</sup>                                          | Uncalibrated PPMU_VIN DAC Settings to Achieve Specified PPMU Range |
|-----------|--------------------------------------------------------------------------|--------------------------------------------------------------------|
| FV        | $V_{OUT} = \text{PPMU\_VINx}$                                            | -2.0 V < PPMU_VINx < +6.5 V                                        |
| MV        | $V_{PPMU\_MEASx} = V_{DUTx}$ (internal sense path)                       | N/A                                                                |
| MV        | $V_{PPMU\_MEASx} = V_{PPMU\_Sx}$ (external sense path)                   | N/A                                                                |
| FI        | $I_{OUT} = [\text{PPMU\_VINx} - (VREF - VREFGND)/2]/(5 \times R_{PPMU})$ | 0.0 V < PPMU_VINx < 5.0 V                                          |

## LEVEL SETTING DACS

Table 23. PPMU Transfer Functions

| PPMU Mode | Transfer Functions <sup>1</sup>                                                                | Uncalibrated PPMU_VIN DAC Settings to Achieve Specified PPMU Range |
|-----------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|
| MI        | $V_{PPMU\_MEASx} = [V_{REF} - V_{REFGND}]/2 + (5 \times I_{OUT} \times R_{PPMU}) + V_{DUTGND}$ | N/A                                                                |

<sup>1</sup> RPPMU = 12.5 Ω for Range A, 500 Ω for Range B, 5.0 kΩ for Range C, 50 kΩ for Range D, and 250 kΩ for Range E.

Table 24. VHH Transfer Functions

| VHH Mode | Transfer Functions                                                  |
|----------|---------------------------------------------------------------------|
| VHH      | $HVOUT = 2 \times [V_{HH} + (V_{REF} - V_{REFGND})/5] + V_{DUTGND}$ |
| VIL      | $HVOUT = V_{IL0} + V_{DUTGND}$                                      |
| VIH      | $HVOUT = V_{IH0} + V_{DUTGND}$                                      |

## GAIN AND OFFSET CORRECTION

Each DAC within the ADATE318 has independent gain (m) and offset (c) correction registers that allow digital trim of gain and offset errors. DACs that are shared between functions or levels are provided with per-level or per-function gain and offset correction registers, as appropriate. These registers provide the ability to calibrate out errors in the complete signal chain, which includes error in pin electronics function as well as the DACs. All m- and c-registers are volatile and must be loaded after power-on as part of a calibration cycle if values other than the defaults are required.

The gain and offset correction function can be bypassed by clearing the DAC\_CAL\_ENABLE bit in the SPI DAC control register (SPI ADDR 0x11[0]; see Figure 116). This bypass mode is available on a per-chip basis only; that is, it is not possible to bypass calibration for a subset of the DACs.

The calibration function, when enabled, adjusts the numerical data sent to each DAC according to the following equation:

$$X_2 = \left[ \left( \frac{m+1}{2^n} \right) \times X_1 \right] + (c - 2^{n-1}) \quad (1)$$

where:

$X_2$  = the data-word loaded into the DAC and returned by an SPI read operation.

$X_1$  = the 16-bit data-word written to the DAC SPI input register.

$m$  = the code in the respective DAC gain register (default code = 0xFFFF =  $2^n - 1$ ).

$c$  = the code in the respective DAC offset register (default code = 0x8000 =  $2^{n-1}$ ).

$n$  = the DAC resolution ( $n = 16$ ).

From this equation, it can be seen that the gain applied to the  $X_1$  value is always less than or equal to 1.0, with the effect that a DAC's output voltage can only be made smaller. To compensate for this numerically imposed limitation, the ADATE318's signal paths are designed to have gain guaranteed to be greater than 1.0 when the default m values (0xFFFF) are applied. This guarantees that proper gain calibration is always possible. Note also that the value of c is expressed in raw DAC LSBs; that is, it is calculated without considering the effect of the m-register.

When enabled, the calibration function applies the above operation to the  $X_2$  register(s) only after a SPI write to the respective  $X_1$  register(s). The  $X_2$  registers are not updated after writes to either the m- or c-register. In the case of a dual channel write to the DAC, two respective  $X_2$  registers are sequentially updated using the appropriate m and c values.

**X<sub>2</sub> REGISTERS**

Each DAC has associated with a single  $X_2$  register. There is no provision for storing separate  $X_2$  values for DACs shared between functions or ranges. Thus, new data must be written to any shared DAC after a mode or range change is performed, even if the old and new DAC data is identical. The ADATE318 provides separate m- and c-registers for all ranges and modes so that the new  $X_2$  value is calculated correctly following the new data write, provided the desired m and c values are stored in advance. The sequence of operations is critical in that the mode or range change must be performed prior to writing the new DAC data, and both m and c values must be present before the new DAC data is written. The m and/or c value can be written either before or after a mode or range change but must be written prior to the DAC data to have the intended effect.

**SAMPLE CALCULATIONS OF M AND C**

Because the ADATE318's on-chip DACs have a theoretical output range that exceeds the operating capabilities of the remainder of its signal channels, calibration points must be chosen to be within the normal operating span. Subject to this constraint, calibration is straightforward. One of the keys to understanding the calibration method is to recognize that the intrinsic DAC offset is defined by its output when the input code is 0x0000. This is quite different from the case of the analog signal paths, where a 0 V level occurs when the DAC code is programmed to near quarter-scale.

As a first example, consider the calibration of a drive high level with a theoretical output span of -2.5 V to +7.5 V, a convenient +10.0 V span in which DAC quarter-scale corresponds to precisely 0.0 V out. The ADATE318 drivers do not of course support this full span, but it is a useful choice for illustration of the calibration methodology.

## LEVEL SETTING DACS

1. Set the channel to drive high and program the VIL and VIT DACs for roughly -1.0 V outputs (Code 0x2700, not critical). Program the VIH DAC to quarter-scale (0x4000) and measure Output Voltage  $V_1$ ; then program the DAC to three-quarter-scale (0xC000) and measure Output Voltage  $V_2$ . Note that  $V_1$  and  $V_2$  should be measured with respect to DUTGND.

2. Calculate

$$Actual\_DAC\_FSR = 2 \times (V_2 - V_1)$$

where  $(V_2 - V_1)$  represents half the full-scale span.

3. Calculate the extrapolated DAC voltage at Code 0x0000.

$$V_0 = V_1 - \left( \frac{Actual\_DAC\_FSR}{4} \right) \quad (2)$$

4. Calculate

$$Actual\_DAC\_LSB = \frac{(V_2 - V_1)}{32,768} \quad (3)$$

5. Calculate

$$m = \left\lceil \frac{5}{(V_2 - V_1)} \times 65,536 \right\rceil - 1 \quad (4)$$

6. Calculate the offset from the ideal -2.5 V.

$$Offset = (-2.5) - V_0 \quad (5)$$

7. Calculate

$$c = 32,768 + \left( \frac{Offset}{Actual\_DAC\_LSB} \right) \quad (6)$$

8. Calculate volts

$$Post\_Calibration\_DAC\_LSB = Actual\_DAC\_LSB \times \left( \frac{5}{V_2 - V_1} \right) \quad (7)$$

The above procedure places the DAC's theoretical 0x0000 output at -2.5 V and its theoretical 0xFFFF output at +7.49985 V (1 LSB below +7.5 V). The useful range extends from below 0x199A (-1.5 V) to above 0xE666 (+6.5 V), a span of at least 52,428 actual DAC codes.

An alternative calibration approach can be used to map all  $2^{16}$  DAC codes onto the part's specified output range by mapping the zero-code to -1.5 V and the full-scale code to +6.5 V.

1. Repeat Step 1 to Step 4 above.
2. Calculate

$$m = \frac{4}{(V_2 - V_1)} \times 65,535 \quad (8)$$

3. Calculate the offset from the desired -1.5 V.

$$Offset = (-1.5) - V_0 \quad (9)$$

4. Calculate DAC

$$c = 32,768 + \left( \frac{Offset}{Actual\_DAC\_LSB} \right) \quad (10)$$

5. Calculate

$$Post\_Calibration\_DAC\_LSB = \frac{8}{65,536} \text{ Volts}$$

Although this second approach gives an apparent 16 bits of resolution covering the full signal range, it must be kept in mind that this is achieved purely by mathematical alteration of the DAC data. The DAC's internal LSB step size is not changed. In this example, the number of internal DAC codes used to cover the signal span remains roughly 52,428 even though the number of user codes has increased to 65,536. A consequence of this is that apparent DNL errors are increased as more input codes are mapped onto the same number of DAC codes. While the second calibration method is included here as an example of what is possible, its use can provide a false sense of improved accuracy and it is therefore not recommended.

## POWER SUPPLY, GROUNDING, AND DECOUPLING STRATEGY

The ADATE318 product is internally divided into a digital core and an analog core.

The VCC and DGND pins provide power and ground, respectively, for the digital core, which includes the SPI and all digital calibration functions. DGND is the logic ground reference for the VCC supply, and VCC should be adequately bypassed to DGND with low ESR bypass capacitors. To reduce transient digital switching noise coupling from the VCC and DGND pins to the analog core, DGND should be connected to a dedicated ground domain that is separate from the analog ground domains. If the application permits, the DGND should share digital ground domain with the system FPGA or ASIC that interfaces with the ADATE318 SPI. All CMOS inputs and outputs are referenced between VCC and DGND, and their valid levels should be guaranteed relative to these.

The analog core of the product includes all analog ATE functional blocks such as DACs, driver, comparator, load, PPMU, VHH driver, and so on. The VPLUS, VDD, and VSS supplies provide power for the analog core. The AGND and PGND are analog ground and analog power ground references, respectively. PGND is generally more noisy with analog switching transients, and it may also have large static dc currents. The AGND is generally more quiet and has relatively small static dc currents. Ideally, these ground domains should be separated, but it is not necessary. They can be connected together outside the chip to a shared analog ground plane. VDD and VSS should be adequately bypassed to the PGND ground domain. Both PGND and AGND (whether separated or shared) should be kept separate from the DGND ground plane as discussed above.

The VPLUS supply pin has the sole purpose to provide high voltage power for the VHH drive capability (HVOUT pin). If the VHH drive capability is used, the VPLUS supply must be provided as specified. If the VHH drive capability is not used, the VPLUS supply can be connected directly to the VDD supply domain to save power.

The ADATE318 also has a DUTGND input pin that can be used to sense the remote DUT ground potential. All DAC functions (with the exception of VIOH and VIOL active load currents and VPMU when in PPMU FI mode) are adjusted relative to this DUTGND input. Further, the PPMU measure out pins (PPMU\_MEASx) are referenced to DUTGND not AGND. This, therefore, requires the system ADC to reference its inputs relative to DUTGND as well. Referencing the system ADC to AGND results in errors, except in the case that DUTGND is tied to AGND. For applications that do not distinguish between DUT ground reference and system analog ground reference, the DUTGND pin can be connected to the same ground plane as AGND.

The ADATE318 should have ample supply decoupling of 0.1  $\mu$ F on each supply pin located as close to the device as possible, ideally right up against the device. In addition, there should be one 10  $\mu$ F tantalum capacitor shared across each power domain. The 0.1  $\mu$ F capacitor should have low effective series resistance (ESR) and effective series inductance (ESL), such as the common

ceramic capacitors that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided because these couple noise onto the device. The analog ground plane should be allowed to run under the device to avoid noise coupling. The power supply lines should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. It is essential to minimize noise on all VREF lines. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough throughout the board. As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

## USER INFORMATION AND TRUTH TABLES

Table 25. Driver Truth Table

| DCL Control Register Bits (0x19) |                                         |                                          |                                               |                                          | High Speed Inputs                       |                   |                   |             |
|----------------------------------|-----------------------------------------|------------------------------------------|-----------------------------------------------|------------------------------------------|-----------------------------------------|-------------------|-------------------|-------------|
| DCL Enable ADDR<br>0x19[0]       | Force Load<br>ADDR 0x19[2] <sup>1</sup> | Force Drive<br>ADDR 0x19[1] <sup>1</sup> | Force State<br>ADDR<br>0x19[4:3] <sup>1</sup> | Load Enable<br>ADDR 0x19[5] <sup>1</sup> | DRV_VT_HIZ ADDR<br>0x19[6] <sup>1</sup> | RCVx <sup>1</sup> | DATx <sup>1</sup> | Driver      |
| 0                                | X                                       | X                                        | XX                                            | X                                        | X                                       | X                 | X                 | Low leakage |
| 1                                | X                                       | 1                                        | 00                                            | X                                        | X                                       | X                 | X                 | VIL         |
| 1                                | X                                       | 1                                        | 01                                            | X                                        | X                                       | X                 | X                 | VIH         |
| 1                                | X                                       | 1                                        | 10                                            | X                                        | X                                       | X                 | X                 | High-Z      |
| 1                                | X                                       | 1                                        | 11                                            | X                                        | X                                       | X                 | X                 | VIT         |
| 1                                | X                                       | 0                                        | XX                                            | X                                        | X                                       | 0                 | 0                 | VIL         |
| 1                                | X                                       | 0                                        | XX                                            | X                                        | X                                       | 0                 | 1                 | VIH         |
| 1                                | X                                       | 0                                        | XX                                            | X                                        | 0                                       | 1                 | X                 | High-Z      |
| 1                                | X                                       | 0                                        | XX                                            | X                                        | 1                                       | 1                 | X                 | VIT         |

<sup>1</sup> X = don't care.

Table 26. Active Load Truth Table

| DCL Control Register Bits (0x19) |                                         |                                          |                                               |                                          | High Speed Inputs                       |                   |                   |             |
|----------------------------------|-----------------------------------------|------------------------------------------|-----------------------------------------------|------------------------------------------|-----------------------------------------|-------------------|-------------------|-------------|
| DCL Enable ADDR<br>0x19[0]       | Force Load<br>ADDR 0x19[2] <sup>1</sup> | Force Drive<br>ADDR 0x19[1] <sup>1</sup> | Force State<br>ADDR<br>0x19[4:3] <sup>1</sup> | Load Enable<br>ADDR 0x19[5] <sup>1</sup> | DRV_VT_HIZ ADDR<br>0x19[6] <sup>1</sup> | RCVx <sup>1</sup> | DATx <sup>1</sup> | Load        |
| 0                                | X                                       | X                                        | XX                                            | X                                        | X                                       | X                 | X                 | Low leakage |
| 1                                | 1                                       | X                                        | XX                                            | X                                        | X                                       | X                 | X                 | Active on   |
| 1                                | 0                                       | X                                        | XX                                            | 0                                        | X                                       | X                 | X                 | Low leakage |
| 1                                | 0                                       | X                                        | XX                                            | 1                                        | X                                       | 0                 | X                 | Active off  |
| 1                                | 0                                       | X                                        | XX                                            | 1                                        | 0                                       | 1                 | X                 | Active on   |
| 1                                | 0                                       | X                                        | XX                                            | 1                                        | 1                                       | 1                 | X                 | Active off  |

<sup>1</sup> X = don't care.

Table 27. VHH and VIH/VIL Driver Truth Table

| VHH_ENABLE ADDR 0x18[0] | CH0 RCV (RCV0) <sup>1</sup> | CH0 DAT (DAT0) <sup>1</sup> | Output of VHH Driver                                                   |
|-------------------------|-----------------------------|-----------------------------|------------------------------------------------------------------------|
| 1                       | 0                           | 0                           | VIL (Channel 0, VIL DAC)                                               |
| 1                       | 0                           | 1                           | VIH (Channel 0, VIH DAC)                                               |
| 1                       | 1                           | X                           | VHH                                                                    |
| 0                       | X                           | X                           | Disabled (HVOUT pin set to 0.0 V, approximately 50 $\Omega$ impedance) |

<sup>1</sup> X = don't care.

Table 28. Comparator Truth Table

| DMC ENABLE<br>ADDR 0x1C[0] | CMPH0                                                                             | CMPL0                                                                             | CMPH1                                                                             | CMPL1                                                                             |
|----------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| 0                          | Normal window compare mode<br>Logic high: VOH0 < VDUT0<br>Logic low: VOH0 > VDUT0 | Normal window compare mode<br>Logic high: VOL0 < VDUT0<br>Logic low: VOL0 > VDUT0 | Normal window compare mode<br>Logic high: VOH1 < VDUT1<br>Logic low: VOH1 > VDUT1 | Normal window compare mode<br>Logic high: VOL1 < VDUT1<br>Logic low: VOL1 > VDUT1 |
| 1                          | Differential compare mode<br>Logic high:<br>VOH0 < VDUT0 – VDUT1                  | Differential compare mode<br>Logic high:<br>VOL0 < VDUT0 – VDUT1                  | Normal window compare mode<br>Logic high: VOH1 < VDUT1<br>Logic low: VOH1 > VDUT1 | Normal window compare mode<br>Logic high: VOL1 < VDUT1<br>Logic low: VOL1 > VDUT1 |

## USER INFORMATION AND TRUTH TABLES

Table 28. Comparator Truth Table

| DMC ENABLE   |                                    |                                    |       |       |
|--------------|------------------------------------|------------------------------------|-------|-------|
| ADDR 0x1C[0] | CMPH0                              | CMPL0                              | CMPH1 | CMPL1 |
|              | Logic low:<br>VOH0 > VDUT0 – VDUT1 | Logic low:<br>VOL0 > VDUT0 – VDUT1 |       |       |

## ALARM FUNCTIONS

The ADATE318 contains per-channel overvoltage detectors (OVD), PPMU voltage/current clamps, and a per-chip thermal alarm to detect and signal fault conditions. The status of these circuits may be interrogated via the SPI by reading the alarm state register (SPI ADDR 0x1E; see [Figure 124](#)). This read-only register is cleared by a read operation. In addition, the fault conditions are combined in the fault alarm logic (see [Figure 136](#)) and drive the open drain ALARM pin to signal that a fault has occurred.

The various alarm circuits are controlled through the alarm mask register (ADDR 0x1D; see [Figure 123](#)). In the default state, the thermal alarm is enabled, and both the overvoltage alarm and the PPMU clamp alarms are masked off.

The only function of the alarm circuits is to detect and signal the presence of a fault. The only actions taken upon detection of a fault are setting of the appropriate register bit and activating the ALARM pin.

## USER INFORMATION AND TRUTH TABLES

## PPMU EXTERNAL CAPACITORS

Table 29. PPMU External Compensation and Feedforward Capacitors

| External Components | Location                    |
|---------------------|-----------------------------|
| 220 pF              | Between FFCAPB0 and FFCAPA0 |
| 220 pF              | Between FFCAPB1 and FFCAPA1 |
| 1000 pF             | Between AGND and SCAP0      |
| 1000 pF             | Between AGND and SCAP1      |

Table 30. Other External Components

| External Components | Location             |
|---------------------|----------------------|
| 10 k $\Omega$       | ALARM pull-up to VCC |
| 1 k $\Omega$        | BUSY pull-up to VCC  |

## TEMPERATURE SENSOR

Table 31.

| Temperature         | Output                                           |
|---------------------|--------------------------------------------------|
| 0 K                 | 0.00 V                                           |
| 300 K               | 3.00 V                                           |
| T <sub>KELVIN</sub> | 0.00 V + (T <sub>KELVIN</sub> ) $\times$ 10 mV/K |

## DEFAULT TEST CONDITIONS

Table 32.

| Name                       | Default Test Condition                                                                                                                                                                          |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VIHx DAC Levels            | 2.0 V                                                                                                                                                                                           |
| VITx/VCOMx DAC Levels      | 1.0 V                                                                                                                                                                                           |
| VILx DAC Levels            | 0.0 V                                                                                                                                                                                           |
| VOHx DAC Levels            | 6.5 V                                                                                                                                                                                           |
| VOLx DAC Levels            | -1.5 V                                                                                                                                                                                          |
| VCHx DAC Levels            | 7.5 V                                                                                                                                                                                           |
| VCLxDAC Levels             | -2.5 V                                                                                                                                                                                          |
| VIOHxDAC Levels            | 0.0 mA                                                                                                                                                                                          |
| VIOLx DAC Levels           | 0.0 mA                                                                                                                                                                                          |
| PPMU_VINx DAC Levels       | 0.0 V                                                                                                                                                                                           |
| VHH DAC Level              | 13.0 V                                                                                                                                                                                          |
| OVDH DAC Levels            | 7.0 V                                                                                                                                                                                           |
| OVDL DAC Levels            | -2.0 V                                                                                                                                                                                          |
| DAC_CONTROL                | 0x0000: DAC calibration disabled, DAC load mode is immediate                                                                                                                                    |
| VHH_CONTROL                | 0x0000: HVOUT (VHH) disabled                                                                                                                                                                    |
| DCL_CONTROL                | 0x0001: DCL enabled, load disabled, high-Z for RCVx = 1, force drive = 0 (to VIL state)                                                                                                         |
| PPMU_CONTROL               | 0x0000: PPMU disabled, PPMU Range E, Force-V <sup>1</sup> /Measure-V <sup>2</sup> , input to V <sub>DUTGND</sub> , internal sense path, clamps disabled, external PPMU_S open, PPMU_POWER_x off |
| PPMU_MEAS_CONTROL          | 0x0000: PPMU_MEASx high-Z                                                                                                                                                                       |
| COMPARATOR_CONTROL         | 0x0000: normal window comparator mode, comparator hysteresis disabled                                                                                                                           |
| ALARM_MASK                 | 0x0045: disable alarm functions                                                                                                                                                                 |
| PRE_EMPHASIS_CONTROL       | 0x0000: disable driver CLC, differential comparator CLC, and normal window comparator CLC                                                                                                       |
| Calibration m-Coefficients | 1.0 (0xFFFF)                                                                                                                                                                                    |
| Calibration c-Coefficients | 0.0 (0x8000)                                                                                                                                                                                    |

USER INFORMATION AND TRUTH TABLES

Table 32.

| Name                 | Default Test Condition |
|----------------------|------------------------|
| DATx, RCVx Inputs    | Logic low              |
| DUTx Pins            | Unterminated           |
| CMPHx, CMPLx Outputs | Unterminated           |
| V <sub>DUTGND</sub>  | 0.0 V                  |

<sup>1</sup> Force-V indicates force voltage.

<sup>2</sup> Measure-V indicates measure voltage.

## DETAILED FUNCTIONAL BLOCK DIAGRAMS

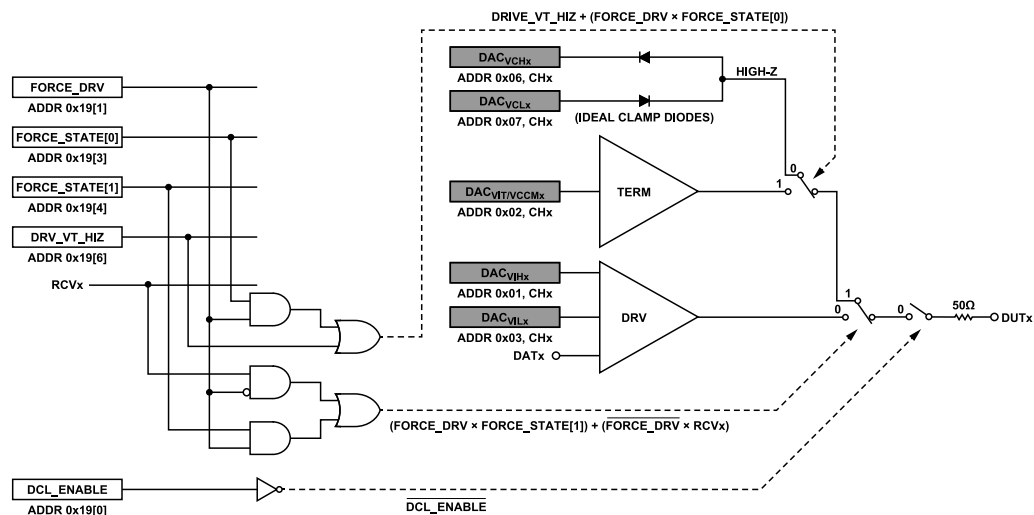
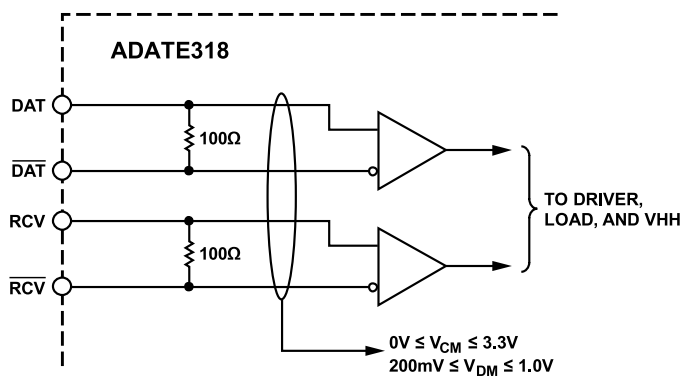


Figure 127. Driver Block Diagram



## TYPICAL INPUT WAVEFORMS

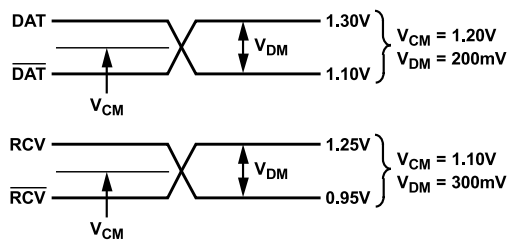


Figure 128. Driver Input Stage Diagram

## DETAILED FUNCTIONAL BLOCK DIAGRAMS

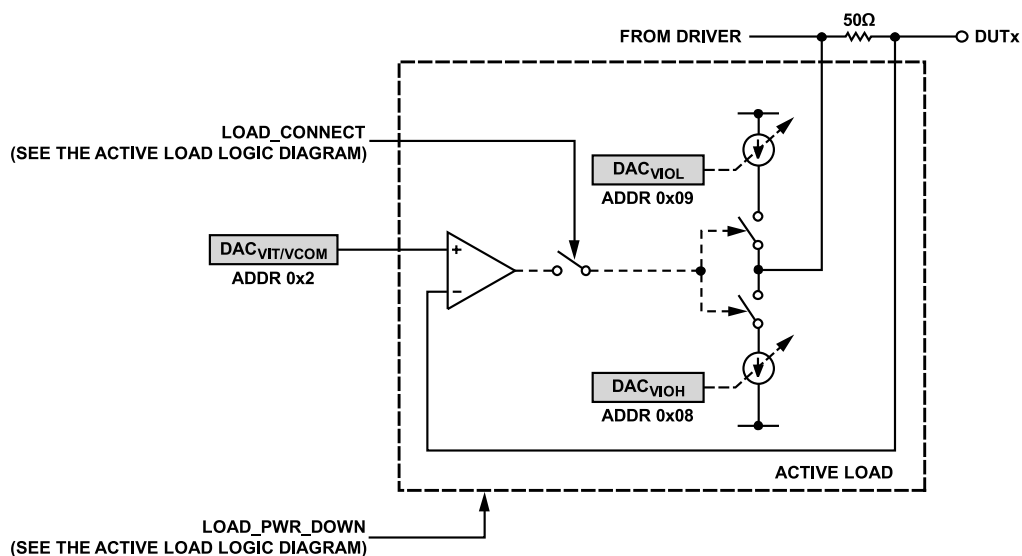
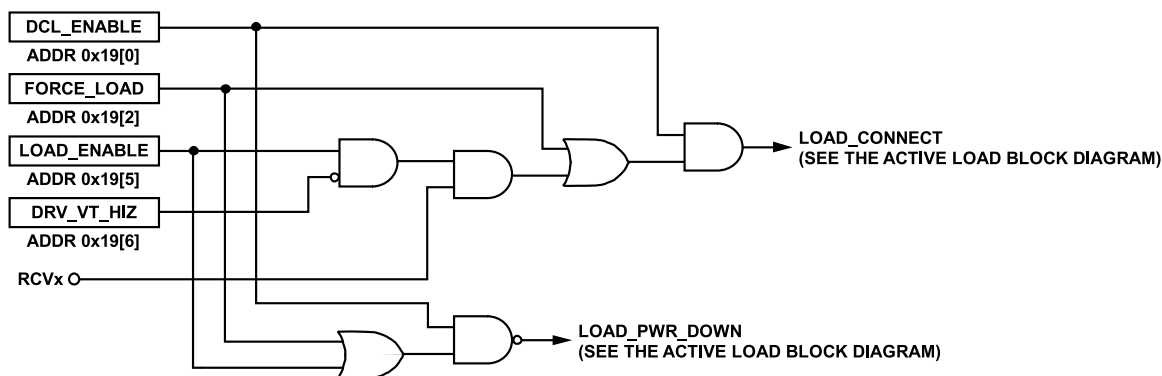


Figure 129. Active Load Block Diagram

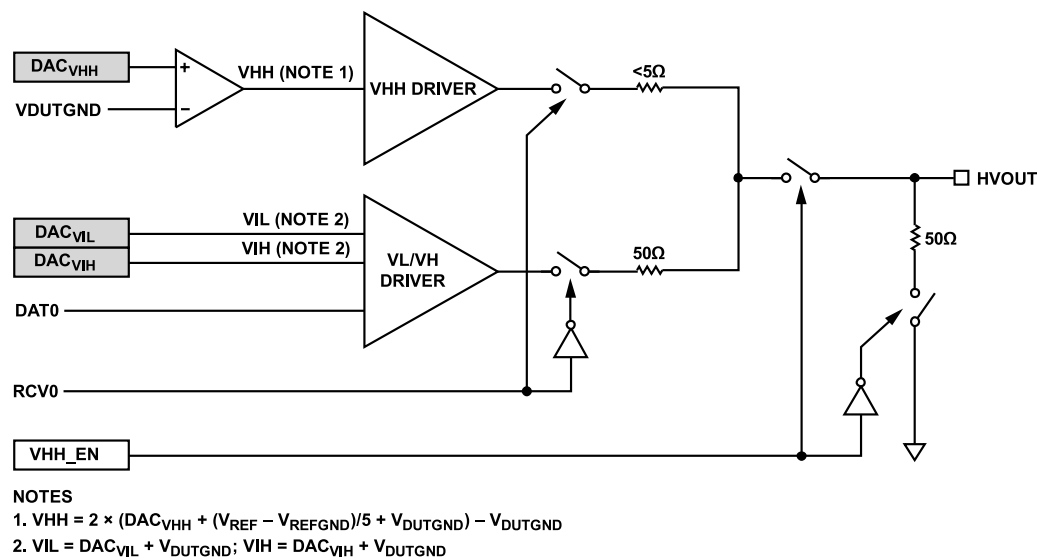


$$\text{LOAD\_CONNECT} = \text{DCL\_ENABLE} \times (\text{FORCE\_LOAD} + \text{RCV}_x \times \overline{\text{DRV\_VT\_HIZ}} \times \text{LOAD\_ENABLE})$$

$$\text{LOAD\_PWR\_DOWN} = \text{DCL\_ENABLE} + \text{FORCE\_LOAD} \times \overline{\text{LOAD\_ENABLE}}$$

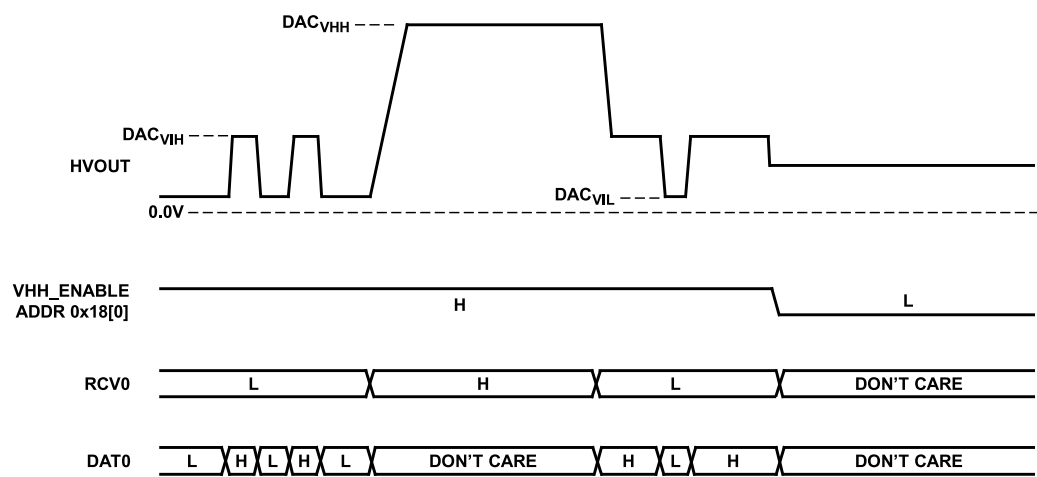
Figure 130. Active Load Logic Diagram

DETAILED FUNCTIONAL BLOCK DIAGRAMS



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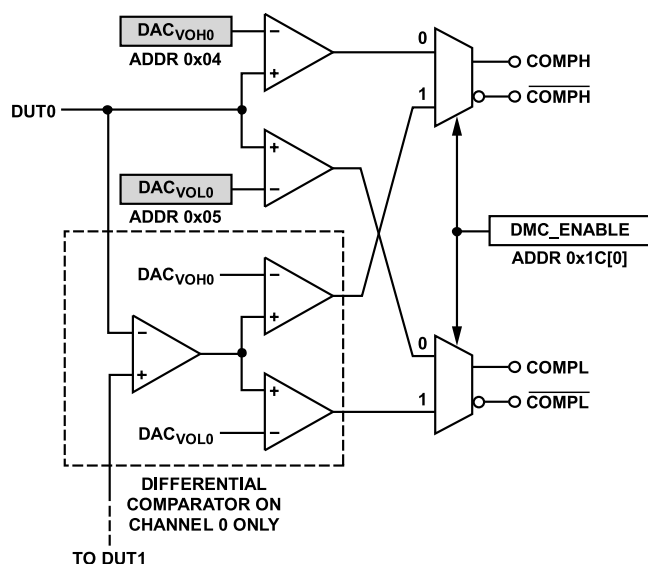
Figure 131. VHH and VIL/VIH Driver Block Diagram



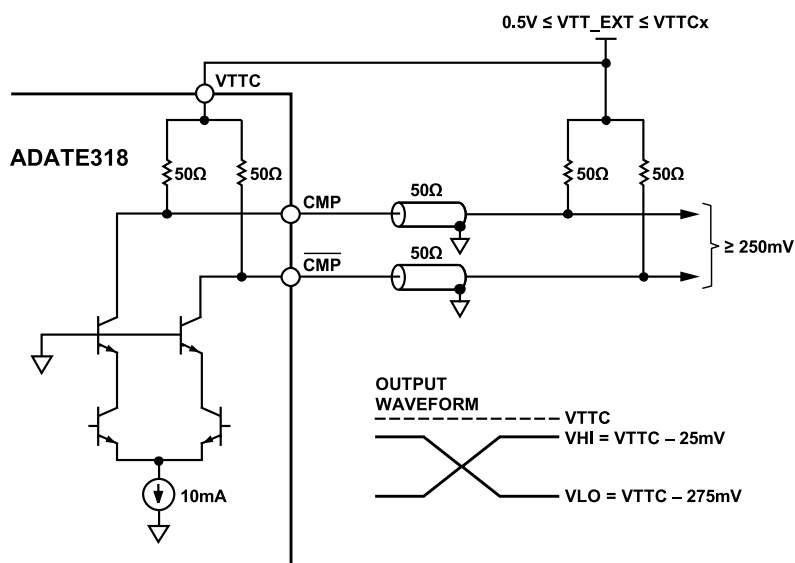
029

Figure 132. VHH and VIL/VIH Waveform Diagram

## DETAILED FUNCTIONAL BLOCK DIAGRAMS



**Figure 133. Comparator Block Diagram**



**Figure 134. Comparator Output Stage Diagram**

DETAILED FUNCTIONAL BLOCK DIAGRAMS

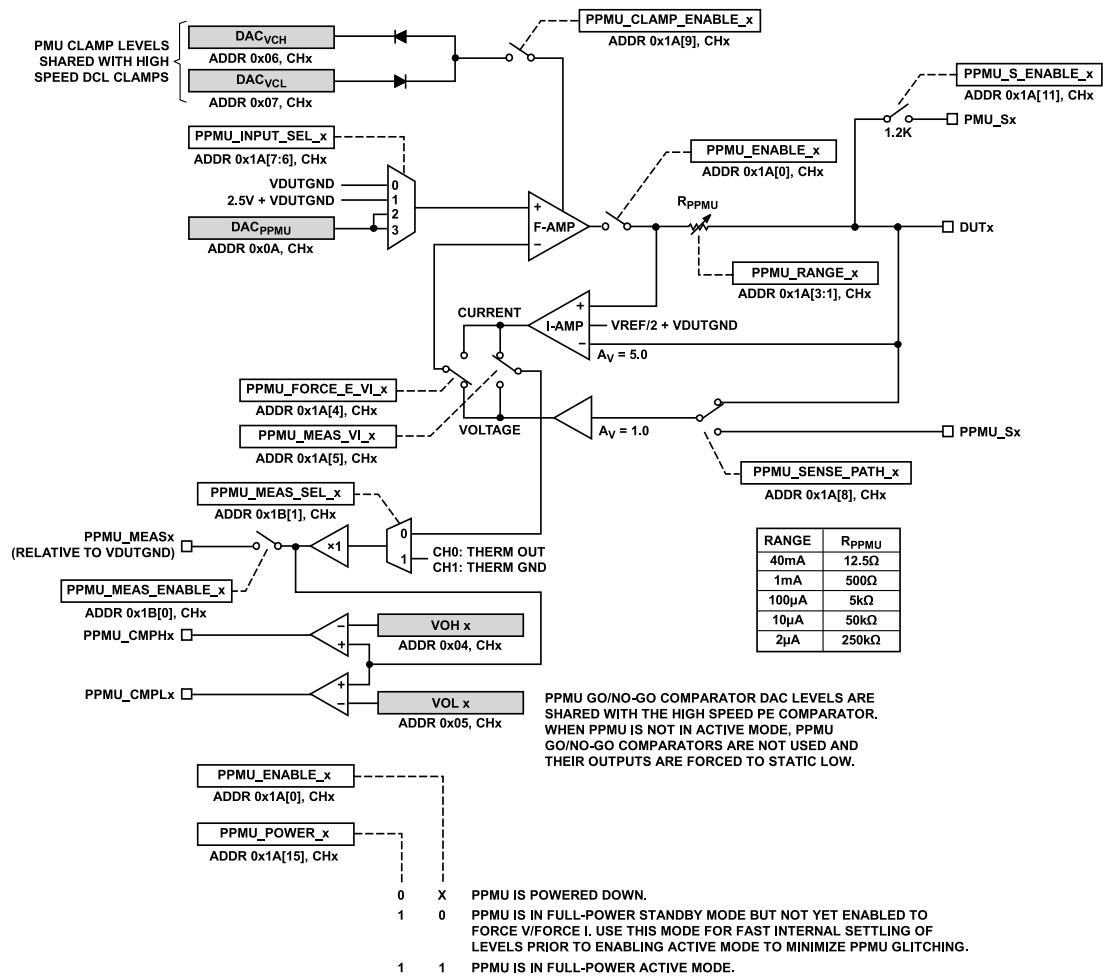


Figure 135. PPMU Block Diagram

## DETAILED FUNCTIONAL BLOCK DIAGRAMS

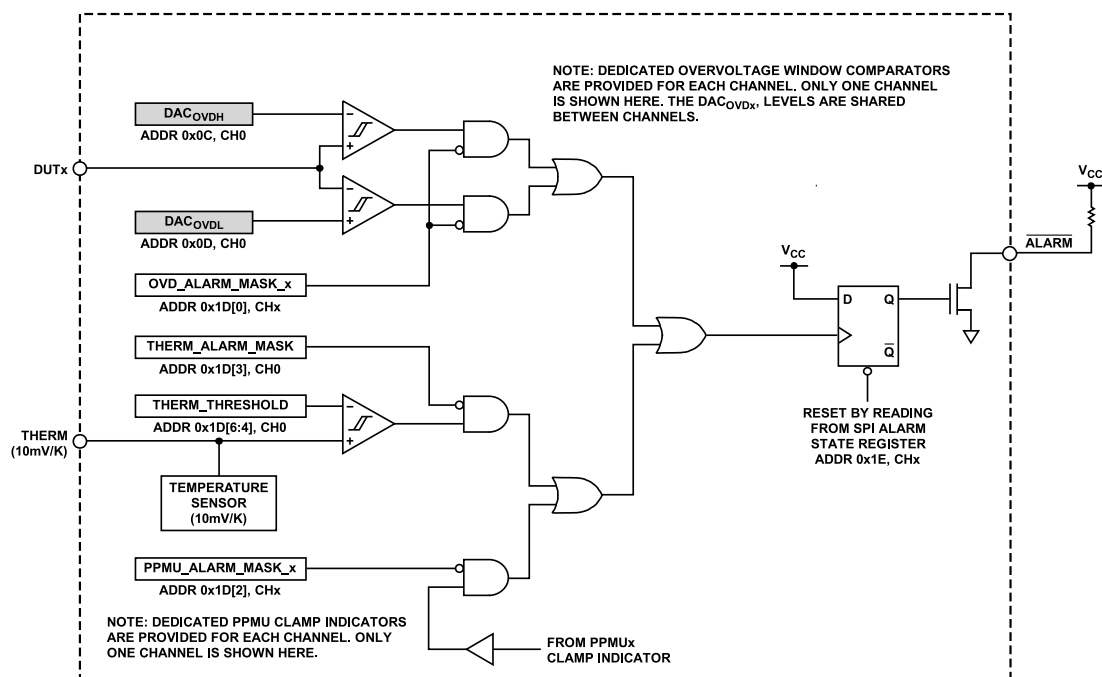
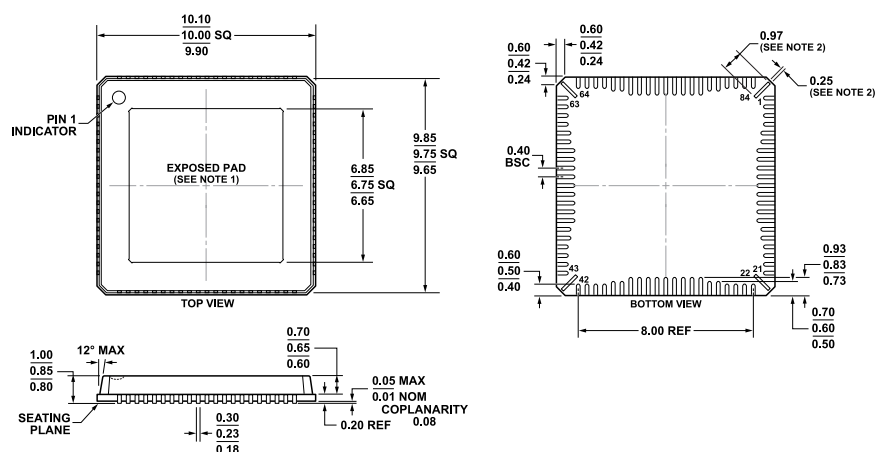


Figure 136. Fault Alarm Block Diagram

## OUTLINE DIMENSIONS



NOTES:  
 1. FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.  
 2. TIEBARS MAY OR MAY NOT BE SOLDERED TO THE BOARD.

**Figure 137. 84-Lead Lead Frame Chip Scale Package [LFCSP]**  
**10 mm × 10 mm Body and 0.85 mm Package Height**  
**(CP-84-2)**  
**Dimensions shown in millimeters**

Updated: August 04, 2022

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description               | Package Option |
|--------------------|-------------------|-----------------------------------|----------------|
| ADATE318BCPZ       | +25°C to +70°C    | 84-Lead LFCSP (10mm x 10mm w/ EP) | CP-84-2        |

<sup>1</sup> Z = RoHS Compliant Part.