SBAS235H – DECEMBER 2001 – REVISED OCTOBER 2013

24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS NO MISSING CODES
- SIMULTANEOUS 50Hz AND 60Hz REJECTION (–90dB MINIMUM)
- 0.0015% INL
- 21 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- PGA GAINS FROM 1 TO 128
- SINGLE-CYCLE SETTLING
- PROGRAMMABLE DATA OUTPUT RATES
- EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 5V
- ON-CHIP CALIBRATION
- SPI™ COMPATIBLE
- 2.7V TO 5.25V SUPPLY RANGE
- 600μW POWER CONSUMPTION
- UP TO EIGHT INPUT CHANNELS
- UP TO EIGHT DATA I/O

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION
- WEIGHT SCALES

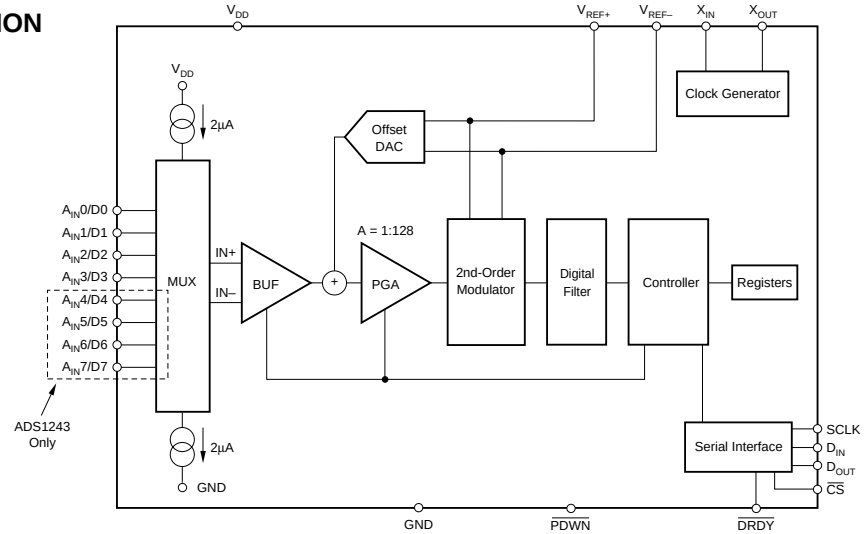
DESCRIPTION

The ADS1242 and ADS1243 are precision, wide dynamic range, delta-sigma, analog-to-digital (A/D) converters with 24-bit resolution operating from 2.7V to 5.25V supplies. These delta-sigma, A/D converters provide up to 24 bits of no missing code performance and effective resolution of 21 bits.

The input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burn-out current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit digital-to-analog converter (DAC) provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The Programmable Gain Amplifier (PGA) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable FIR filter that provides a simultaneous 50Hz and 60Hz notch. The reference input is differential and can be used for ratiometric conversion.

The serial interface is SPI compatible. Up to eight bits of data I/O are also provided that can be used for input or output. The ADS1242 and ADS1243 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.



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ABSOLUTE MAXIMUM RATINGS(1)

V_{DD} to GND	–0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
A_{IN}	GND – 0.5V to V_{DD} + 0.5V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–60°C to +100°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DIGITAL CHARACTERISTICS: T_{MIN} to T_{MAX}, V_{DD} 2.7V to 5.25V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input/Output					
Logic Family			CMOS		
Logic Level: V_{IH}		0.8 • V_{DD}		V_{DD}	V
V_{IL}(1)		GND		0.2 • V_{DD}	V
V_{OH}	I_{OH} = 1mA	V_{DD} – 0.4			V
V_{OL}	I_{OL} = 1mA	GND		GND + 0.4	V
Input Leakage: I_{IH}	$V_I = V_{DD}$			10	µA
I_{IL}	V_I = 0	–10			µA
Master Clock Rate: f_{OSC}		1		5	MHz
Master Clock Period: t_{OSC}	$1/f_{OSC}$	200		1000	ns

NOTE: (1) V_{IL} for X_{IN} is GND to GND + 0.05V.

ELECTRICAL CHARACTERISTICS: V_{DD} = 5V

All specifications T_{MIN} to T_{MAX}, V_{DD} = +5V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, f_{DATA} = 15Hz, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1242 ADS1243 MIN	TYP	MAX	UNITS
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$)					
Analog Input Range	Buffer OFF	GND – 0.1		V_{DD} + 0.1	V
	Buffer ON	GND + 0.05		V_{DD} – 1.5	V
Full-Scale Input Range	(In+) – (In–), See Block Diagram, RANGE = 0			$\pm V_{REF}$/PGA	V
	RANGE = 1			$\pm V_{REF}$/(2 • PGA)	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
	Buffer ON		5		GΩ
Bandwidth					
f_{DATA} = 3.75Hz	–3dB		1.65		Hz
f_{DATA} = 7.50Hz	–3dB		3.44		Hz
f_{DATA} = 15.00Hz	–3dB		14.6		Hz
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		µA
OFFSET DAC					
Offset DAC Range	RANGE = 0		$\pm V_{REF}$/(2 • PGA)		V
	RANGE = 1		$\pm V_{REF}$/(4 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±10		%
Offset DAC Gain Error Drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution	No Missing Codes	24			Bits
Integral Nonlinearity	End Point Fit			±0.0015	% of FS
Offset Error(1)			7.5		ppm of FS
Offset Drift(1)			0.02		ppm of FS/°C
Gain Error(1)			0.005		%
Gain Error Drift(1)			0.5		ppm/°C
Common-Mode Rejection	at DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 15Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
Normal-Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 15Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 15Hz		100		dB
Output Noise			See Typical Characteristics		
Power-Supply Rejection	at DC, dB = –20 log($\Delta V_{OUT}/V_{DD}$)(2)	80	95		dB
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN–	0		V_{DD}	V
V_{REF}	$V_{REF} \equiv$ (REF IN+) – (REF IN–), RANGE = 0	0.1	2.5	2.6	V
	RANGE = 1	0.1		V_{DD}	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	f_{VREFCM} = 60Hz, f_{DATA} = 15Hz		120		dB
Bias Current(3)	V_{REF} = 2.5V		1.3		µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	V_{DD}	4.75		5.25	V
Current	PGA = 1, Buffer OFF		240	375	µA
	PGA = 128, Buffer OFF		450	800	µA
	PGA = 1, Buffer ON		290	425	µA
	PGA = 128, Buffer ON		960	1400	µA
	SLEEP Mode		60		µA
	Read Data Continuous Mode		230		µA
	$\overline{PDWN}$		0.5		nA
Power Dissipation	PGA = 1, Buffer OFF		1.2	1.9	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Calibration can minimize these errors.
(2) ΔV_{OUT} is a change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: V_{DD} = 3V

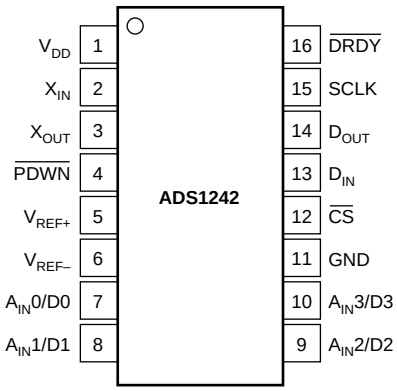
All specifications T_{MIN} to T_{MAX}, V_{DD} = +3V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, f_{DATA} = 15Hz, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +1.25V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1242 ADS1243 MIN	TYP	MAX	UNITS
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$)					
Analog Input Range	Buffer OFF	GND – 0.1		V_{DD} + 0.1	V
	Buffer ON	GND + 0.05		V_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Block Diagram, RANGE = 0			$\pm V_{REF}$/PGA	V
	RANGE = 1			$\pm V_{REF}$/(2 • PGA)	V
Input Impedance	Buffer OFF		5/PGA		MΩ
	Buffer ON		5		GΩ
Bandwidth					
f_{DATA} = 3.75Hz	–3dB		1.65		Hz
f_{DATA} = 7.50Hz	–3dB		3.44		Hz
f_{DATA} = 15.00Hz	–3dB		14.6		Hz
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		µA
OFFSET DAC					
Offset DAC Range	RANGE = 0		$\pm V_{REF}$/(2 • PGA)		V
	RANGE = 1		$\pm V_{REF}$/(4 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±10		%
Offset DAC Gain Error Drift			2		ppm/°C
SYSTEM PERFORMANCE					
Resolution	No Missing Codes	24			Bits
Integral Nonlinearity	End Point Fit			±0.0015	% of FS
Offset Error[1]			15		ppm of FS
Offset Drift[1]			0.04		ppm of FS/°C
Gain Error[1]			0.01		%
Gain Error Drift[1]			1.0		ppm/°C
Common-Mode Rejection	at DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 15Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
Normal-Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 15Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 15Hz		100		dB
Output Noise			See Typical Characteristics		
Power-Supply Rejection	at DC, dB = –20 log($\Delta V_{OUT}/V_{DD}$)[2]	75	90		dB
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN–	0		V_{DD}	V
V_{REF}	$V_{REF} \equiv$ (REF IN+) – (REF IN–), RANGE = 0	0.1	1.25	1.30	V
	RANGE = 1	0.1	2.5	2.6	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	f_{VREFCM} = 60Hz, f_{DATA} = 15Hz		120		dB
Bias Current[3]	V_{REF} = 1.25		0.65		µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	V_{DD}	2.7		3.3	V
Current	PGA = 1, Buffer OFF		190	375	µA
	PGA = 128, Buffer OFF		460	700	µA
	PGA = 1, Buffer ON		240	375	µA
	PGA = 128, Buffer ON		870	1325	µA
	SLEEP Mode		75		µA
	Read Data Continuous Mode		113		µA
	$\overline{PDWN}$ = 0		0.5		nA
Power Dissipation	PGA = 1, Buffer OFF		0.6	1.2	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Calibration can minimize these errors.
(2) ΔV_{OUT} is a change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

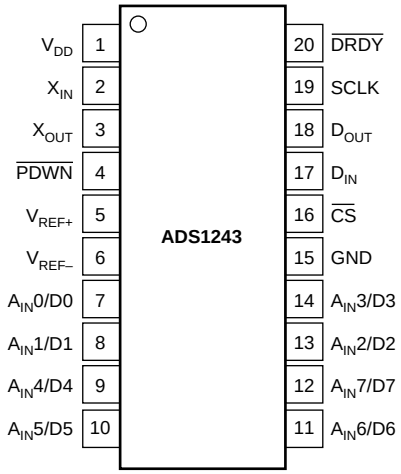
PIN CONFIGURATION (ADS1242)

Top View TSSOP



PIN CONFIGURATION (ADS1243)

Top View TSSOP



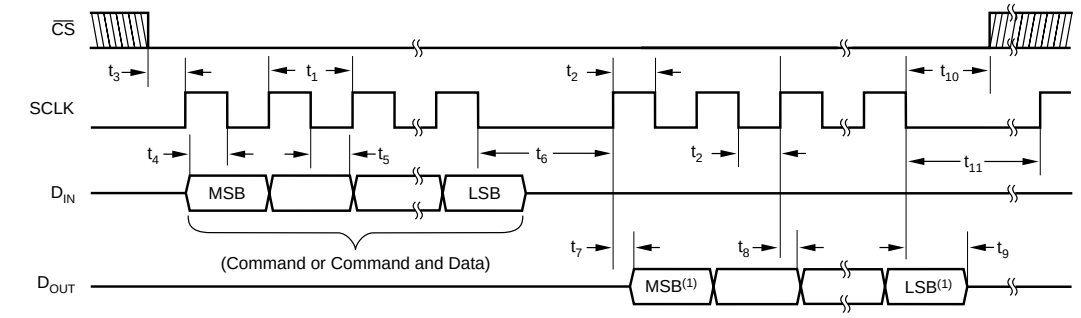
PIN DESCRIPTIONS (ADS1242)

PIN NUMBER	NAME	DESCRIPTION
1	V_{DD}	Power Supply
2	X_{IN}	Clock Input
3	X_{OUT}	Clock Output, used with crystal or ceramic resonator.
4	$\overline{PDWN}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
5	V_{REF+}	Positive Differential Reference Input
6	V_{REF-}	Negative Differential Reference Input
7	$A_{IN}0/D0$	Analog Input 0/Data I/O 0
8	$A_{IN}1/D1$	Analog Input 1/Data I/O 1
9	$A_{IN}2/D2$	Analog Input 2/Data I/O 2
10	$A_{IN}3/D3$	Analog Input 3/Data I/O 3
11	GND	Ground
12	$\overline{CS}$	Active LOW, Chip Select
13	D_{IN}	Serial Data Input, Schmitt Trigger
14	D_{OUT}	Serial Data Output
15	SCLK	Serial Clock, Schmitt Trigger
16	$\overline{DRDY}$	Active LOW, Data Ready

PIN DESCRIPTIONS (ADS1243)

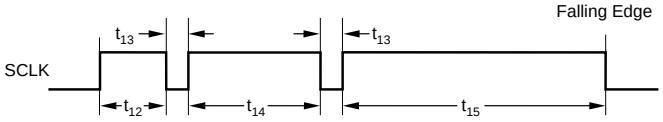
PIN NUMBER	NAME	DESCRIPTION
1	V_{DD}	Power Supply
2	X_{IN}	Clock Input
3	X_{OUT}	Clock Output, used with crystal or ceramic resonator.
4	$\overline{PDWN}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
5	V_{REF+}	Positive Differential Reference Input
6	V_{REF-}	Negative Differential Reference Input
7	$A_{IN}0/D0$	Analog Input 0/Data I/O 0
8	$A_{IN}1/D1$	Analog Input 1/Data I/O 1
9	$A_{IN}4/D4$	Analog Input 4/Data I/O 4
10	$A_{IN}5/D5$	Analog Input 5/Data I/O 5
11	$A_{IN}6/D6$	Analog Input 6/Data I/O 6
12	$A_{IN}7/D7$	Analog Input 7/Data I/O 7
13	$A_{IN}2/D2$	Analog Input 2/Data I/O 2
14	$A_{IN}3/D3$	Analog Input 3/Data I/O 3
15	GND	Ground
16	$\overline{CS}$	Active LOW, Chip Select
17	D_{IN}	Serial Data Input, Schmitt Trigger
18	D_{OUT}	Serial Data Output
19	SCLK	Serial Clock, Schmitt Trigger
20	$\overline{DRDY}$	Active LOW, Data Ready

TIMING DIAGRAMS



NOTE: (1) Bit order = 0.

SCLK Reset Waveform



ADS1242 or ADS1243
Resets On
Falling Edge

$300 \cdot t_{OSC} < t_{12} < 500 \cdot t_{OSC}$
$t_{13} : > 5 \cdot t_{OSC}$
$550 \cdot t_{OSC} < t_{14} < 750 \cdot t_{OSC}$
$1050 \cdot t_{OSC} < t_{15} < 1250 \cdot t_{OSC}$

DIAGRAM 1.

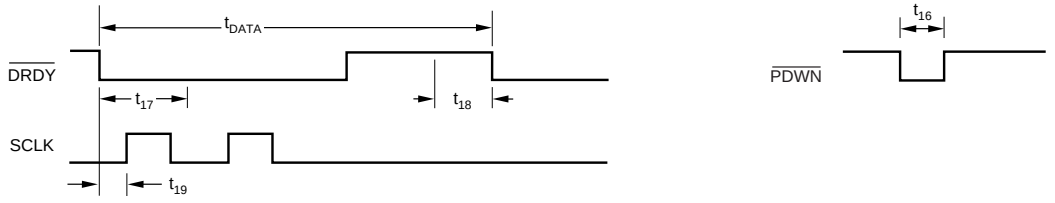


DIAGRAM 2.

TIMING CHARACTERISTICS TABLE

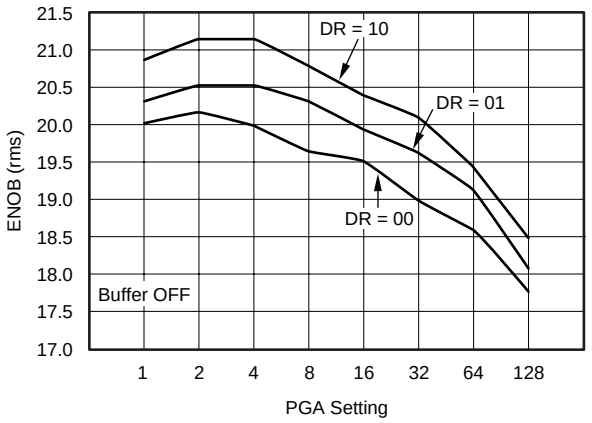
SPEC	DESCRIPTION	MIN	MAX	UNITS
t_1	SCLK Period	4		t_{OSC} Periods
			3	$\overline{DRDY}$ Periods
t_2	SCLK Pulse Width, HIGH and LOW	200		ns
t_3	$\overline{CS}$ low to first SCLK Edge; Setup Time(2)	0		ns
t_4	D_{IN} Valid to SCLK Edge; Setup Time	50		ns
t_5	Valid D_{IN} to SCLK Edge; Hold Time	50		ns
t_6	Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT}:			
	RDATA, RDATAC, RREG, WREG	50		t_{OSC} Periods
t_7(1)	SCLK Edge to Valid New D_{OUT}		50	ns
t_8(1)	SCLK Edge to D_{OUT}, Hold Time	0		ns
t_9	Last SCLK Edge to D_{OUT} Tri-State	6	10	t_{OSC} Periods
	NOTE: D_{OUT} goes tri-state immediately when $\overline{CS}$ goes HIGH.			
t_{10}	$\overline{CS}$ LOW time after final SCLK edge.			
	Read from the device	0		t_{OSC} Periods
	Write to the device	8		t_{OSC} Periods
t_{11}	Final SCLK edge of one command until first edge SCLK of next command:			
	RREG, WREG, DSYNC, SLEEP, RDATA, RDATAC, STOPC	4		t_{OSC} Periods
	SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL	2		$\overline{DRDY}$ Periods
	SELFCAL	4		$\overline{DRDY}$ Periods
	RESET (also SCLK Reset)	16		t_{OSC} Periods
t_{16}	Pulse Width	4		t_{OSC} Periods
t_{17}	Allowed analog input change for next valid conversion.		5000	t_{OSC} Periods
t_{18}	DOR update, DOR data not valid.	4		t_{OSC} Periods
t_{19}	First SCLK after DRDY goes LOW:			
	RDATAC Mode	10		t_{OSC} Periods
	Any other mode	0		t_{OSC} Periods

NOTES: (1) Load = 20pF ||10kΩ to GND.
(2) $\overline{CS}$ may be tied LOW.

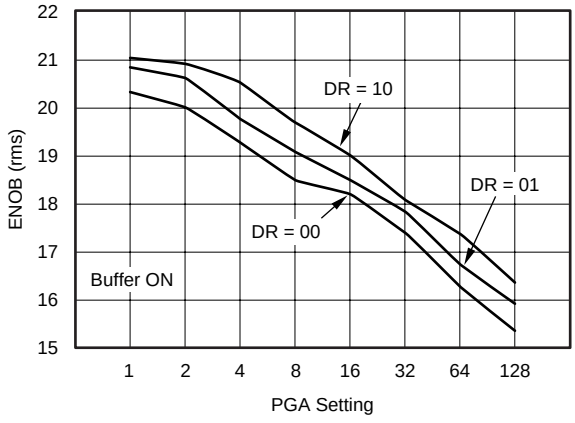
TYPICAL CHARACTERISTICS

All specifications V_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, f_{DATA} = 15Hz, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

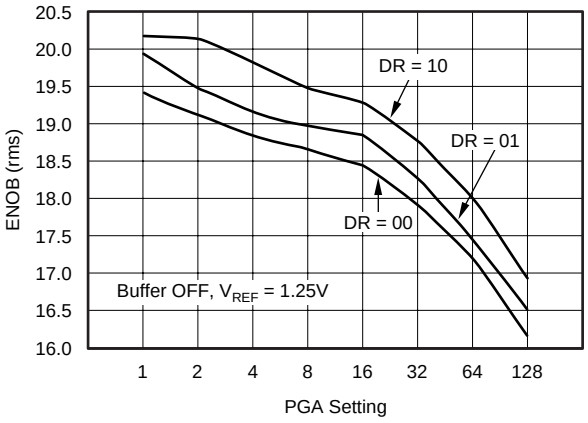
EFFECTIVE NUMBER OF BITS vs PGA SETTING



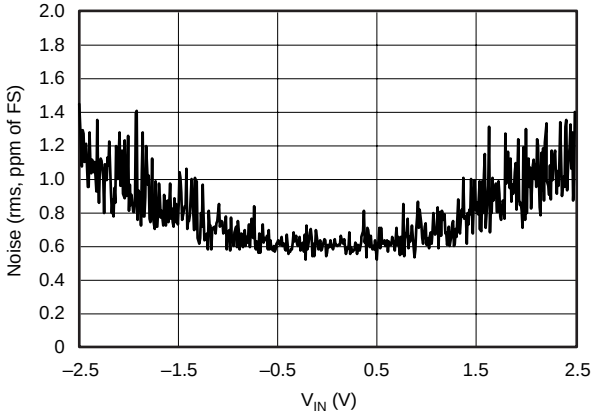
EFFECTIVE NUMBER OF BITS vs PGA SETTING



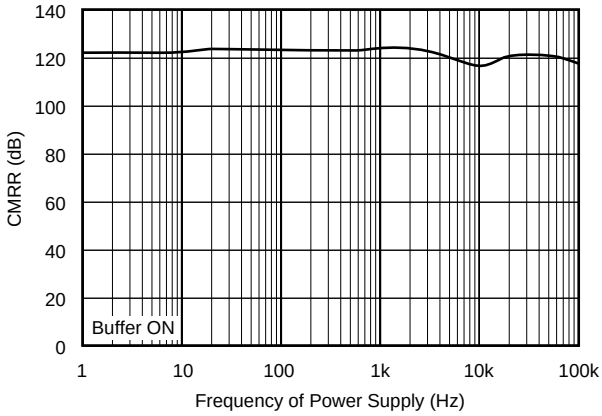
EFFECTIVE NUMBER OF BITS vs PGA SETTING



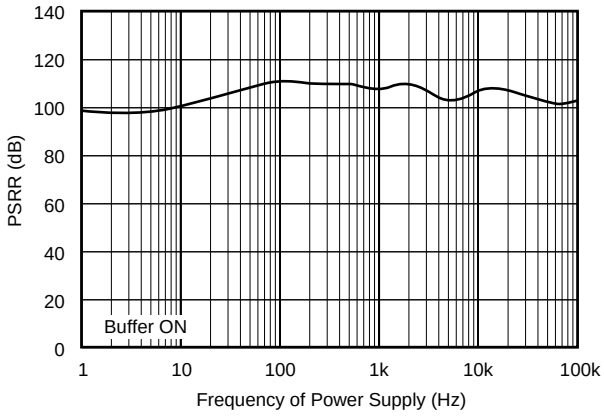
NOISE vs INPUT SIGNAL



COMMON-MODE REJECTION RATIO vs FREQUENCY



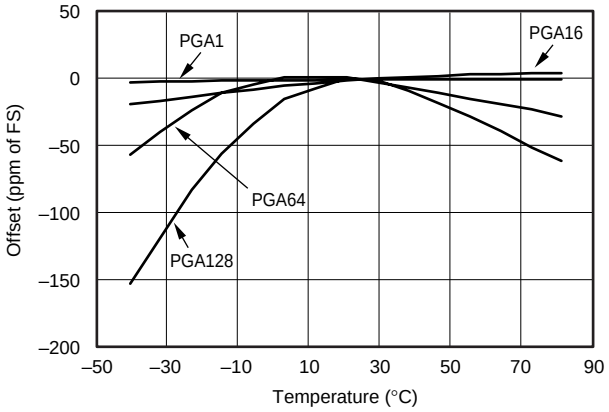
POWER SUPPLY REJECTION RATIO vs FREQUENCY



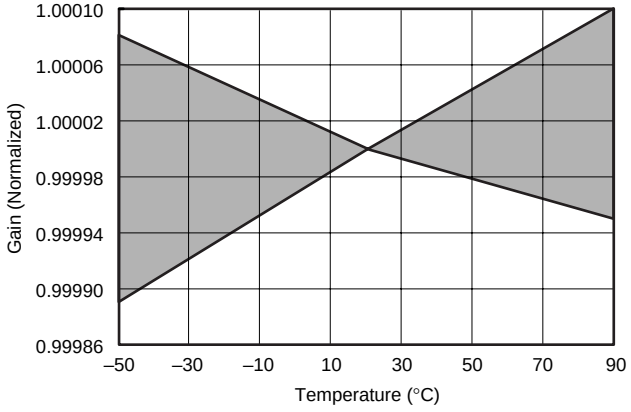
TYPICAL CHARACTERISTICS (Cont.)

All specification V_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, f_{DATA} = 15Hz, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

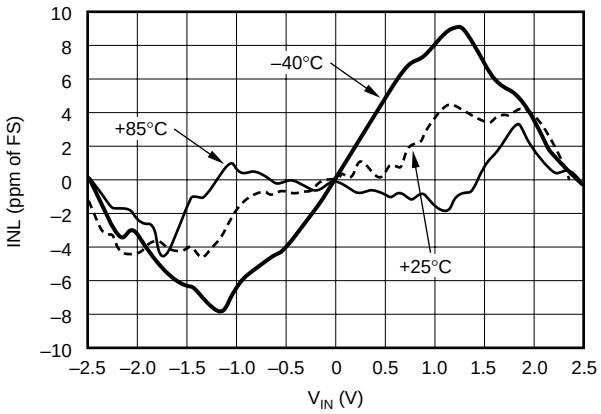
OFFSET vs TEMPERATURE
(Cal at 25°C)



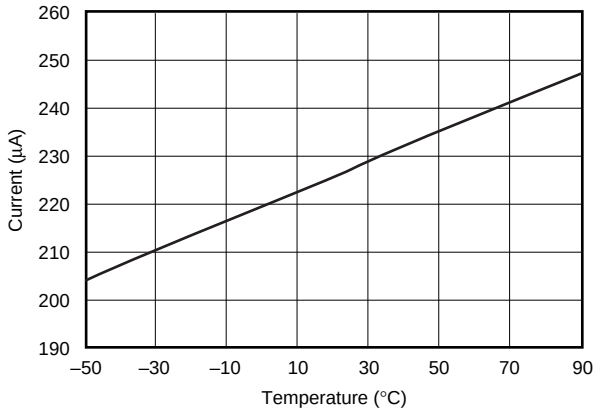
GAIN vs TEMPERATURE
(Cal at 25°C)



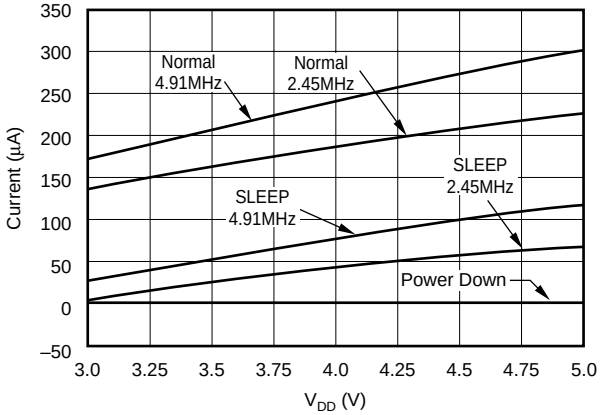
INTEGRAL NONLINEARITY vs INPUT SIGNAL



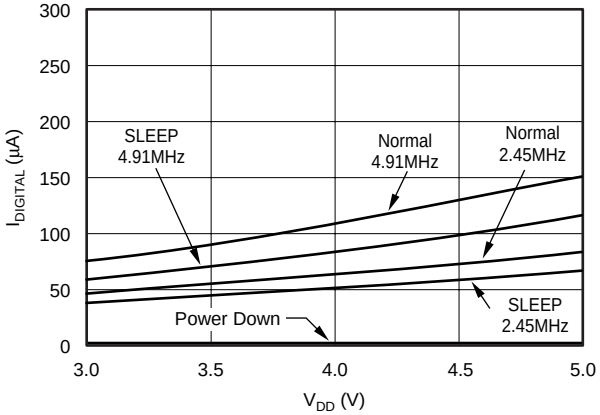
CURRENT vs TEMPERATURE
(Buffer Off)



CURRENT vs VOLTAGE



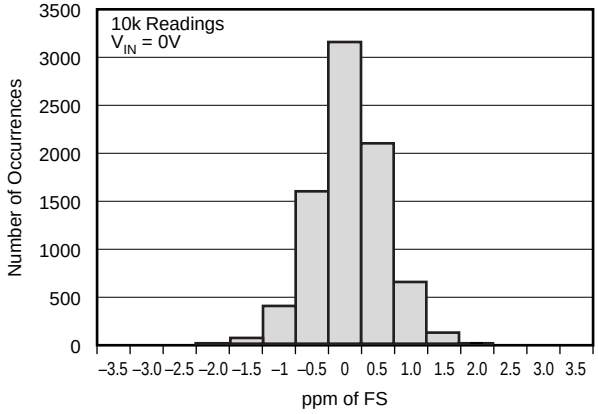
SUPPLY CURRENT vs SUPPLY



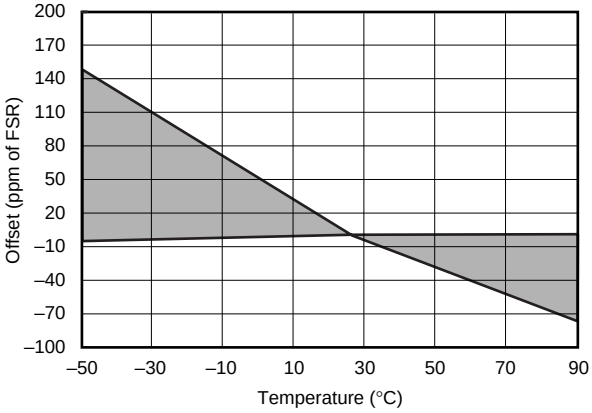
TYPICAL CHARACTERISTICS (Cont.)

All specification V_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, f_{DATA} = 15Hz, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

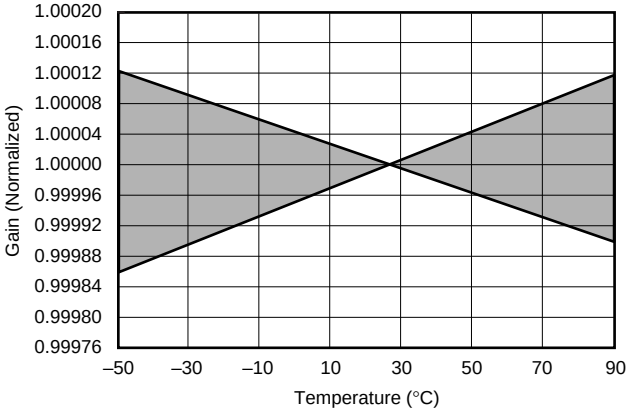
NOISE HISTOGRAM



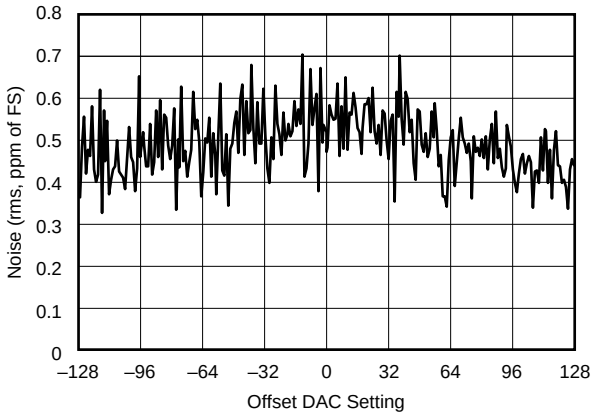
OFFSET DAC
OFFSET vs TEMPERATURE
(Cal at 25°C)



OFFSET DAC
GAIN vs TEMPERATURE
(Cal at 25°C)



OFFSET DAC
NOISE vs SETTING



OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. For example, if $A_{IN}0$ is selected as the positive differential input channel, any other channel can be selected as the negative terminal for the differential input channel. With this method, it is possible to have up to seven single-ended input channels or four independent differential input channels for the ADS1243, and three single-ended input channels or two independent differential input channels for the ADS1242.

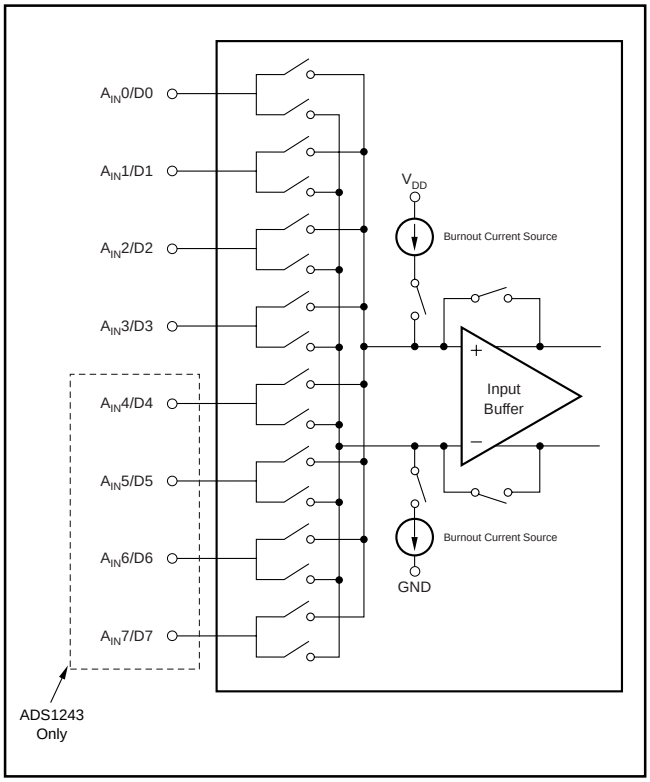


FIGURE 1. Input Multiplexer Configuration.

The ADS1242 and ADS1243 feature a single-cycle settling digital filter that provides valid data on the first conversion after a new channel selection. In order to minimize the settling error, synchronize MUX changes to the conversion beginning, which is indicated by the falling edge of $\overline{DRDY}$. In other words, issuing a MUX change through the WREG command immediately after $\overline{DRDY}$ goes LOW minimizes the settling error. Increasing the time between the conversion beginning ($\overline{DRDY}$ goes LOW) and the MUX change command (t_{DELAY}) results in a settling error in the conversion data, as shown in Figure 2.

BURNOUT CURRENT SOURCES

The Burnout Current Sources can be used to detect sensor short-circuit or open-circuit conditions. Setting the Burnout Current Sources (BOCS) bit in the SETUP register activates two 2µA current sources called burnout current sources. One of the current sources is connected to the converter's negative input and the other is connected to the converter's positive input.

Figure 3 shows the situation for an open-circuit sensor. This is a potential failure mode for many kinds of remotely connected sensors. The current source on the positive input acts as a pull-up, causing the positive input to go to the positive analog supply, and the current source on the negative input acts as a pull-down, causing the negative input to go to ground. The ADS1242/43 therefore outputs full-scale (7FFFFF Hex).

Figure 4 shows a short-circuited sensor. Since the inputs are

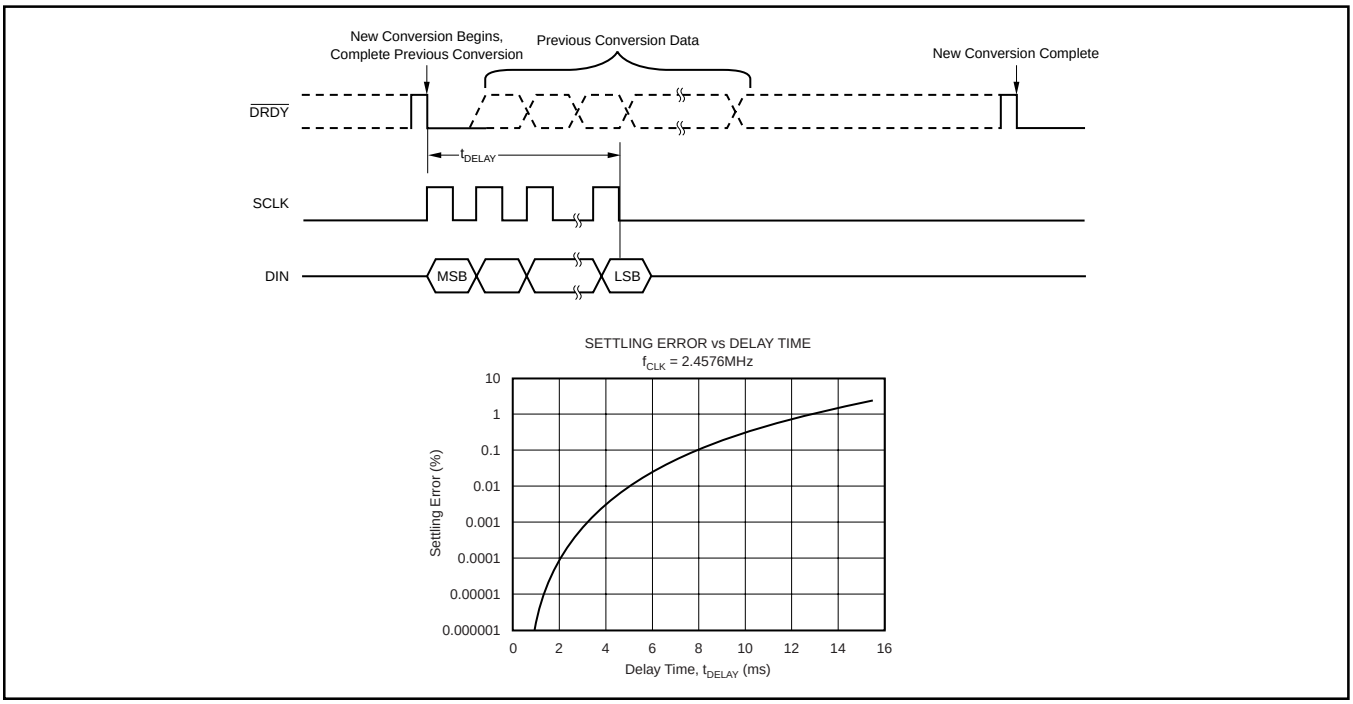


FIGURE 2. Input Multiplexer Configuration.

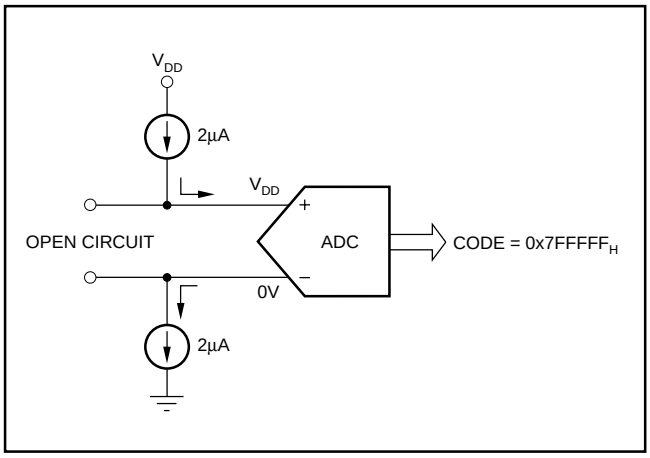


FIGURE 3. Burnout detection while sensor is open-circuited.

shorted and at the same potential, the ADS1242/43 signal outputs are approximately zero. (Note that the code for shorted inputs is not exactly zero due to internal series resistance, low-level noise and other error sources.)

INPUT BUFFER

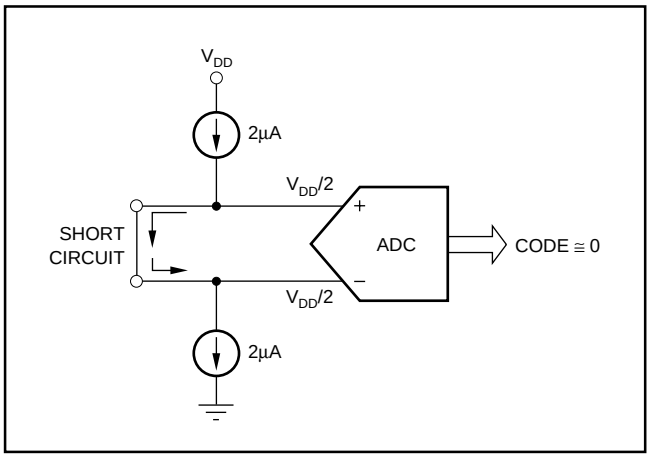


FIGURE 4. Burnout detection while sensor is short-circuited.

The input impedance of the ADS1242/43 without the buffer enabled is approximately 5MΩ/PGA. For systems requiring very high input impedance, the ADS1242/43 provides a chopper-stabilized differential FET-input voltage buffer. When activated, the buffer raises the ADS1242/43 input impedance to approximately 5GΩ.

The buffer's input range is approximately 50mV to V_{DD} – 1.5V. The buffer's linearity will degrade beyond this range. Differential signals should be adjusted so that both signals are within the buffer's input range.

The buffer can be enabled using the BUFEN pin or the BUFEN bit in the ACR register. The buffer is on when the BUFEN pin is high and the BUFEN bit is set to one. If the BUFEN pin is low, the buffer is disabled. If the BUFEN bit is set to zero, the buffer is also disabled.

The buffer draws additional current when activated. The current required by the buffer depends on the PGA setting. When the PGA is set to 1, the buffer uses approximately 50µA; when the PGA is set to 128, the buffer uses approximately 500µA.

PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale signal, the A/D converter can resolve down to 1µV. With a PGA of 128 and a full-scale signal of 39mV, the A/D converter can resolve down to 75nV. V_{DD} current increases with PGA settings higher than 4.

OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA using the Offset DAC (ODAC) register. The ODAC register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the offset DAC does not reduce the performance of the A/D converter. For more details on the ODAC in the ADS1242/43, please refer to TI application report SBAA077 (available through the TI website).

MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the SETUP register, as shown in Table I.

f_{OSC}	SPEED BIT	f_{MOD}	DR BITS 00	DR BITS 01	DR BITS 10	1st NOTCH FREQ.
2.4576MHz	0	19,200Hz	15Hz	7.5Hz	3.75Hz	50/60Hz
	1	9,600Hz	7.5Hz	3.75Hz	1.875Hz	25/30Hz
4.9152MHz	0	38,400Hz	30Hz	15Hz	7.5Hz	100/120Hz
	1	19,200Hz	15Hz	7.5Hz	3.75Hz	50/60Hz

TABLE I. Output Configuration.

CALIBRATION

The offset and gain errors can be minimized with calibration. The ADS1242 and ADS1243 support both self and system calibration.

Self-calibration of the ADS1242 and ADS1243 corrects internal offset and gain errors and is handled by three commands: SELFCAL, SELFGAL, and SELFOCAL. The SELFCAL command performs both an offset and gain calibration. SELFGCAL performs a gain calibration and SELFOCAL performs an offset calibration, each of which takes two t_{DATA} periods to complete. During self-calibration, the ADC inputs are disconnected internally from the input pins. The PGA must be set to 1 prior to issuing a SELFCAL or SELFGCAL command. Any PGA is allowed when issuing a SELFOCAL command. For

example, if using PGA = 64, first set PGA = 1 and issue SELFGCAL. Afterwards, set PGA = 64 and issue SELFOCAL. For operation with a reference voltage greater than (V_{DD} – 1.5) volts, the buffer must also be turned off during gain self-calibration to avoid exceeding the buffer input range.

System calibration corrects both internal and external offset and gain errors. While performing system calibration, the appropriate signal must be applied to the inputs. The system offset calibration command (SYSOCAL) requires a zero input differential signal (see Table IV, page 18). It then computes the offset that nullifies the offset in the system. The system gain calibration command (SYSGCAL) requires a positive full-scale input signal. It then computes a value to nullify the gain error in the system. Each of these calibrations takes two t_{DATA} periods to complete. System gain calibration is recommended for the best gain calibration at higher PGAs.

Calibration should be performed after power on, a change in temperature, or a change of the PGA. The RANGE bit (ACR bit 2) must be zero during calibration.

Calibration removes the effects of the ODAC; therefore, disable the ODAC during calibration, and enable again after calibration is complete.

At the completion of calibration, the $\overline{DRDY}$ signal goes low, indicating the calibration is finished. The first data after calibration should be discarded since it may be corrupt from calibration data remaining in the filter. The second data is always valid.

EXTERNAL VOLTAGE REFERENCE

The ADS1242 and ADS1243 require an external voltage reference. The selection for the voltage reference value is made through the ACR register.

The external voltage reference is differential and is represented by the voltage difference between the pins: $+V_{REF}$ and $–V_{REF}$. The absolute voltage on either pin, $+V_{REF}$ or $–V_{REF,}$ can range from GND to V_{DD}. However, the following limitations apply:

For V_{DD} = 5.0V and RANGE = 0 in the ACR, the differential V_{REF} must not exceed 2.5V.

For V_{DD} = 5.0V and RANGE = 1 in the ACR, the differential V_{REF} must not exceed 5V.

For V_{DD} = 3.0V and RANGE = 0 in the ACR, the differential V_{REF} must not exceed 1.25V.

For V_{DD} = 3.0V and RANGE = 1 in the ACR, the differential V_{REF} must not exceed 2.5V.

CLOCK GENERATOR

The clock source for the ADS1242 and ADS1243 can be provided from a crystal, oscillator, or external clock. When the clock source is a crystal, external capacitors must be provided to ensure start-up and stable clock frequency. This is shown in both Figure 5 and Table II. X_{OUT} is only for use with external crystals and it should not be used as a clock driver for external circuitry.

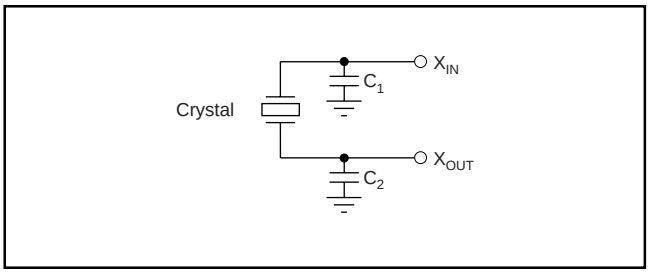


FIGURE 5. Crystal Connection.

CLOCK SOURCE	FREQUENCY	C_1	C_2	PART NUMBER
Crystal	2.4576	0-20pF	0-20pF	ECS, ECSD 2.45 - 32
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSL 4.91
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSD 4.91
Crystal	4.9152	0-20pF	0-20pF	CTS, MP 042 4M9182

TABLE II. Recommended Crystals.

DIGITAL FILTER

The ADS1242 and ADS1243 have a 1279 tap linear phase Finite Impulse Response (FIR) digital filter that a user can configure for various output data rates. When a 2.4576MHz crystal is used, the device can be programmed for an output data rate of 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference. Figure 6 shows the digital filter frequency response for data output rates of 15Hz, 7.5Hz, and 3.75Hz.

If a different data output rate is desired, a different crystal frequency can be used. However, the rejection frequencies shift accordingly. For example, a 3.6864MHz master clock with the default register condition has:

(3.6864MHz/2.4576MHz) • 15Hz = 22.5Hz data output rate

and the first and second notch is:

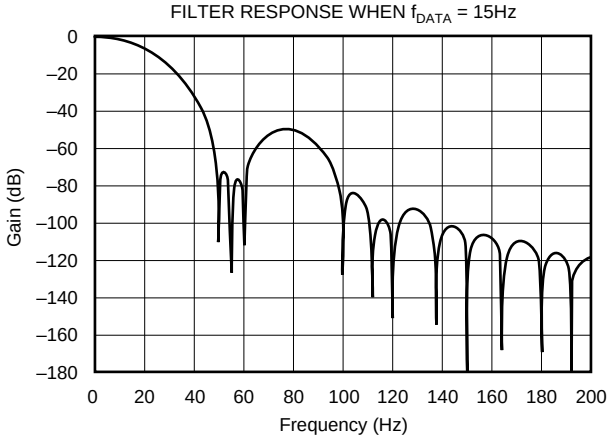
1.5 • (50Hz and 60Hz) = 75Hz and 90Hz

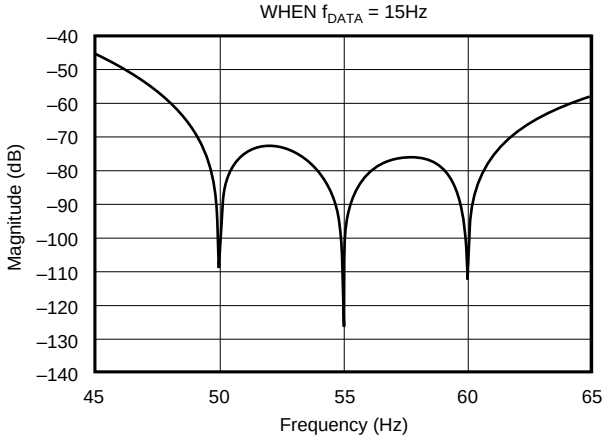
DATA I/O INTERFACE

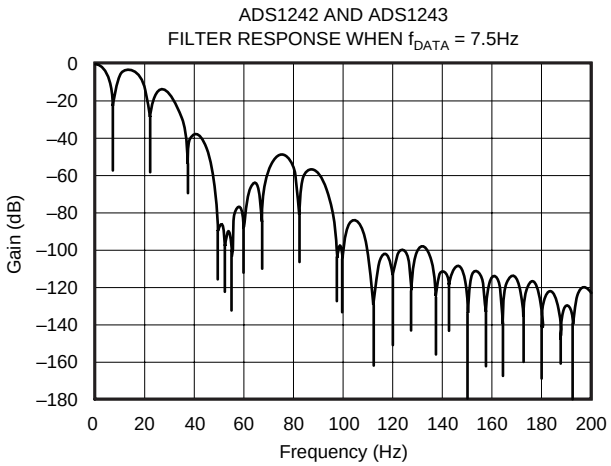
The ADS1242 has four pins and the ADS1243 has eight pins that serve a dual purpose as both analog inputs and data I/O. These pins are configured through the IOCON, DIR, and DIO registers and can be individually configured as either analog inputs or data I/O. See Figure 7 (page 14) for the equivalent schematic of an Analog/Data I/O pin.

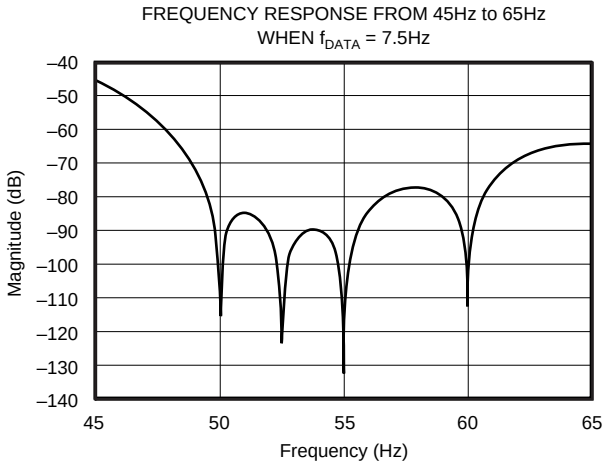
The IOCON register defines the pin as either an analog input or data I/O. The power-up state is an analog input. If the pin is configured as an analog input in the IOCON register, the DIR and DIO registers have no effect on the state of the pin.

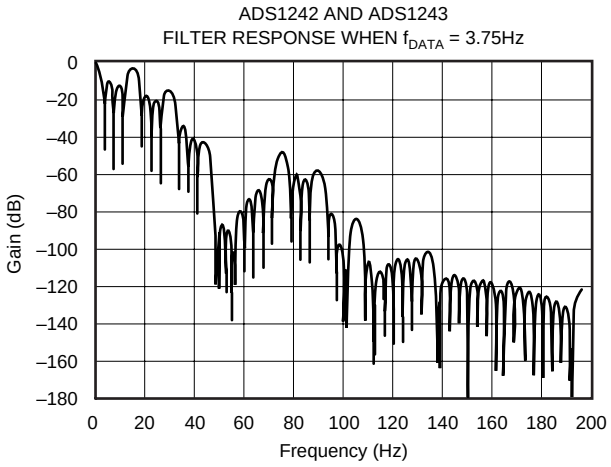
If the pin is configured as data I/O in the IOCON register, then DIR and DIO are used to control the state of the pin. The DIR register controls the direction of the data pin, either as an input or output. If the pin is configured as an input in the DIR register, then the corresponding DIO register bit reflects the state of the pin. Make sure the pin is driven to a logic one or zero when configured as an input to prevent

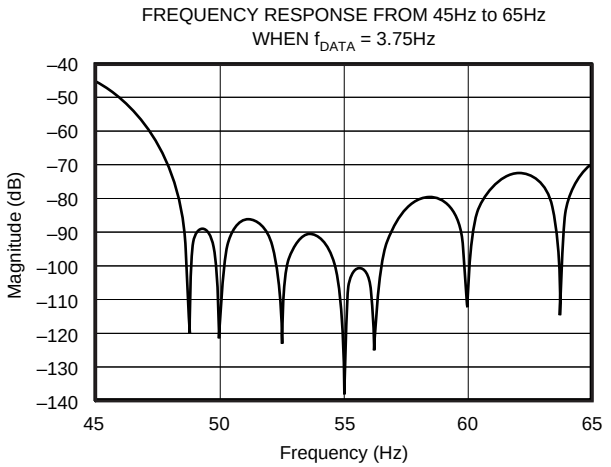












f_{OSC} = 2.4576MHz, SPEED = 0 or f_{OSC} = 4.9152MHz, SPEED = 1

DATA OUTPUT RATE	–3dB BANDWIDTH	ATTENUATION			
		f_{IN} = 50 ±0.3Hz	f_{IN} = 60 ±0.3Hz	f_{IN} = 50 ±1Hz	f_{IN} = 60 ±1Hz
15Hz	14.6Hz	–80.8dB	–87.3dB	–68.5dB	–76.1dB
7.5Hz	3.44Hz	–85.9dB	–87.4dB	–71.5dB	–76.2dB
3.75Hz	1.65Hz	–93.8dB	–88.6dB	–86.8dB	–77.3dB

FIGURE 6. Filter Frequency Responses.

excess current dissipation. If the pin is configured as an output in the DIR register, then the corresponding DIO register bit value determines the state of the output pin (0 = GND, 1 = V_{DD}).

It is still possible to perform A/D conversions on a pin configured as data I/O. This may be useful as a test mode, where the data I/O pin is driven and an A/D conversion is done on the pin.

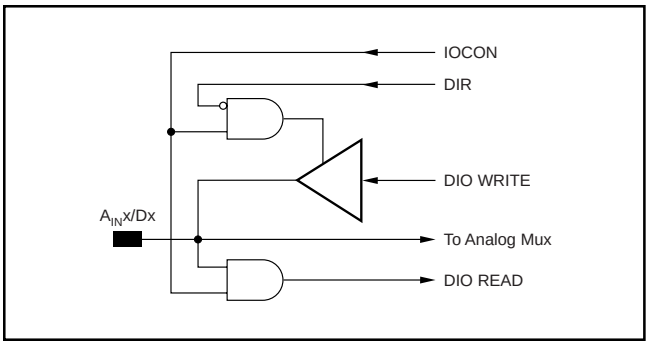


FIGURE 7. Analog/Data Interface Pin.

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) allows a controller to communicate synchronously with the ADS1242 and ADS1243. The ADS1242 and ADS1243 operate in slave-only mode. The serial interface is a standard four-wire SPI ($\overline{CS}$, SCLK, D_{IN} and D_{OUT}) interface.

Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input must be externally asserted before communicating with the ADS1242 or ADS1243. $\overline{CS}$ must stay LOW for the duration of the communication. Whenever $\overline{CS}$ goes HIGH, the serial interface is reset. $\overline{CS}$ may be hard-wired LOW.

Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock D_{IN} and D_{OUT} data. Make sure to have a clean SCLK to prevent accidental double-shifting of the data. If SCLK is not toggled within three $\overline{DRDY}$ pulses, the serial interface resets on the next SCLK pulse and starts a new communication cycle. A special pattern on SCLK resets the entire chip; see the RESET section for additional information.

Data Input (D_{IN}) and Data Output (D_{OUT})

The data input (D_{IN}) and data output (D_{OUT}) receive and send data from the ADS1242 and ADS1243. D_{OUT} is high impedance when not in use to allow D_{IN} and D_{OUT} to be connected together and driven by a bidirectional bus. Note: the Read Data Continuous Mode (RDATAC) command should not be issued when D_{IN} and D_{OUT} are connected. While in RDATAC mode, D_{IN} looks for the STOPC or RESET command. If either of these 8-bit bytes appear on D_{OUT} (which is connected to D_{IN}), the RDATAC mode ends.

DATA READY ($\overline{DRDY}$) PIN

The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the internal data register. $\overline{DRDY}$ goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

The status of $\overline{DRDY}$ can also be obtained by interrogating bit 7 of the ACR register (address 2_H). The serial interface can operate in 3-wire mode by tying the $\overline{CS}$ input LOW. In this case, the SCLK, D_{IN}, and D_{OUT} lines are used to communicate with the ADS1242 and ADS1243. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit of the microcontroller.

DSYNC OPERATION

Synchronization can be achieved through the DSYNC command. When the DSYNC command is sent, the digital filter is reset on the edge of the last SCLK of the DSYNC command. The modulator is held in RESET until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK following the DSYNC command.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

ADS1242 AND ADS1243 REGISTERS

The operation of the device is set up through individual registers. Collectively, the registers contain all the information needed to configure the part, such as data format, multiplexer settings, calibration settings, data rate, etc. The 16 registers are shown in Table III.

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00_H	SETUP	ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0
01_H	MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02_H	ACR	$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0
03_H	ODAC	SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
04_H	DIO	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
05_H	DIR	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
06_H	IOCON	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
07_H	OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
08_H	OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
09_H	OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
$0A_H$	FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
$0B_H$	FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
$0C_H$	FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
$0D_H$	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
$0E_H$	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
$0F_H$	DOR0	DOR07	DOR16	FSR21	DOR04	DOR03	DOR02	DOR01	DOR00

TABLE III. Registers.

DETAILED REGISTER DEFINITIONS

SETUP (Address 00_H) Setup Register
Reset Value = iiii0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0

bit 7-4 Factory Programmed Bits

bit 3 BOCS: Burnout Current Source
0 = Disabled (default)
1 = Enabled

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX (Address 01_H) Multiplexer Control Register
Reset Value = 01_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select
0000 = $A_{IN}0$ (default)
0001 = $A_{IN}1$
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$
1111 = Reserved

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select
0000 = $A_{IN}0$
0001 = $A_{IN}1$ (default)
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$
1111 = Reserved

ACR (Address 02_H) Analog Control Register
Reset Value = $X0_H$

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0

bit 7 $\overline{DRDY}$: Data Ready (Read Only)
This bit duplicates the state of the $\overline{DRDY}$ pin.

bit 6 U/$\overline{B}$: Data Format
0 = Bipolar (default)
1 = Unipolar

U/$\overline{B}$	ANALOG INPUT	DIGITAL OUTPUT (Hex)
0	+FSR	0x7FFFFF
	Zero	0x000000
	–FSR	0x800000
1	+FSR	0xFFFFFF
	Zero	0x000000
	–FSR	0x000000

bit 5 SPEED: Modulator Clock Speed
0 = $f_{MOD} = f_{OSC}/128$ (default)
1 = $f_{MOD} = f_{OSC}/256$

bit 4 BUFEN: Buffer Enable
0 = Buffer Disabled (default)
1 = Buffer Enabled

bit 3 BIT ORDER: Data Output Bit Order
0 = Most Significant Bit Transmitted First (default)
1 = Least Significant Bit Transmitted First
Data is always shifted in or out MSB first.

bit 2 RANGE: Range Select
0 = Full-Scale Input Range equal to $\pm V_{REF}$ (default).
1 = Full-Scale Input Range equal to $\pm 1/2\ V_{REF}$
NOTE: This allows reference voltages as high as V_{DD}, but even with a 5V reference voltage the calibration must be performed with this bit set to 0.

bit 1-0 DR1: DR0: Data Rate
(f_{OSC} = 2.4576MHz, SPEED = 0)
00 = 15Hz (default)
01 = 7.5Hz
10 = 3.75Hz
11 = Reserved

ODAC (Address 03) Offset DAC
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

bit 7 Sign
0 = Positive
1 = Negative

$$\text{Offset} = \frac{V_{REF}}{2 \bullet \text{PGA}} \bullet \left(\frac{\text{OSET}[6:0]}{127} \right) \quad \text{RANGE} = 0$$

$$\text{Offset} = \frac{V_{REF}}{4 \bullet \text{PGA}} \bullet \left(\frac{\text{OSET}[6:0]}{127} \right) \quad \text{RANGE} = 1$$

NOTE: The offset DAC must be enabled after calibration or the calibration nullifies the effects.

DIO (Address 04_H) Data I/O
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIO 7	DIO 6	DIO 5	DIO 4	DIO 3	DIO 2	DIO 1	DIO 0

If the IOCON register is configured for data, a value written to this register appears on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register returns the value of the data I/O pins.

Bits 4 to 7 are not used in ADS1242.

DIR (Address 05_H) Direction Control for Data I/O
Reset Value = FF_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Each bit controls whether the corresponding data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

Bits 4 to 7 are not used in ADS1242.

IOCON (Address 06_H) I/O Configuration Register
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

bit 7-0 IO7: IO0: Data I/O Configuration
0 = Analog (default)
1 = Data

Configuring the pin as a data I/O pin allows it to be controlled through the DIO and DIR registers.

Bits 4 to 7 are not used in ADS1242.

OCR0 (Address 07_H) Offset Calibration Coefficient (Least Significant Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 (Address 08_H) Offset Calibration Coefficient (Middle Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 (Address 09_H) Offset Calibration Coefficient (Most Significant Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 (Address $0A_H$) Full-Scale Register (Least Significant Byte)
Reset Value = 59_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 (Address $0B_H$) Full-Scale Register (Middle Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2 (Address $0C_H$) Full-Scale Register (Most Significant Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DOR2 (Address $0D_H$) Data Output Register (Most Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16

DOR1 (Address $0E_H$) Data Output Register (Middle Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08

DOR0 (Address $0F_H$) Data Output Register (Least Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

ADS1242 AND ADS1243 CONTROL COMMAND DEFINITIONS

The commands listed in Table IV control the operations of the ADS1242 and ADS1243. Some of the commands are stand-alone commands (for example, RESET) while others require additional bytes (for example, WREG requires the count and data bytes).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

COMMANDS	DESCRIPTION	OP CODE	2nd COMMAND BYTE
RDATA	Read Data	0000 0001 (01_H)	—
RDATAC	Read Data Continuously	0000 0011 (03_H)	—
STOPC	Stop Read Data Continuously	0000 1111 ($0F_H$)	—
RREG	Read from REG "rrrr"	0001 r r r r ($1x_H$)	xxxx_nnnn (# of regs-1)
WREG	Write to REG "rrrr"	0101 r r r r ($5x_H$)	xxxx_nnnn (# of regs-1)
SELFCAL	Offset and Gain Self Cal	1111 0000 ($F0_H$)	—
SELFOCAL	Self Offset Cal	1111 0001 ($F1_H$)	—
SELFGCAL	Self Gain Cal	1111 0010 ($F2_H$)	—
SYSOCAL	Sys Offset Cal	1111 0011 ($F3_H$)	—
SYSGCAL	Sys GainCal	1111 0100 ($F4_H$)	—
WAKEUP	Wakup from SLEEP Mode	1111 1011 (FB_H)	—
DSYNC	Sync $\overline{DRDY}$	1111 1100 (FC_H)	—
SLEEP	Put in SLEEP Mode	1111 1101 (FD_H)	—
RESET	Reset to Power-Up Values	1111 1110 (FE_H)	—

NOTE: The received data format is always MSB first; the data out format is set by the BIT ORDER bit in the ACR register.

TABLE IV. Command Summary.

RDATA–Read Data

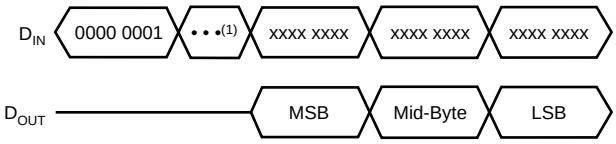
Description: Read the most recent conversion result from the Data Output Register (DOR). This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE: (1) For wait time, refer to timing specification.

RDATAC–Read Data Continuous

Description: Read Data Continuous mode enables the continuous output of new data on each $\overline{DRDY}$. This command eliminates the need to send the Read Data Command on each $\overline{DRDY}$. This mode may be terminated by either the STOPC command or the RESET command. Wait at least 10 f_{OSC} after $\overline{DRDY}$ falls before reading.

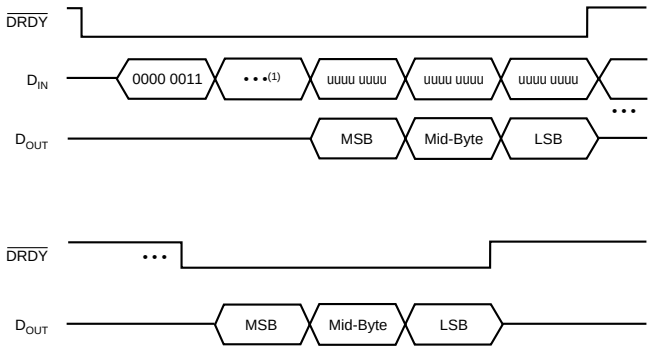
Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:

Command terminated when "uuuu uuuu" equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

STOPC–Stop Continuous

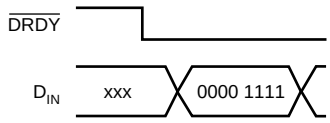
Description: Ends the continuous data output mode. Issue after $\overline{DRDY}$ goes LOW.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG–Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte count. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

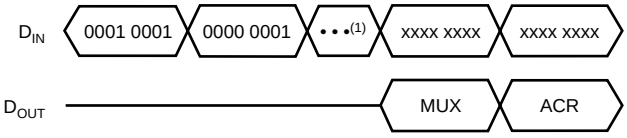
Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:

Read Two Registers Starting from Register 01_H (MUX)



NOTE: (1) For wait time, refer to timing specification.

WREG–Write to Registers

Description: Write to the registers starting with the register address specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

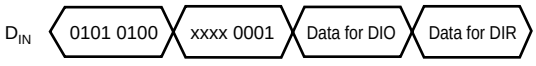
Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:

Write Two Registers Starting from 04_H (DIO)



SELFCAL–Offset and Gain Self Calibration

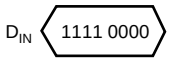
Description: Starts the process of self calibration. The Offset Calibration Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL–Offset Self Calibration

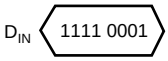
Description: Starts the process of self-calibration for offset. The Offset Calibration Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL–Gain Self Calibration

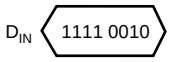
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL–System Offset Calibration

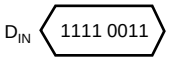
Description: Initiates a system offset calibration. The input should be set to 0V, and the ADS1242 and ADS1243 compute the OCR value that compensates for offset errors. The Offset Calibration Register (OCR) is updated after this operation. The user must apply a zero input signal to the appropriate analog inputs. The OCR register is automatically updated afterwards.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL–System Gain Calibration

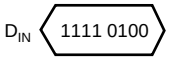
Description: Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the ADS1242 and ADS1243 compute the FSR value that will compensate for gain errors. The FSR is updated after this operation. To initiate a system gain calibration, the user must apply a full-scale input signal to the appropriate analog inputs. FCR register is updated automatically.

Operands: None

Bytes: 1

Encoding: 1111 0100

Data Transfer Sequence:



WAKEUP

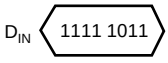
Description: Wakes the ADS1242 and ADS1243 from SLEEP mode.

Operands: None

Bytes: 1

Encoding: 1111 1011

Data Transfer Sequence:



DSYNC–Sync $\overline{\text{DRDY}}$

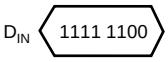
Description: Synchronizes the ADS1242 and ADS1243 to an external event.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence:



SLEEP–Sleep Mode

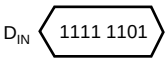
Description: Puts the ADS1242 and ADS1243 into a low power sleep mode. To exit sleep mode, issue the WAKEUP command.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence:



RESET–Reset to Default Values

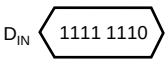
Description: Restore the registers to their power-up values. This command stops the Read Continuous mode.

Operands: None

Bytes: 1

Encoding: 1111 1110

Data Transfer Sequence:



APPLICATION EXAMPLES

GENERAL-PURPOSE WEIGHT SCALE

Figure 8 shows a typical schematic of a general-purpose weight scale application using the ADS1242. In this example, the internal PGA is set to either 64 or 128 (depending on the maximum output voltage of the load cell) so that the load cell output can be directly applied to the differential inputs of ADS1242.

HIGH PRECISION WEIGHT SCALE

Figure 9 shows the typical schematic of a high-precision weight scale application using the ADS1242. The front-end differential amplifier helps maximize the dynamic range.

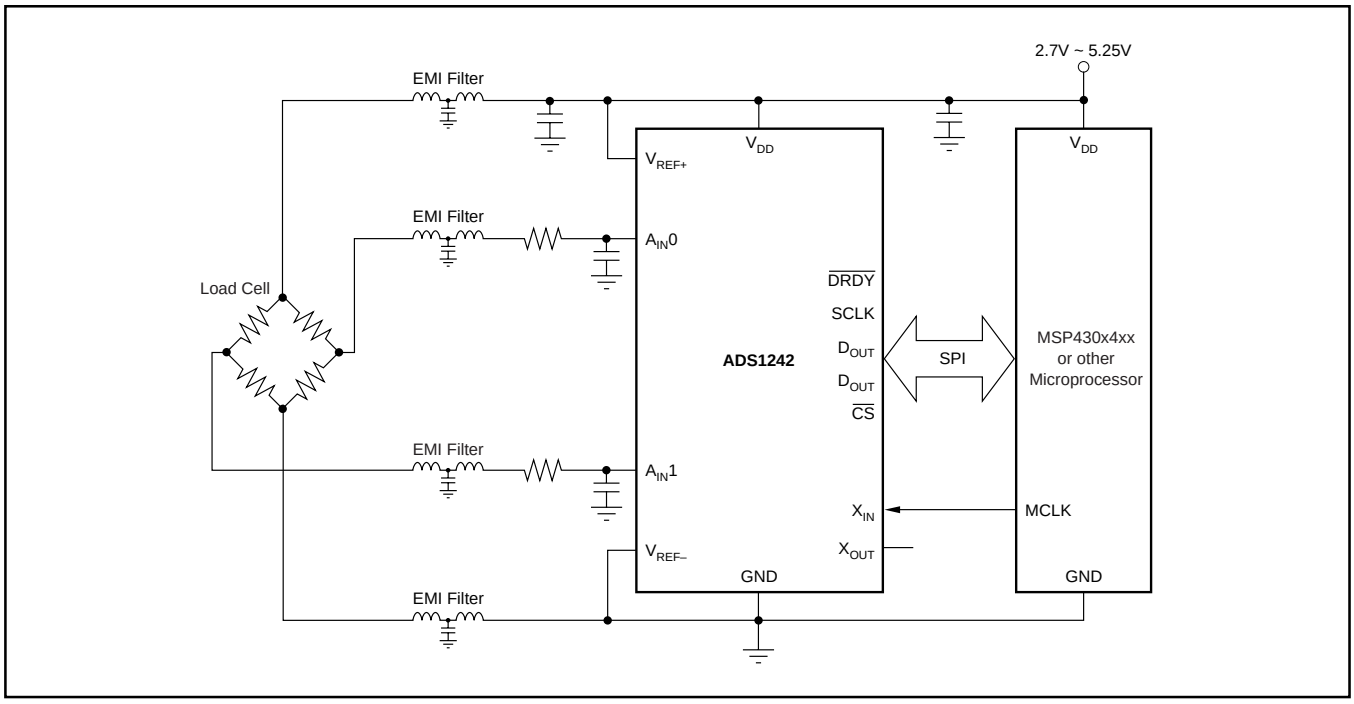


FIGURE 8. Schematic of a General-Purpose Weight Scale.

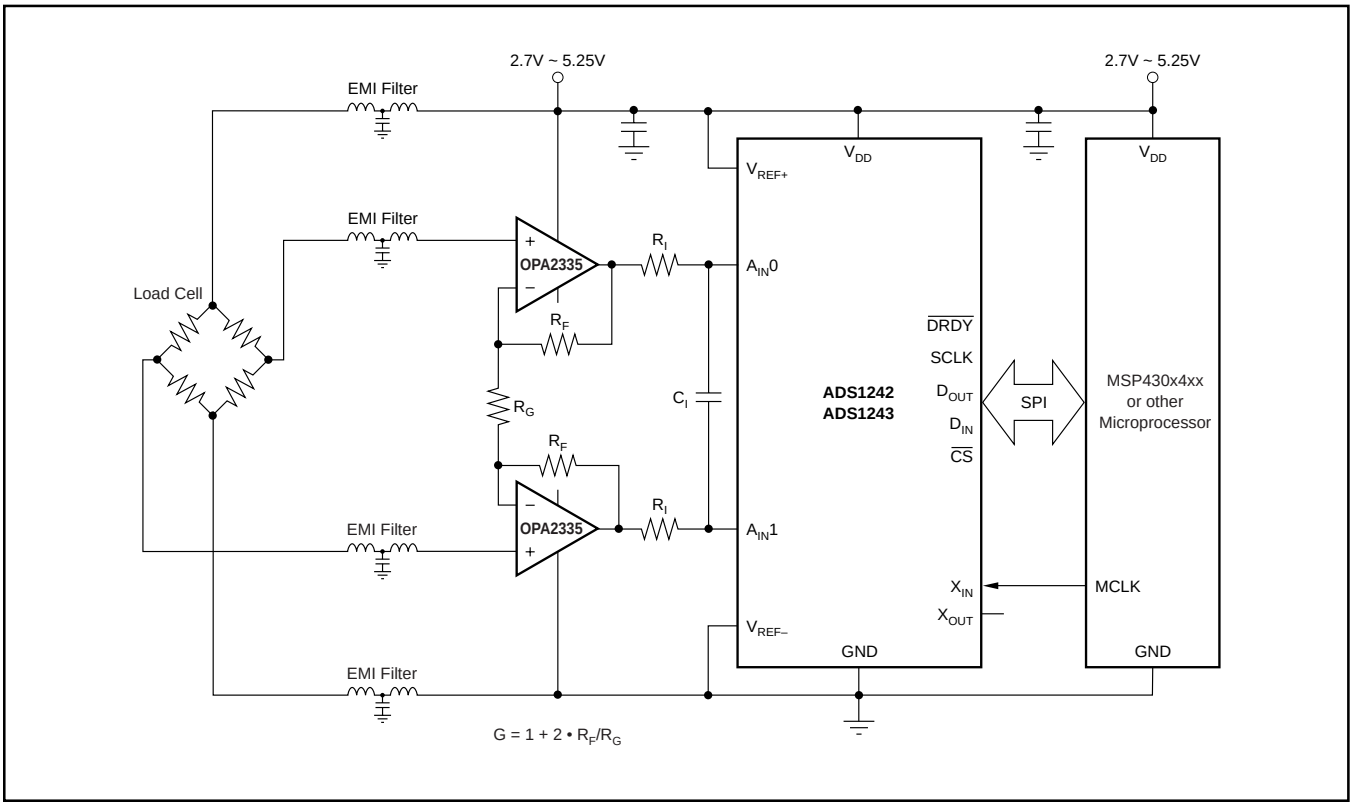


FIGURE 9. Block Diagram for a High-Precision Weight Scale.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Voltage—the voltage at any one analog input relative to GND.

Analog Input Differential Voltage—given by the following equation: (IN+) – (IN–). Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the GND to V_{DD} range.

Conversion Cycle—the term *conversion cycle* usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period.

Data Rate—The rate at which conversions are completed. See definition for f_{DATA}.

$$f_{DATA} = \frac{f_{osc}}{128 \bullet 2^{SPEED} \bullet 1280 \bullet 2^{DR}}$$

$$SPEED = 0,1$$

$$DR = 0,1, 2$$

f_{OSC}—the frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1242 and ADS1243.

f_{MOD}—the frequency or speed at which the modulator of the ADS1242 and ADS1243 is running. This depends on the SPEED bit as given by the following equation:

$$f_{MOD} = \frac{f_{osc}}{mfactor} = \frac{f_{osc}}{128 \bullet 2^{SPEED}}$$

	SPEED = 0	SPEED = 1
mfactor	128	256

PGA SETTING	SAMPLING FREQUENCY
1, 2, 4, 8	$f_{SAMP} = \frac{f_{OSC}}{mfactor}$
16	$f_{SAMP} = \frac{f_{OSC} \bullet 2}{mfactor}$
32	$f_{SAMP} = \frac{f_{OSC} \bullet 4}{mfactor}$
64, 128	$f_{SAMP} = \frac{f_{OSC} \bullet 8}{mfactor}$

f_{SAMP}—the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

f_{DATA}—the frequency of the digital output data produced by the ADS1242 and ADS1243, f_{DATA} is also referred to as the Data Rate.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1242 and ADS1243 is defined as the input, that produces the positive full-scale digital output minus the input, that produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) minus –1.25V (negative full-scale)] = 2.5V.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input has to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full} - \text{Scale Range}}{2^N - 1}$$

where N is the number of bits in the digital output.

t_{DATA}—the inverse of f_{DATA}, or the period between each data output.

	+5V SUPPLY ANALOG INPUT(1)			GENERAL EQUATIONS		
GAIN SETTING	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA OFFSET RANGE	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA SHIFT RANGE
1	5V	±2.5V	±1.25V	RANGE = 0		
2	2.5V	±1.25V	±0.625V			
4	1.25V	±0.625V	±312.5mV			
8	0.625V	±312.5mV	±156.25mV			
16	312.5mV	±156.25mV	±78.125mV	$\frac{V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{2 \bullet PGA}$	$\frac{\pm V_{REF}}{4 \bullet PGA}$
32	156.25mV	±78.125mV	±39.0625mV			
64	78.125mV	±39.0625mV	±19.531mV			
128	39.0625mV	±19.531mV	±9.766mV	RANGE = 1		

NOTES: (1) With a +2.5V reference. (2) Refer to electrical specification for analog input voltage range.

TABLE VI. Full-Scale Range versus PGA Setting.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/13	H	21	Application Examples	Changed Figure 9; switched plus and minus in upper op amp.
2/07	G	10	Overview	Changed 1st paragraph of *Input Multiplexer* subsection.
		15	Registers	Deleted 1xxx from Mux Register definition.
12/06	F	14	Overview	Added DSYNC Operation subsection.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1242IPWR	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS 1242	Samples
ADS1242IPWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS 1242	Samples
ADS1243IPWR	ACTIVE	TSSOP	PW	20	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1243	Samples
ADS1243IPWRG4	ACTIVE	TSSOP	PW	20	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1243	Samples
ADS1243IPWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1243	Samples
ADS1243IPWTG4	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ADS1243	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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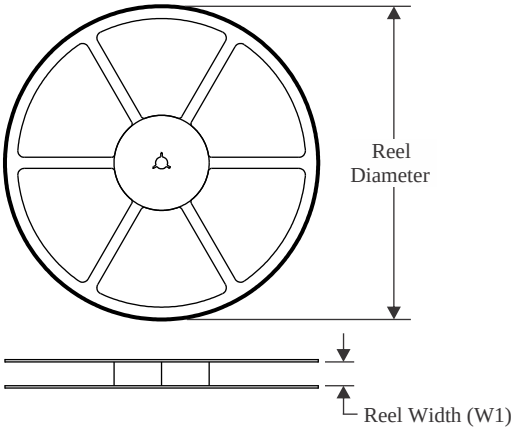
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS1243 :

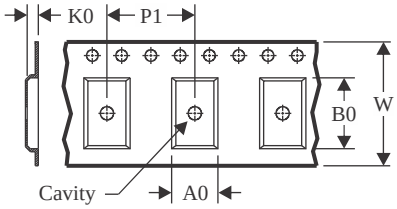
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

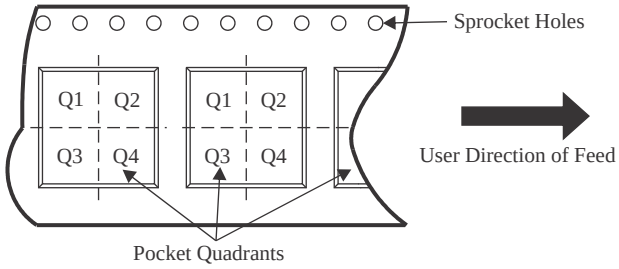


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

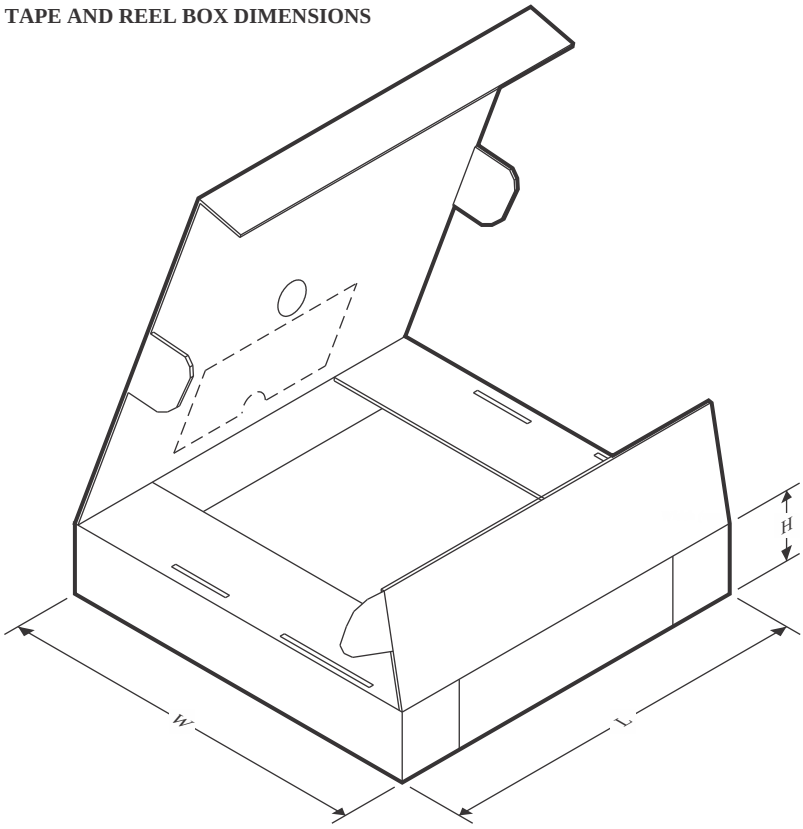
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1242IPWR	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS1242IPWT	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS1243IPWR	TSSOP	PW	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
ADS1243IPWT	TSSOP	PW	20	250	180.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

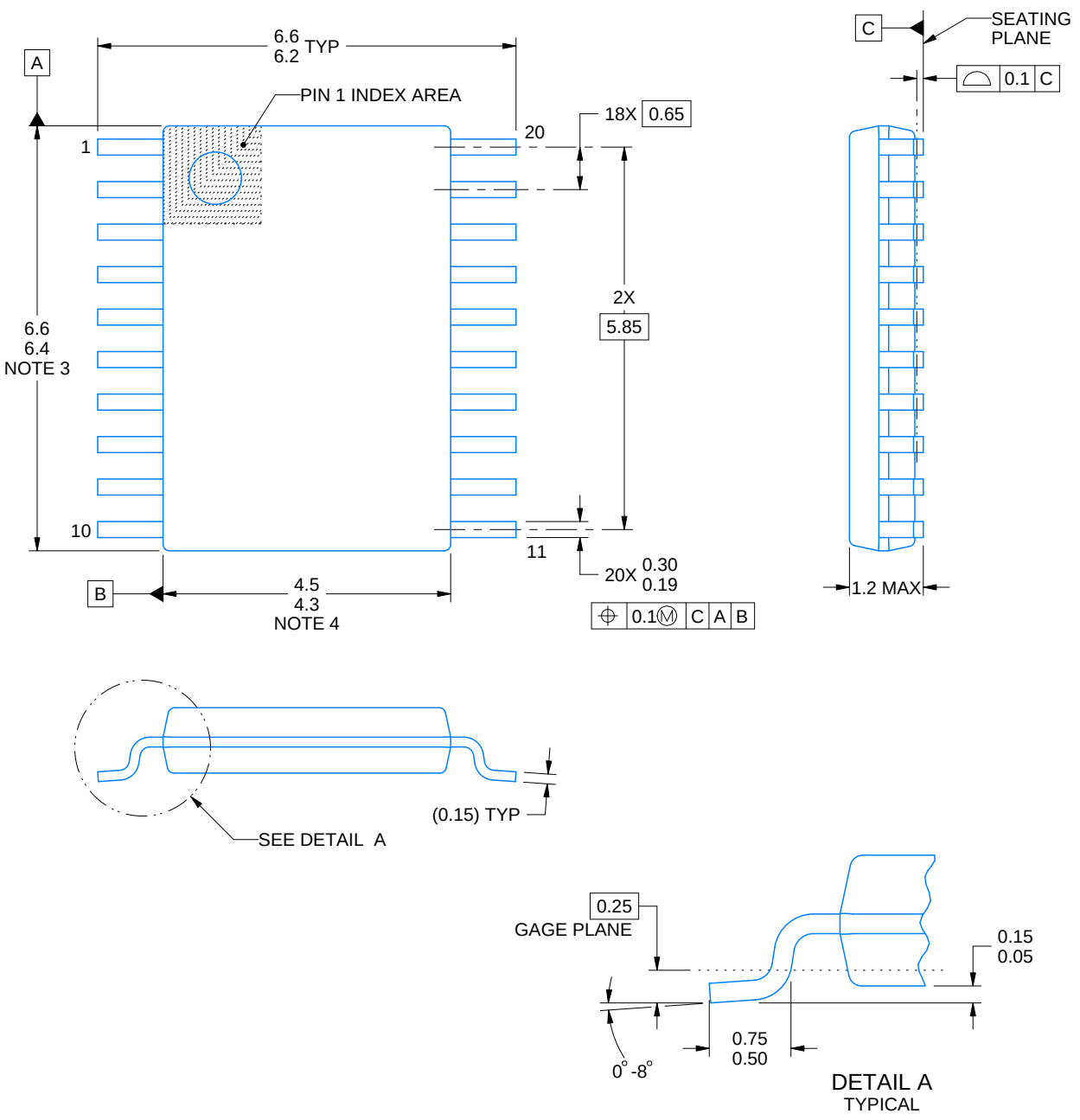
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1242IPWR	TSSOP	PW	16	2500	367.0	367.0	35.0
ADS1242IPWT	TSSOP	PW	16	250	210.0	185.0	35.0
ADS1243IPWR	TSSOP	PW	20	2500	356.0	356.0	35.0
ADS1243IPWT	TSSOP	PW	20	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0020A

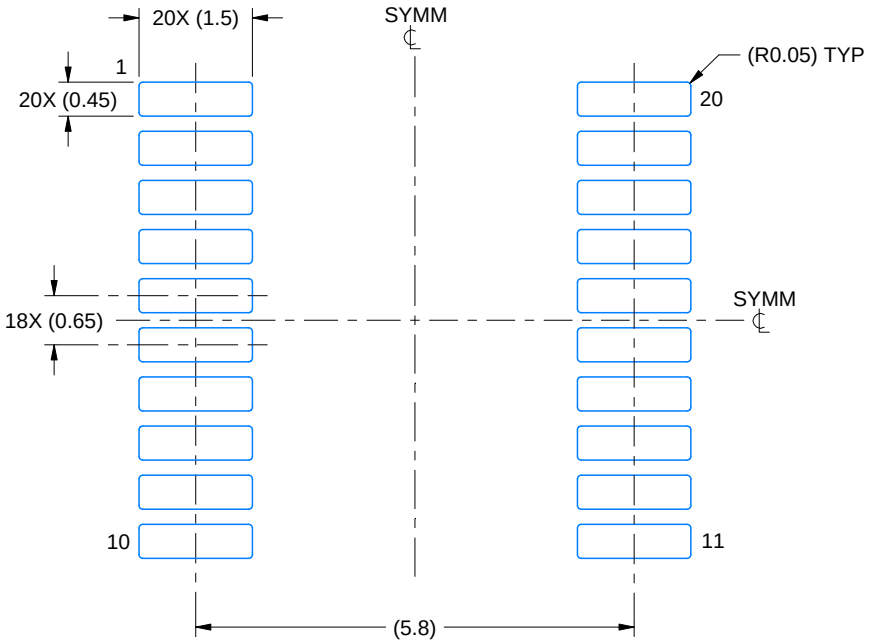
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

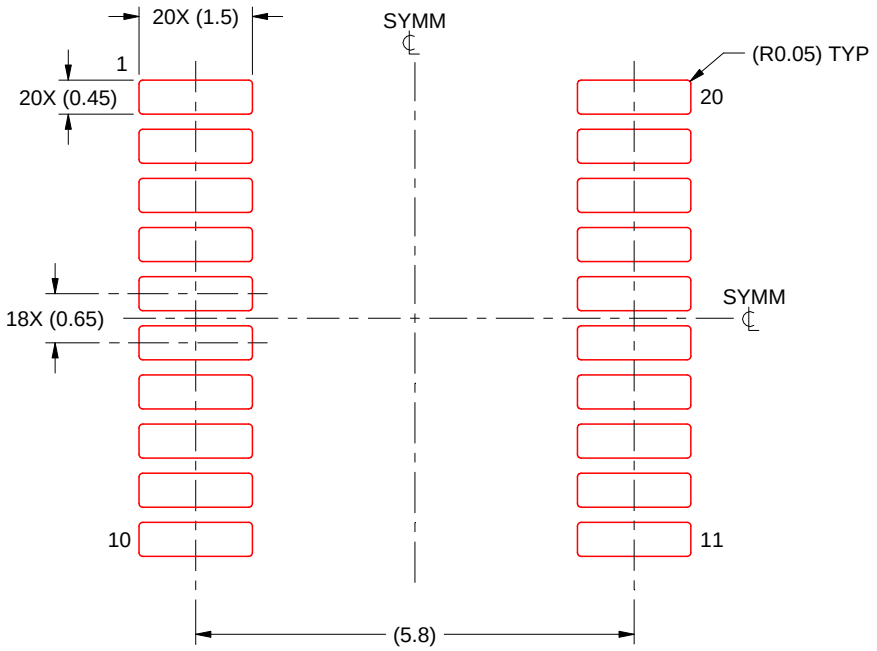


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



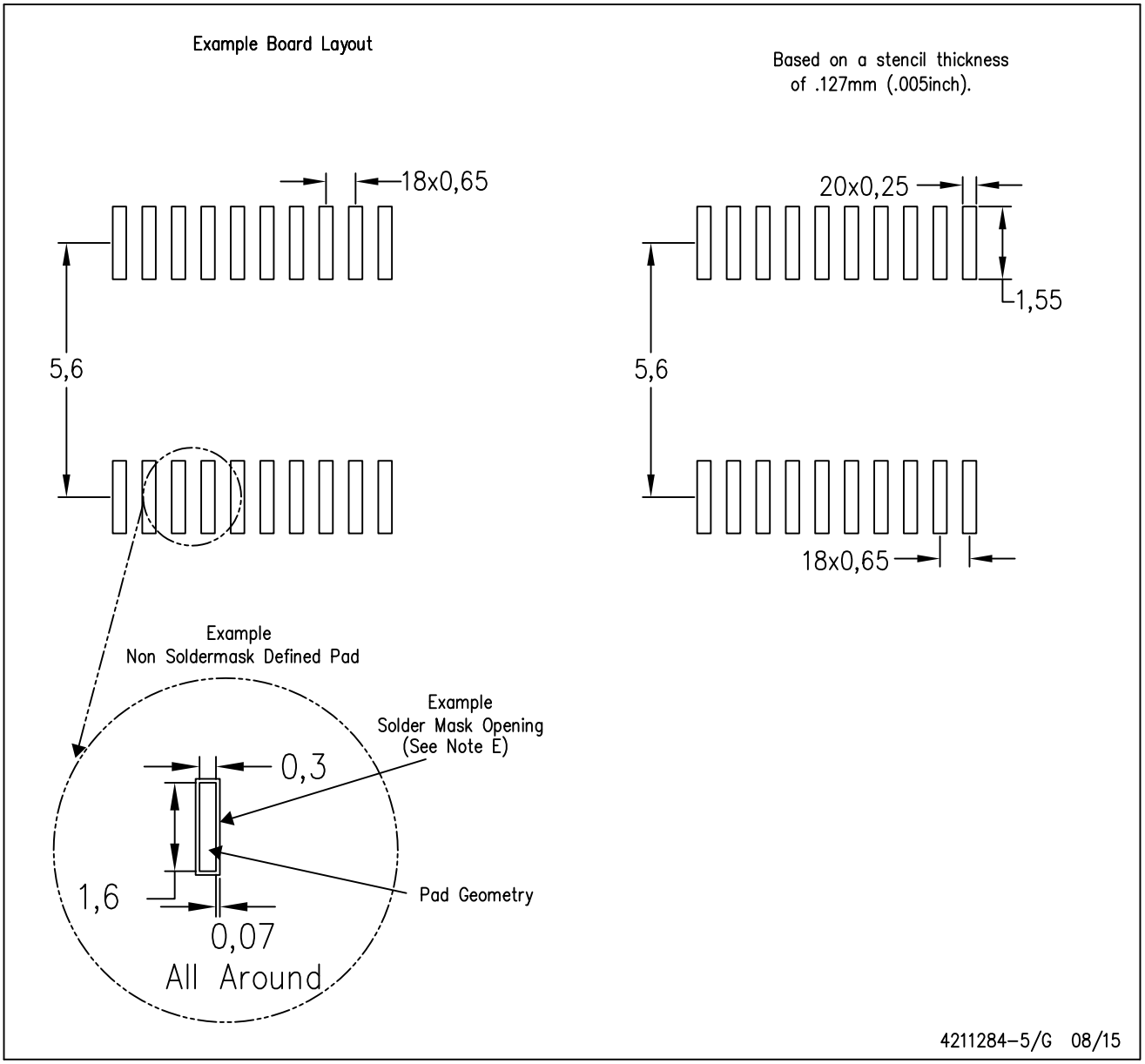
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



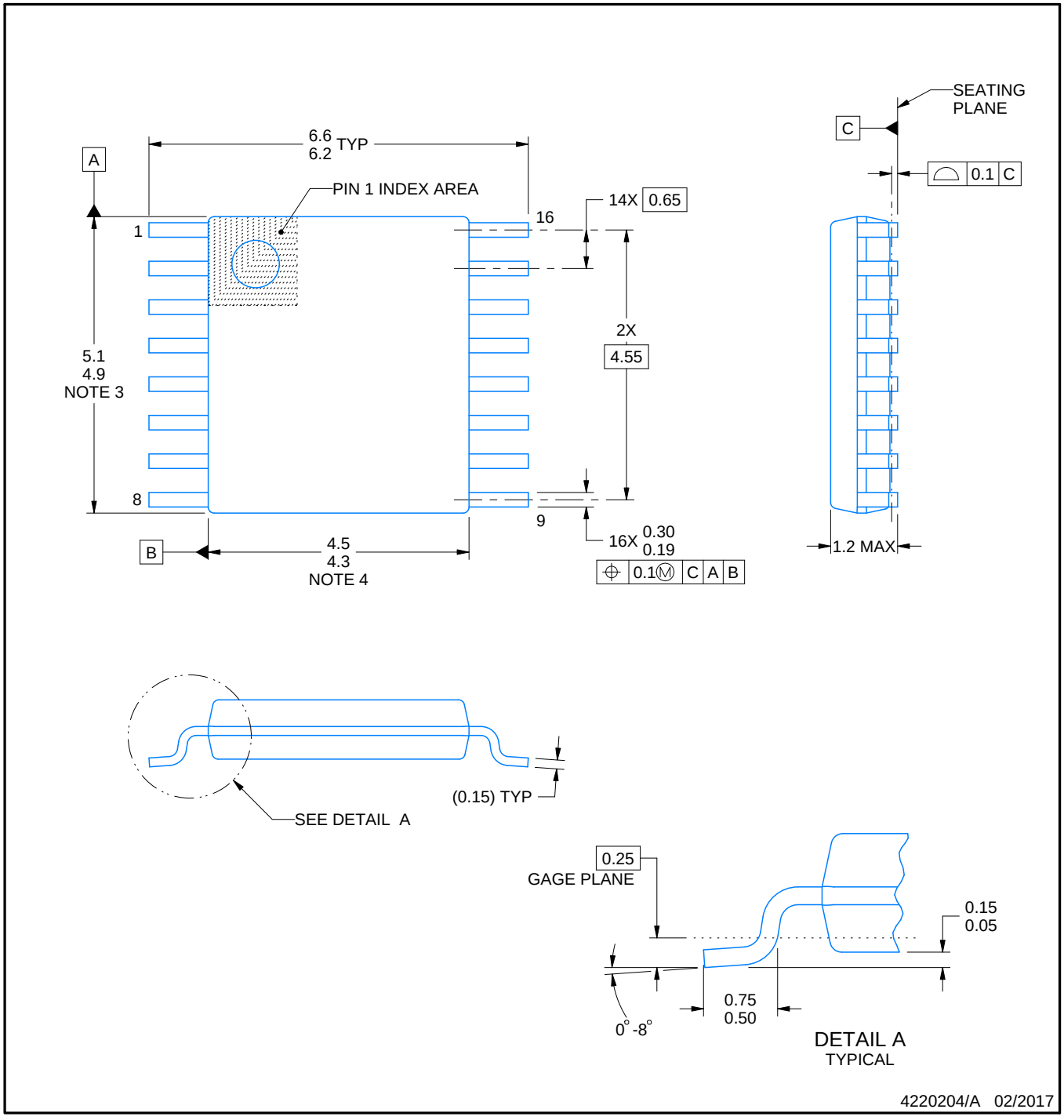
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

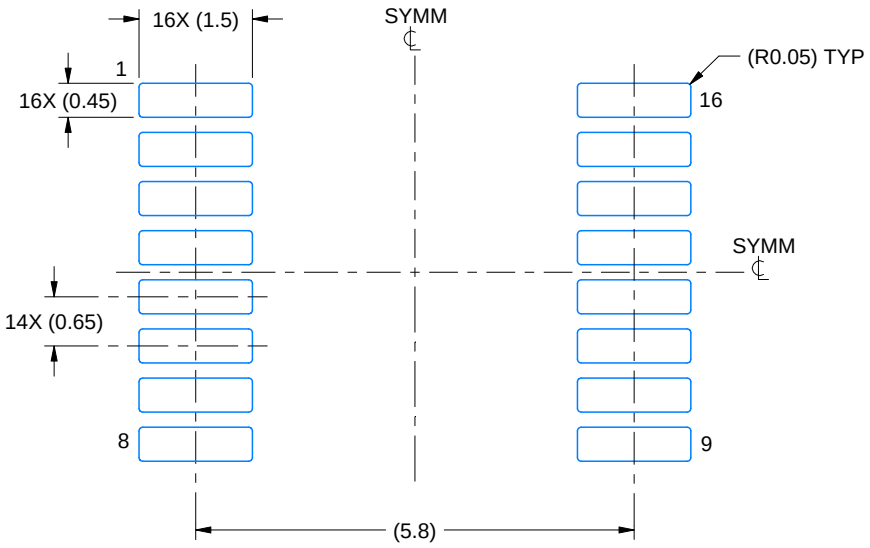
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

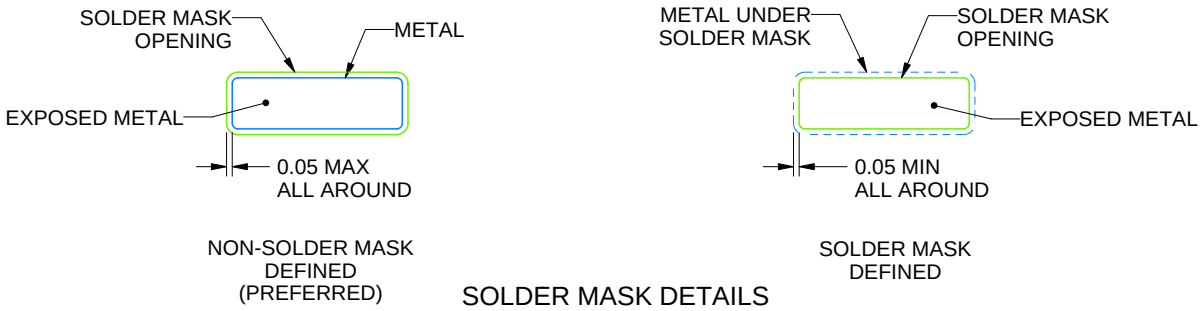


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

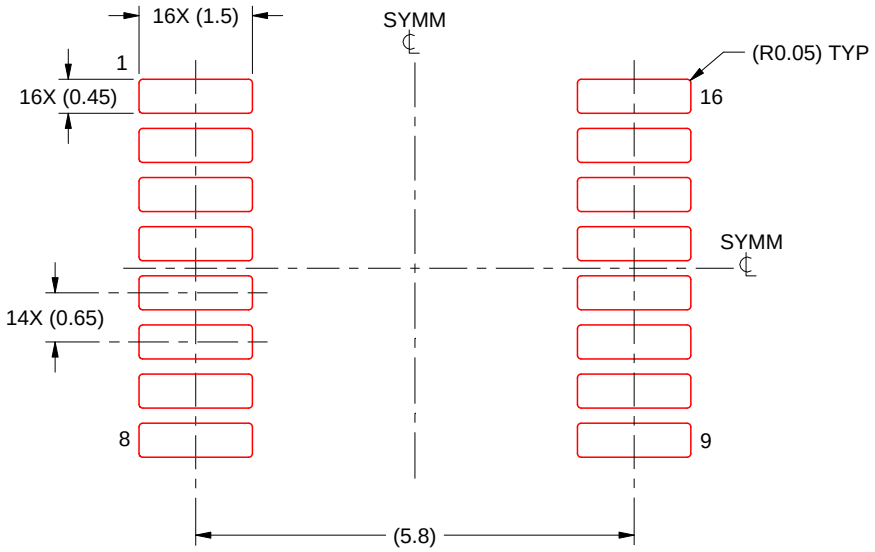


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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