

R2A20104/114 Series

Continuous Conduction Mode Interleaving PFC Control IC

R03DS0008EJ0301

Rev.3.01

Jan 08, 2016

Description

R2A20104/114 series is a boost converter control IC with PFC (Power Factor Correction). Employing continuous conduction mode interleaving PFC, it performs higher efficiency and lower switching noise even for high power use. The control of continuous conduction mode is carried out by detecting the current in power MOSFET. The R2A20114 series supports two types of current detection methods; current detection by current transformers (R2A20104SP/FP), and that by shunt resistors (R2A20114SP/FP). So that, it can be applicable for a variety of applications. Interleaving control of the boost converters, namely, producing 180 degrees phase shift between the output signals (GD1,2) driving the boost converters, enables the system to perform high conversion efficiency and low switching noises and, at the same time, to reduce ripple currents in input and output current and then this allows use of smaller components such as boost inductors, input filters and output capacitors. R2A20114 series integrates a various kinds of protection circuits, such as the detection circuit of breaking of wire in feedback loop, two modes of over voltage protection circuits, over current protection circuit and error output circuit (*1), which improve the reliability of the power supply system and reduce the number of component parts on the system.

Features

- Maximum Ratings
 - Supply voltage Vcc: 24 V
 - Junction temperature Tj: from -40 to +150 degrees centigrade
- Electrical characteristics
 - VFB feedback voltage VREF: 2.5 V ± 1.5%
 - UVLO (Undervoltage Lockout) operation start voltage VH: 10.4 V ± 0.7 V
 - UVLO operation shutdown voltage VL: 8.9 V ± 0.5 V
 - UVLO hysteresis voltage Hysvvl : 1.5 V ± 0.5 V
- Functions
 - Boost converter control with continuous conduction mode
 - Interleaving control
 - Frequency modulation (*2)
 - Brownout
 - Phase drop (*1)
 - External clock synchronization input
 - External clock synchronization output (*1)
 - Two modes of over voltage protections
 - Mode 1: Dynamic OVP preventing over voltage after sudden variation of load.
 - Mode 2: Static OVP preventing over voltage in the period of normal operation.
 - Feedback loop wire breaking/open detector
 - Dual over voltage protection circuits (*1): FB and OVP2 terminals
 - Current balance control
 - Phase 1 and Phase 2 independent over current protection
 - Package line-up
 - Pb-free LQFP-40 (R2A20104FP, R2A20114FP)
 - Pb-free SOP-20 (R2A20104SP, R2A20114SP)

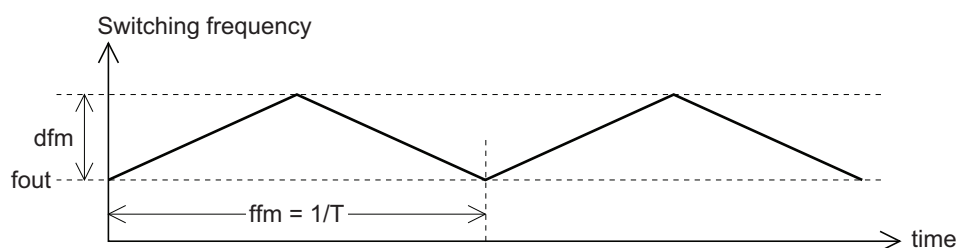
Notes: *1 Supported only by R2A20104FP and R2A20114FP

*2 Frequency modulation periods (dfm) of R2A20104SP and R2A20114SP are fixed.

The Function List of R2A20104/114 Series

| Item | | R2A20104SP | R2A20104FP | R2A20114SP | R2A20114FP |
|--------------------------------------|---|--|------------|--|------------|
| PFC control | | Continuous conduction mode interleaving | | | |
| Current detection method | | Current transformer | | Shunt resistor | |
| Package | | SOP-20 | LQFP-40 | SOP-20 | LQFP-40 |
| Protection circuits | Brownout detection | Supported | Supported | Supported | Supported |
| | 2nd OVP | Not supported | Supported | Not supported | Supported |
| | Phase error | Not supported | Supported | Not supported | Supported |
| Noise reduction | Jitter generation (Frequency modulation) | Supported (But, frequency modulation period (dfm) ^(*1) is fixed) | Supported | Supported (But, frequency modulation period (dfm) ^(*1) is fixed) | Supported |
| Synchronization with external signal | Input | Supported | Supported | Supported | Supported |
| | Output | Not supported | Supported | Not supported | Supported |
| Efficiency improvement | Phase drop | Not supported | Supported | Not supported | Supported |

Note: *1 Refer to the figure depicted below:

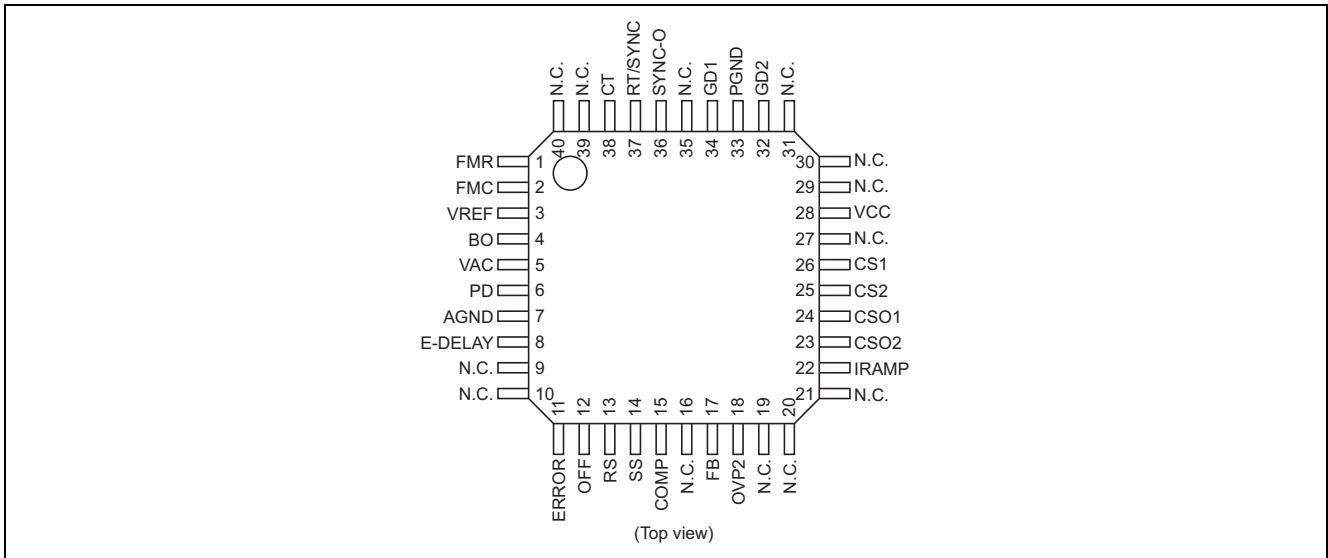


Ordering Information

| Part No. | Package Name | Package Code | Package Abbreviation | Taping Abbreviation (Quantity) | Remarks |
|--------------|--------------|--------------|----------------------|--------------------------------|---------|
| R2A20104FPW0 | FP-40EV | PLQP0040JB-C | FP | W (2000 pcs/reel) | non-HF |
| R2A20104FPW5 | | | | | HF |
| R2A20114FPW0 | FP-20DAV | PRSP0020DD-B | SP | W (2000 pcs/reel) | non-HF |
| R2A20114FPW5 | | | | | HF |
| R2A20104SPW0 | FP-20DAV | PRSP0020DD-B | SP | W (2000 pcs/reel) | non-HF |
| R2A20104SPW5 | | | | | HF |
| R2A20114SPW0 | | | | | non-HF |
| R2A20114SPW5 | | | | | HF |

Note: HF: Halogen-Free

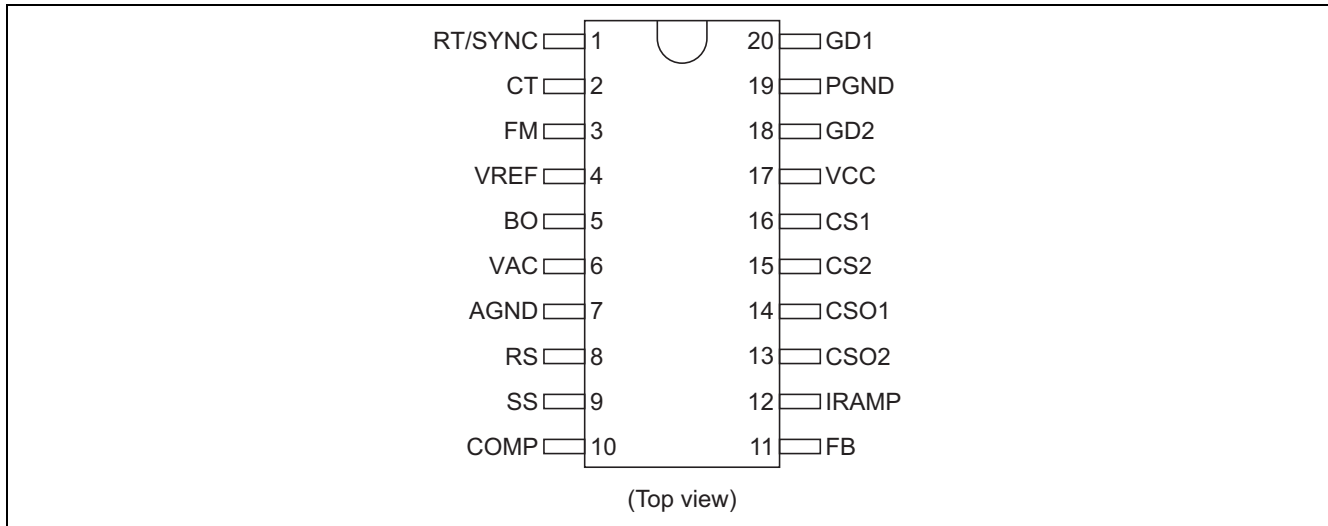
Pin Arrangement of R2A20104FP and R2A20114FP



Pin Functions of R2A20104FP and R2A20114FP

| Pin No. | Pin Name | Input/Output | Function |
|---------|----------|--------------|--|
| 1 | FMR | Input | Frequency modulation setting resistor connecting terminal |
| 2 | FMC | Input | Frequency modulation setting capacitor connecting terminal |
| 3 | VREF | Output | Reference voltage output terminal |
| 4 | BO | Input | Brownout input terminal |
| 5 | VAC | Input | AC voltage input terminal |
| 6 | PD | Input | Phase drop input terminal |
| 7 | AGND | — | Analog ground |
| 8 | E-DELAY | Input | Delay of the Error signal setting terminal |
| 9, 10 | N.C. | — | Open |
| 11 | ERROR | Output | Error output terminal |
| 12 | OFF | Input | Shutdown terminal (VCC Reset) |
| 13 | RS | Input | Current correction setting resistor connecting terminal |
| 14 | SS | Input | Soft start setting capacitor connecting terminal |
| 15 | COMP | Output | Error amplifier output terminal (to be phase-compensated) |
| 16 | N.C. | — | Open |
| 17 | FB | Input | Error amplifier input terminal (feedback voltage input terminal) |
| 18 | QVP2 | Input | OVP2 input terminal |
| 19-21 | N.C. | — | Open |
| 22 | IRAMP | Input | Ramp waveform setting resistor connecting terminal |
| 23 | CSO2 | Output | Current sense amplifier 2 output terminal (to be phase-compensated) |
| 24 | CSO1 | Output | Current sense amplifier 1 output terminal (to be phase-compensated) |
| 25 | CS2 | Input | Current sense 2 input terminal |
| 26 | CS1 | Input | Current sense 1 input terminal |
| 27 | N.C. | — | Open |
| 28 | VCC | Input | Supply voltage terminal |
| 29-31 | N.C. | — | Open |
| 32 | GD2 | Output | Converter 2 Power MOSFET drive terminal |
| 33 | PGND | — | Power ground |
| 34 | GD1 | Output | Converter 1 Power MOSFET drive terminal |
| 35 | N.C. | — | Open |
| 36 | SYNC-O | Output | Synchronization signal output terminal |
| 37 | RT/SYNC | Input | Frequency setting resistor connecting terminal / Sync. Signal input terminal |
| 38 | CT | Input | Frequency setting capacitor connecting terminal |
| 39, 40 | N.C. | — | Open |

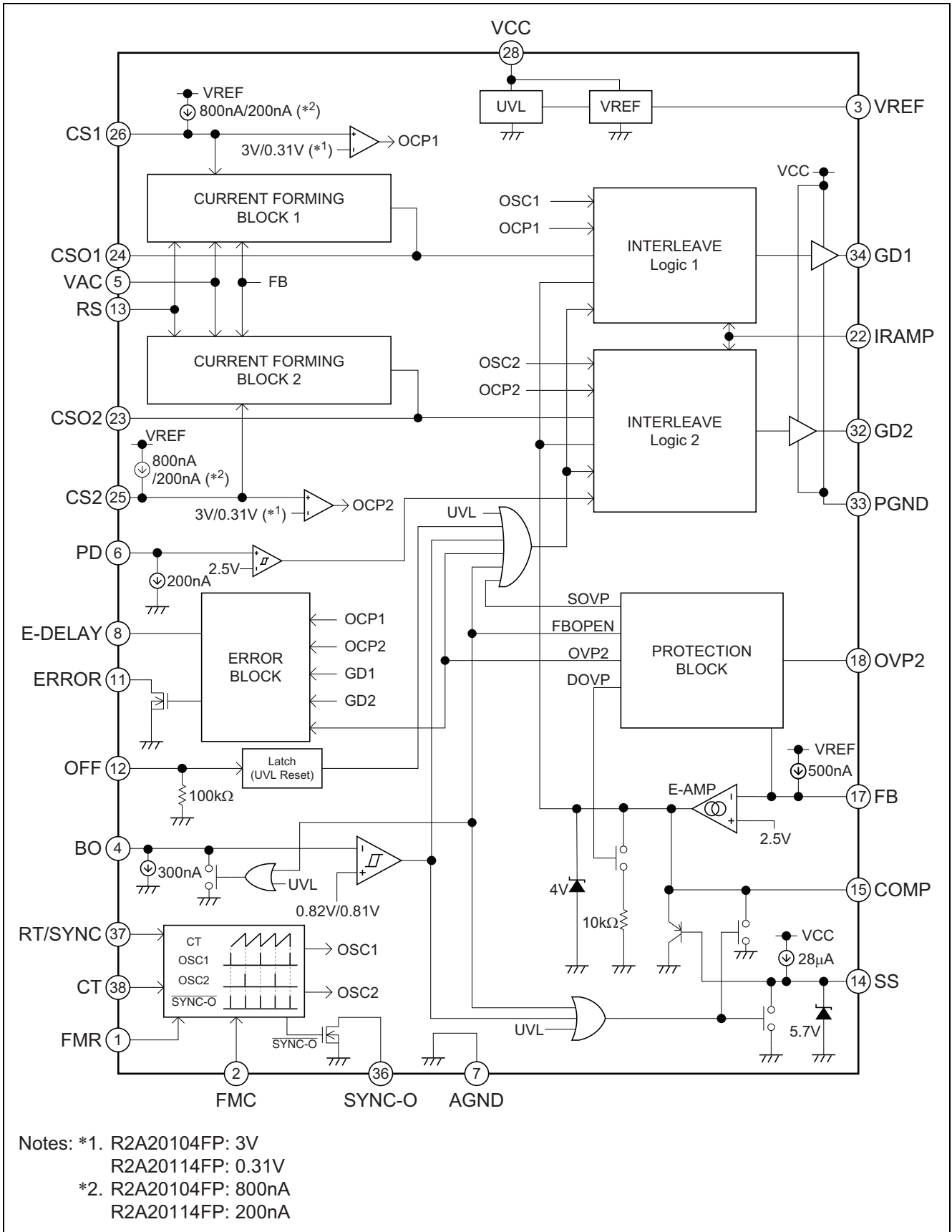
Pin Arrangement of R2A20104SP and R2A20114SP



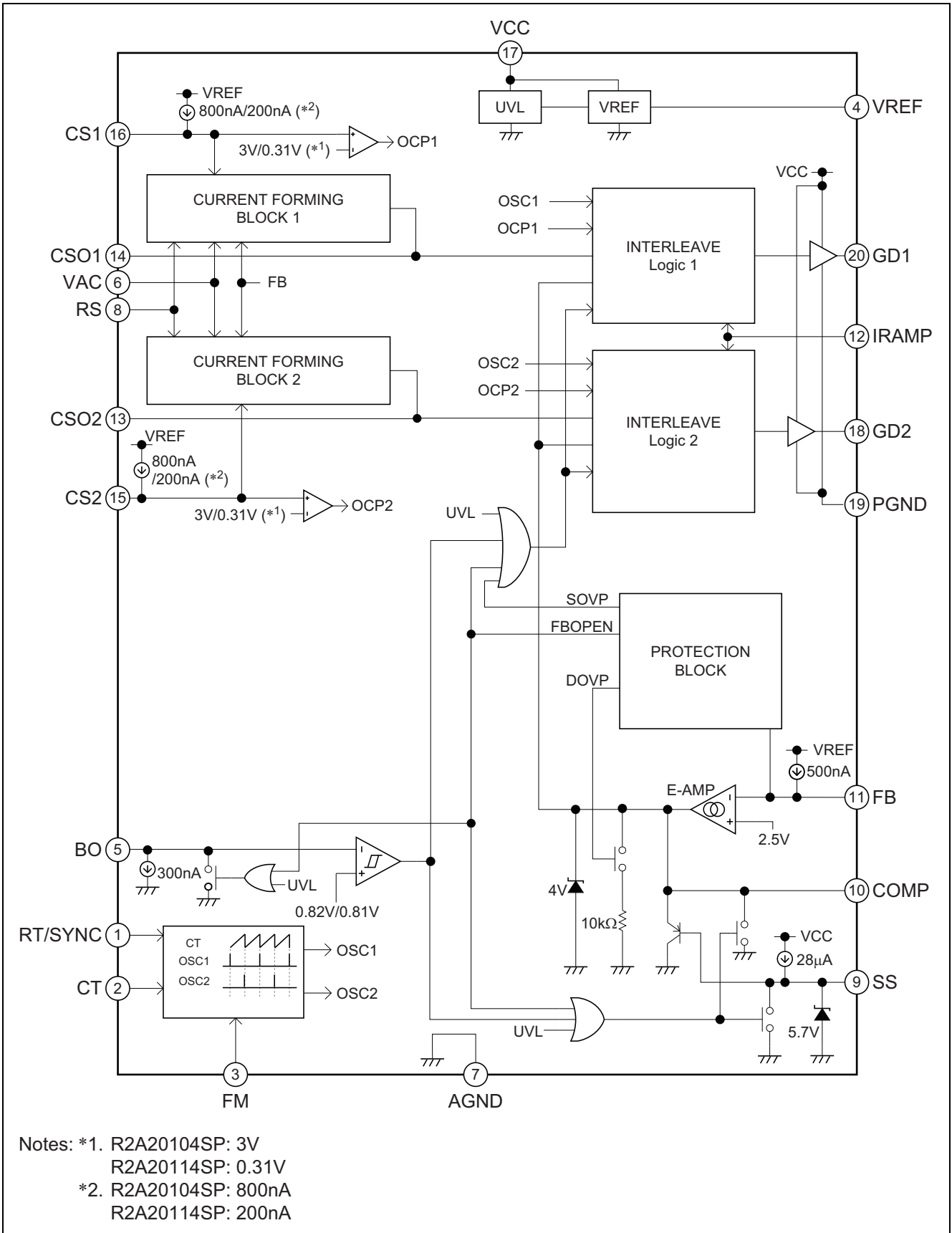
Pin Functions of R2A20104SP and R2A20114SP

| Pin No. | Pin Name | Input/Output | Function |
|---------|----------|--------------|---|
| 1 | RT/SYNC | Input | Frequency setting timing resistor connecting terminal / Sync. signal input terminal |
| 2 | CT | Input | Frequency setting timing capacitor connecting terminal |
| 3 | FM | Input | Frequency modulation setting timing capacitor connecting terminal |
| 4 | VREF | Output | Reference voltage output terminal |
| 5 | BO | Input | Brownout input terminal |
| 6 | VAC | Input | AC voltage input terminal |
| 7 | AGND | — | Analog ground |
| 8 | RS | Input | Current correction setting resistor connecting terminal |
| 9 | SS | Input | Soft start setting capacitor connecting terminal |
| 10 | COMP | Output | Error amplifier output terminal (to be phase-compensated) |
| 11 | FB | Input | Error amplifier input terminal (feedback voltage input terminal) |
| 12 | IRAMP | Input | Ramp waveform setting resistor connecting terminal |
| 13 | CSO2 | Output | Current sense amplifier 2 output terminal (to be phase-compensated) |
| 14 | CSO1 | Output | Current sense amplifier Output 1 output terminal (to be phase-compensated) |
| 15 | CS2 | Input | Current sense 2 input terminal |
| 16 | CS1 | Input | Current sense 1 input terminal |
| 17 | VCC | Input | Supply voltage terminal |
| 18 | GD2 | Output | Converter 2 Power MOSFET drive terminal |
| 19 | PGND | — | Power ground |
| 20 | GD1 | Output | Converter 1 Power MOSFET drive terminal |

Block Diagram of R2A20104FP and R2A20114FP



Block Diagram of R2A20104SP and R2A20114SP



Absolute Maximum Ratings

| Item | Symbol | Value | Unit | Note |
|-------------------------------|----------------------|---|------|------|
| Supply voltage | VCC | -0.3 to +24 | V | 3 |
| GD1 and 2 | Peak current | l _{pk-gd1} , l _{pk-gd2} | ±1 | 3, 4 |
| | DC current | l _{dc-gd1} , l _{dc-gd2} | ±0.1 | 3 |
| Vref terminal current | I _{ref} | -5 | mA | 3 |
| Terminal current | I _{t-group} | ±1 | mA | 3, 5 |
| RS terminal current | I _{rs} | -500 | μA | 3 |
| RT terminal current | I _{rt} | -200 | μA | 3 |
| RAMP terminal current | I _{ramp} | -200 | μA | 3 |
| BO clamp current | I _{bo} | 300 | μA | 3 |
| Terminal voltage | V _{t-group} | -0.3 to V _{ref} | V | 3, 6 |
| Vref terminal voltage | V _{t-ref} | -0.3 to V _{ref} +0.3 | V | 3 |
| SS terminal voltage | V _{t-ss} | -0.3 to V _{ref} +1 | V | 3 |
| Power dissipation | P _t | 1 | W | 3, 7 |
| Operating ambient temperature | T _{a-opr} | -40 to +125 | °C | |
| Junction temperature | T _j | -40 to +150 | °C | 8 |
| Storage temperature | T _{stg} | -55 to +150 | °C | |

- Notes:
- Rated voltages are with reference to the AGND and PGND terminal.
 - For the direction of Rated currents, (+) denotes the current flowing into the IC, and (-) denotes the current flowing out of the IC.
 - Ambience temperature, T_a is 25 degrees centigrade.
 - Transient current when driving a capacitive load.
 - Rated currents of the terminals listed below:
COMP, CSO1, CSO2
 - Rated voltages of the terminals listed below:
in the case of R2A20104FP/R2A20114FP: CS1, CS2, VAC, RS, FB, PD, BO, ERROR, E-DLAY, OFF, OVP2, FMC, FMR, RT/SYNC, IRAMP, SYNC-O, CT, COMP, CSO1, CSO2
in the case of R2A20104SP/R2A20114SP: CS1, CS2, VAC, RS, FB, BO, IRAMP, FM, RT/SYNC, CT, COMP, CSO1, CSO2
 - Thermal resistor
in the case of R2A20104FP/R2A20114FP: θ_{ja} = 85.3 degrees centigrade/W
in the case of R2A20104SP/R2A20114SP: θ_{ja} = 120 degrees centigrade/W
These values are obtained under the condition that the IC is mounted on the glass epoxy board, of which size is 50 × 50 × 1.6 [mm] and wiring density is 10%.
 - Stresses exceeding the absolute maximum ratings may damage the device.
These are stress ratings only. Functional operation above the recommended operating ambient temperature range is not implied.
Extended exposure to stresses above the absolute maximum ratings may affect device reliability.

Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $C_T = 1000\text{ pF}$, $R_T = 27\text{ k}\Omega$, $CS1, CS2 = \text{GND}$, $IRAMP = 10\text{ k}\Omega$, $BO = 1\text{ V}$, $V_{AC} = 0\text{ V}$, $RS = 220\text{ k}\Omega$, $FMC = \text{GND}$ (*¹), $FM = \text{GND}$ (*²), $FB = \text{COMP}$)

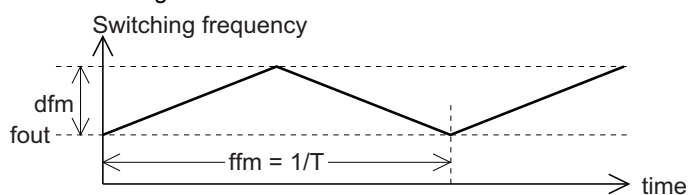
| | Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|-----------------|--|--|-------|-----------|-------|-----------------------|--|
| Supply | UVLO turn-on threshold | Vuvlh | 9.7 | 10.4 | 11.1 | V | |
| | UVLO turn-off threshold | Vuvll | 8.4 | 8.9 | 9.4 | V | |
| | UVLO hysteresis | Hysuvl | 1.0 | 1.5 | 2.0 | V | |
| | Standby current | Istby | — | 100 | 160 | μA | $V_{CC} = 8.9\text{ V}$ |
| | Operating current | Icc | — | 5 | 7.5 | mA | |
| VREF | Output voltage | Vref | 4.85 | 5.00 | 5.15 | V | Isource = -1 mA |
| | Line regulation | Vref-line | — | 5 | 20 | mV | Isource = -1 mA, $V_{CC} = 10\text{ V to }24\text{ V}$ |
| | Load regulation | Vref-load | — | 5 | 20 | mV | Isource = -1 mA to -5 mA |
| | Temperature stability | dVref | — | ± 80 | — | ppm/ $^\circ\text{C}$ | $T_a = -40\text{ to }125^\circ\text{C}$ (* ³) |
| Error amplifier | Feedback voltage | Vfb | 2.462 | 2.500 | 2.538 | V | FB-COMP Short |
| | Input bias current | Ifb | -0.8 | -0.5 | -0.2 | μA | Measured pin: FB |
| | Open loop gain | Av | — | 40 | — | dB | (* ³) |
| | Upper clamp voltage | Vclamp-comp | 3.8 | 4.0 | 4.3 | V | FB = 2.0 V, COMP: Open |
| | Low voltage | Vl-comp | 0.0 | 0.1 | 0.3 | V | FB = 3.0 V, COMP: Open |
| | Source current | Isrc-comp | -190 | -135 | -80 | μA | FB = 1.5 V, COMP = 2.5 V |
| | Sink current 1 | Isnk-comp1 | — | 120 | — | μA | (* ³) |
| | Sink current 2 | Isnk-comp2 | 220 | 320 | 420 | μA | FB = 3.5 V, COMP = 2.5 V |
| Brownout | Transconductance | gm | 120 | 200 | 290 | μs | FB = 2.45 V \leftrightarrow 2.55 V, COMP = 2.5 V |
| | PFC enable voltage | Von-pfc | 0.74 | 0.82 | 0.9 | V | Input pin: BO |
| | PFC disable voltage | Voff-pfc | 0.73 | 0.81 | 0.89 | V | Input pin: BO |
| Oscillator | Initial accuracy | fout | 70 | 78 | 86 | kHz | Measured pin: OUT, FMC = 0 V |
| | fout temperature stability | dfout/dTa | — | ± 0.1 | — | %/ $^\circ\text{C}$ | $T_a = -40\text{ to }125^\circ\text{C}$ (* ³) |
| | fout voltage stability | fout-line | -1.5 | 0.5 | 1.5 | % | $V_{CC} = 12\text{ V to }18\text{ V}$ |
| | CT top voltage | Vct-H | — | 3.6 | 4.0 | V | (* ³) |
| | RT voltage | Vrt | 1.15 | 1.25 | 1.35 | V | |
| | FMC sink current (* ¹)/ FM sink current (* ²) | Isnk-fmc (* ¹)/ Isnk-fm (* ²) | 6 | 11 | 16 | μA | FMC = 1 V (* ¹)/ FM = 1 V (* ²) |
| | FMC source current (* ¹)/ FM source current (* ²) | Iso-fmc (* ¹)/ Iso-fm (* ²) | -16.5 | -11.5 | -6.5 | μA | FMC = 1 V (* ¹)/ FM = 1 V (* ²) |
| | FM magnitude change | dfm | 19 | 24 | 29 | kHz | FMC = 5 V (* ¹)/FM = 5 V (* ²) (* ³ , * ⁴) |
| | FM frequency 1 (* ¹) | ffm1 | 0.25 | 0.38 | 0.5 | kHz | FMC = 6.8 nF, FMR = 4 V (* ⁴) |
| | FM frequency 2 (* ¹) | ffm2 | 14 | 25 | 35 | kHz | FM = 220 pF, FMR = 1.2 V (* ⁴) |
| | FM frequency (* ²) | ffm | 6 | 10 | 14 | kHz | FMC = 220 pF (* ⁴) |

Notes: *1 Applied to R2A20104FP, R2A20114FP

*2 Applied to R2A20104SP, R2A20114SP

*3 Design Specification (Reference data)

*4 Refer to the figure shown below:



Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 12 V, CT = 1000 pF, RT = 27 kΩ, CS1, CS2 = GND, IRAMP = 10 kΩ, BO = 1 V, VAC = 0 V, RS = 220 kΩ, FMC = GND (*1), FM = GND (*2), FB = COMP)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|-------------------------------|-----------------------------------|----------|---------------|---------------|---------------|-----------------|--|
| Synchroni- zation | SYNC threshold voltage (rising) | Vsync | 2.0 | 2.5 | 3.0 | V | |
| | SYNC Min. pulse | Psync | 2 | — | — | μs | |
| | SYNC-OUT shunt current (*1) | Isync-s | 5.0 | — | — | mA | |
| | SYNC-OUT leakage current (*1) | Isync-l | — | — | 1.0 | μA | |
| Current slope | RS output voltage 1 | Vrs1 | 0.56 | 0.65 | 0.74 | V | VAC = 0 V, VFB = 2.5 V |
| | RS output voltage 2 | Vrs2 | 0.04 | 0.14 | 0.26 | V | VAC = 2.5 V, VFB = 0 V |
| | VAC bias current | Ivac | -0.4 | -0.2 | -0.05 | μA | Measured pin: VAC |
| Soft start | Source current | Iss | -40 | -28 | -16 | μA | SS = 2 V |
| Phase drop | Phase drop threshold voltage (*1) | Vpd | 2.4 | 2.5 | 2.6 | V | |
| | Phase drop hysteresis (*1) | Hya-pd | 150 | 200 | 250 | mV | |
| | PD bias current (*1) | Ipd | 0.05 | 0.2 | 0.5 | μA | Measured pin: PD |
| AMP1, 2 | CSO offset voltage1 (*5) | Voffset | 0.68 | 0.88 | 1.0 | V | Vcs = 0 V |
| | CSO offset voltage1 (*6) | Voffset | 0.54 | 0.74 | 0.86 | V | Vcs = 0 V |
| | CSO offset voltage2 | Vcaoh | 2.83 | 3 | 3.17 | V | Vcs = 0.24 V (*5), Vcs = 2.3 V (*6) |
| | CS Bias current (*5) | Ics-r | -0.4 | -0.2 | -0.05 | μA | Measured pin: CS1, 2 |
| | CS Bias current (*6) | Ics-ct | -1.1 | -0.8 | -0.5 | μA | Measured pin: CS1, 2 |
| Gate drive 1, 2 | Gate drive rise time | tr-gd | — | 30 | 100 | ns | CL = 500 pF |
| | Gate drive fall time | tf-gd | — | 30 | 100 | ns | CL = 500 pF |
| | Gate drive low voltage | Vol1-gd | — | 0.05 | 0.2 | V | Isink = 10 mA |
| | | Vol2-gd | — | 1 | 1.25 | V | Isink = 0.25 mA, VCC = 5 V |
| | Gate drive high voltage | Voh-gd | 11.5 | 11.9 | — | V | Isource = -10 mA |
| | Minimum duty cycle | Dmin-out | — | — | 0 | % | |
| Maximum duty cycle | Dmax-out | 90 | 95 | 98 | % | | |
| Over voltage protection | Dynamic OVP Threshold voltage | Vdovp | VFB× 1.025 | VFB× 1.040 | VFB× 1.055 | V | |
| | Static OVP Threshold voltage | Vsovp | VFB× 1.065 | VFB× 1.080 | VFB× 1.095 | V | COMP = OPEN |
| | Static OVP Hysteresis | Hys-sovp | 30 | 80 | 130 | mV | COMP = OPEN |
| | OVP2 Threshold voltage (*1) | Vovp2 | VFB× 1.065 | VFB× 1.080 | VFB× 1.095 | μA | |
| | OVP2 Hysteresis (*1) | Hys-ovp2 | 30 | 80 | 130 | mV | COMP = OPEN |
| | OVP2 Bias current (*1) | Iovp2 | -0.5 | -0.3 | -0.05 | μA | Measured pin: OVP2 |
| | FB Open Detect Threshold voltage | Vfbopen | 0.45 | 0.5 | 0.55 | V | |
| | FB Open Detect hysteresis | Vfbopen | 0.16 | 0.2 | 0.24 | V | |
| Over current protection | OCP Threshold voltage (*5) | VCL | 0.28 | 0.31 | 0.34 | V | |
| | OCP Threshold voltage (*6) | VCL | 2.9 | 3 | 3.1 | V | |
| | Delay to output | td-CL | — | 100 | 250 | ns | |

Notes: *1 Applied to R2A20104FP, R2A20114FP

*2 Applied to R2A20104SP, R2A20114SP

*5 Applied to R2A20114FP, R2A20114SP

*6 Applied to R2A20104FP, R2A20104SP

Electrical Characteristics (cont.)

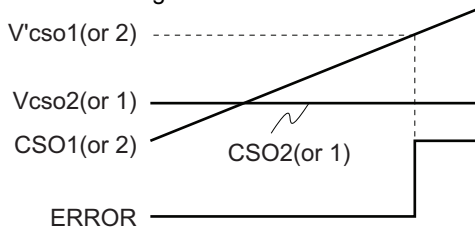
(Ta = 25°C, VCC = 12 V, CT = 1000 pF, RT = 27 kΩ, CS1, CS2 = GND, IRAMP = 10 kΩ, BO = 1 V, VAC = 0 V, RS = 220 kΩ, FMC = GND (*1), FM = GND (*2), FB = COMP)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|--------------|--------------------------------|--------|------|------|------|-----------------|---|
| Error signal | ERROR shunt current (*1) | 5.0 | — | — | mA | | |
| | ERROR leakage current (*1) | — | — | 1.0 | μA | | |
| | Phase error detect point | Perror | 1.1 | 1.35 | 1.6 | — | Vcso1 or 2 = 2.5 V, Vcso2 or 1: sweep (*7) |
| | OFF threshold voltage (*1) | Voff | 3.3 | 4.0 | 4.7 | V | |
| | E-DELAY charge current (*1) | led-c | -55 | -36 | -20 | μA | |
| | E-DELAY discharge current (*1) | led-d | 20 | 36 | 55 | μA | |
| | E-DELAY threshold voltage (*1) | Vdelay | 2.35 | 2.45 | 2.55 | V | |

Notes: *1 Applied to R2A20104FP, R2A20114FP

*2 Applied to R2A20104SP, R2A20114SP

*7 Refer to the figure shown below:



$$P_{error} = \frac{V'_{cso1(or 2)}[V] - 0.55[V]}{V_{cso2(or 1)}[V] - 0.55[V]}$$

Package Dimensions

• R2A20104FP and R2A20114FP

| | | | |
|---|-------------------------------|--------------------------|--------------------|
| JEITA Package Code P-LQFP40-7x7-0.65 | RENEASAS Code PLQP0040JB-C | Previous Code FP-40EV | MASS[Typ.] 0.2g |
|---|-------------------------------|--------------------------|--------------------|

NOTE)
1. DIMENSIONS**1"AND**2"
DO NOT INCLUDE MOLD FLASH
2. DIMENSION**3"DOES NOT
INCLUDE TRIM OFFSET.

Terminal cross section
(Ni/Pd/Au plating)

Detail F

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| A ₂ | — | 1.40 | — |
| H _D | 8.8 | 9.0 | 9.2 |
| H _E | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.70 |
| A ₁ | 0.08 | 0.13 | 0.22 |
| b _p | 0.17 | 0.22 | 0.27 |
| b ₁ | — | — | — |
| c | 0.10 | 0.15 | 0.20 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| Ⓜ | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| Z _D | — | 0.575 | — |
| Z _E | — | 0.575 | — |
| L | 0.40 | 0.50 | 0.60 |
| L ₁ | — | 1.0 | — |

• R2A20104SP and R2A20114SP

| | | | |
|---|-------------------------------|---------------------------|---------------------|
| JEITA Package Code P-SOP20-5.5x12.6-1.27 | RENEASAS Code PRSP0020DD-B | Previous Code FP-20DAV | MASS[Typ.] 0.31g |
|---|-------------------------------|---------------------------|---------------------|

NOTE)
1. DIMENSIONS**1 (Nom)"AND**2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3"DOES NOT
INCLUDE TRIM OFFSET.

Terminal cross section
(Ni/Pd/Au plating)

Detail F

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | — | 12.60 | 13.0 |
| E | — | 5.50 | — |
| A ₂ | — | — | — |
| A ₁ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| b _p | 0.34 | 0.40 | 0.46 |
| b ₁ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| H _E | 7.50 | 7.80 | 8.00 |
| Ⓜ | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| L ₁ | — | 1.15 | — |

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