Data Sheet | July 25, 2011 | FN6378.4

34µA Micro-power Single and Dual Rail-to-Rail Input-Output (RRIO) Low Input Bias Current Op Amps

The ISL28168 and ISL28268 are micro-power operational amplifiers optimized for single supply operation over a power supply range of 2.4VDC to 5.5VDC. These devices draw minimal supply current and operate rail-to-rail at the input and output, while providing excellent DC-accuracy, noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micro-power supply current.

The parts feature an Input Range Enhancement Circuit (IREC), which enables them to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.25V above the positive supply and to 100mV below the negative supply with only a slight degradation of the CMRR performance. The output operation is rail-to-rail.

The 1/f corner of the voltage noise spectrum is at 100Hz. This results in low frequency noise performance, which can only be found on devices with an order of magnitude higher supply current.

ISL28168 and ISL28268 can be operated from one lithium cell or two Ni-Cd batteries. The ISL28168 contains an enable pin feature that allows the device to be shutdown when not in use.

Features

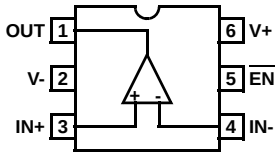
- 34µA typical supply current
- 10pA typical input bias current
- 200kHz gain bandwidth product
- 2.4V to 5.5V single supply voltage range
- Rail-to-rail input and output
- Enable pin (ISL28168 only)
- Pb-free (RoHS compliant)

Applications

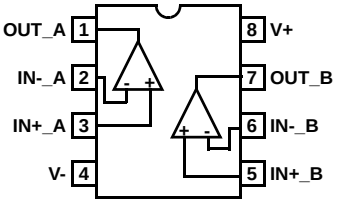
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

Pinouts

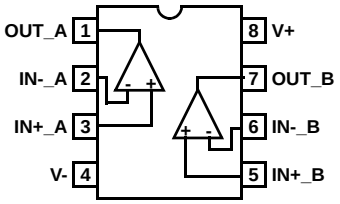
ISL28168
(6 LD SOT-23)
TOP VIEW



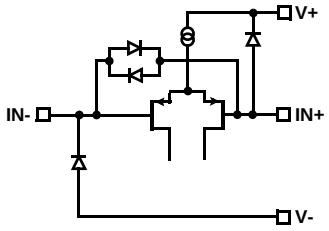
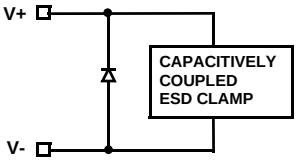
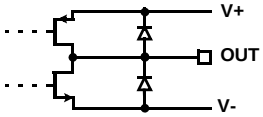
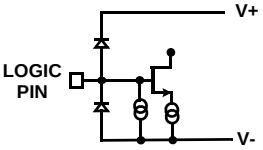
ISL28268
(8 LD SOIC)
TOP VIEW



ISL28268
(8 LD MSOP)
TOP VIEW



Pin Descriptions

ISL28168 (6 Ld SOT-23)	ISL28268 (8 Ld SOIC) (8 Ld MSOP)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
4	2 (A) 6 (B)	IN- IN-_A IN-_B	Inverting input	 CIRCUIT 1
3	3 (A) 5 (B)	IN+ IN+_A IN+_B	Non-inverting input	See Circuit 1
2	4	V-	Negative supply	 CIRCUIT 2
1	1 (A) 7 (B)	OUT OUT_A OUT_B	Output	 CIRCUIT 3
6	8	V+	Positive supply	See Circuit 2
5		$\overline{EN}$	Chip enable	 CIRCUIT 3

Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL28168FHZ-T7 (Note 1)	GACA (Note 5)	6 Ld SOT-23	P6.064A
ISL28168FHZ-T7A (Note 1)	GACA (Note 5)	6 Ld SOT-23	P6.064A
ISL28268FBZ (Note 2)	28268 FBZ	8 Ld SOIC	M8.15E
ISL28268FUZ (Note 2)	8268Z	8 Ld MSOP	M8.118A
ISL28168EVAL1Z	Evaluation Board - 6 Ld SOT-23		
ISL28268SOICEVAL1Z	Evaluation Board - 8 Ld SOIC		
ISL28268MSOPEVAL1Z	Evaluation Board - 8 Ld MSOP		

1. Please refer to TB347 for details on reel specifications.
2. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL28168, ISL28268. For more information on MSL please see techbrief TB363.
5. The part marking is located on the bottom of the part.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.75V
Supply Turn-on Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
Human Body Model 3kV
Machine Model 300V
Charge Device Model 1500V

Thermal Information

Thermal Resistance (Note 6)	θ_{JA} (°C/W)
6 Ld SOT-23 Package	230
8 Ld SOIC Package	120
8 Ld MSOP Package	160

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-Free Reflow Profilesee link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	ISL28168	-1.6 **-1.8**	±0.09	1.6 **1.8**	mV
		ISL28268	-2.4 **-2.6**	±0.09	2.4 **2.6**	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			0.3		µV/°C
I_{OS}	Input Offset Current	T_A = -40°C to +85°C	-35 **-80**	±5	35 **80**	pA
I_B	Input Bias Current	T_A = -40°C to +85°C	-30 **-80**	±10	30 **80**	pA
CMIR	Common-Mode Voltage Range	Guaranteed by CMRR	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	75 **70**	98		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5.5V	80 **75**	98		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ to V_{CM}	100 **75**	220		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ to V_{CM}		45		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ to V_{CM}		5.5	6 **20**	mV
		Output low, R_L = 1kΩ to V_{CM}		135	150 **250**	mV
		Output high, R_L = 100kΩ to V_{CM}	4.992 **4.990**	4.995		V
		Output high, R_L = 1kΩ to V_{CM}	4.84 **4.77**	4.874		V
$I_{S,ON}$	Quiescent Supply Current, Enabled	Per Amp		34	43 **55**	µA

Electrical Specifications $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open, $T_A = +25°C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$I_{S,OFF}$	Quiescent Supply Current, Disabled (ISL28168)			10	14 **19**	µA
I_O+	Short-Circuit Output Source Current	$R_L = 10\Omega$ to V_{CM}	27 **15**	30		mA
I_O-	Short-Circuit Output Sink Current	$R_L = 10\Omega$ to V_{CM}		-25	-22 **-15**	mA
V_{SUPPLY}	Supply Operating Range	V_+ to V_-	2.4		5.5	V
V_{INH}	$\overline{EN}$ Pin High Level (ISL28168)		2			V
V_{INL}	$\overline{EN}$ Pin Low Level (ISL28168)				0.8	V
I_{ENH}	$\overline{EN}$ Pin Input High Current (ISL28168)	$V_{\overline{EN}} = V_+$		1	1.5 **1.6**	µA
I_{ENL}	$\overline{EN}$ Pin Input Low Current (ISL28168)	$V_{\overline{EN}} = V_-$		12	25 **30**	nA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	$A_V = 100$, $R_F = 100k\Omega$, $R_G = 1k\Omega$, $R_L = 10k\Omega$ to V_{CM}		200		kHz
Unity Gain Bandwidth	-3dB Bandwidth	$A_V = 1$, $R_F = 0\Omega$, $V_{OUT} = 10mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		420		kHz
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		1.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz		64		$nV/\sqrt{Hz}$
i_N	Input Noise Current Density	f_O = 10kHz		0.19		$pA/\sqrt{Hz}$
CMRR @ 60Hz	Input Common Mode Rejection Ratio	$V_{CM} = 1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		-70		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio - +V	V_+, V_- = ±1.2V and ±2.5V, $V_{SOURCE} = 1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		-64		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio - -V	V_+, V_- = ±1.2V and ±2.5V $V_{SOURCE} = 1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		-85		dB
TRANSIENT RESPONSE						
SR	Slew Rate			0.1		V/µs
t_r, t_f, Large Signal	Rise Time, 10% to 90%, V_{OUT}	$A_V = +2$, $V_{OUT} = 1V_{P-P}$, $R_g = R_f = 10k\Omega$ $R_L = 10k\Omega$ to V_{CM}		10		µs
	Fall Time, 90% to 10%, V_{OUT}	$A_V = +2$, $V_{OUT} = 1V_{P-P}$, $R_g = R_f = 10k\Omega$ $R_L = 10k\Omega$ to V_{CM}		9		µs
t_r, t_f, Small Signal	Rise Time, 10% to 90%, V_{OUT}	$A_V = +2$, $V_{OUT} = 10mV_{P-P}$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		650		ns
	Fall Time, 90% to 10%, V_{OUT}	$A_V = +2$, $V_{OUT} = 10mV_{P-P}$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		640		ns
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}, (ISL28168)	$V_{\overline{EN}}$ = 5V to 0V, $A_V = +2$, $R_g = R_f = R_L = 1k$ to V_{CM}		15		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}, (ISL28168)	$V_{\overline{EN}}$ = 0V to 5V, $A_V = +2$, $R_g = R_f = R_L = 1k$ to V_{CM}		0.5		µs

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$

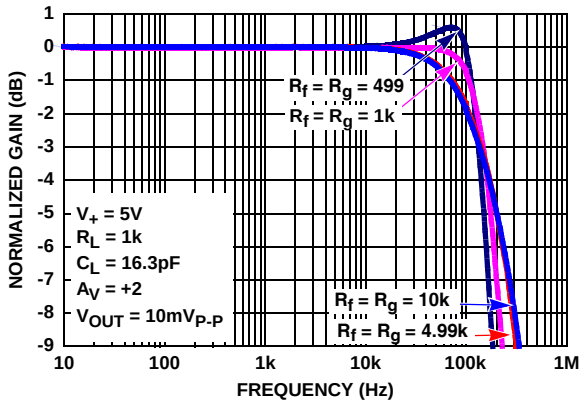


FIGURE 1. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

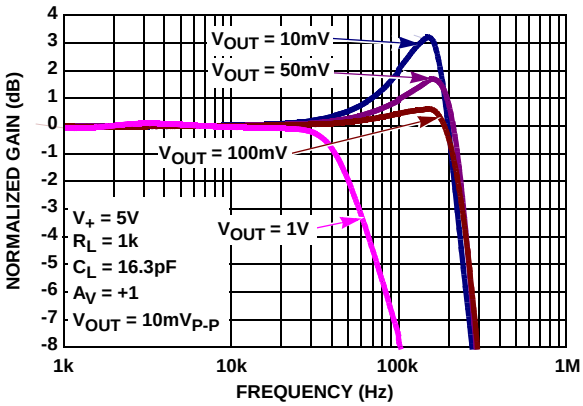


FIGURE 2. GAIN vs FREQUENCY vs V_{OUT}, R_L = 1k

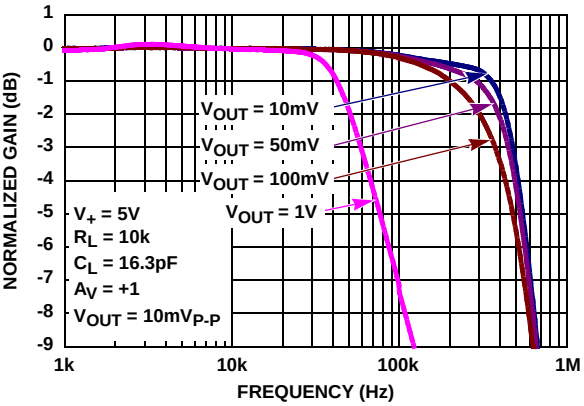


FIGURE 3. GAIN vs FREQUENCY vs V_{OUT}, R_L = 10k

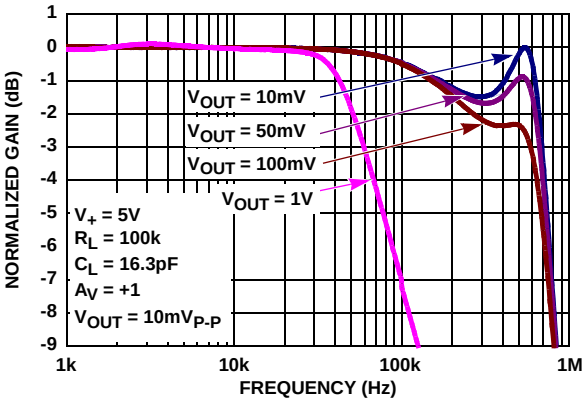


FIGURE 4. GAIN vs FREQUENCY vs V_{OUT}, R_L = 100k

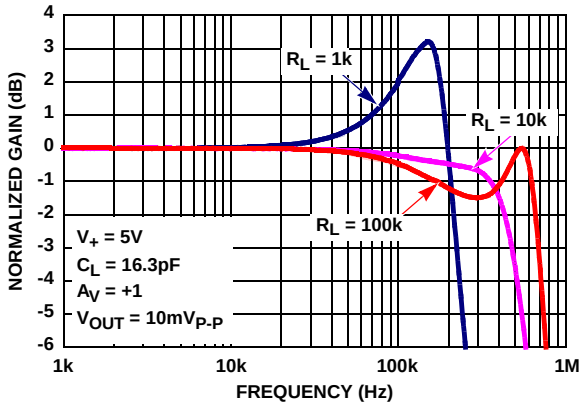


FIGURE 5. GAIN vs FREQUENCY vs R_L

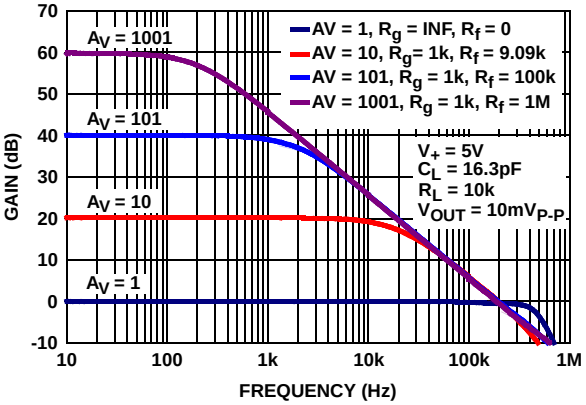


FIGURE 6. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

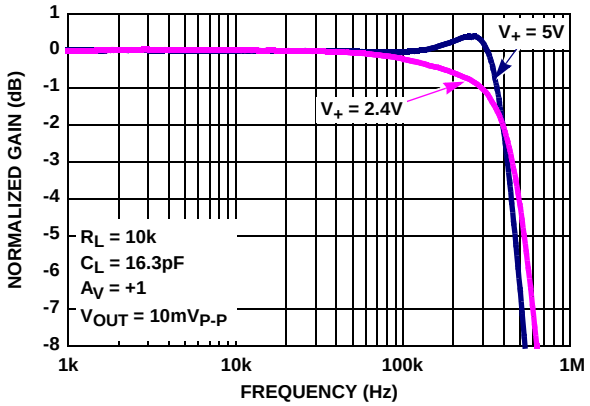


FIGURE 7. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

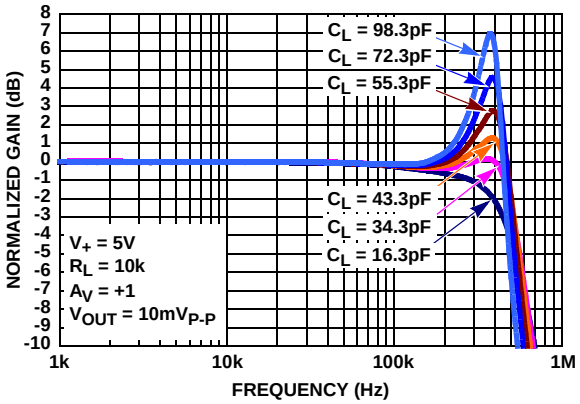


FIGURE 8. GAIN vs FREQUENCY vs C_L

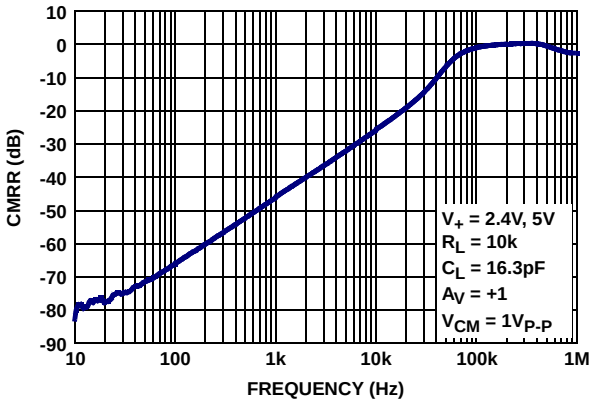


FIGURE 9. CMRR vs FREQUENCY, $V_+ = 2.4V$ AND 5V

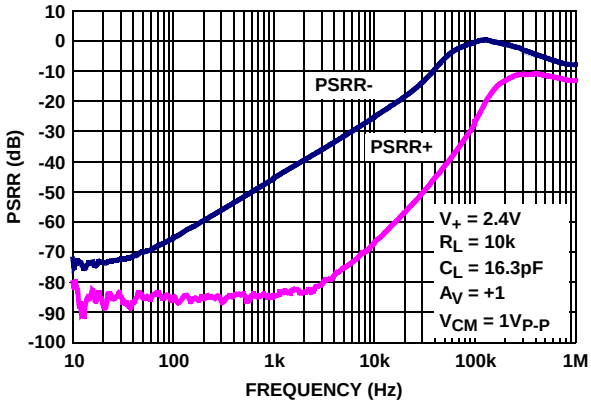


FIGURE 10. PSRR vs FREQUENCY, V_+, V_- = ±1.2V

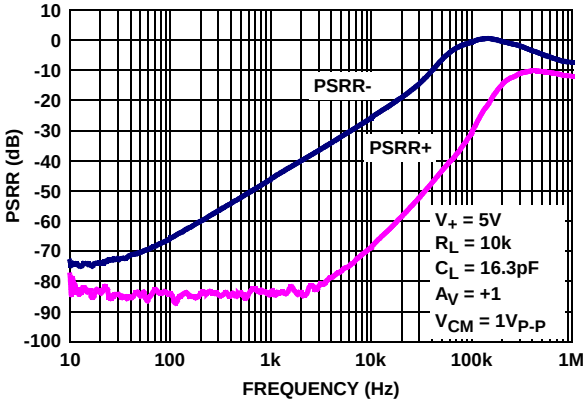


FIGURE 11. PSRR vs FREQUENCY, V_+, V_- = ±1.2V

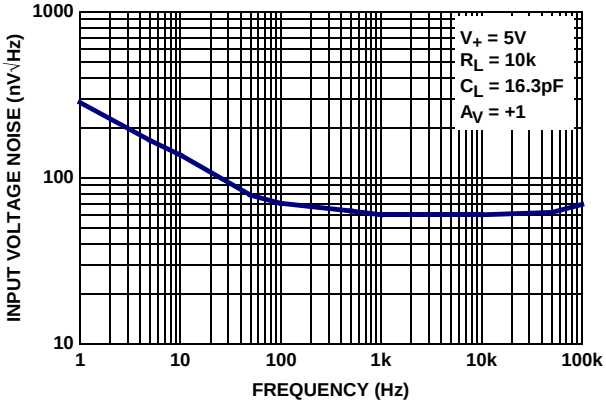


FIGURE 12. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

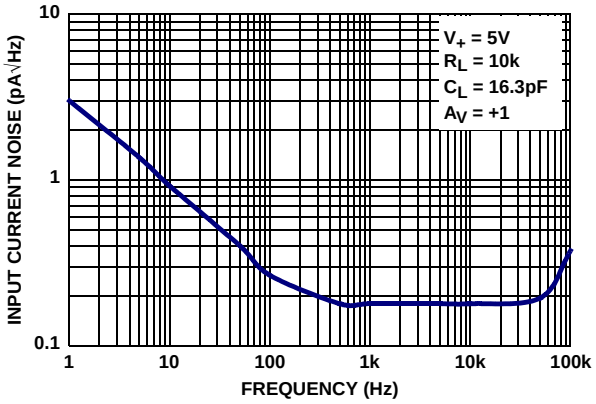


FIGURE 13. INPUT CURRENT NOISE DENSITY vs FREQUENCY

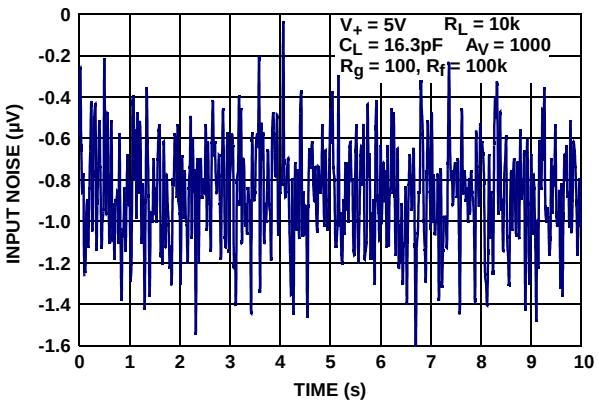


FIGURE 14. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz

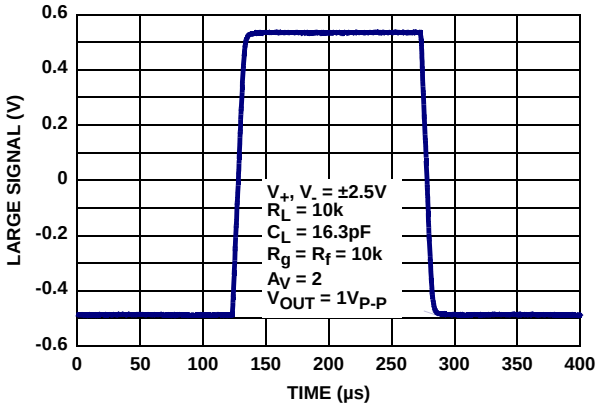


FIGURE 15. LARGE SIGNAL STEP RESPONSE

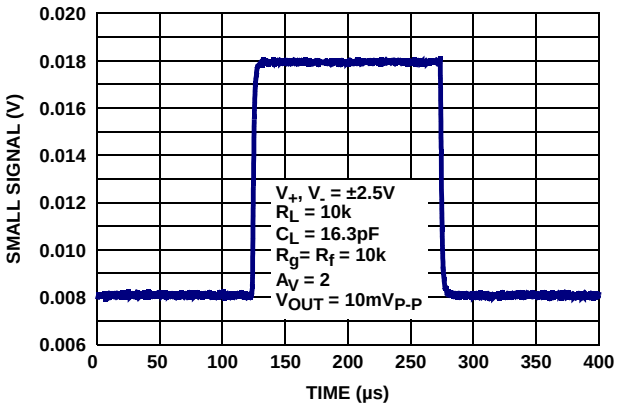


FIGURE 16. SMALL SIGNAL STEP RESPONSE

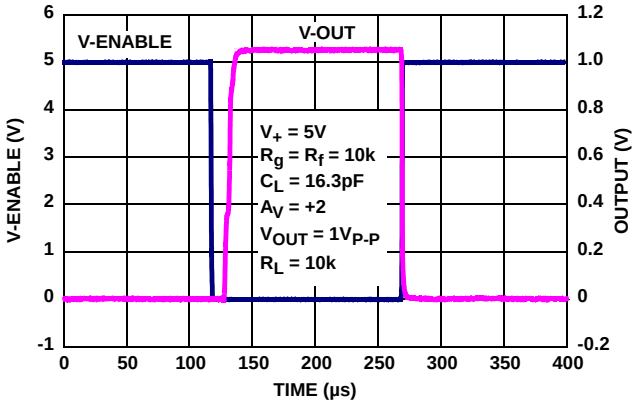


FIGURE 17. ISL28168 ENABLE TO OUTPUT RESPONSE

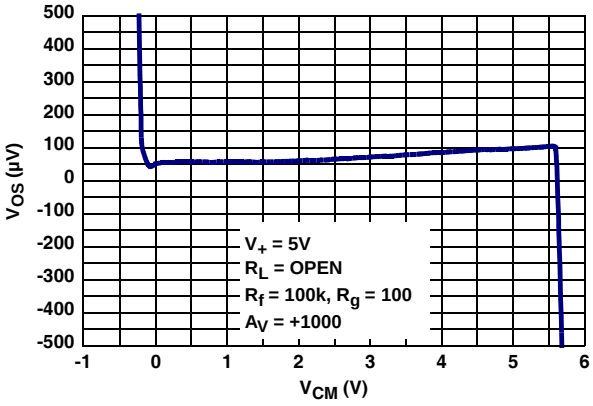


FIGURE 18. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

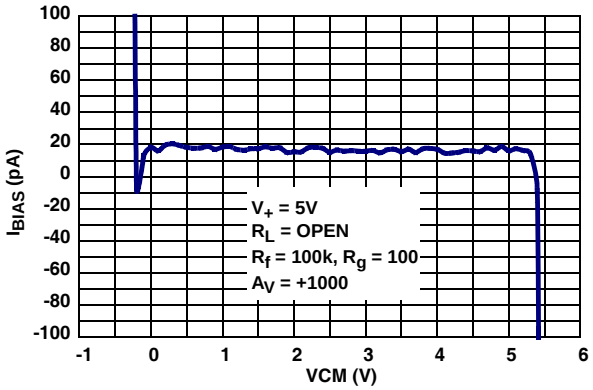


FIGURE 19. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE

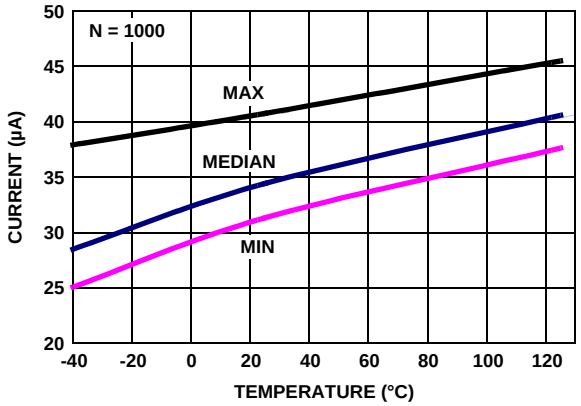


FIGURE 20. SUPPLY CURRENT ENABLED vs TEMPERATURE, V_+, V_- = ±2.5V

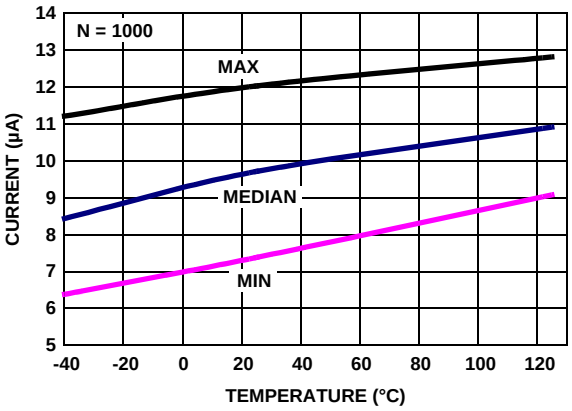


FIGURE 21. SUPPLY CURRENT DISABLED vs TEMPERATURE, V_+, V_- = ±2.5V

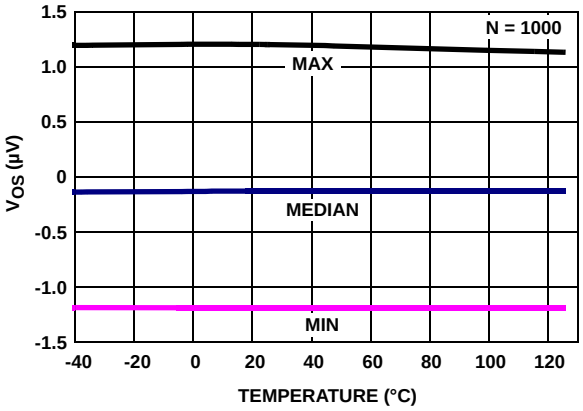


FIGURE 22. V_{OS} (SOT PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.75V

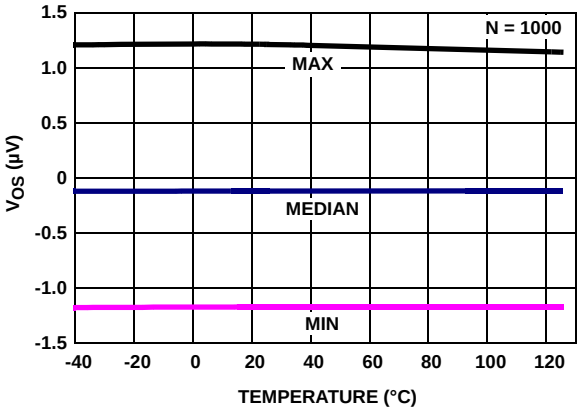


FIGURE 23. V_{OS} (SOT PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.5V

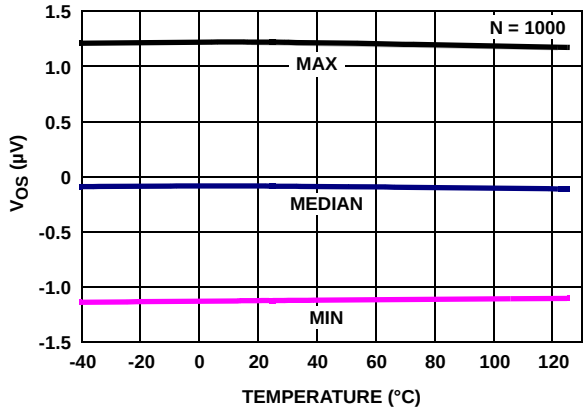


FIGURE 24. V_{OS} (SOT PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±1.2V

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

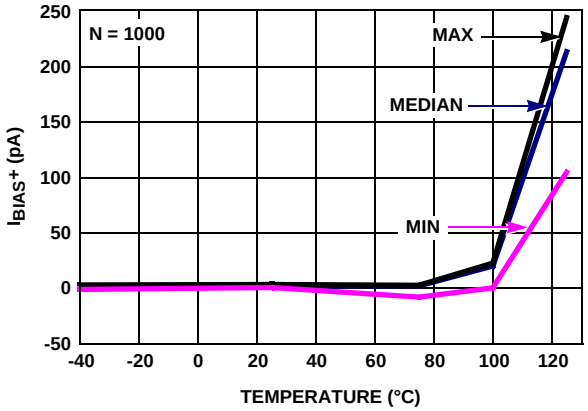


FIGURE 25. $I_{BIAS}+$ vs TEMPERATURE, V_+, V_- = ±2.5V

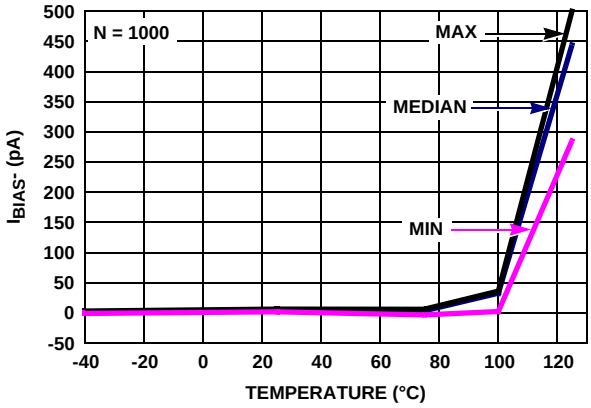


FIGURE 26. $I_{BIAS}-$ vs TEMPERATURE, V_+, V_- = ±2.5V

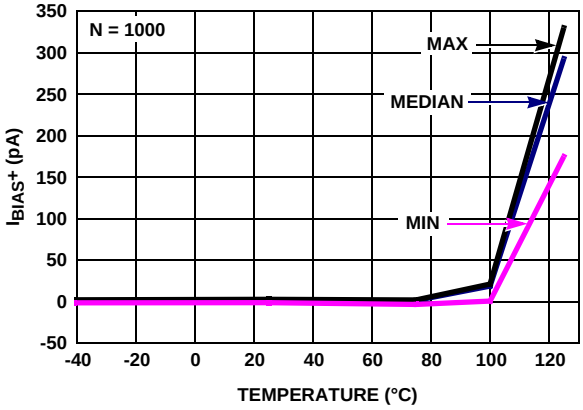


FIGURE 27. $I_{BIAS}+$ vs TEMPERATURE, V_+, V_- = ±1.2V

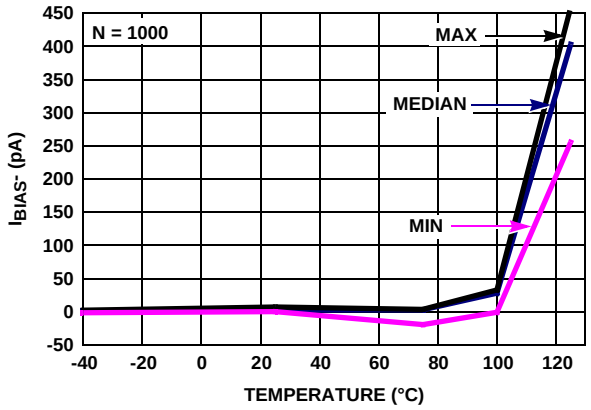


FIGURE 28. $I_{BIAS}-$ vs TEMPERATURE, V_+, V_- = ±1.2V

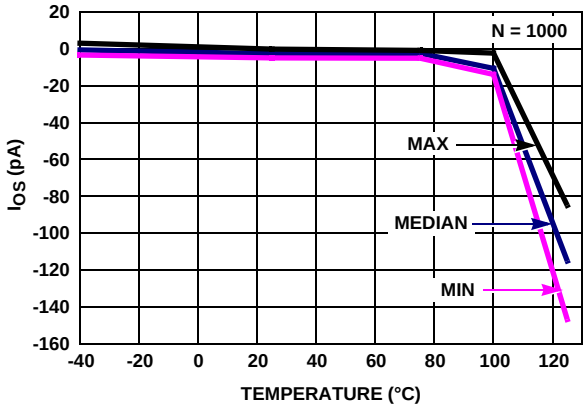


FIGURE 29. I_{OS} vs TEMPERATURE, V_+, V_- = ±2.5

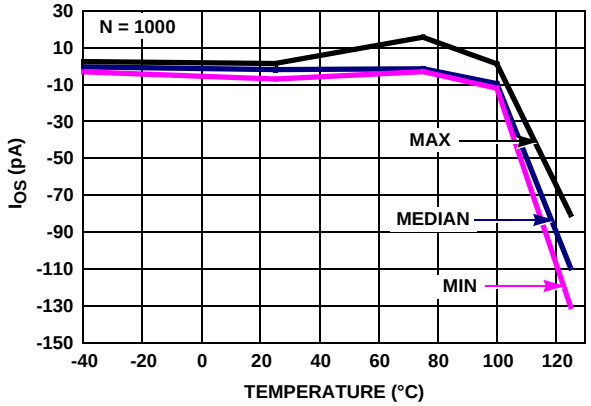


FIGURE 30. I_{OS} vs TEMPERATURE, V_+, V_- = ±1.2V

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

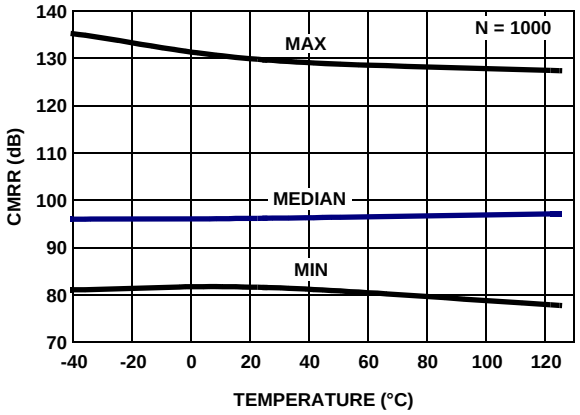


FIGURE 31. CMRR vs TEMPERATURE, V_{CM} = -2.5V TO +2.5V, V_+, V_- = ±2.5V

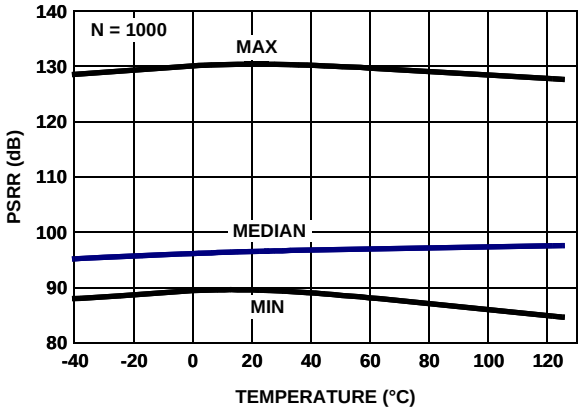


FIGURE 32. PSRR vs TEMPERATURE, V_+, V_- = ±1.2V TO ±2.75V

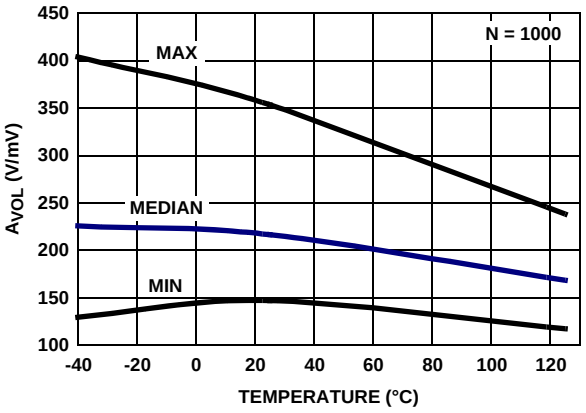


FIGURE 33. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, V_O = -2V TO +2V, R_L = 100k

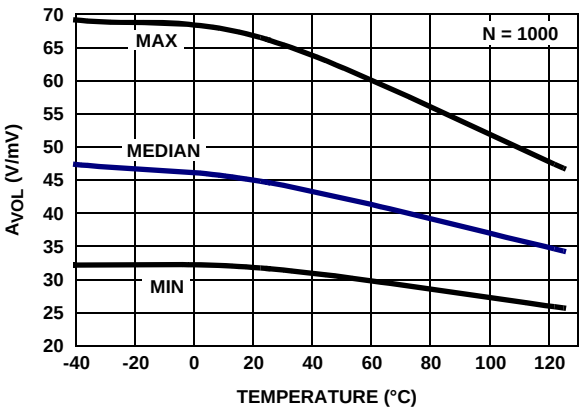


FIGURE 34. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, V_O = -2V TO +2V, R_L = 1k

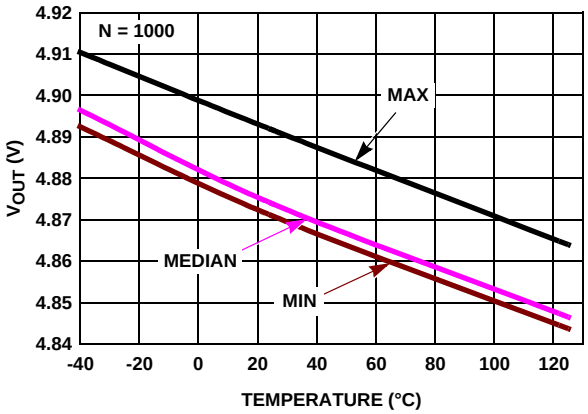


FIGURE 35. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

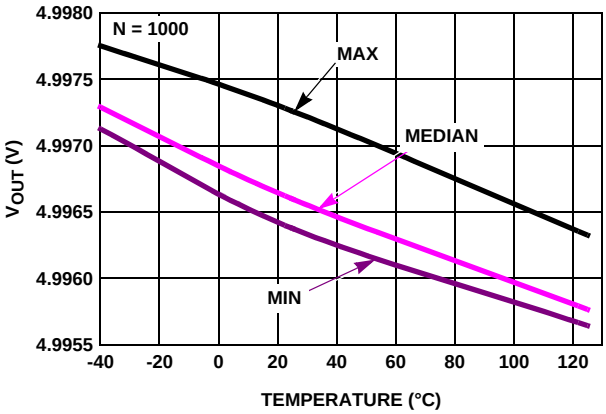


FIGURE 36. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

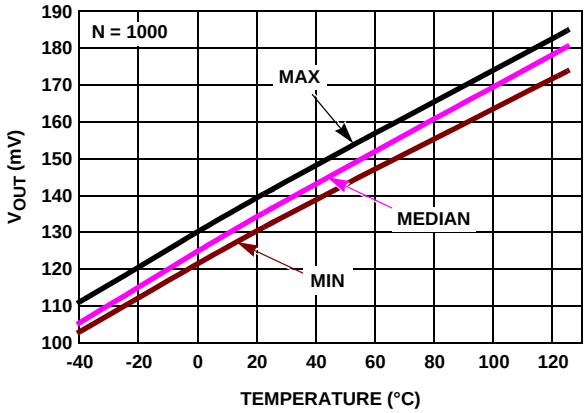


FIGURE 37. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

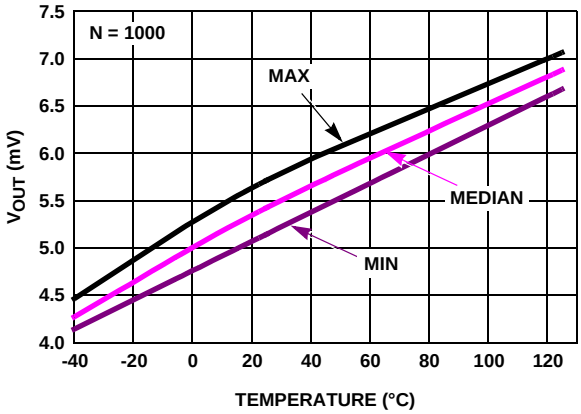


FIGURE 38. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

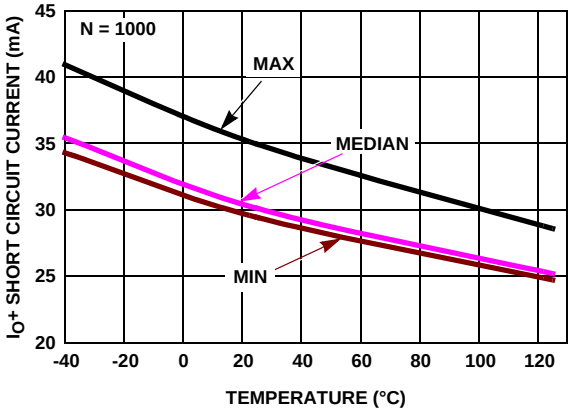


FIGURE 39. I_O+ SHORT CIRCUIT OUTPUT CURRENT vs TEMPERATURE, V_{IN} = -2.55V, R_L = 10k, V_+, V_- = ±2.5V

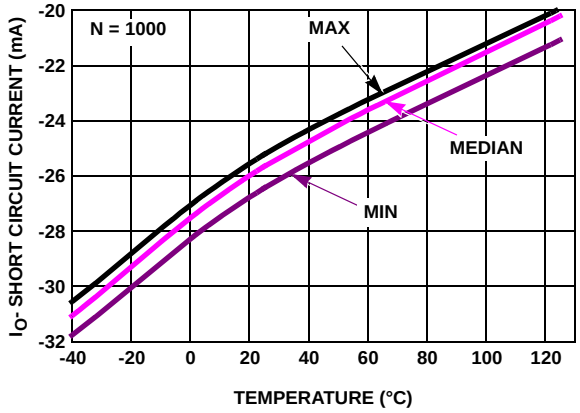


FIGURE 40. I_O- SHORT CIRCUIT OUTPUT CURRENT vs TEMPERATURE, V_{IN} = +2.55V, R_L = 10k, V_+, V_- = ±2.5V

Applications Information

Introduction

The ISL28168 is a single CMOS rail-to-rail input, output (RRIO) operational amplifier with an enable feature. The ISL28268 is a dual version without the enable feature. Both devices are designed to operate from single supply (2.4V to 5.5V) or dual supplies (±1.2V to ±2.75V).

Rail-to-Rail Input/Output

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28168 and ISL28268 achieve input rail-to-rail operation without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives us an undistorted behavior from typically 100mV below the negative rail, and 0.25V higher than the V+ rail. The CMOS output stage features excellent drive capability, typically swinging to within 6mV of either rail with a 100kΩ load.

Results of Over-Driving the Output

Caution should be used when over-driving the output for long periods of time. Over-driving the output can occur in two ways.

1. The input voltage times the gain of the amplifier exceeds the supply voltage by a large value

2. The output current required is higher than the output stage can deliver. These conditions can result in a shift in the Input Offset Voltage (V_{OS}) as much as 1µV/hr. of exposure under these conditions.

IN+ and IN- Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals (see "Pin Descriptions" on page 2 - Circuit 1). For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 5mA (see Figure 41).

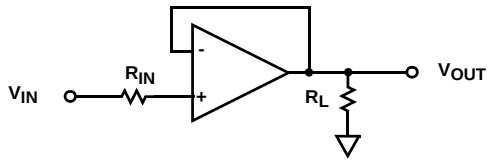


FIGURE 41. INPUT CURRENT LIMITING

Enable/Disable Feature

The ISL28168 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10µA at room temperature. By disabling the part, multiple ISL28168 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. Note that feed through from the IN+ to IN- pins occurs on any Mux Amp disabled channel where the input differential voltage exceeds 0.5V (e.g., active channel V_{OUT} = 1V, while disabled channel V_{IN} = GND), so the Mux implementation is best suited for small signal applications. If large signals are required, use series IN+ resistors, or large value R_F, to keep the feed-through current low enough to minimize the impact on the active channel. See "Limitations of the Differential Input Protection" on page 13 for more details.

To disable the part, the user needs to supply the 1.5µA required to pull the $\overline{EN}$ pin to the V_+ rail. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default. If the $\overline{EN}$ function is not required (no need to turn the part off), as a precaution, it is recommended that the user tie the $\overline{EN}$ pin to the V_- pin.

Limitations of the Differential Input Protection

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For non inverting unity gain applications, the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback (R_F) and gain setting (R_G) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

1. During open loop (comparator) operation. Used this way, the IN+ and IN- voltages don't track, so differentials arise.
2. When the amplifier is disabled but an input signal is still present. An R_L or R_G to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel V_{OUT} determines the voltage on the IN- terminal.
3. When the slew rate of the input pulse is considerably faster than the op amp's slew rate. If the V_{OUT} can't keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 0.1V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled I_{CC}.

Using Only One Channel

The ISL28268 is a dual op amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 42).

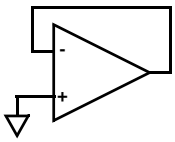


FIGURE 42. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 43 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents,

components can be mounted to the PC board using Teflon standoff insulators.

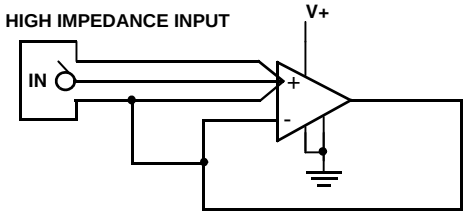


FIGURE 43. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

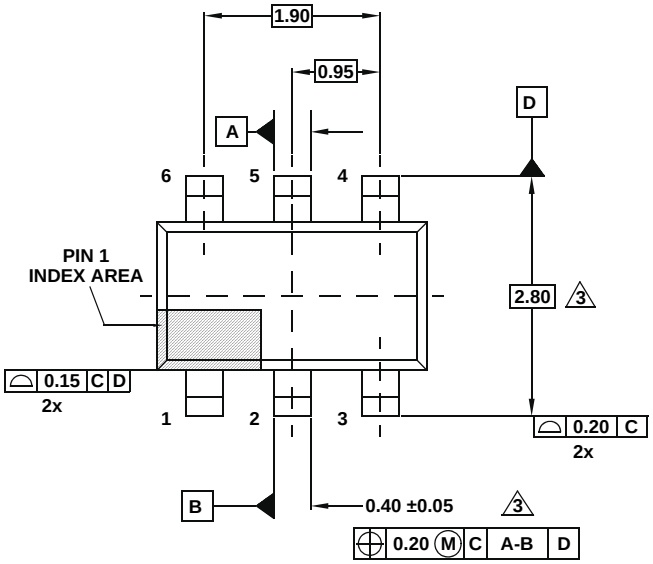
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

R_L = Load resistance

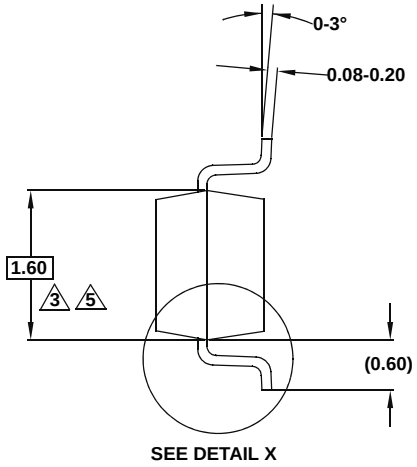
Package Outline Drawing

P6.064A

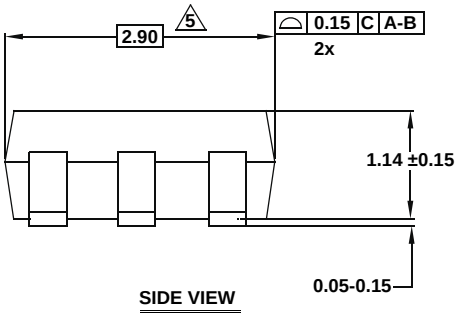
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



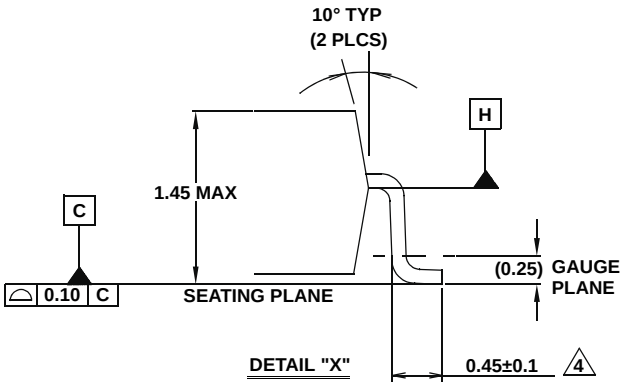
TOP VIEW

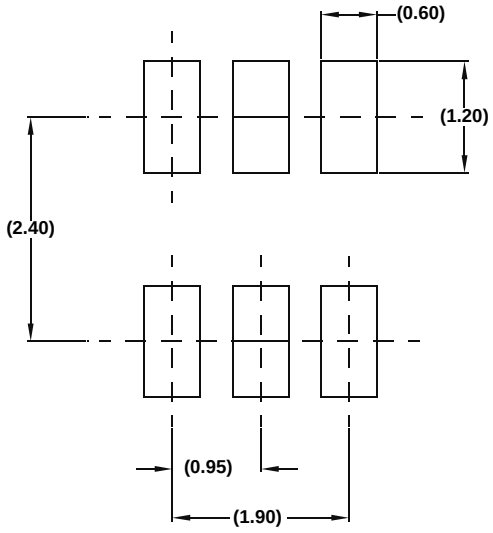


END VIEW



SIDE VIEW





TYPICAL RECOMMENDED LAND PATTERN

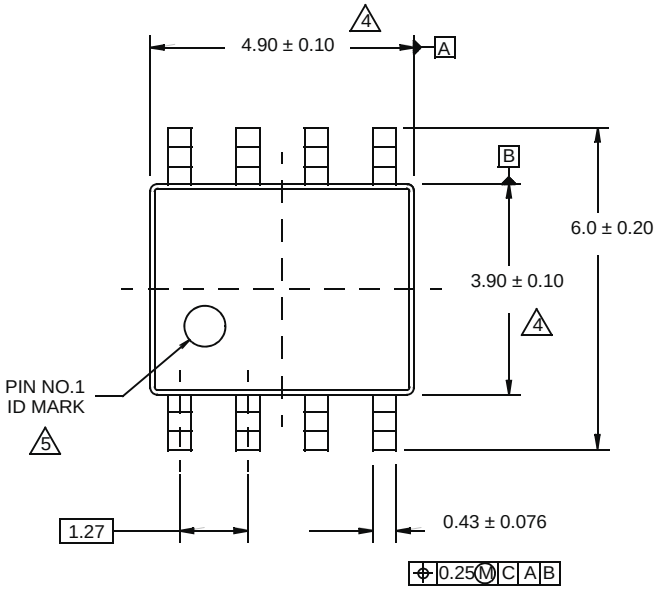
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

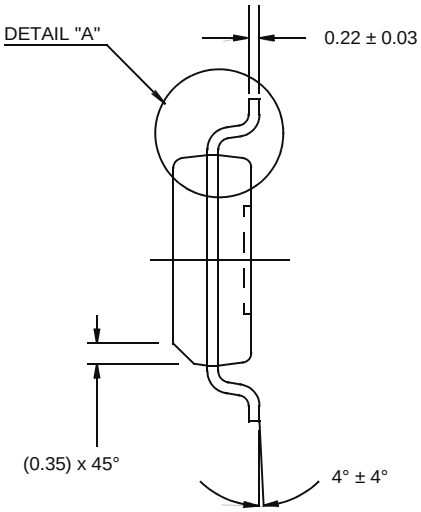
Package Outline Drawing

M8.15E

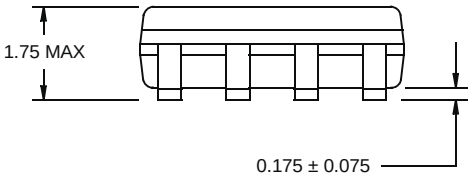
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



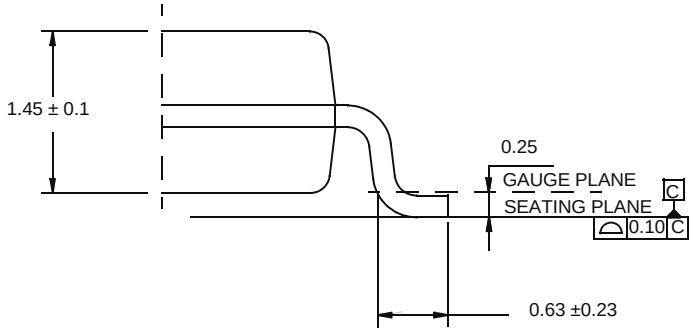
TOP VIEW



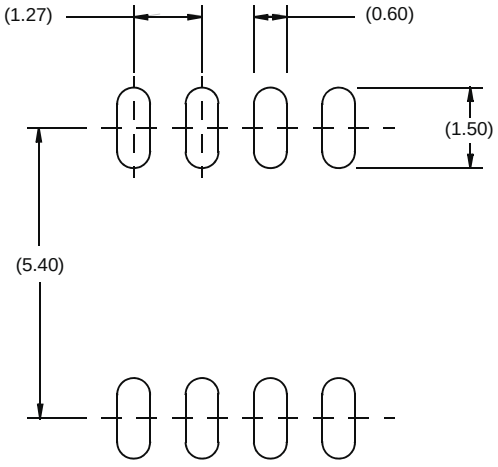
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

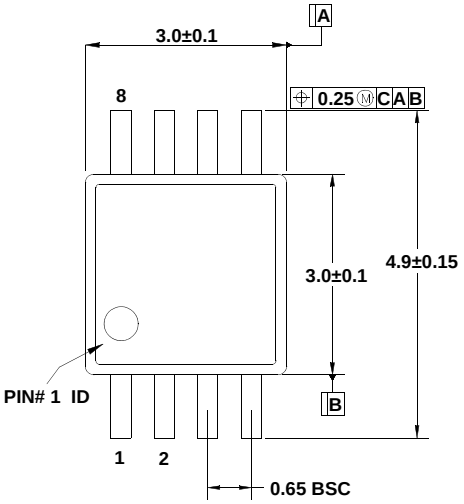
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

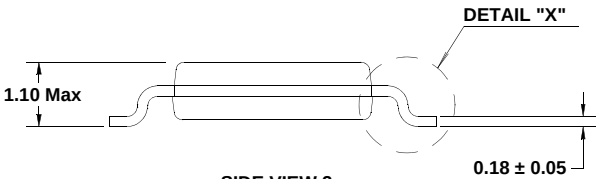
Package Outline Drawing

M8.118A

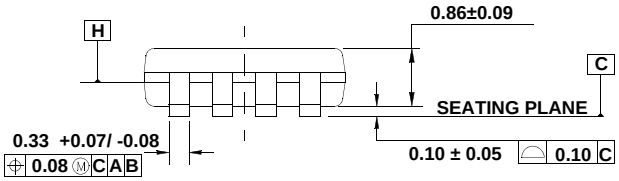
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



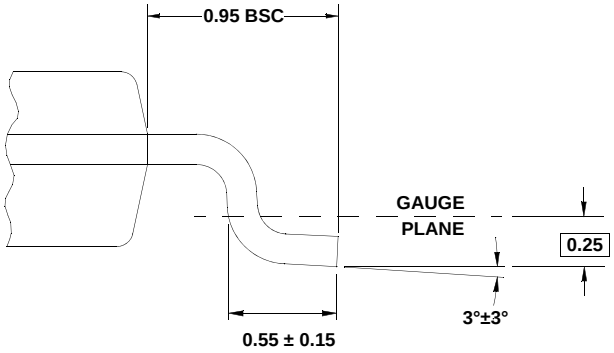
TOP VIEW



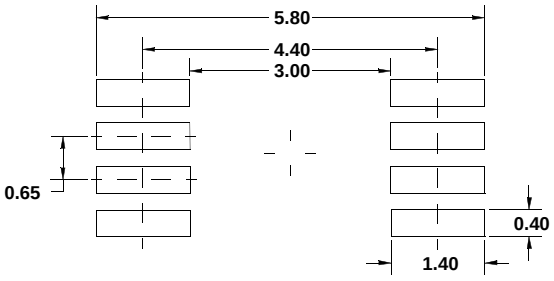
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.