

FEATURES

- High Slew Rate 130V/ μ s Min
- Fast Settling Time (+10V, 0.1%) 100ns Typ
- Gain-Bandwidth Product ($A_{VCL} = +5$) 80MHz Typ
- Low Supply Current 8mA Max
- Low Noise 8nV/ $\sqrt{\text{Hz}}$ Typ
- Low Offset Voltage 1mV Max
- High Output Current ± 80 mA Typ
- Eliminates External Buffer
- Standard 8-Pin Packages
- Available in Die Form

ORDERING INFORMATION [†]

$T_A = +25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC 8-PIN	HERMETIC LCC 20-CONTACT	
1.0	OP64AJ*	OP64AZ*	—	OP64ARC/883	MIL
1.0	OP64EJ	OP64EZ	—	—	XIND
2.0	OP64FJ	OP64FZ	—	—	XIND
2.5	—	—	OP64GP	—	XIND
2.5	—	—	OP64GS ^{††}	—	XIND

XIND = Extended Industrial Temperature Range, -40°C to $+85^\circ\text{C}$

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-99 can packages.

^{††} For availability and burn-in information on SO and PLCC packages, contact your local sales office.

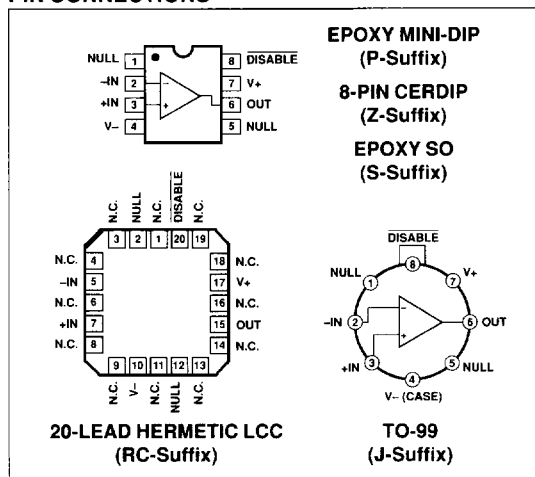
GENERAL DESCRIPTION

The OP-64 is a high-performance monolithic operational amplifier that combines high speed and wide bandwidth with low power consumption. Advanced processing techniques have en-

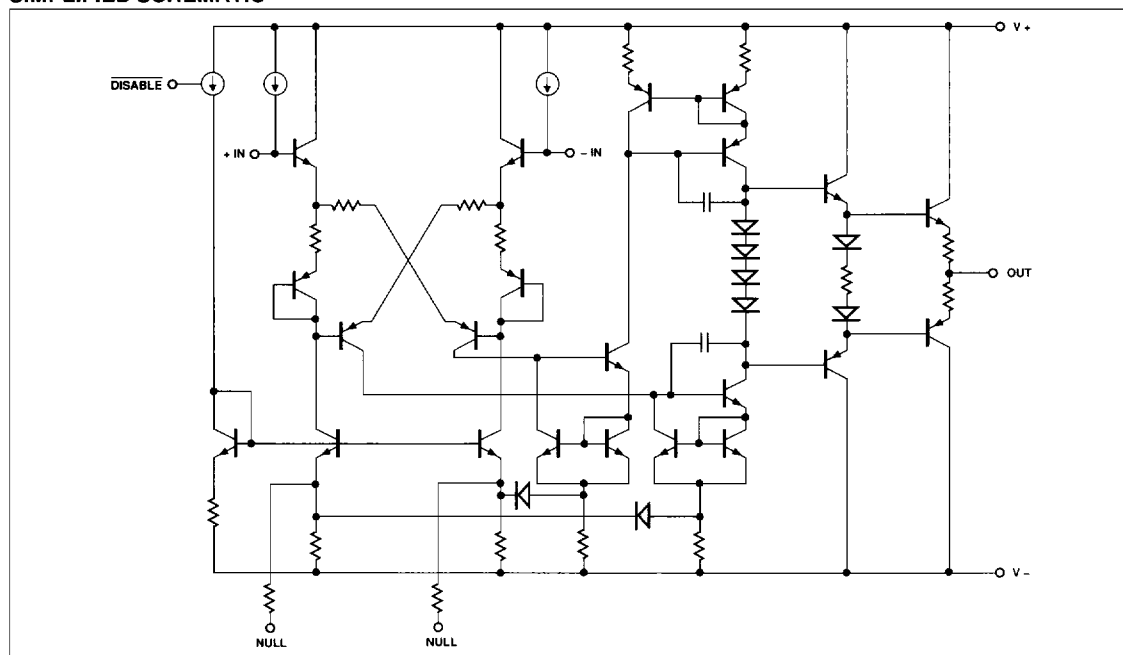
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2

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OP-64

GENERAL DESCRIPTION *Continued*

enabled PMI to make the OP-64 superior in cost and performance to many dielectrically-isolated and hybrid op amps.

Slew rate of the OP-64 is over 130V/ μ s. It is stable in gains of ≥ 5 and has a settling time of only 100ns to 0.1% with a 10V step input. However, unlike other high-speed op amps which have high supply requirements, the OP-64 needs less than 8mA of supply current. This enables the OP-64 to be packaged in space saving 8-pin packages. The OP-64 can deliver ± 80 mA of output current eliminating the need for a separate buffer amplifier in many applications. Noise of the OP-64 is only 8nV/Hz, reducing system noise in wideband applications. In addition to its dynamic performance, the OP-64 adds DC precision with an input offset voltage of under 1mV.

The OP-64 is an ideal choice for RF, video and pulse amplifier applications and in new designs can replace the HA-5190/95 or EL-2190/95 with improved performance and reduced power consumption. Its high output current also suits the OP-64 for use in A/D or cable driver applications. The OP-64 includes a DIS-ABLE pin which, when set low, shuts the amplifier off and reduces the supply current to 0.75mA.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	± 18 V
Input Voltage	Supply Voltage
Differential Input Voltage	20V

DISABLE Input Voltage	Supply Voltage
Output Short-Circuit Duration	10 sec
Storage Temperature Range (J, Z, RC)	-65°C to $+175^{\circ}\text{C}$
(P, S)	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range OP-64A (J, Z, RC)	-55°C to $+125^{\circ}\text{C}$
OP-64E, F (J, Z)	-40°C to $+85^{\circ}\text{C}$
OP-64G (P, S)	-40°C to $+85^{\circ}\text{C}$
Maximum Junction Temperature OP-64A (J, Z, RC)	$+175^{\circ}\text{C}$
OP-64E, F (J, Z)	$+175^{\circ}\text{C}$
OP-64G (P, S)	$+150^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^{\circ}\text{C}$

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
TO-99 (J)	150	18	$^{\circ}\text{C/W}$
8-Pin Hermetic DIP (Z)	148	16	$^{\circ}\text{C/W}$
8-Pin Plastic DIP (P)	103	43	$^{\circ}\text{C/W}$
20-Contact LCC (RC, TC)	98	38	$^{\circ}\text{C/W}$
8-Pin SO (S)	158	43	$^{\circ}\text{C/W}$

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15$ V, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A/E			OP-64F			OP-64G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.4	1	—	0.8	2	—	1.2	2.5	mV
Input Bias Current	I_B	$V_{CM} = 0$ V	—	0.2	1	—	0.4	2	—	0.8	2.5	μ A
Input Offset Current	I_{OS}	$V_{CM} = 0$ V	—	0.1	1	—	0.3	2	—	0.6	2.5	μ A
Input Voltage Range	IVR	(Note 1)	± 11	—	—	± 11	—	—	± 11	—	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11$ V	90	100	—	84	94	—	84	94	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5$ V to ± 18 V	—	5	17.8	—	15	31.6	—	15	31.6	μ V/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 2$ k Ω , $V_O = \pm 10$ V	30	45	—	20	35	—	20	35	—	V/mV
		$R_L = 200\Omega$, $V_O = \pm 5$ V	12.5	18	—	10	16	—	10	16	—	
Output Voltage Swing	V_O	$R_L = 2$ k Ω	± 11	± 12.5	—	± 11	± 12.5	—	± 11	± 12.5	—	V
		$R_L = 200\Omega$	± 10	± 11.7	—	± 10	± 11.7	—	± 10	± 11.7	—	
Output Current	I_{OUT}		—	± 80	—	—	± 80	—	—	± 80	—	mA
Supply Current	I_{SV}	No Load	—	6.2	8	—	6.2	8	—	6.2	8	mA

NOTE:

1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A/E			OP-64F			OP-64G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Disable Supply Current	$I_{SY \overline{DIS}}$	$\overline{DISABLE} = 0V$ Total for both supplies	—	0.75	1	—	0.75	1	—	0.75	1	mA
$\overline{DISABLE}$ Current	$I_{\overline{DIS}}$	$\overline{DISABLE} = 0V$	—	0.5	—	—	0.5	—	—	0.5	—	mA
Slew Rate	SR	$R_L = 2k\Omega$	130	170	—	130	170	—	130	170	—	V/ μs
Full-Power Bandwidth	BW_p	(Note 2)	2	2.7	—	2	2.7	—	2	2.7	—	MHz
Gain-Bandwidth Product	GBWP	$A_V = +5$	—	80	—	—	80	—	—	80	—	MHz
Settling Time	t_s	10V Step 0.1%	—	100	—	—	100	—	—	100	—	ns
Phase Margin	ϕ_m	$A_V = +5$	—	57	—	—	57	—	—	57	—	degrees
Input Capacitance	C_{IN}		—	5	—	—	5	—	—	5	—	pF
Open-Loop Output Resistance	R_O		—	30	—	—	30	—	—	30	—	Ω
Voltage Noise Density	e_n	$f_o = 10Hz$	—	30	—	—	30	—	—	30	—	nV/ $\sqrt{Hz}$
		$f_o = 100Hz$	—	10	—	—	10	—	—	10	—	
		$f_o = 1kHz$	—	8	—	—	8	—	—	8	—	
		$f_o = 10kHz$	—	8	—	—	8	—	—	8	—	
Current Noise Density	i_n	$f_o = 10kHz$	—	7.5	—	—	7.5	—	—	7.5	—	pA/ $\sqrt{Hz}$
External V_{OS} Trim Range	$R_{pot} = 20k\Omega$		—	4	—	—	4	—	—	4	—	mV
Supply Voltage Range	V_S		± 5	± 15	± 18	± 5	± 15	± 18	± 5	± 15	± 18	V

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.

OP-64

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40^\circ C \leq T_A \leq +85^\circ C$ for OP-64E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64E			OP-64F			OP-64G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		–	0.5	1.5	–	1.0	3	–	1.5	3.5	mV
Input Bias Current	I_B	$V_{CM} = 0V$	–	0.3	2.5	–	0.5	3	–	1.5	3.5	μA
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	0.2	2.5	–	0.5	3	–	1.0	3.5	μA
Input Voltage Range	IVR	(Note 1)	± 11	–	–	± 11	–	–	± 11	–	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11$	86	100	–	80	94	–	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 18V$	–	5	31.6	–	15	50	–	15	50	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$, $V_O = \pm 10V$	20	40	–	15	35	–	15	35	–	V/mV
		$R_L = 200\Omega$, $V_O = \pm 5V$	7.5	12	–	5	10	–	5	10	–	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 11	± 12.3	–	± 11	± 12.3	–	± 11	± 12.3	–	V
		$R_L = 200\Omega$	± 10	± 11.5	–	± 10	± 11.5	–	± 10	± 11.5	–	
Supply Current	I_{SY}	No Load	–	6.3	8.5	–	6.3	8.5	–	6.3	8.5	mA

NOTE:

1. Guaranteed by CMR test.

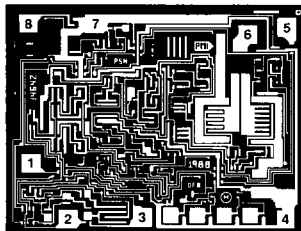
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-64A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A			UNITS
			MIN	TYP	MAX	
Offset Voltage	V_{OS}		–	0.4	2	mV
Input Bias Current	I_B	$V_{CM} = 0V$	–	0.35	2	μA
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	0.3	2	μA
Input Voltage Range	IVR	(Note 1)	± 11	–	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11$	86	100	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 18V$	–	8	31.6	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$, $V_O = \pm 10V$	20	30	–	V/mV
		$R_L = 200\Omega$, $V_O = \pm 5V$	7.5	10	–	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 11	± 12	–	V
		$R_L = 200\Omega$	± 7.5	± 10	–	
Supply Current	I_{SY}	No Load	–	6.4	8.5	mA

NOTE:

1. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. NULL
2. -IN
3. +IN
4. V-
5. NULL
6. OUT
7. V+
8. DISABLE

DIE SIZE 0.086 x 0.065 inch, 5,590 sq. mils
(2.18 x 1.65 mm, 3.60 sq. mm)

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

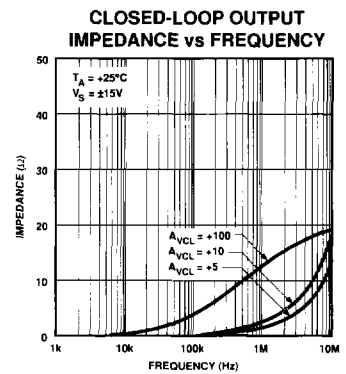
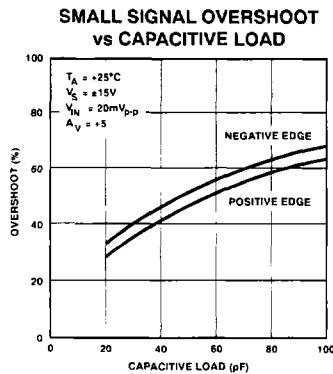
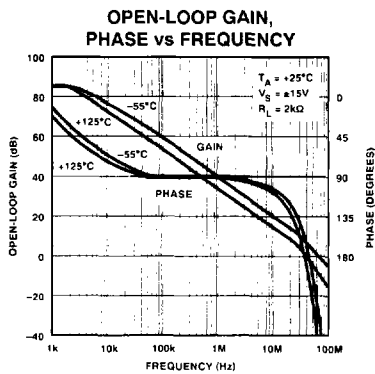
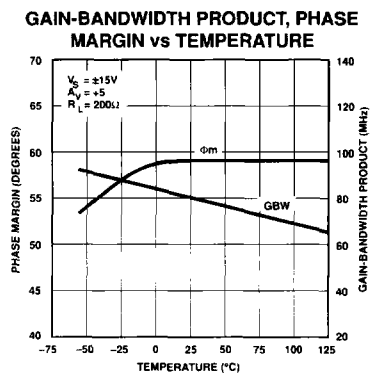
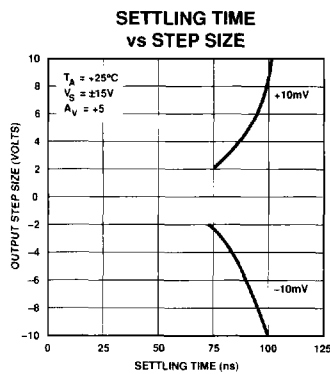
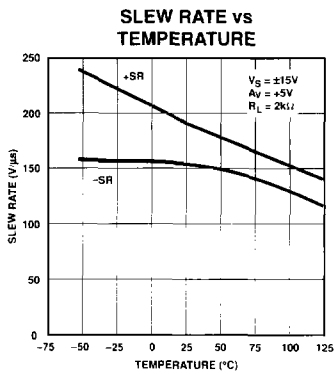
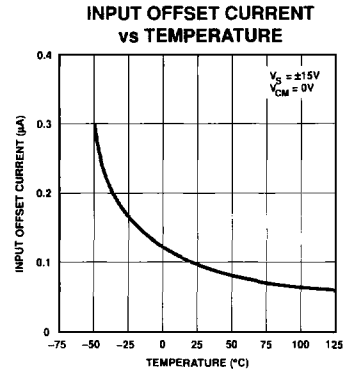
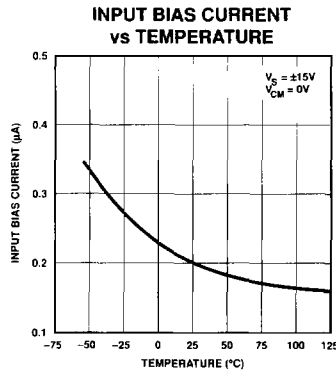
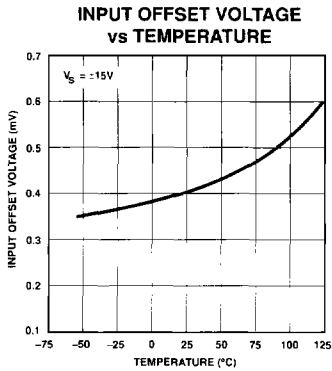
PARAMETER	SYMBOL	CONDITIONS	OP-64GBC LIMITS	UNITS
Offset Voltage	V_{OS}		2.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	2.5	μA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	2.5	μA MAX
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 18V$	31.6	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$, $V_O = \pm 10V$ $R_L = 200\Omega$, $V_O = \pm 5V$	20 10	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$ $R_L = 200\Omega$	± 11 ± 10	V MIN
Slew Rate	SR	$R_L = 2k\Omega$	120	V/ μs MIN
Supply Current	I_{SY}	No Load	8	mA MAX

NOTES:

1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

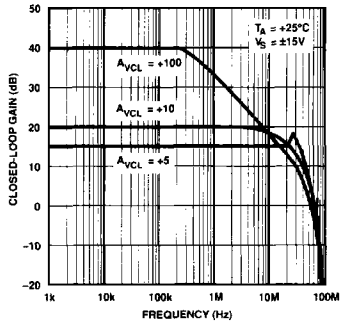
TYPICAL PERFORMANCE CHARACTERISTICS



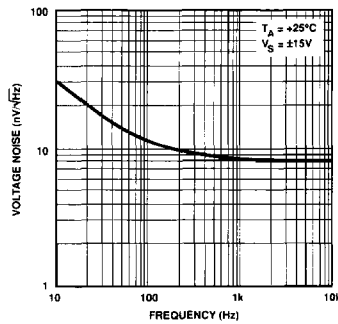
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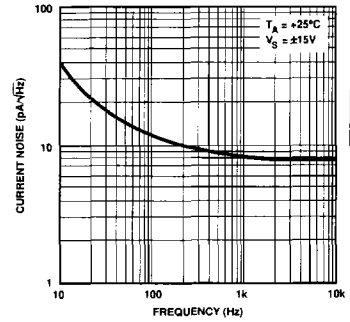
**CLOSED-LOOP GAIN
vs FREQUENCY**



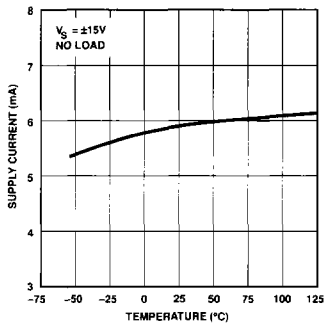
**VOLTAGE NOISE DENSITY
vs FREQUENCY**



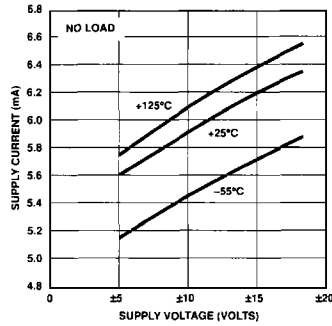
**CURRENT NOISE DENSITY
vs FREQUENCY**



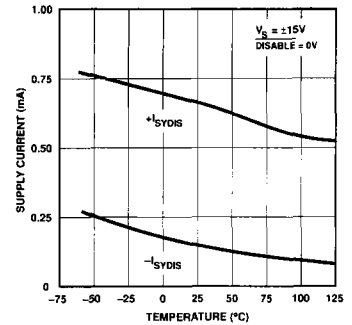
**SUPPLY CURRENT
vs TEMPERATURE**



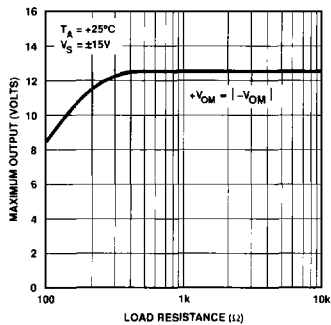
**SUPPLY CURRENT
vs SUPPLY VOLTAGE**



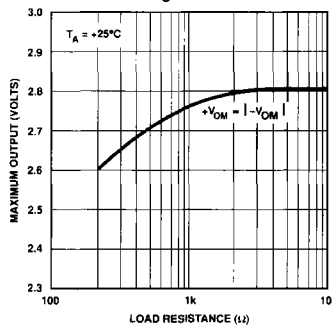
**I_{SY} DISABLE vs
TEMPERATURE**



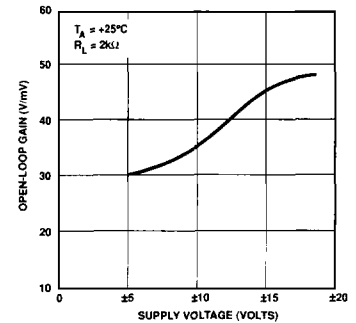
**MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE
 $V_S = \pm 15\text{V}$**



**MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE
 $V_S = \pm 5\text{V}$**

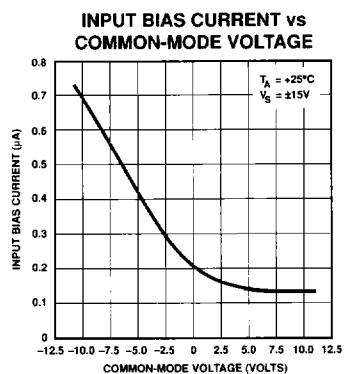
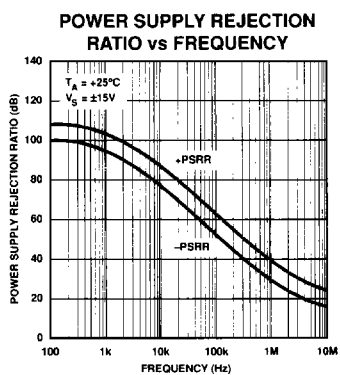
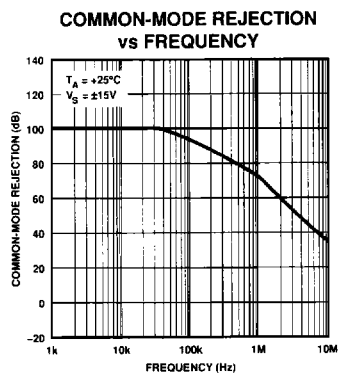
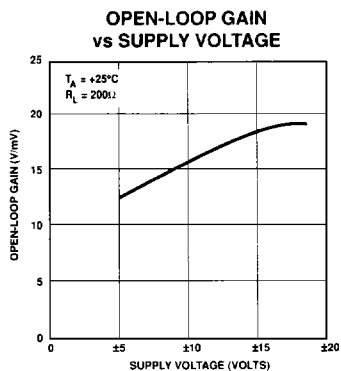


**OPEN-LOOP GAIN
vs SUPPLY VOLTAGE**

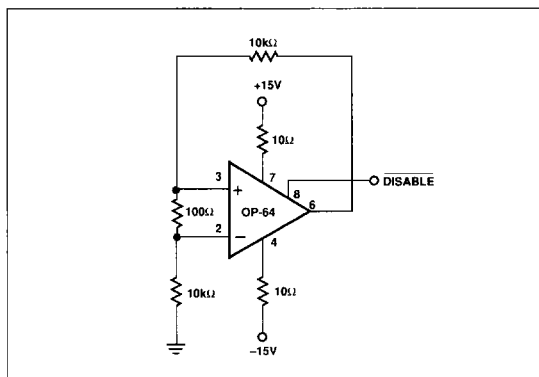


OP-64

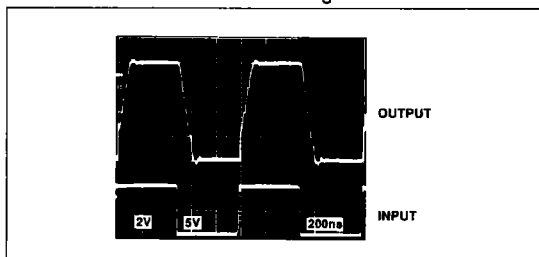
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*



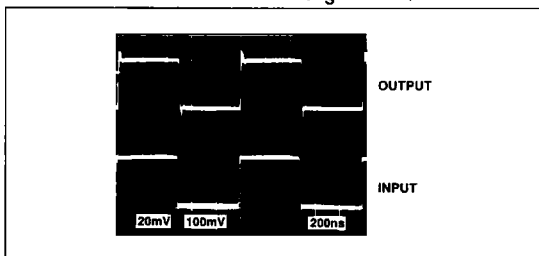
BURN-IN CIRCUIT



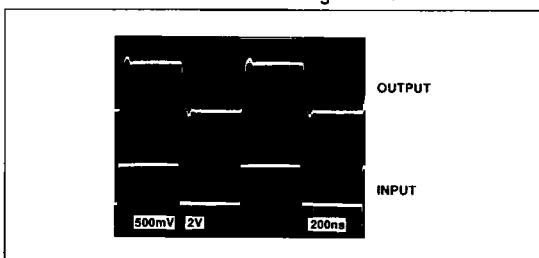
LARGE SIGNAL RESPONSE ($V_S = \pm 15V$)



SMALL SIGNAL RESPONSE ($V_S = \pm 15V$)



LARGE SIGNAL RESPONSE ($V_S = \pm 5V$)

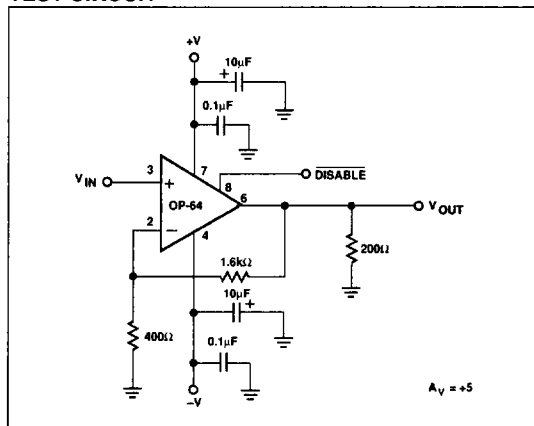


APPLICATIONS INFORMATION

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-64, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10 μ F and 0.1 μ F ceramic bypass capacitor are recommended for each supply, as shown in Figure 1, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-64. As with all high frequency amplifiers, circuit layout is a critical factor in

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



obtaining optimum performance from the OP-64. Proper high frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

During PC board layout, keep all lead lengths and traces as short as possible to minimize inductance. The feedback and gain-setting resistors should be as close as possible to the inverting input to reduce stray capacitance at that point. To further

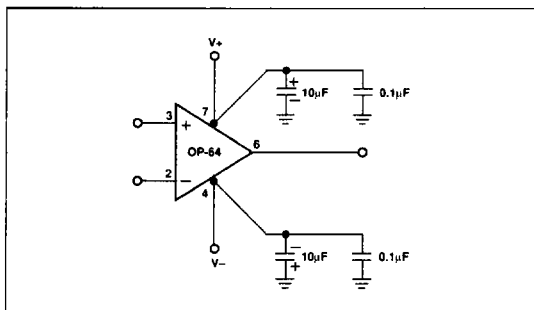


FIGURE 1: Proper power supply bypassing is required to obtain optimum performance with the OP-64.

reduce stray capacitance, remove the ground plane from the area around the inputs of the OP-64. Elsewhere, the use of a solid unbroken ground plane will insure a good high-frequency ground.

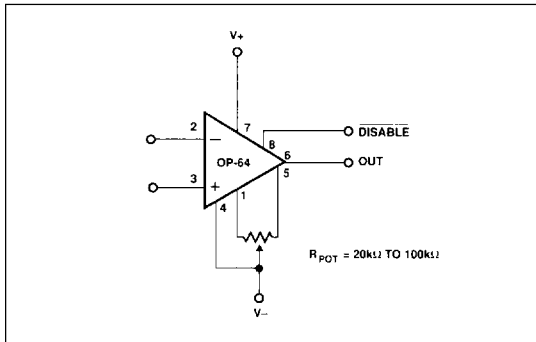


FIGURE 2: Input Offset Voltage Nulling

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a $20k\Omega$ potentiometer as shown in Figure 2. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V^- supply. The typical trim range is $\pm 4mV$.

OP-64 $\overline{DISABLE}$ AMPLIFIER SHUTDOWN

Pin 8 of the OP-64, $\overline{DISABLE}$, is an amplifier shutdown control input. The OP-64 operates normally when Pin 8 is left floating. When greater than $250\mu A$ is drawn from the $\overline{DISABLE}$ pin, the OP-64 is disabled. The supply current drops to $1mA$ and the output impedance rises to $2k\Omega$. To draw current from the $\overline{DISABLE}$ pin, an open collector output logic gate or a discrete NPN transistor can be used as shown in Figure 3. An internal resistor

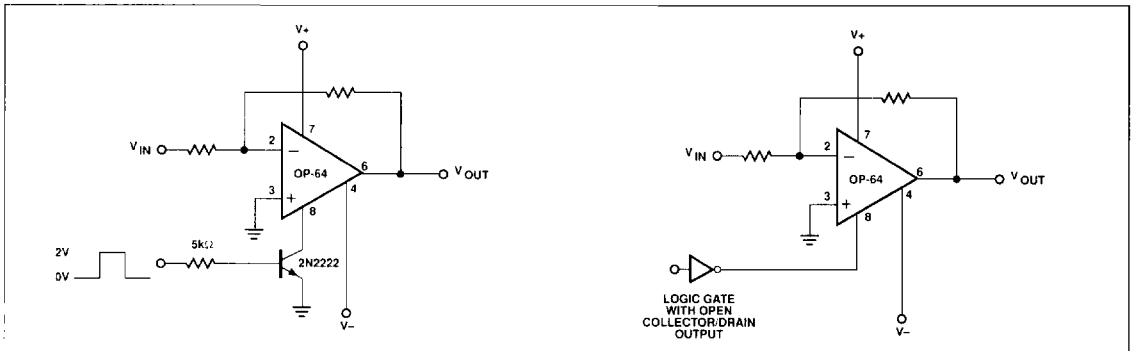


FIGURE 3: Simple circuits allow the OP-64 to be shut down.

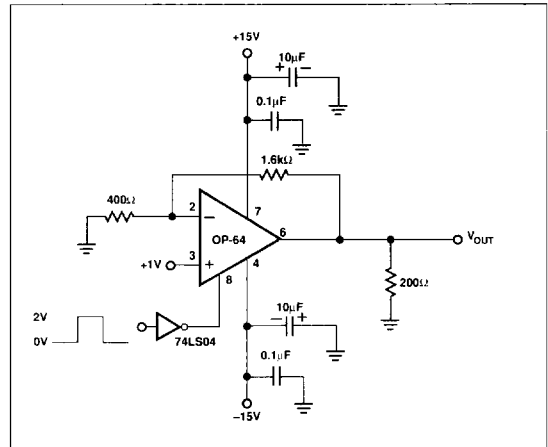


FIGURE 4: $\overline{DISABLE}$ Turn-On/Turn-Off Test Circuit

limits the $\overline{DISABLE}$ current to around $500\mu A$ if the $\overline{DISABLE}$ pin is grounded with the OP-64 powered by $\pm 15V$ supplies. These logic interface methods have the added advantage of level shifting the TTL signal to whatever supply voltage is used to power the OP-64.

Figure 4 shows a test circuit for measuring the turn-on and turn-off times for the OP-64. The OP-64 is in a gain of 5 with a $+1V$ DC input. As the input pulse to the 74LS04 rises its output falls,

drawing current from the $\overline{\text{DISABLE}}$ pin and disabling the amplifier. The output voltage delay is shown in Figure 5 and takes 500 μs to reach ground due to the extra current supplied to the amplifier by the 10 μF electrolytic bypass capacitors. The turn-on time is much quicker than the turn-off time. In this situation as the input to the 74LS04 falls its output rises, returning the OP-64 to normal operation. The amplifier's output turns on in 250ns.

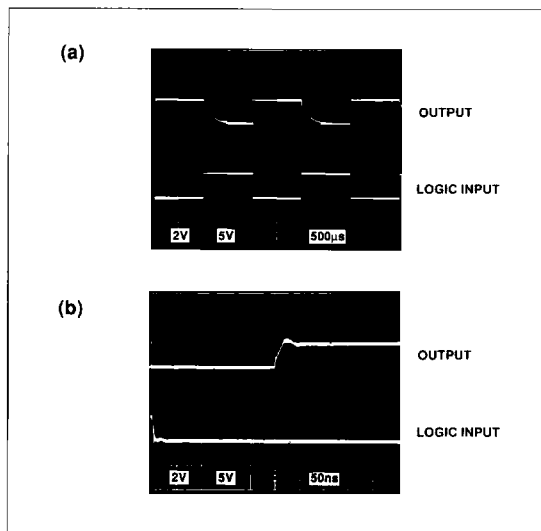


FIGURE 5: (a) OP-64 turn-on and turn-off performance. (b) Expanded scale showing turn-on performance of the OP-64.

OVERDRIVE RECOVERY

Figure 6 shows the overdrive recovery performance of the OP-64. Typical recovery time is 270ns from negative overdrive and 80ns from positive overdrive.

VIDEO AMPLIFIER/TERMINATED LINE DRIVER

The OP-64 can be used as a video amplifier/terminated line driver as shown in Figure 8. With its high output current capability, the OP-64 eliminates the need for an external buffer.

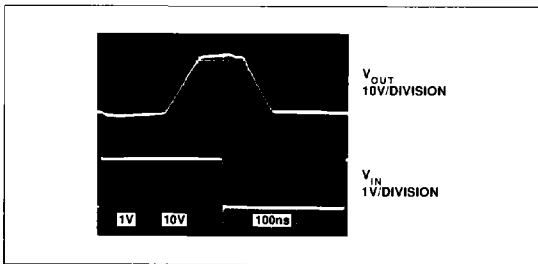


FIGURE 6: OP-64 Overdrive Recovery

The 75 Ω cable termination resistor minimizes reflections from the end of the cable. The 75 Ω series output resistor absorbs any reflections caused by a mismatch between the 75 Ω termination resistor and the characteristic cable impedance. In this circuit the output voltage, V_{OUT} , is one-half of the OP-64's output voltage due to the divider formed by the 75 Ω terminating resistors. The output voltage at the end of the terminated cable, V_{OUT} , spans -1V to +1V. The differential gain and phase for the video amplifier is summarized in Table 1.

TABLE 1: Differential Gain and Phase of Video Amplifier/Line Driver

V_s	Differential Gain		Differential Phase	
	3.58MHz	5MHz	3.58MHz	5MHz
$\pm 15\text{V}$	0.008dB	0.016dB	0.03°	0.03°
$\pm 12\text{V}$	0.008dB	0.018dB	0.03°	0.03°

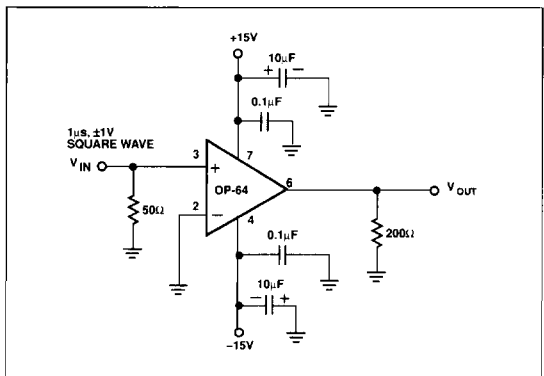


FIGURE 7: Overdrive Recovery Test Circuit

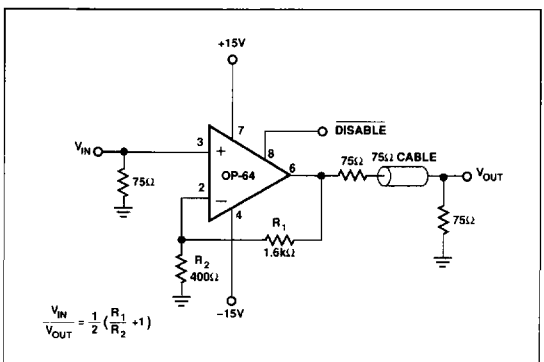


FIGURE 8: Video Amplifier/Terminated Line Driver

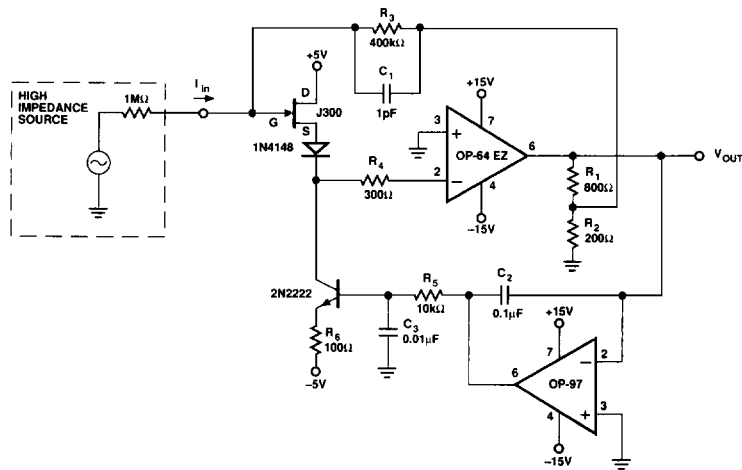


FIGURE 9: Fast Transimpedance Amplifier

FAST TRANSIMPEDANCE AMPLIFIER

The circuit shown in Figure 9 is a fast transimpedance amplifier designed to handle high speed signals from a high impedance source such as the output of a photomultiplier tube. The input current is amplified and converted to an output voltage by the transimpedance amplifier.

A JFET source-follower input is used to reduce the input bias current of the amplifier to 100 pA and lower the input current noise. Transimpedance of the amplifier is:

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{R_1}{R_2} + 1 \right) R_3$$

and for the values shown equals

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{800\Omega}{200\Omega} + 1 \right) 400k\Omega = 2V/\mu A$$

Figure 10 shows the output of the transimpedance amplifier when driven from a 1MΩ source impedance. The input signal of 10μA_{p-p} is converted into an output voltage of (10μA) 2V/μA = 20V_{p-p}. Output slew rate is 100V/μs. The slew rate is limited by the combination of the capacitance of the JFET gate with the 1MΩ source impedance. For best performance, the stray input capacitance should be kept as small as possible. The OP-97 is used in an integrator loop to reduce the total amplifier offset voltage to under 25μV.

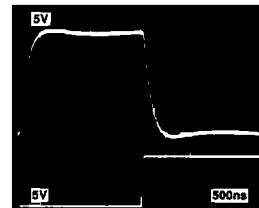


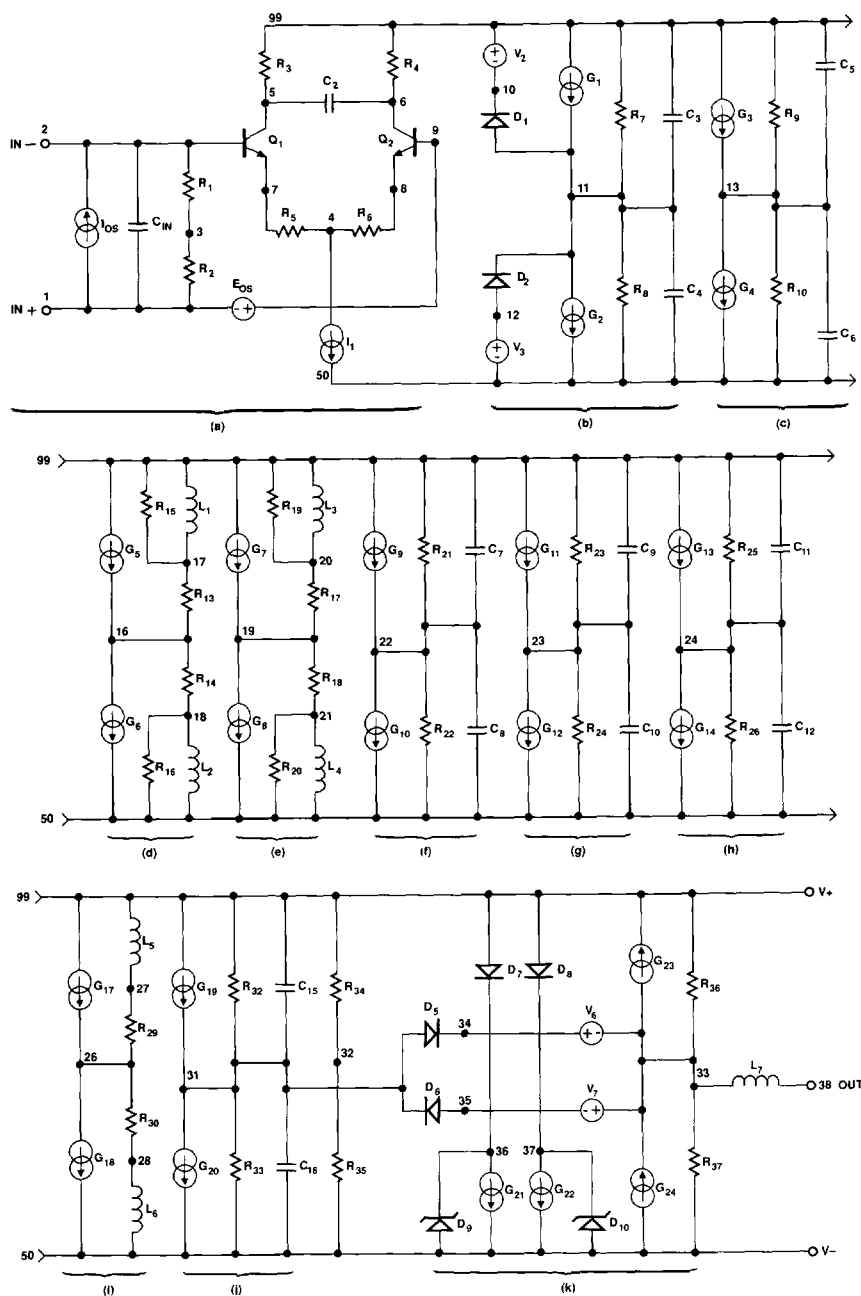
FIGURE 10: Output of the Fast Transimpedance Amplifier

OP-64 SPICE MACRO-MODEL

Figure 11 shows the node and net list for a SPICE macro-model of the OP-64. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS} , I_{OS} , I_B , A_{VO} , CMR, V_O and I_{SY} . AC parameters such as slew rate, gain and phase response and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-64. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP-64. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C (see following pages).

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FIGURE 11a: OP-64 SPICE Macro-Model Schematic and Node List

* PSpice is a registered trademark of MicroSim Corporation
 ** HSPICE is a trademark of Meta-Software, Inc.

OP-64 MACRO-MODEL ©PMI 1989

* subckt OP-64 1 2 38 99 50

* INPUT STAGE & POLE AT 39.8 MHz

```

r1 2 3 5E11
r2 1 3 5E11
r3 5 99 474.86
r4 6 99 474.86
r5 4 7 423.26
r6 4 8 423.26
cin 1 2 5E-12
c2 5 6 4.2106E-12
i1 4 50 1E-3
ios 1 2 1E-7
eos 9 1 poly(1) 26 32 4E-4 1
q1 5 2 7 qx
q2 6 9 8 qx

```

* SECOND STAGE & POLE AT 3.8 kHz

```

r7 11 99 7.1229E6
r8 11 50 7.1229E6
c3 11 99 5.88E-12
c4 11 50 5.88E-12
g1 99 11 poly(1) 5 6 4.31E-3 2.1059E-3
g2 11 50 poly(1) 6 5 4.31E-3 2.1059E-3
v2 99 10 2.25
v3 12 50 2.25
d1 11 10 dx
d2 12 11 dx

```

* POLE AT 39.8 MHz

```

r9 13 99 1E6
r10 13 50 1E6
c5 13 99 4E-15
c6 13 50 4E-15
g3 99 13 11 32 1E-6
g4 13 50 32 11 1E-6

```

* ZERO-POLE PAIR AT 26.5 MHz / 159 MHz

```

r13 16 17 1E6
r14 16 18 1E6
r15 17 99 5E6
r16 18 50 5E6
i1 17 99 5.005E-3
i2 18 50 5.005E-3
g5 99 16 13 32 1E-6
g6 16 50 32 13 1E-6

```

* ZERO-POLE PAIR AT 31.8 MHz / 39.8 MHz

```

r17 19 20 1E6
r18 19 21 1E6
r19 20 99 2.5157E5
r20 21 50 2.5157E5
i3 20 99 1.006E-3
i4 21 50 1.006E-3
g7 99 19 16 32 1E-6
g8 19 50 32 16 1E-6

```

* POLE AT 100 MHz

```

r21 22 99 1E6
r22 22 50 1E6
c7 22 99 1.59E-15
c8 22 50 1.59E-15
g9 99 22 19 32 1E-6
g10 22 50 32 19 1E-6

```

* POLE AT 159 MHz

```

r23 23 99 1E6
r24 23 50 1E6
c9 23 99 1E-15
c10 23 50 1E-15
g11 99 23 22 32 1E-6
g12 23 50 32 22 1E-6

```

* POLE AT 159 MHz

```

r25 24 99 1E6
r26 24 50 1E6
c11 24 99 1E-15
c12 24 50 1E-15
g13 99 24 23 32 1E-6
g14 24 50 32 23 1E-6

```

* COMMON-MODE GAIN NETWORK WITH ZERO AT 20kHz

```

r29 26 27 1E6
r30 26 28 1E6
i5 27 99 7.9575
i6 28 50 7.9575
g17 99 26 33 32 1E-11
g18 26 50 32 33 1E-11

```

* POLE AT 159 MHz

```

r32 31 99 1E6
r33 31 50 1E6
c15 31 99 1E-15
c16 31 50 1E-15
g19 99 31 24 32 1E-6
g20 31 50 32 24 1E-6

```

* OUTPUT STAGE

```

r34 32 99 20.0E3
r35 32 50 20.0E3
r36 33 99 60
r37 33 50 60
i7 33 38 2.9E-7
g21 36 50 31 33 16.6666667E-3
g22 37 50 33 31 16.6666667E-3
g23 33 99 99 31 16.6666667E-3
g24 50 33 31 50 16.6666667E-3
v6 34 33 1.7
v7 33 35 1.7
d5 31 34 dx
d6 35 31 dx
d7 99 36 dx
d8 99 37 dx
d9 50 36 dy
d10 50 37 dy

```

* MODELS USED

```

*model qx NPN(BF=2500)
*model dx D(IS=1E-15)
*model dy D(IS=1E-15 BV=50)
*ends OP-64

```

FIGURE 11b: OP-64 SPICE Net-List