

High-Speed CMOS Logic

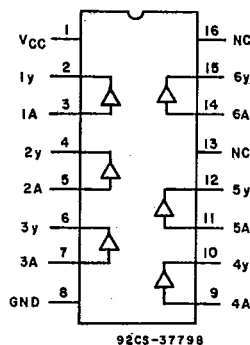


- Typical propagation delay = 6 ns
@ $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{ C}$
- High-to-low voltage level converter
for up to $V_I = 16\text{ V}$

Family Features

- **Fanout (Over Temperature Range):**
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- **Wide Operating Temperature Range:**
CD74HC/HCT: -40 to +85°C
- **Balanced Propagation and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **Alternate Source is Philips/Signetics**
- **CD54HC/CD74HC Types:**
2 to 6 V Operation
- **High Noise Immunity:** $N_{IL} = 30\%, V_{CC}$,
 $N_{IH} = 30\% V_{CC}$; @ $V_{CC} = 5 V$

FUNCTIONAL DIAGRAM



92CS-37797

LOGIC DIAGRAMS

CD54/74HC4050

CD54/74HC4049 CD54/74HC4050

HARRIS SEMICONDUCTOR

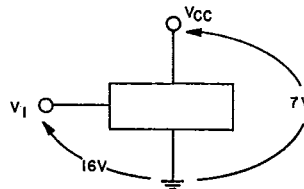
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MAXIMUM RATINGS, Absolute-Maximum Values:
DC SUPPLY-VOLTAGE, (V_{CC}) -0.5 to +7 V
DC INPUT VOLTAGE, (V_i) -0.5 to +16 V

(Voltages referenced to ground) -0.5 to +16 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V) -20 mADC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ± 20 mADC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V) ± 25 mADC V_{CC} OR GROUND CURRENT (I_{CC}) ± 50 mA**POWER DISSIPATION PER PACKAGE (P_D):**For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mWFor $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mWFor $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H) 500 mWFor $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mWFor $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) 400 mWFor $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW**OPERATING-TEMPERATURE RANGE (T_A):**PACKAGE TYPE F, H -55 to $+125^\circ\text{C}$ PACKAGE TYPE E, M -40 to $+85^\circ\text{C}$ STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ\text{C}$ **LEAD TEMPERATURE (DURING SOLDERING):**At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$ Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)with solder contacting lead tips only $+300^\circ\text{C}$

Voltage Relationships:
(Maximum Positive Limits)



92CS-37799R1

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC}^*			
CD54/74HC Types	2	6	V
DC Output Voltage, V_o	0	V_{CC}	V
DC Input Voltage (V_i)	0	15	V
Operating Temperature, T_A :			
CD74 Types	-40	+85	$^\circ\text{C}$
CD54 Types	-55	+125	$^\circ\text{C}$
Input Rise and Fall Times, t_r, t_f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4049 CD54/74HC4050

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CD54/74HC4049, CD54/74HC4050										UNITS	
		TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES			
								-40/ +85°C		-55/ +125°C			
		V _I V	I _O mA	V _{CC} V	+25°C			Min.	Max.	Min.	Max.		
High-Level Input Voltage	V _{IH}			2	1.5	—	—	1.5	—	1.5	—	V	
				4.5	3.15	—	—	3.15	—	3.15	—		
				6	4.2	—	—	4.2	—	4.2	—		
Low-Level Input Voltage	V _{IL}			2	—	—	0.5	—	0.5	—	0.5	V	
				4.5	—	—	1.35	—	1.35	—	1.35		—
				6	—	—	1.8	—	1.8	—	1.8		—
High-Level Output Voltage CMOS Loads	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V	
				4.5	4.4	—	—	4.4	—	4.4	—		
				6	5.9	—	—	5.9	—	5.9	—		
TTL Loads (Standard Output)	V _{IL} or V _{IH}	-4 -5.2	4.5	3.98	—	—	3.84	—	3.7	—	V		
			6	5.48	—	—	5.34	—	5.2	—			
Low-Level Output Voltage CMOS Loads	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V	
				4.5	—	—	0.1	—	0.1	—	0.1		—
				6	—	—	0.1	—	0.1	—	0.1		—
TTL Loads (Standard Output)	V _{IL} or V _{IH}	4 5.2	4.5	—	—	0.26	—	0.33	—	0.4	V		
			6	—	—	0.26	—	0.33	—	0.4		—	
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	μA	
		15		6	—	—	±0.5	—	±5	—	±5		
Quiescent Device Current	I _{CC}	15 or Gnd	0	6	—	—	2	—	20	—	40	μA	

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	54HC AND 74HC	
		TYPICAL	UNITS
Propagation Delay, Data Input to Output (C _L = 15 pF)	HC4049 HC4050 t _{PLH} , t _{PHL}	6	ns
Power Dissipation Capacitance*	C _{PD}	35	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter

P_D = V_{CC}² f_i(C_{PD} + C_L) where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V _{CC}	25°C		-40°C to +85°C		-55°C to +125°C		UNITS
			HC		74HC		54HC		
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay nA to nY HC4049 nA to nY HC4050	t _{PLH} , t _{PHL}	2	—	85	—	105	—	130	ns
		4.5	—	17	—	21	—	26	
		6	—	14	—	18	—	22	
Transition Time	t _{TLH} , t _{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C _i	—	—	10	—	10	—	10	pF

HARRIS SEMICONDUCTOR 27E D 4302271 0017920 0 HAS

CD54/74HC4049
CD54/74HC4050

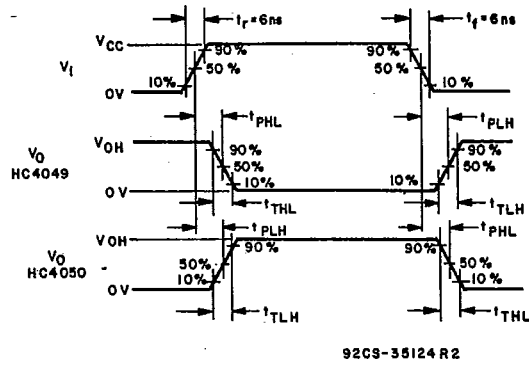


Fig. 1 - Transition times and propagation delay times, combination logic.