

16-Bit Registered Transceivers

Features

- I_{off} supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16952T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162952T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162H952T Features:

- Bus hold retains last active state
- Eliminates the need for external pull-up or pull-down resistors

Functional Description

These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B, CEAB must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when OEAB is LOW. Control of data from B-to-A is similar and is controlled by using the CEBA, CLKBA, and OEBA inputs.

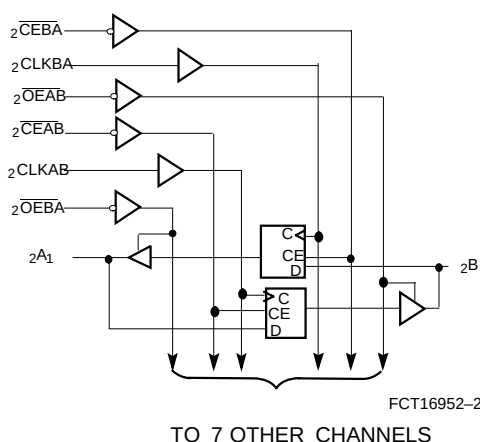
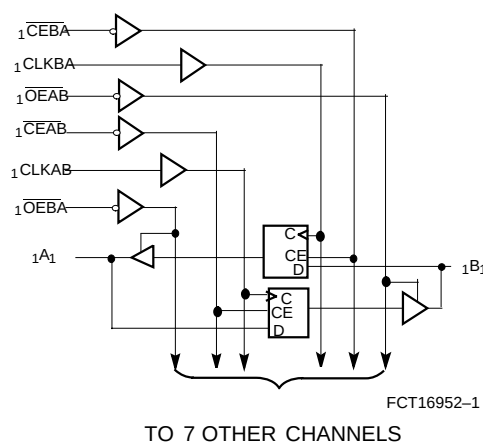
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Logic Block Diagrams



Pin Configuration SSOP/TSSOP Top View

1 OEAB	1	56	1 OEBA
1 CLKAB	2	55	1 CLKBA
1 CEAB	3	54	1 CEBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
VCC	7	50	VCC
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
VCC	22	35	VCC
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

FCT16952-3

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs ^[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs ^[1]

Function Table^[2, 3]

For A-to-B (Symmetric with B-to-A)

Inputs				Outputs
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B ^[4]
X	L	L	X	B ^[4]
L	$\downarrow$	L	L	L
L	$\uparrow$	L	H	H
X	X	H	X	Z

Notes:

- On the CY74FCT162H952T these pins have bus hold.
- A-to-B data flow is shown: B-to-A data flow is similar but uses, $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
- H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Don't Care.
 $\downarrow$ = LOW-to-HIGH Transition.
Z = HIGH Impedance.
- Level of B before the indicated steady-state input conditions were established.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Maximum Ratings^[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with
Power Applied -55°C to +125°C

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[8]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	Standard	V _{CC} =Max., V _I =V _{CC}		±1	μA
		Bus Hold			±100	
I _{IL}	Input LOW Current	Standard	V _{CC} =Max., V _I =GND		±1	μA
		Bus Hold			±100	μA
I _{BBH} I _{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[9]	V _{CC} =Min., V _I =2.0V	-50			μA
		V _I =0.8V	+50			μA
I _{BHHO} I _{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[9]	V _{CC} =Max., V _I =1.5V			TBD	mA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[10]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[10]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[11]			±1	μA

Output Drive Characteristics for CY74FCT16952T

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} = -3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} = -15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} = -32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
I _{ODL}	Output LOW Current ^[10]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[10]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} = -24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[8] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Note:

7. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
8. This parameter is specified but not tested.
9. Pins with bus hold are described in the Pin Description.
10. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
11. Tested at +25°C.

Power Supply Characteristics

Parameter	Description	Test Conditions ^[12]		Typ. ^[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V^{[13]}$	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[14]	$V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB or OEBA=GND	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	75	120	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ^[15]	$V_{CC} = \text{Max.}$, $F_1 = 5 \text{ MHz}$, $F_0 = 10 \text{ MHz}$ (CLKAB) OEAB = CEAB = GND OEBA = V_{CC} 50% Duty Cycle, Outputs Open, One Bit Toggling	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.8	1.7	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	1.3	3.2	
		$V_{CC} = \text{Max.}$, $f_0 = 10 \text{ MHz}$ (CLKAB) $f_1 = 2.5 \text{ MHz}$, OEAB = CEAB = GND OEBA = V_{CC} 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	3.8	6.5 ^[16]	
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	8.3	20.0 ^[16]	

Notes:

12. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
13. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[17]

Parameter	Description	CY74FCT16952AT CY74FCT162952AT CY74FCT162H952AT		CY74FCT162952BT		Unit	Fig. No. ^[18]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLKAB, CLKBA to B, A	2.0	10.0	2.0	7.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA, OEAB to A, B	1.5	10.5	1.5	8.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA, OEAB to A, B	1.5	10.0	1.5	7.5	ns	1, 7, 8
t _{SU}	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA	2.5	—	2.5	—	ns	4
t _H	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA	2.0	—	1.5	—	ns	4
t _{SU}	Set-Up Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	3.0	—	3.0	—	ns	4
t _H	Hold Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	2.0	—	2.0	—	ns	4
t _W	Pulse Width HIGH or LOW CLKAB or CLKBA ^[19]	3.0	—	3.0	—	ns	5
t _{SK(O)}	Output Skew ^[20]	—	0.5	—	0.5	ns	—

Parameter	Description	CY74FCT16952CT CY74FCT162H952CT		Unit	Fig. No. ^[18]
		Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLKAB, CLKBA to B, A	2.0	6.3	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA, OEAB to A, B	1.5	7.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA, OEAB to A, B	1.5	6.5	ns	1, 7, 8
t _{SU}	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA	2.5	—	ns	4
t _H	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA	1.5	—	ns	4
t _{SU}	Set-Up Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	3.0	—	ns	4
t _H	Hold Time, HIGH or LOW CEAB, CEBA to CLKAB, CLKBA	2.0	—	ns	4
t _W	Pulse Width HIGH or LOW CLKAB or CLKBA ^[19]	3.0	—	ns	5
t _{SK(O)}	Output Skew ^[20]	—	0.5	ns	—

Notes:

17. Minimum limits are specified but not tested on Propagation Delays.
18. See "Parameter Measurement Information" in the General Information section.
19. This parameter is specified but not tested.
20. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16952

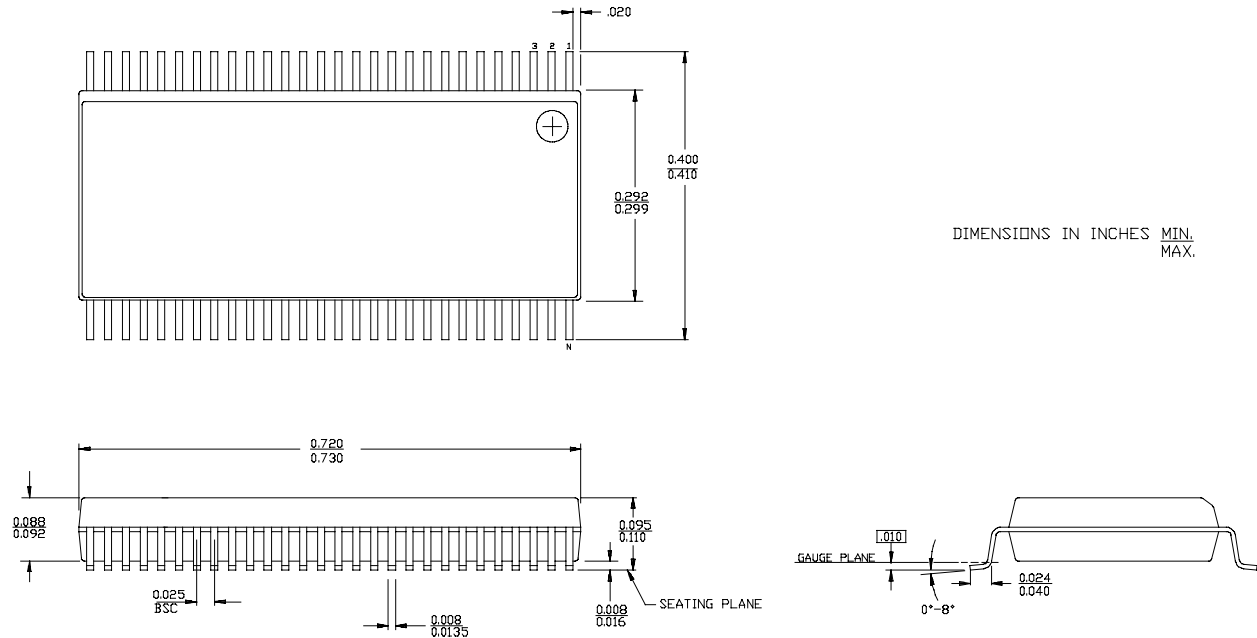
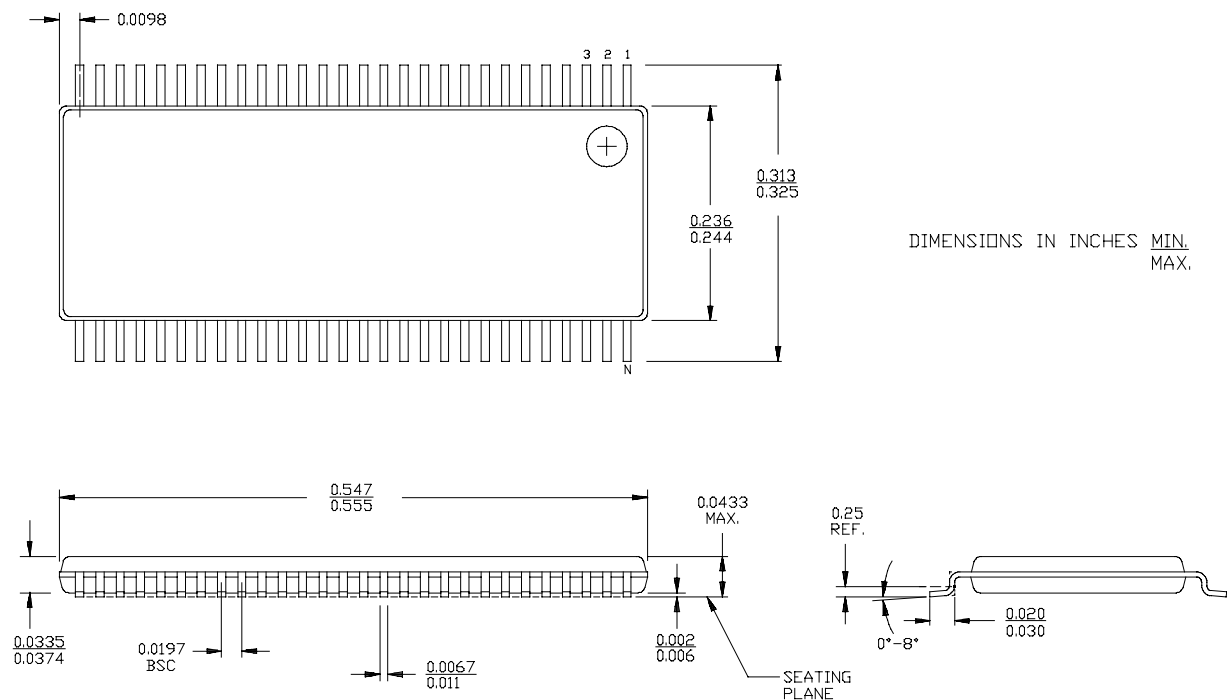
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT16952CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
10.0	CY74FCT16952ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7.5	CY74FCT162952BTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162952BTPVCT	O56	56-Lead (300-Mil) SSOP	
10.0	74FCT162952ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

Ordering Information CY74FCT162H952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	74FCT162H952CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
10.0	74FCT162H952ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

Package Diagrams
56-Lead Shrunken Small Outline Package O56

56-Lead Thin Shrunken Small Outline Package Z56


PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74FCT162952BTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162952ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162952ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT162H952ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162H952ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT16952ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16952CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16952CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162952BTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162952ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT162952ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16952ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16952CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16952ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16952ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

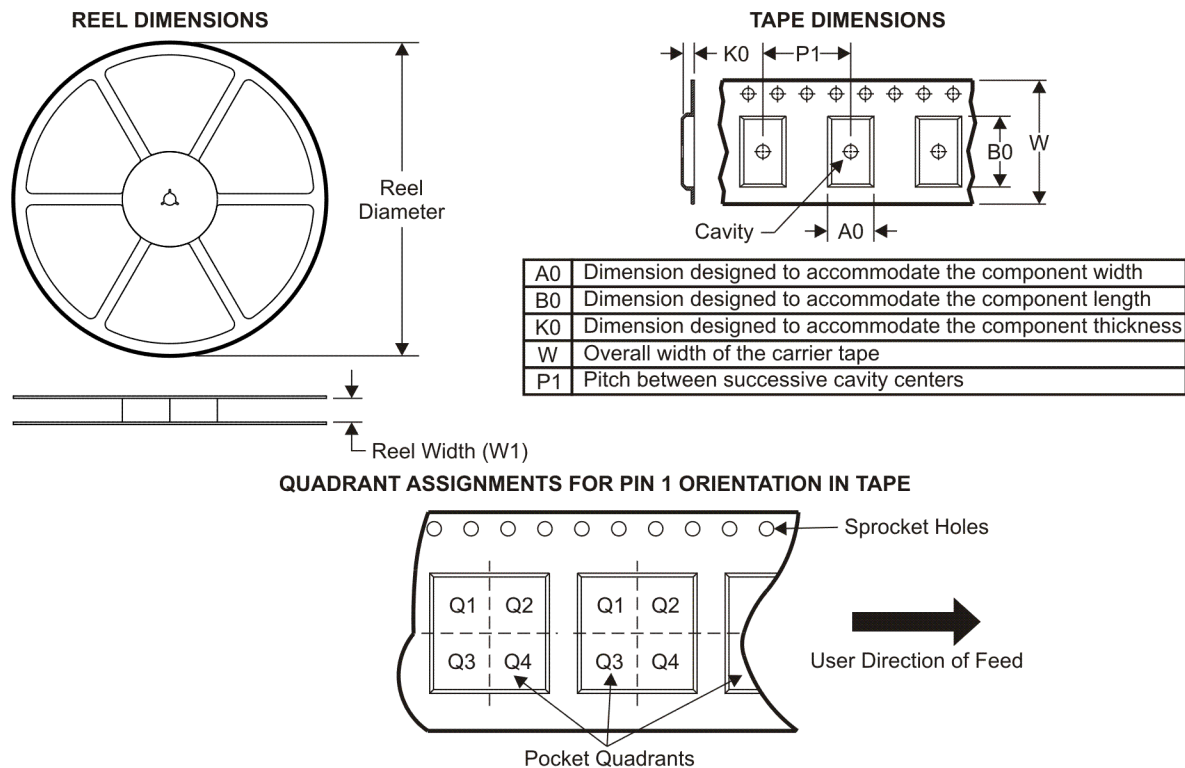
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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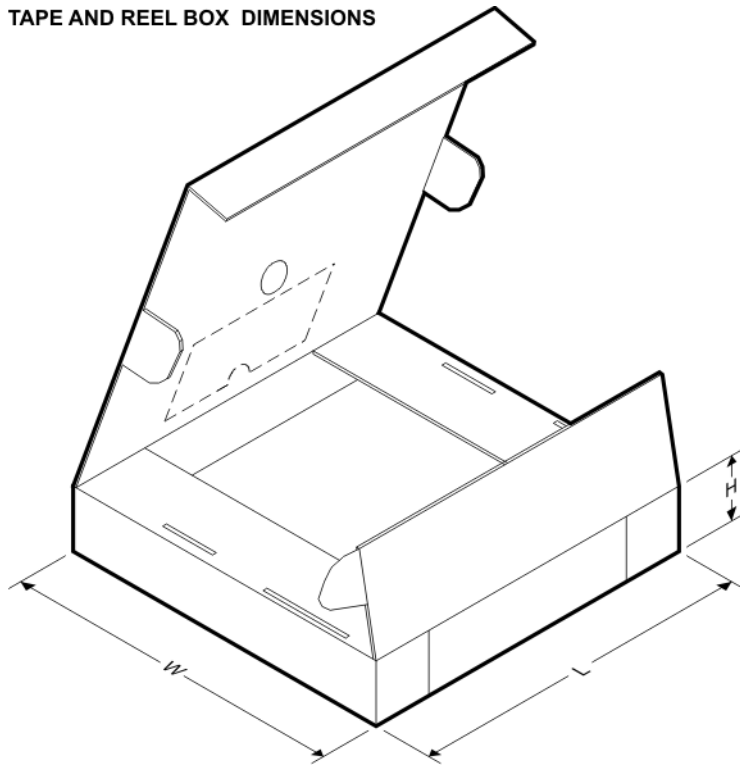
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT16952CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



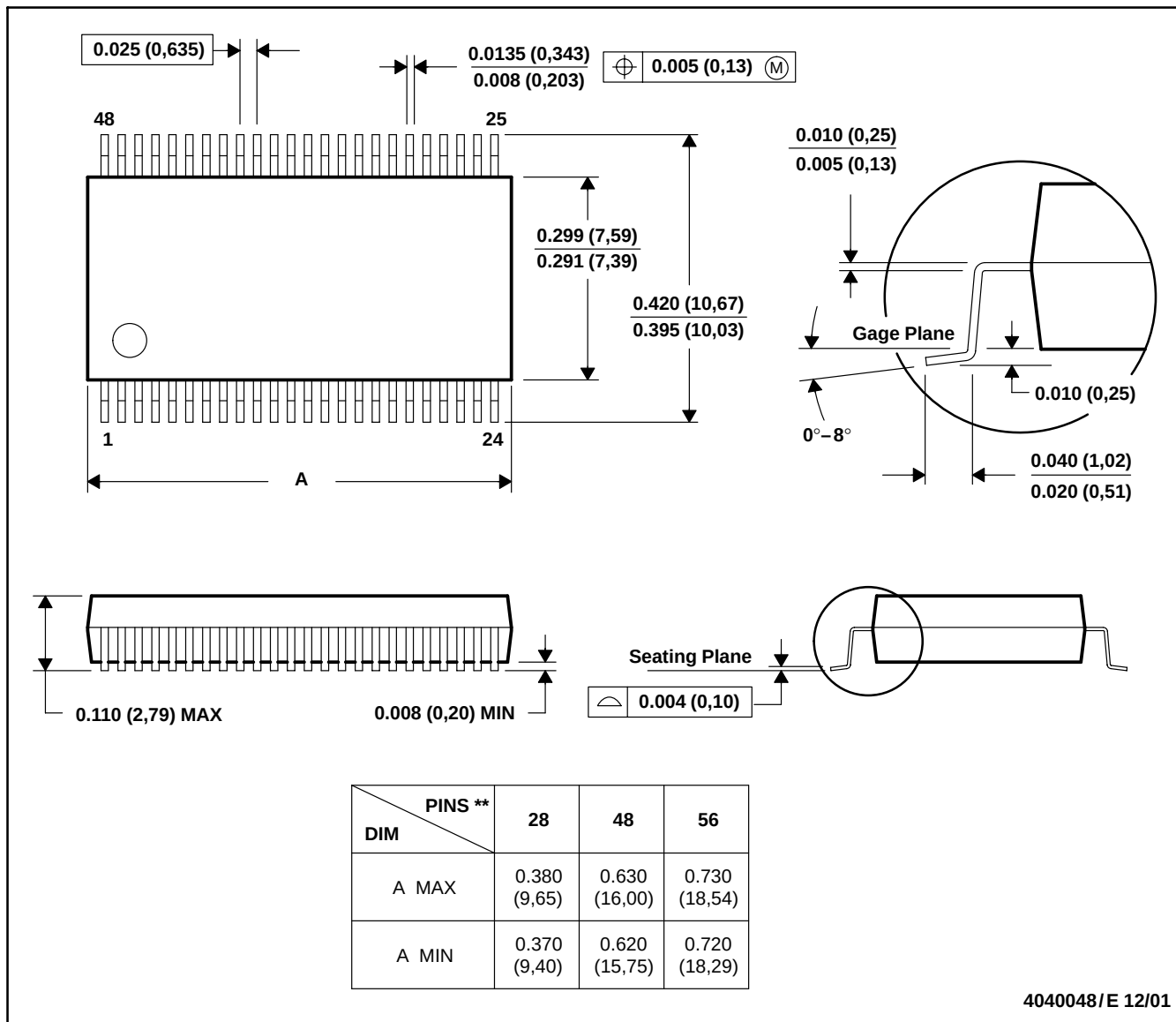
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT16952CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

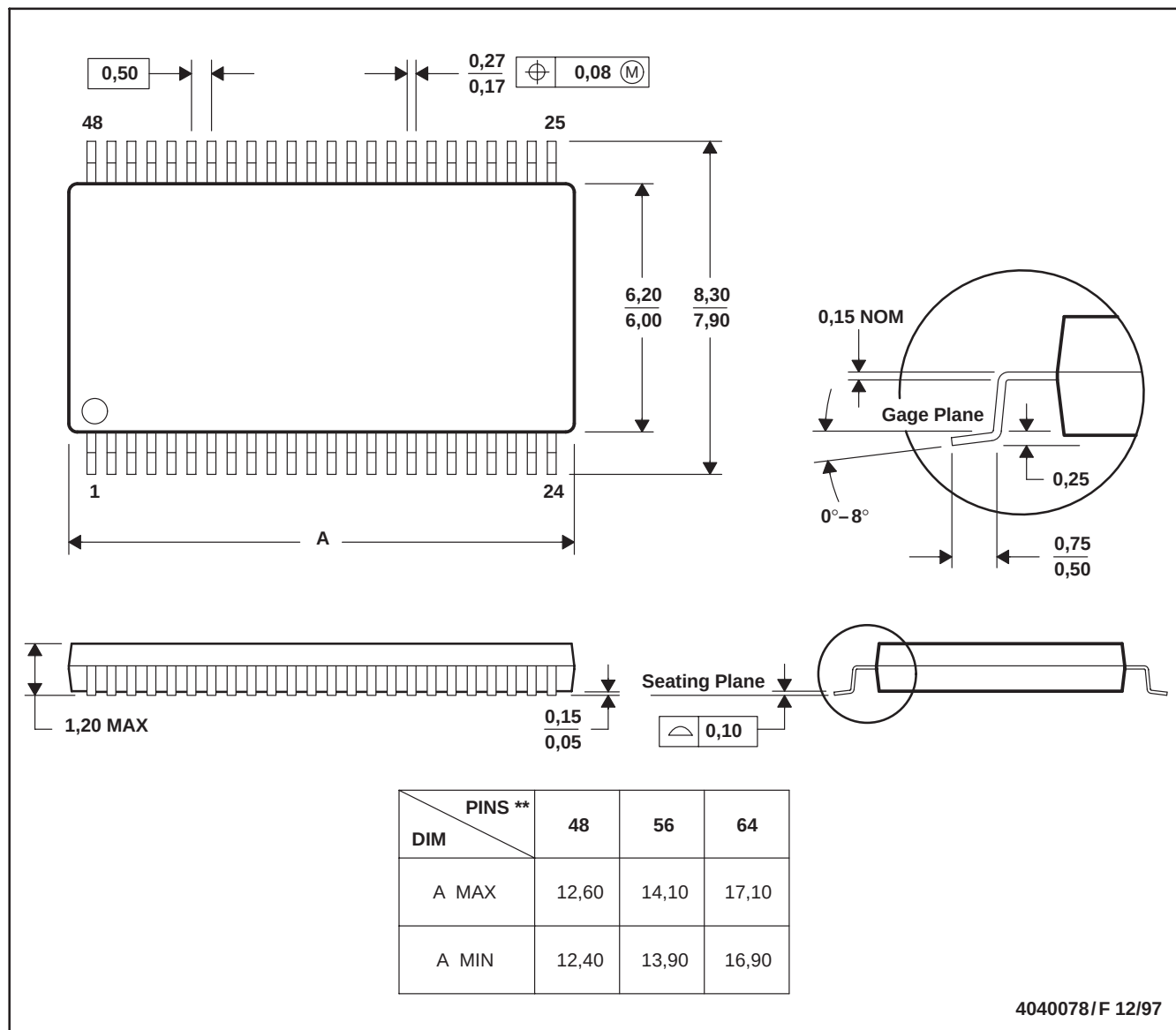


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162952ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
74FCT162952ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
74FCT162H952ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
74FCT162H952ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
74FCT16952ATPVC4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16952A	Samples
CY74FCT162952BTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162952B	Samples
CY74FCT162952ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162952ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16952ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16952A	Samples
CY74FCT16952CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16952C	Samples
CY74FCT16952ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16952ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

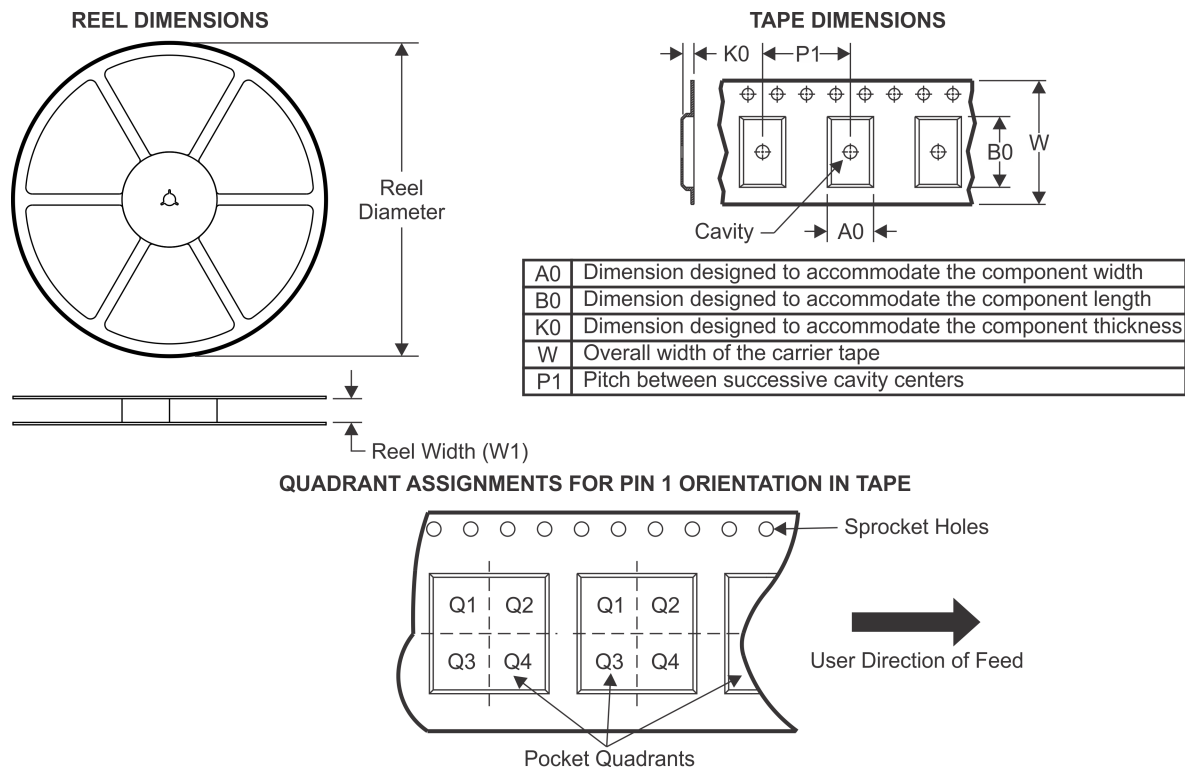
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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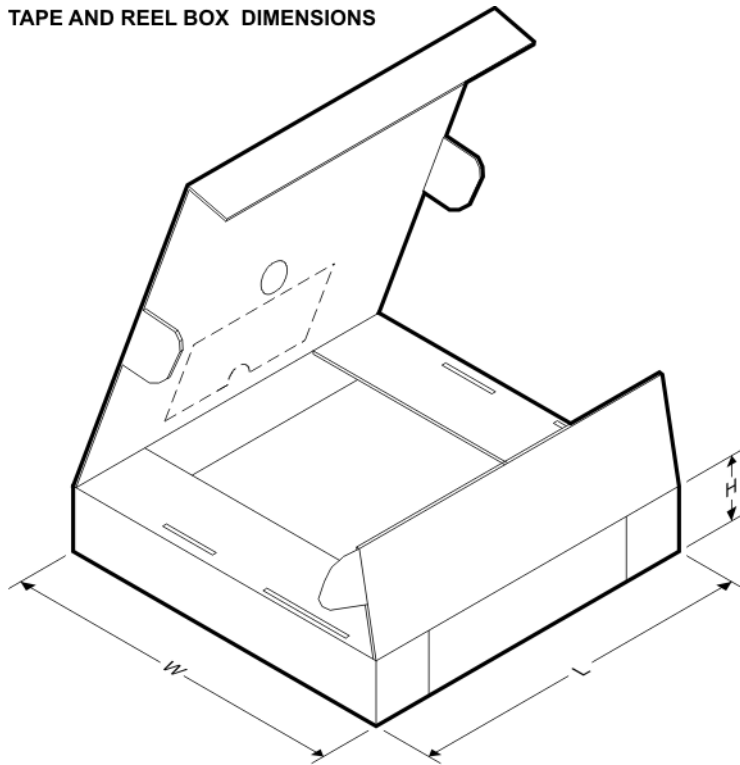
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT16952CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

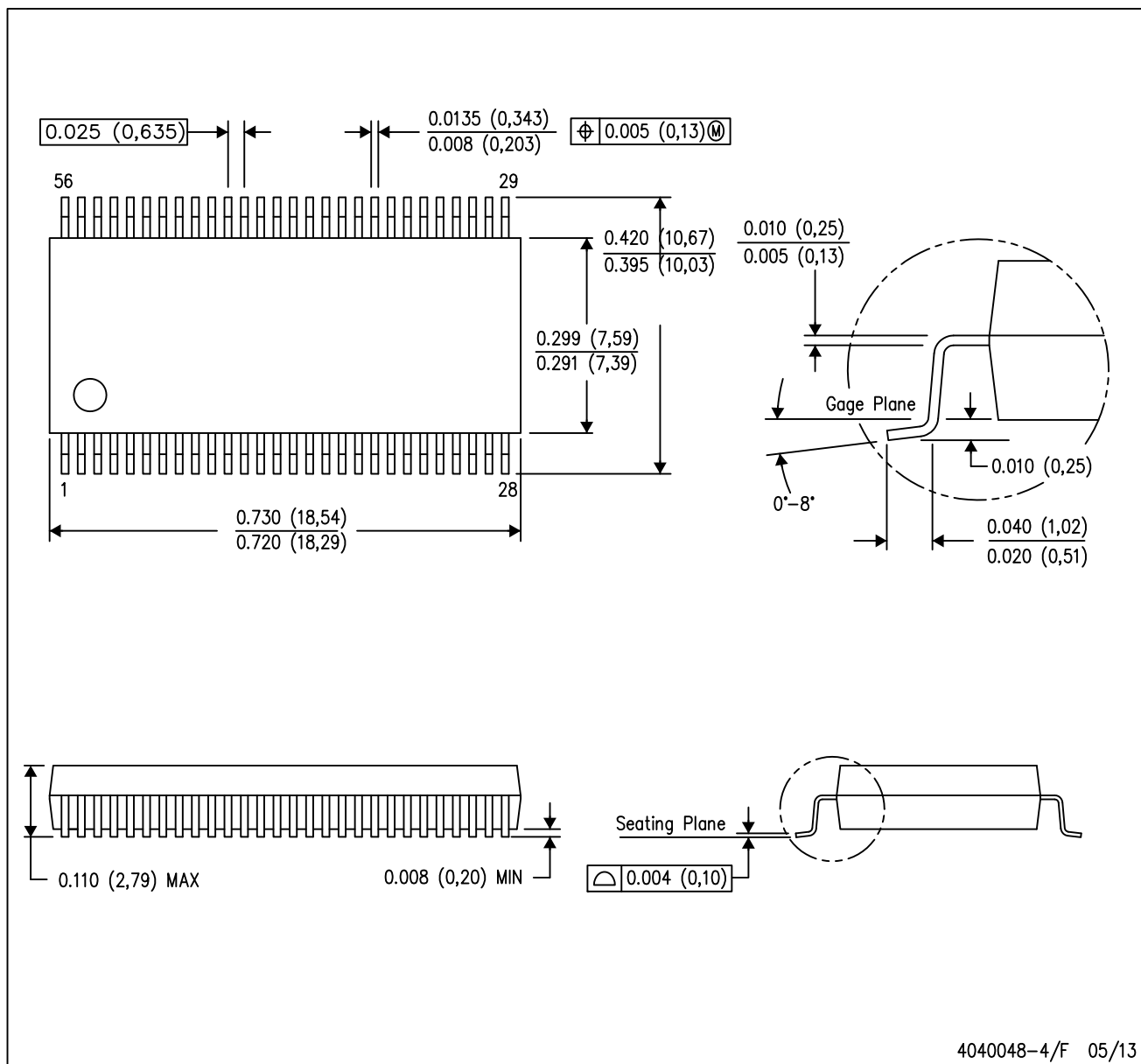


*All dimensions are nominal

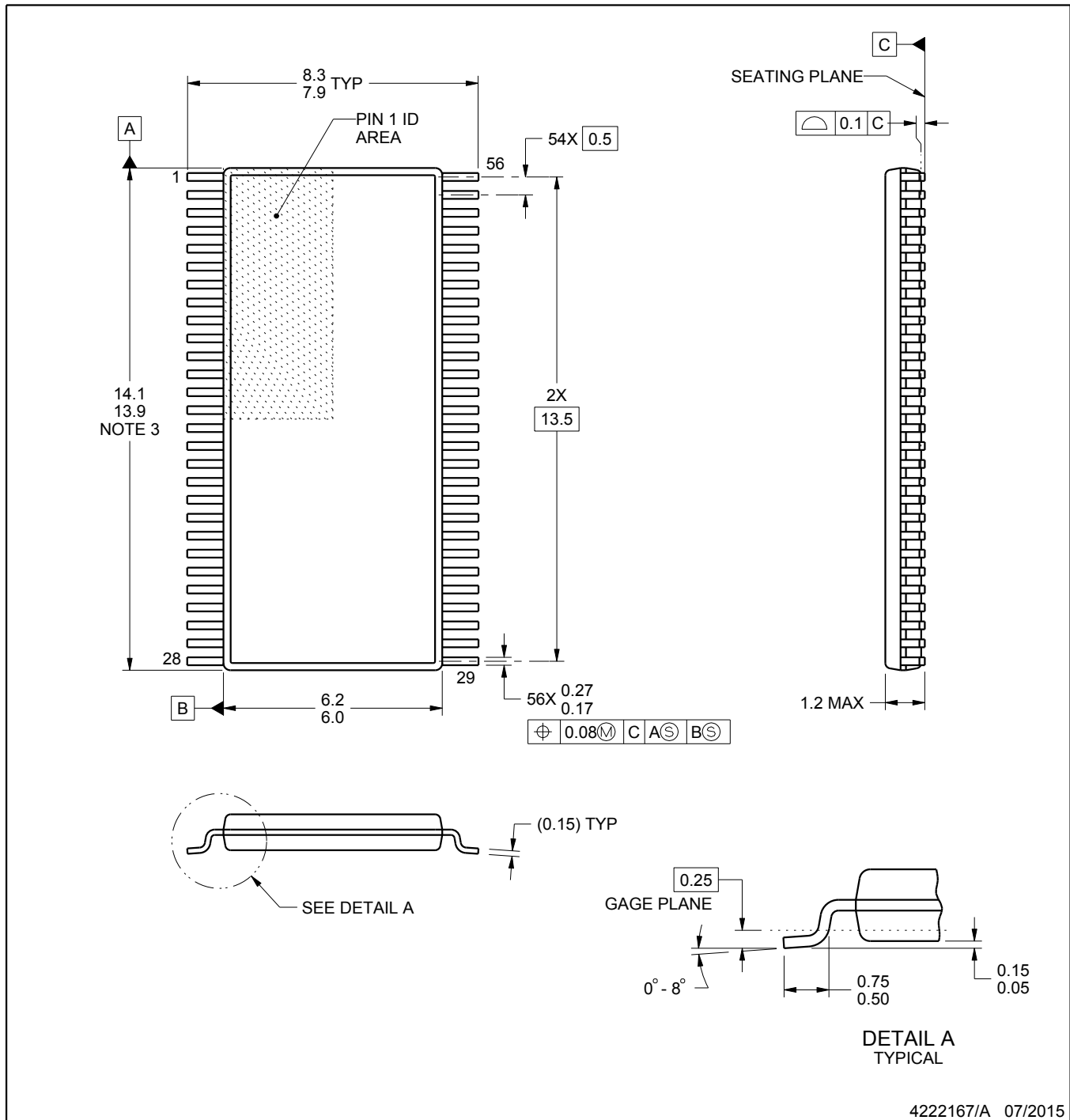
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT16952CTPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

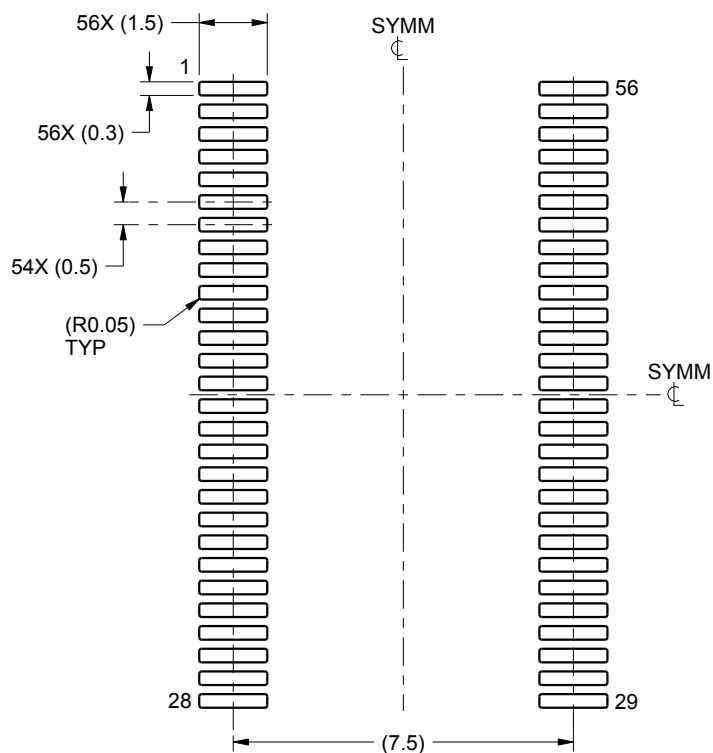
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

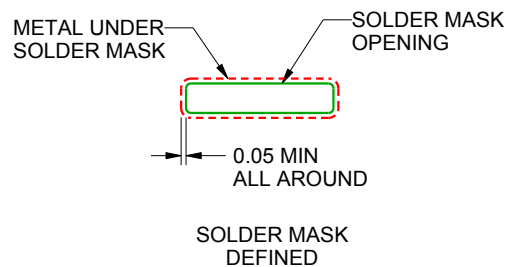
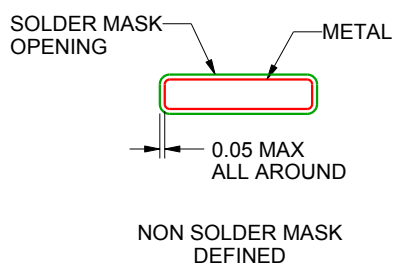
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

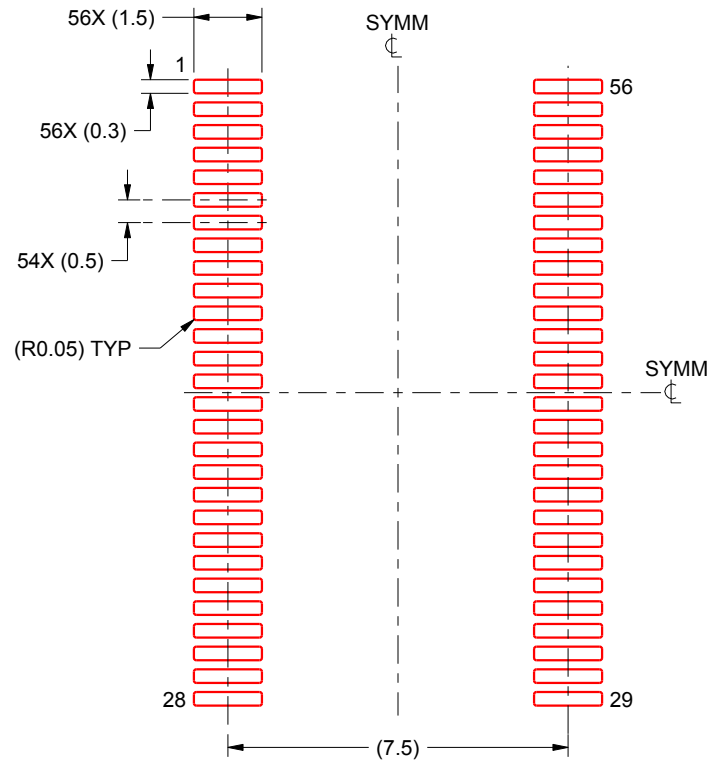
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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