

VSC8491

WAN/LAN/Backplane RXAU/XAUI to SFP+/KR 10 GbE SerDes PHY with VeriTime™ and MACsec

Microsemi's 10G/1G SerDes PHY provides MACsec, IEEE 1588v2, and hardware-based KR support for timing-critical applications, including all industry-standard protocol encapsulations.

The VSC8491 device offers a seamless integration between IEEE 1588v2 and the MACsec engine with no loss of precision. It also includes one serial port routed to one or both of the RXAU/XAUI interfaces using the integrated crosspoint.

VeriTime™ is Microsemi's patent-pending timing technology that delivers the industry's most accurate IEEE 1588v2 timing implementation. IEEE 1588v2 timing integrated in the PHY is the quickest, lowest cost method of implementing the timing accuracy that is critical to maintaining existing timing-critical capabilities during the migration from TDM to packet-based architectures.

The VSC8491 device supports 1-step and 2-step PTP frames for ordinary clock, boundary clock, and transparent clock applications, along with complete Y.1731 OAM performance monitoring capabilities.

MACsec (IEEE 802.1AE) defines a set of protocols to meet the security requirements for protecting data traversing Ethernet LANs, such as input classification, frame encryption/decryption, and performance and latency monitoring.

The VSC8491 device meets the SFP+ SR/LR/ER/ZR/220MMF host requirements in accordance with the SFF-8431 specifications. It also compensates for optical impairments in SFP+ applications, along with degradations of the PCB. The VSC8491 device provides full KR support, including KR state machine, for autonegotiation and link optimization. The transmit path incorporates a multitap output driver to provide flexibility to meet the demanding 10GBASE-KR (IEEE 802.3ap) Tx output launch requirements.

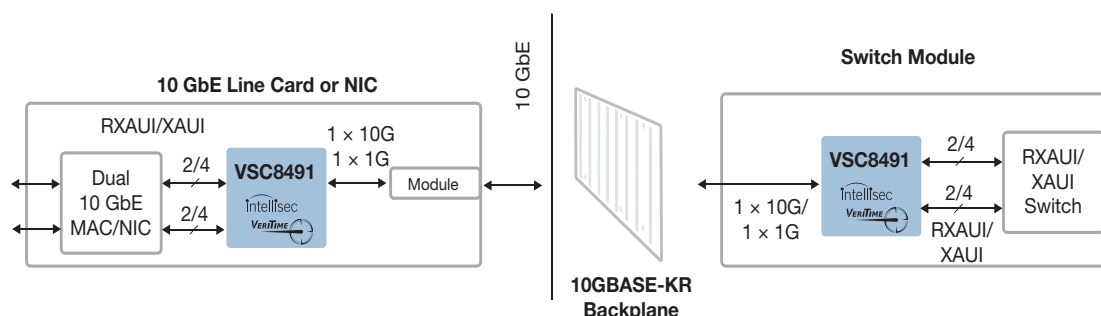
A complete suite of BIST functionality includes line and client loopbacks along with pattern generation and error detection. Highly flexible clocking options support LAN and WAN operation using single 156.25 MHz reference clock rate inputs for seamless Synchronous Ethernet support. The VSC8491 device includes a failover switching capability for protection routing, along with selectable lane ordering.

Highlights

- IEEE 1588v2 compliant
- 128/256-bit MACsec support
- RXAU/XAUI support
- SFP+ I/O with KR support
- 1 GbE support

Applications

- Multiple-port RXAU/XAUI to
- SFI/ SFP+ line cards or NICs
- 10GBASE-KR compliant backplane transceivers
- Carrier Ethernet networks requiring IEEE 1588v2 timing
- Secure data center-to-data center interconnects
- 10 GbE switch cards, router cards, and NICs



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Range of Support

- IEEE 1588v2/Y.1731 OAM precision timing support to within 4 ns accuracy at 1.25 Gbps and 10.3 Gbps
- Compliant to IEEE 802.1AE specifications for 128/256-bit MACsec support
- Compliant to IEEE 802.3ae and SFF-8431 electrical (SFI) specifications
- 9.95 Gbps WAN and 10.3 Gbps LAN operation, as well as 1.25 Gbps Ethernet support
- Supports all standard SFP+ applications
- Support for 10GBASE-KR (IEEE 802.3ap) for 10G backplanes, including 1.25 Gbps and 10.3 Gbps auto-negotiation
- Adaptive equalization receiver and programmable, multitap transmitter pre-emphasis
- Synchronous Ethernet support
- MDIO/SPI and two-wire serial slave management interfaces

Key Specifications

- 1.15 W typical for each bidirectional channel
- 1.2 V and 1.0 V core power supplies (2.5 V TTL supply)

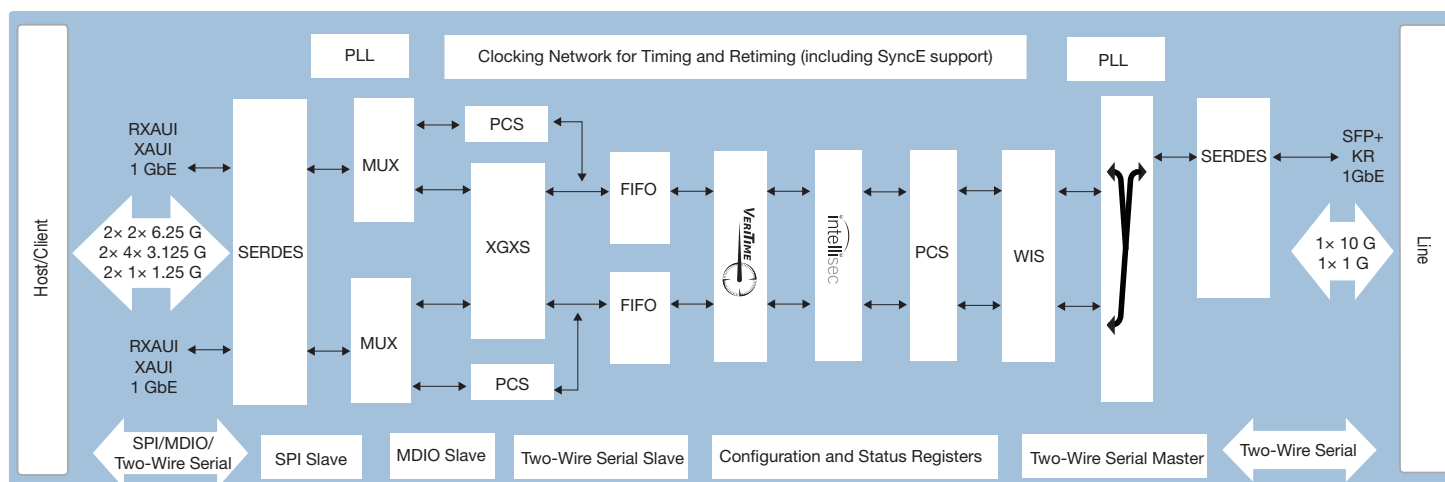
Flexibility

- Failover switching and lane ordering
- VScope input signal monitoring integrated circuit
- Host-side and line-side loopbacks with BIST functions
- I/O programmability for lane swap, invert, amplitude, slew, pre-emphasis, and equalization
- Optional forward error correction (FEC)
- Flexible clocking options enable Layer 1 support for Synchronous Ethernet
- Passive copper cable support for minimum transmission cost

Related Products

Visit www.microsemi.com for information about these related products:

- VSC8487-15
- VSC8488-15
- VSC8489
- VSC8490
- VSC8572/VSC8574
- VSC8584



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