

# 74LVC16374A-Q100; 74LVCH16374A-Q100

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Rev. 3 — 27 September 2021

Product data sheet

## 1. General description

The 74LVC16374A-Q100; 74LVCH16374A-Q100 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. The device features two clocks (1CP and 2CP) and two output enables (1 $\overline{OE}$  and 2 $\overline{OE}$ ), each controlling 8-bits. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (nCP) transition. A HIGH on n $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the n $\overline{OE}$  input does not affect the state of the flip-flops. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- Multibyte flow-through standard pinout architecture
- Low inductance multiple supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16374A-Q100 only)
- High-impedance outputs when V<sub>CC</sub> = 0 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC16374ADGG-Q100	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16374ADGG-Q100				

### 4. Functional diagram

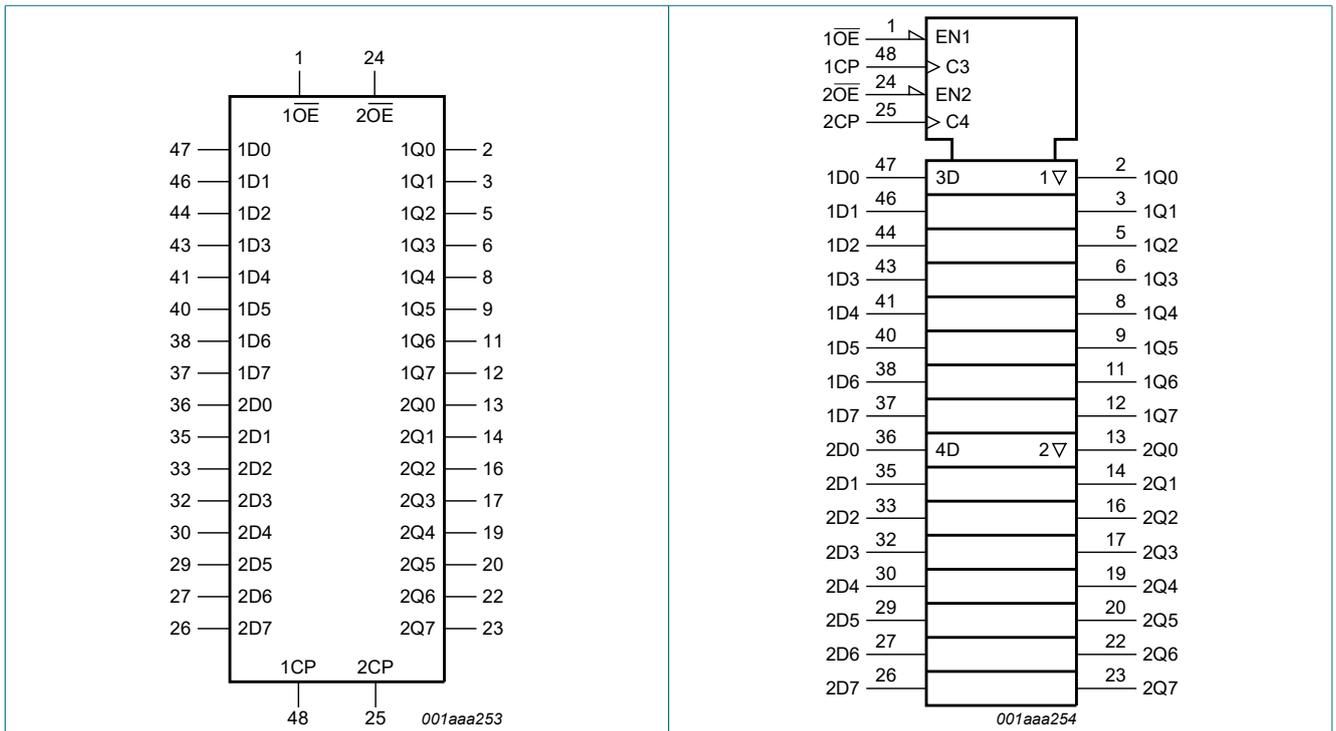


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

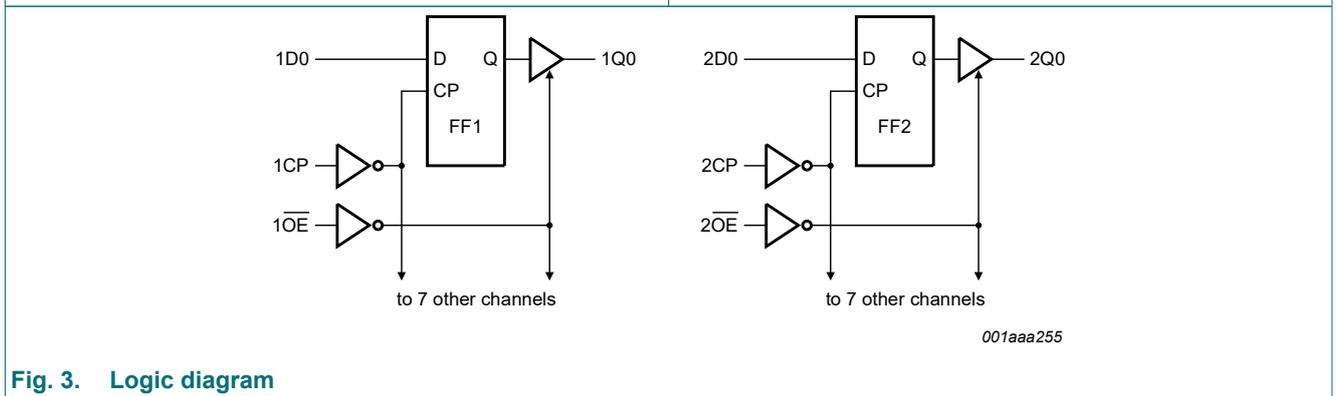


Fig. 3. Logic diagram

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

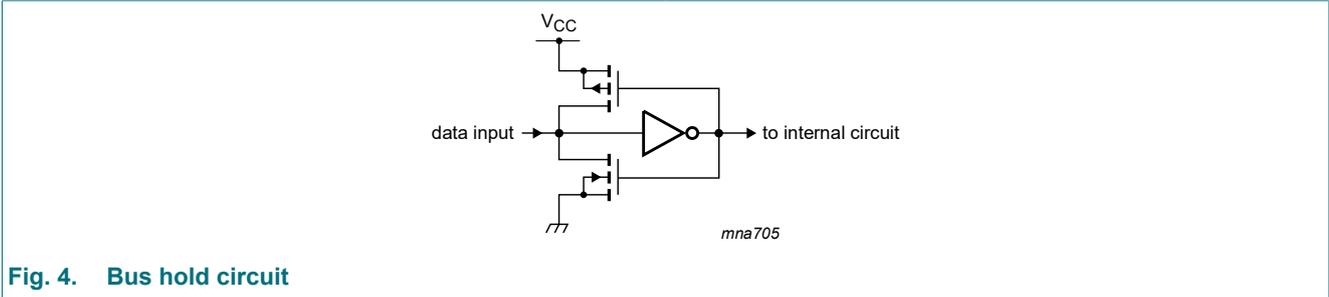


Fig. 4. Bus hold circuit

## 5. Pinning information

### 5.1. Pinning

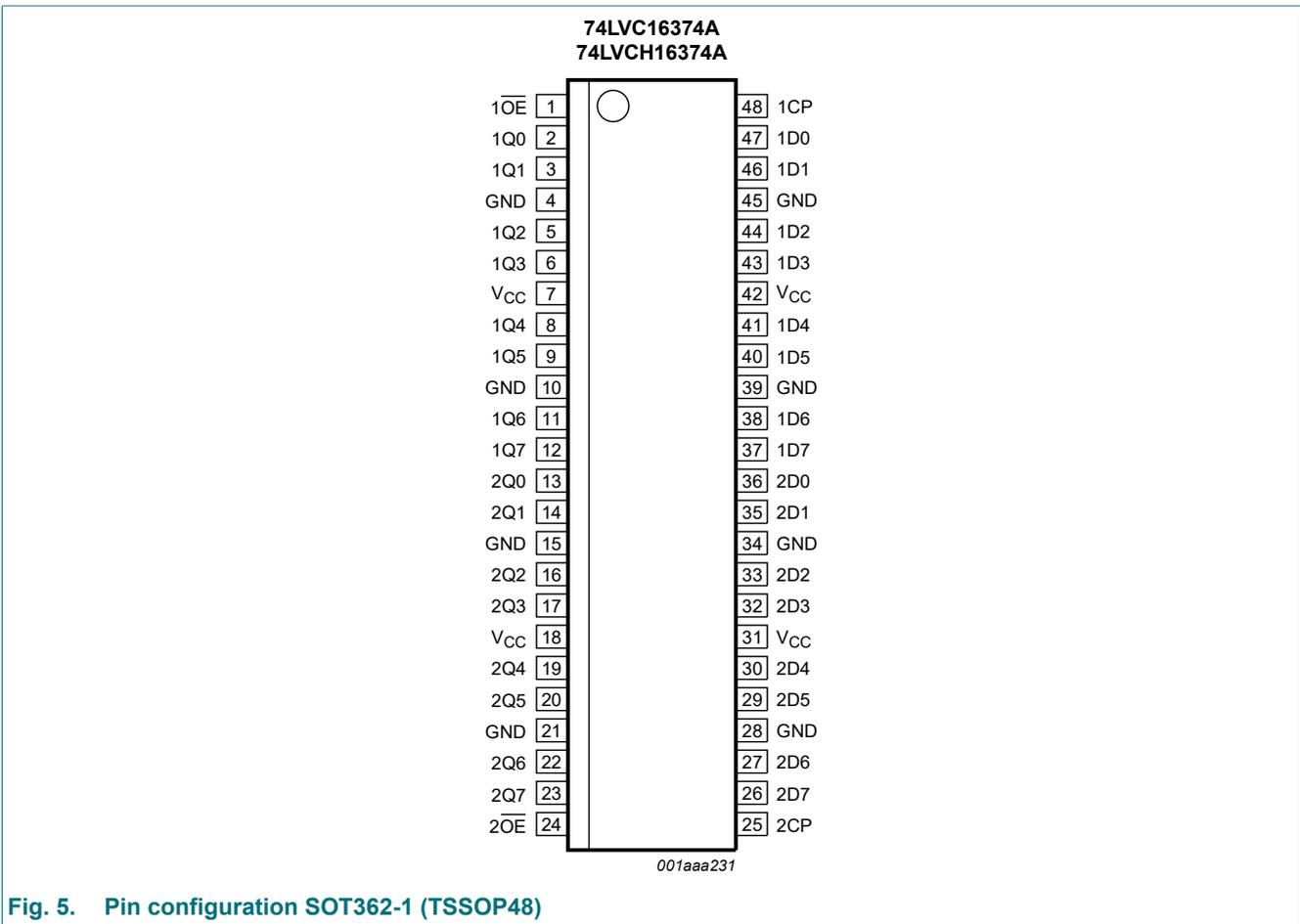


Fig. 5. Pin configuration SOT362-1 (TSSOP48)

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 24	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data output
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data output
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data input
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data input
1CP, 2CP	48, 25	clock input

## 6. Functional description

Table 3. Function selection

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;  
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;  
Z = high-impedance OFF-state; ↑ = LOW-to-HIGH transition.

Operating mode	Input			Internal flip-flop	Output nQ0 to nQ7
	nOE	nCP	nDn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH-or LOW-state	[2] -0.5	V <sub>CC</sub> + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT362-1 (TSSOP48) packages: P<sub>tot</sub> derates linearly with 12.2 mW/K above 109 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	active mode	0	-	V <sub>CC</sub>	V
		power-down mode; V <sub>CC</sub> = 0 V	0	-	5.5	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	0	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND [2]	-	±0.1	±5	-	±20	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 5.5 V or GND [2]	-	±0.1	±5	-	±20	μA

## 16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 5.5\text{ V}$	-	$\pm 0.1$	$\pm 10$	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.1	20	-	80	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ ; $V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$	-	5	500	-	5000	$\mu\text{A}$
$C_I$	input capacitance	$V_{CC} = 0\text{ V}$ to $3.6\text{ V}$ ; $V_I = \text{GND}$ to $V_{CC}$	-	5.0	-	-	-	pF
$I_{BHL}$	bus hold LOW current	$V_{CC} = 1.65\text{ V}$ ; $V_I = 0.58\text{ V}$ [3] [4]	10	-	-	10	-	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V}$ ; $V_I = 0.7\text{ V}$	30	-	-	25	-	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}$ ; $V_I = 0.8\text{ V}$	75	-	-	60	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 1.65\text{ V}$ ; $V_I = 1.07\text{ V}$ [3] [4]	-10	-	-	-10	-	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V}$ ; $V_I = 1.7\text{ V}$	-30	-	-	-25	-	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}$ ; $V_I = 2.0\text{ V}$	-75	-	-	-60	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 1.95\text{ V}$ [3] [5]	200	-	-	200	-	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V}$	300	-	-	300	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	500	-	-	500	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 1.95\text{ V}$ [3] [5]	-200	-	-	-200	-	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V}$	-300	-	-	-300	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	-500	-	-	-500	-	$\mu\text{A}$

[1] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  (unless stated otherwise) and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

[2] The bus hold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input pin.

[3] Valid for data inputs (74LVCH16374A) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified  $V_I$  level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	nCP to nQn; see Fig. 6 [2]						
		$V_{CC} = 1.2\text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	2.1	6.9	13.5	2.1	15.6	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.5	3.7	6.7	1.5	7.7	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.4	6.0	1.5	7.5	ns
$t_{en}$	enable time	$n\overline{OE}$ to nQn; see Fig. 7 [2]						
		$V_{CC} = 1.2\text{ V}$	-	20	-	-	-	ns
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	1.5	5.9	13.1	1.5	15.1	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.5	3.4	6.9	1.5	8.0	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.6	6.0	1.5	7.5	ns
	$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1.0	2.7	5.2	1.0	6.5	ns	

## 16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>dis</sub>	disable time	n $\overline{OE}$ to nQn; see Fig. 7 [2]						
		V <sub>CC</sub> = 1.2 V	-	12	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.8	4.6	9.1	2.8	10.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.5	4.9	1.0	5.7	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	5.1	1.5	6.5	ns
t <sub>w</sub>	pulse width	nCP HIGH; see Fig. 6						
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	1.5	-	3.0	-	ns
t <sub>su</sub>	set-up time	nDn to nCP; see Fig. 8						
		V <sub>CC</sub> = 1.65 V to 1.95 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 2.7 V	1.9	-	-	1.9	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.9	0.3	-	1.9	-	ns
t <sub>h</sub>	hold time	nDn to nCP; see Fig. 8						
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V <sub>CC</sub> = 2.7 V	1.1	-	-	1.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	+1.5	-0.3	-	1.5	-	ns
f <sub>max</sub>	maximum frequency	see Fig. 6						
		V <sub>CC</sub> = 1.65 V to 1.95 V	100	-	-	80	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	125	-	-	100	-	ns
		V <sub>CC</sub> = 2.7 V	150	-	-	120	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	150	300	-	120	-	MHz
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> [4]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	14.1	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	16.4	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	18.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

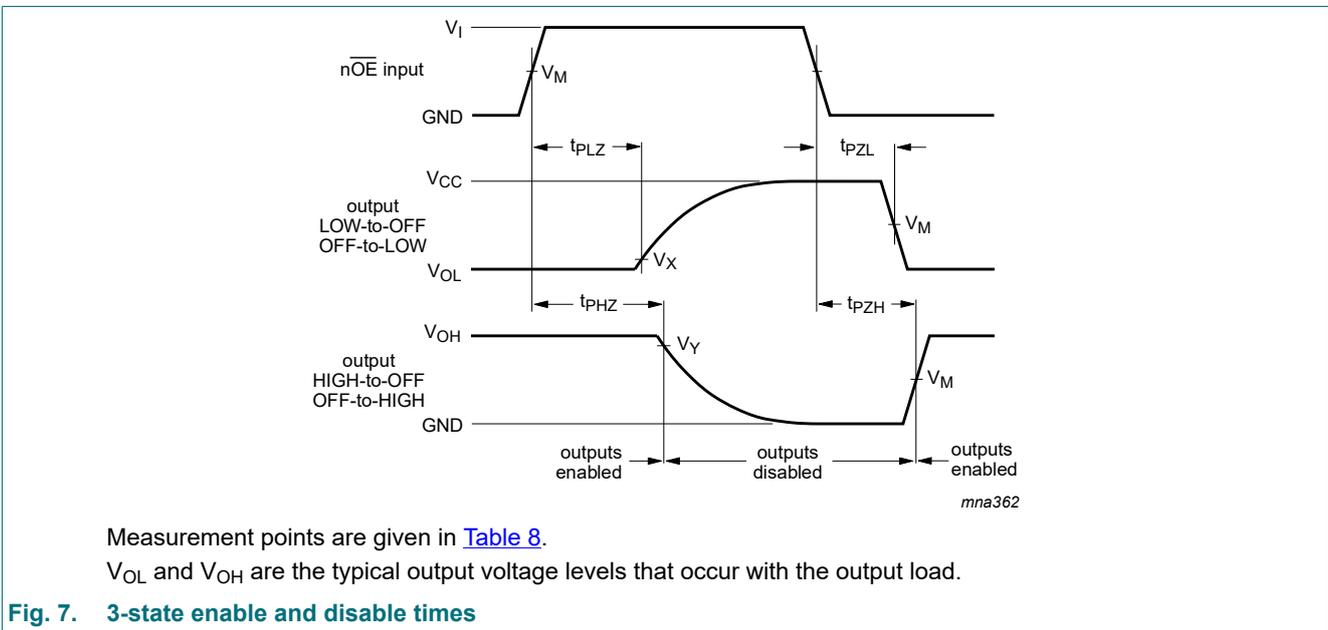
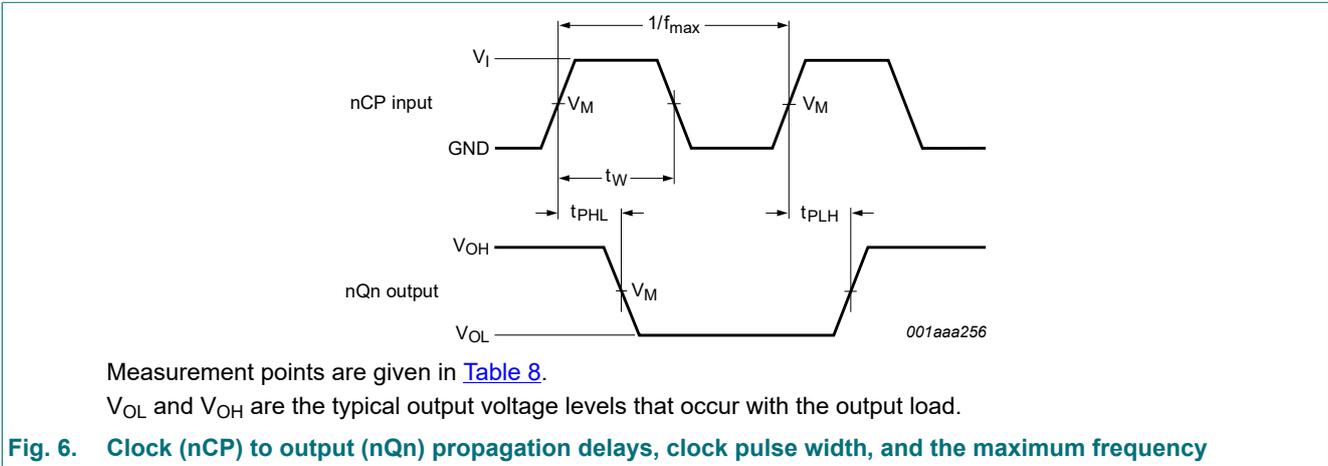
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

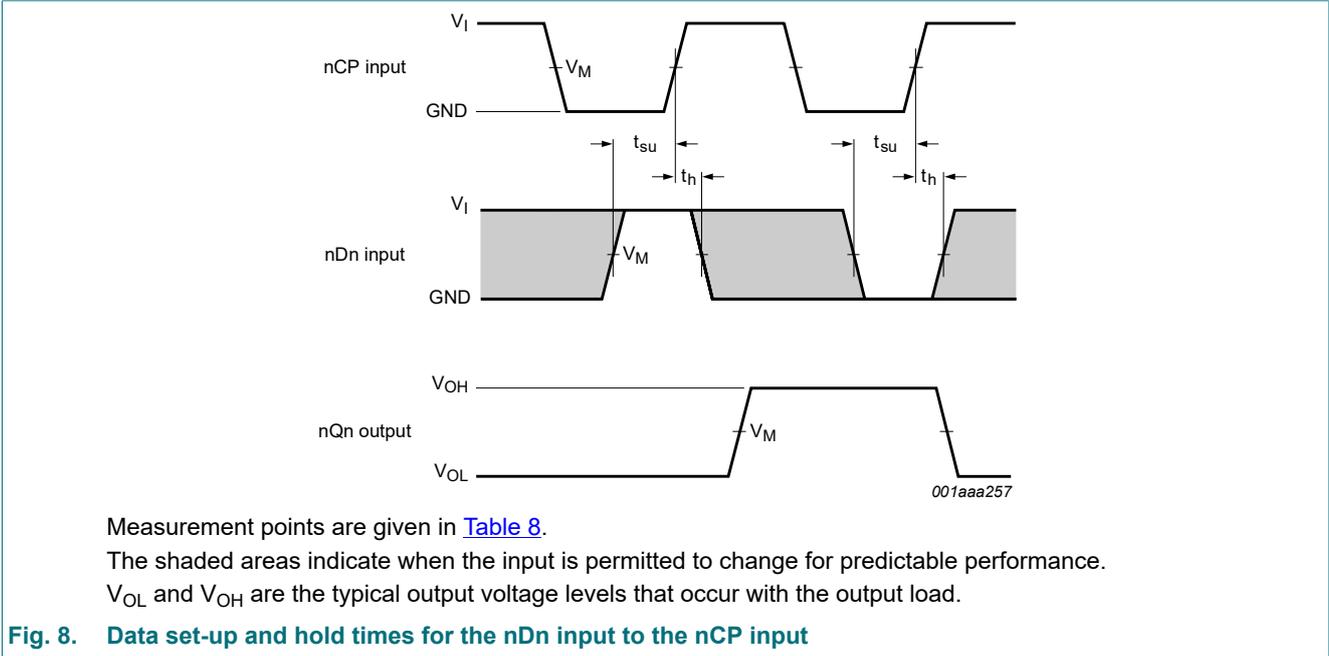
N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

10.1. Waveforms and test circuit



16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

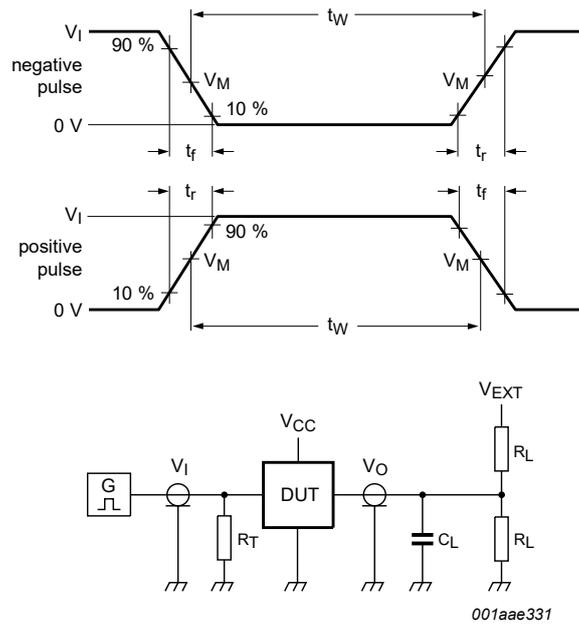


**Fig. 8. Data set-up and hold times for the nDn input to the nCP input**

**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state



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Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 9. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

### 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

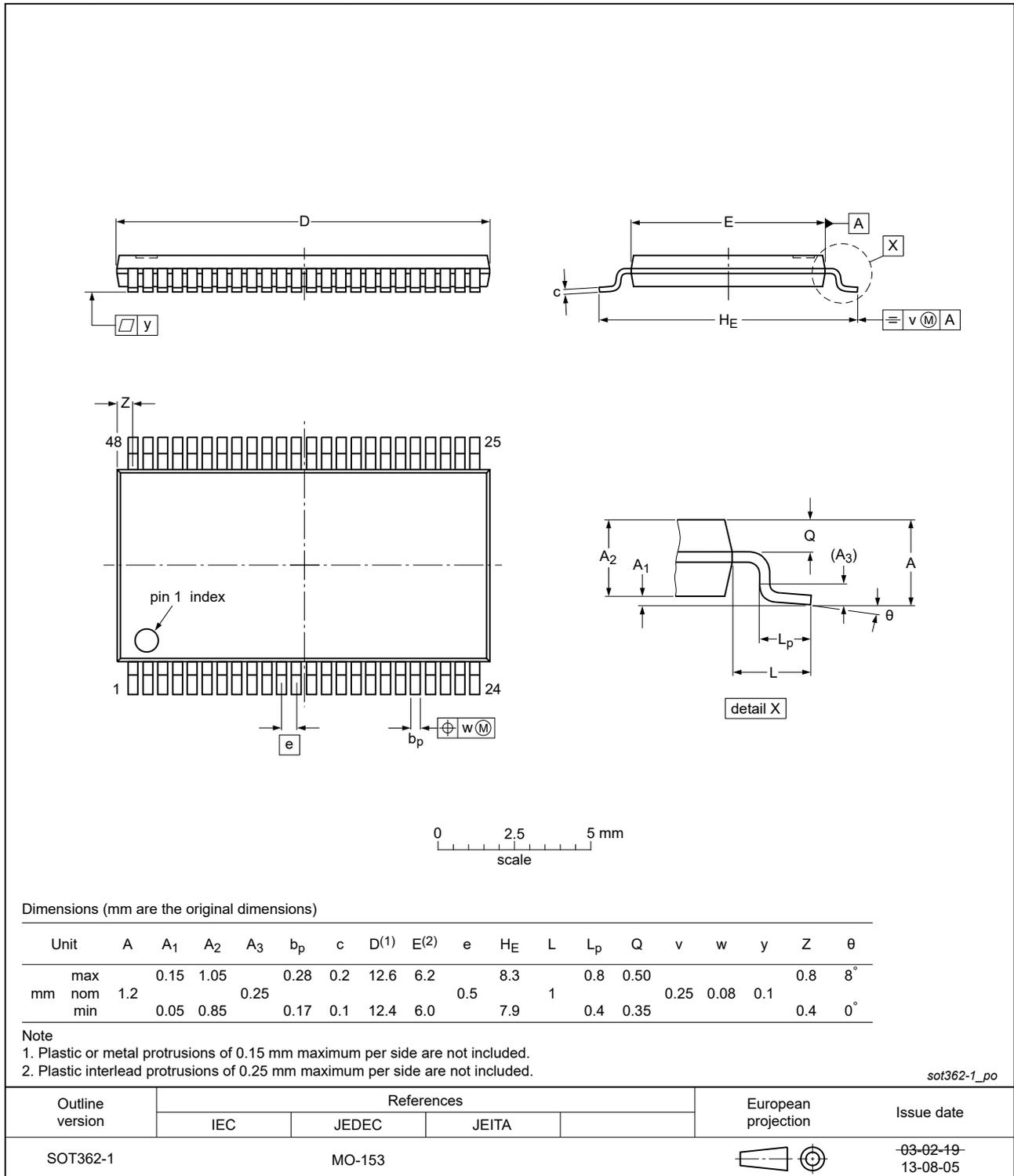


Fig. 10. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16374A_Q100 v.3	20210927	Product data sheet	-	74LVC_LVCH16374A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74LVC_LVCH16374A_Q100 v.2	20181120	Product data sheet	-	74LVC_LVCH16374A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVC_LVCH16374A_Q100 v.1	20130128	Product data sheet	-	-

## 16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

## 14. Legal information

## Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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