

**NuMicro<sup>®</sup> Family**  
**1T 8051-based Microcontroller**

# ML51/ML54/ML56 Series Datasheet

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## 1 GENERAL DESCRIPTION

The NuMicro®ML51/ML54/ML56 series is a Flash embedded 1T 8051-based microcontroller. The instruction set of the ML51 series is fully compatible with the standard 80C51 with enhanced performance; This series is a three-to-one single microcontrollers, integrated with up to 14 channels of capacitive touch and LCD driver.

The ML51/ML54/ML56 series is 1T 8051 core based low-power microcontrollers running at less 80μA/MHz in normal run mode, and power down current is below 1uA. It Provides operating frequency up to 24 MHz. 16KB and 32KB Flash of ML51 series voltage range supports 1.8V to 5.5V, and 64KB Flash of ML51 series supports 1.8 to 3.6V voltage range.

The ML51/ML54/ML56 series microcontroller provides 3 power modes to reduce power consumption — Low power run mode, Low power Idle mode, and Power-down mode. In Low power run mode, the power consumption can be down to 15 uA at 38.4 kHz LIRC. In Low power idle mode, CPU processing is suspended by holding the Program Counter. No program code is fetched and run in low power idle mode if the power consumption does not exceed 13 uA. Power-down mode stops the whole system clock for minimum power consumption with the leakage current less than 1 uA. The system clock of the ML51 series can also be slowed down by software clock divider, which allows for flexibility between execution performance and power consumption.

The ML51/ML54/ML56 series provides rich peripherals including 256 bytes of SRAM, 4 Kbytes of auxiliary RAM (XRAM), up to 56 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, two ISO7816 Smartcard interface, two SPI, two I2C, 6 enhanced PWM output channels with dead zone control, 6 PWM output channels with 3 individual configurable period, two analog comparators, eight-channel shared pin interrupt for all I/O ports, and one 12-bit ADC at 500 ksp/s. There are a total of 31 sources with 4-level-priority interrupts capability.

All series contains up to 64 Kbytes Flash, called APROM designed for programming. Flash supports In-Application-Programming (IAP) function, which supports on-chip firmware upgrade. Partial flash can be configured as Data Flash programmed by IAP and read by IAP or MOVC instruction. The ML51/ML54/ML56 series includes an additional configurable up to 4/3/2/1 Kbytes Flash area called LDROM, in which the Boot Code normally resides for carrying out the In-System-Programming (ISP). To facilitate mass production programming and verification, the Flash is allowed to be programmed and read electronically by parallel Writer/Programmer or In-Circuit-Programming (ICP) with Nu-Link. Once programmed and verified, the programmed code can be protected by the Flash lock mechanism from being read out by external programming tool.

Through the high performance and low power features of ML51/ML54/ML56 series, this series benefits for low-power, battery powered devices, general purpose, home appliances, and motor control system.

| Series                           | V <sub>DD</sub> Voltage | LCD Driver | Touch Key |
|----------------------------------|-------------------------|------------|-----------|
| <b>ML51 32/16KB Flash Series</b> | 1.8 ~ 5.5 V             | -          | -         |
| <b>ML51 64KB Flash Series</b>    | 1.8 ~3.6 V              | -          | -         |
| <b>ML54 Series</b>               | 1.8 ~3.6 V              | ✓          | -         |
| <b>ML56 Series</b>               | 1.8 ~3.6 V              | ✓          | ✓         |

## 2 FEATURES

| <i>Core and System</i>          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>8051</b>                     | <ul style="list-style-type: none"> <li>Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller.</li> <li>Instruction set fully compatible with MCS-51.</li> <li>4-priority-level interrupts capability.</li> <li>Dual Data Pointers (DPTRs).</li> </ul>                                                                                                                                                                                        |
| <b>Power on Reset (POR)</b>     | <ul style="list-style-type: none"> <li>POR with 1.55V threshold voltage level</li> </ul>                                                                                                                                                                                                                                                                                                                                                                             |
| <b>Brown-out Detector (BOD)</b> | <ul style="list-style-type: none"> <li>7-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 3.0V / 2.7V / 2.4V / 2.0V / 1.8V)</li> </ul>                                                                                                                                                                                                                                                                                                     |
| <b>Low Voltage Reset (LVR)</b>  | <ul style="list-style-type: none"> <li>LVR with 1.63V threshold voltage level</li> </ul>                                                                                                                                                                                                                                                                                                                                                                             |
| <b>Security</b>                 | <ul style="list-style-type: none"> <li>96-bit Unique ID (UID)</li> <li>128-bit Unique Customer ID (UCID)</li> <li>128-bytes security protection memory SPROM</li> </ul>                                                                                                                                                                                                                                                                                              |
| <i>Memories</i>                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Flash</b>                    | <ul style="list-style-type: none"> <li>Up to 64 KBytes of APROM for User Code.</li> <li>4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP)</li> <li>Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash</li> <li>An additional 128 bytes security protection memory SPROM</li> <li>Code lock for security by CONFIG</li> </ul> |
| <b>SRAM</b>                     | <ul style="list-style-type: none"> <li>256 Bytes on-chip RAM.</li> <li>Additional 4 KBytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.</li> </ul>                                                                                                                                                                                                                                                                                                     |
| <b>PDMA:</b>                    | <ul style="list-style-type: none"> <li>Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer.</li> <li>Source address and destination address must be word alignment in all modes.</li> <li>Memory-to-memory mode: transfer length must be word alignment.</li> </ul>                                                                                                                                                               |
| <i>Clocks</i>                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>External Clock Source</b>    | <ul style="list-style-type: none"> <li>4~24 MHz High-speed external crystal oscillator (HXT) for</li> </ul>                                                                                                                                                                                                                                                                                                                                                          |

|                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                       | <ul style="list-style-type: none"> <li>precise timing operation</li> <li>32.768 kHz High-speed external crystal oscillator (LXT) for RTC operation</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Internal Clock Source | <ul style="list-style-type: none"> <li>Default 24 MHz high-speed internal oscillator (HIRC) trimmed to <math>\pm 1\%</math> (accuracy at 25 °C, 3.3 V), <math>\pm 2\%</math> in -20~105°C.</li> <li>38.4 kHz low-speed internal oscillator (LIRC) calibrating to <math>\pm 2\%</math> by software from high-speed internal oscillator</li> </ul>                                                                                                                                                                                                                                                                                              |
| <b>Timers</b>         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 16-bit Timer          | <ul style="list-style-type: none"> <li>Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.</li> <li>One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected.</li> <li>One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.</li> </ul>                                                                                                                                                                                                                                                                                                                           |
| Watchdog              | <ul style="list-style-type: none"> <li>6-bit free running up counter for WDT time-out interval.</li> <li>Selectable time-out interval is 1.66 ms ~ 3413.12 ms since WDT_CLK = 38.4 kHz (LIRC).</li> <li>Able to wake up from Power-down or Idle mode</li> <li>Interrupt or reset selectable on watchdog time-out</li> </ul>                                                                                                                                                                                                                                                                                                                   |
| Wake-up Timer         | <ul style="list-style-type: none"> <li>16-bit free running up counter for time-out interval.</li> <li>Clock sources from LIRC</li> <li>Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value.</li> <li>Supports Interrupt</li> </ul>                                                                                                                                                                                                                                                                                                                                                                            |
| PWM                   | <ul style="list-style-type: none"> <li>Up To 12 output pins can be selected</li> <li>Supports maximum clock source frequency up to 24 MHz</li> <li>Supports up to Three PWM modules, each module provides 6 output channels.</li> <li>Supports independent mode for PWM output</li> <li>Supports complementary mode for 3 complementary paired PWM output channels</li> <li>Dead-time insertion with 8-bit resolution</li> <li>Supports 16-bit resolution PWM counter</li> <li>Supports mask function and tri-state enable for each PWM pin</li> <li>Supports brake function</li> <li>Supports trigger ADC on the following events</li> </ul> |
| RTC                   | <ul style="list-style-type: none"> <li>Supports real time counter and calendar counter for RTC time and calendar check.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

- Supports alarm time and calendar settings
- Supports alarm time and calendar mask enable settings.
- Selectable 12-hour or 24-hour time scale setting.
- Supports Leap Year indication setting.
- Supports Day of the Week counter setting.
- Frequency of RTC clock source compensate by RTC\_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Support clock source selectable from LXT or LIRC.

#### Analog Interfaces

##### Analog-to-Digital Converter (ADC)

- Analog input voltage range: 0 ~ AV<sub>DD</sub>.
- External or internal Voltage reference input selectable.
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels
- 1 internal channels, they are band-gap voltage (VBG).
- Maximum ADC peripheral clock frequency is 1 MHz.
- Up to 500 KSPS sampling rate.
- Software Write 1 to ADCS bit to trig ADC start.
- External pin (STADC) trigger
- PWM trigger.

#### Communication Interfaces

##### UART

- Supports up to 2 UARTs: UART0, UART1
- Supports 2 Smart Card configuration as UART function as UART2 and UART3.
- UART baud rate clock from HIRC or HXT.
- Full-duplex asynchronous communications
- Programmable 9<sup>th</sup> bit.
- TXD and RXD pins of UART0 exchangeable via software.

##### I<sup>2</sup>C

- 2 sets of I<sup>2</sup>C devices
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)

|                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                   | <ul style="list-style-type: none"> <li>• 7-bit addressing mode</li> <li>• Standard mode (100 kbps) and Fast mode (400 kbps).</li> <li>• Supports 8-bit time-out counter requesting the I<sup>2</sup>C interrupt if the I<sup>2</sup>C bus hangs up and timer-out counter overflows</li> <li>• Multiple address recognition (four slave addresses with mask option)</li> <li>• Supports hold time programmable</li> </ul>                                                                                                                                                                                                                                                                                                                                                        |
| <b>SPI</b>        | <ul style="list-style-type: none"> <li>• 2 sets of SPI devices</li> <li>• Supports Master or Slave mode operation</li> <li>• Supports MSB first or LSB first transfer sequence</li> <li>• Slave mode up to 12 Mhz</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>ISO 7816-3</b> | <ul style="list-style-type: none"> <li>• Two sets ISO 7816-3 device</li> <li>• Supports ISO 7816-3 compliant T=0, T=1</li> <li>• Supports full-duplex UART mode.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>GPIO</b>       | <ul style="list-style-type: none"> <li>• Four I/O modes:</li> <li>• Quasi-bidirectional mode</li> <li>• Push-Pull Output mode</li> <li>• Open-Drain Output mode</li> <li>• Input only with high impedance mode</li> <li>• Schmitt trigger input / TTL mode selectable.</li> <li>• Each I/O pin configured as interrupt source with edge/level trigger setting</li> <li>• Standard interrupt pins INT0 and INT1.</li> <li>• Supports high drive and high sink current I/O</li> <li>• I/O pin internal pull-up or pull-down resistor enabled in input mode.</li> <li>• Maximum I/O Speed is 24 MHz</li> <li>• Enabling the pin interrupt function will also enable the wake-up function</li> <li>• Supports 5V-tolerance function for ML51 64KB Flash/ML54/ML56 Series</li> </ul> |
| <b>LCD Driver</b> | <ul style="list-style-type: none"> <li>• Support Internal resistor bias</li> <li>• Support programmable internal VLCD charge pump mode</li> <li>• 1/2, 1/3, 1/4 bias selectable</li> <li>• 4 COM x 32 SEG / 6 COM x 30 SEG / 8 COM x 28 SEG</li> <li>• Support 1.8V to 5.5V LCD operating voltage</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>Touch Key</b>  | <ul style="list-style-type: none"> <li>• Supports up to 14 Touch Keys + Reference Pad + Shielding Electrode</li> <li>• Supports any TK pin as reference pad and any one of CLK0</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

pin as shielding electrode.

- Programmable sensitivity levels for each channel.
- Programmable scanning speed for different applications.
- Supports effect when in Power-down mode.
- Supports single key-scan and programmable periodic key-scan.
- Programmable interrupt options for key-scan complete with hardware without threshold control.

#### ESD & EFT

##### ESD

- HBM  $\pm 8$  kV for ML51 32KB/16KB Flash Series pass
- HBM  $\pm 7$  kV for ML51 64KB Flash/ML54/ML56 Series pass

##### EFT

- $> \pm 4.4$  kV

##### Latch-up

- 150 mA for ML51 32KB/16KB Flash Series pass
- 200 mA for ML51 64KB Flash/ML54/ML56 Series pass

### 3 PART INFORMATION

#### 3.1 ML51/ML54/ML56 Series Package Type

| Package    | ML51      |           |           | ML54      | ML56      |
|------------|-----------|-----------|-----------|-----------|-----------|
|            | ML51xB    | ML51xC    | ML51xD    | ML54xD    | ML56xD    |
| MSOP10     | ML51BB9AE |           |           |           |           |
| TSSOP14    | ML51DB9AE |           |           |           |           |
| TSSOP20    | ML51FB9AE |           |           |           |           |
| SOP20      | ML51OB9AE |           |           |           |           |
| QFN20(3x3) | ML51XB9AE |           |           |           |           |
| TSSOP28    | ML51EB9AE | ML51EC0AE |           |           |           |
| SOP28      | ML51UB9AE | ML51UC0AE |           |           |           |
| LQFP32     | ML51PB9AE | ML51PC0AE |           |           |           |
| QFN33(4x4) | ML51TB9AE | ML51TC0AE | ML51TD1AE |           |           |
| LQFP44     |           |           |           | ML54MD1AE | ML56MD1AE |
| LQFP48     | ML51LD1AE |           |           | ML54LD1AE | ML56LD1AE |
| LQFP64     | ML51SD1AE |           |           | ML54SD1AE | ML56SD1AE |

### 3.2 ML51/ML54/ML56 Series Selection Guide

#### 3.2.1 ML51 Series

##### ML51 16KB Flash Series

| Part Number                                                                                                                                                    |                  | ML51   |         |         |       |       |         |       |        |       |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------|---------|---------|-------|-------|---------|-------|--------|-------|
|                                                                                                                                                                |                  | BB9AE  | DB9AE   | FB9AE   | OB9AE | XB9AE | EB9AE   | UB9AE | PB9AE  | TB9AE |
| Flash (KB)                                                                                                                                                     |                  | 16     | 16      | 16      | 16    | 16    | 16      | 16    | 16     | 16    |
| SRAM (KB)                                                                                                                                                      |                  | 1      | 1       | 1       | 1     | 1     | 1       | 2     | 2      | 2     |
| ISP ROM (KB)                                                                                                                                                   |                  | 4      | 4       | 4       | 4     | 4     | 4       | 4     | 4      | 4     |
| SPROM (bytes)                                                                                                                                                  |                  | 128    | 128     | 128     | 128   | 128   | 128     | 128   | 128    | 128   |
| System Frequency ( MHz)                                                                                                                                        |                  | 24     | 24      | 24      | 24    | 24    | 24      | 24    | 24     | 24    |
| GPIO                                                                                                                                                           |                  | 7      | 11      | 16      | 16    | 17    | 24      | 24    | 28     | 28    |
| 16-bit Timer                                                                                                                                                   |                  | 4      | 4       | 4       | 4     | 4     | 4       | 4     | 4      | 4     |
| PWM                                                                                                                                                            |                  | 5      | 6       | 6       | 6     | 6     | 6       | 6     | 6      | 6     |
| Analog Comparator                                                                                                                                              |                  | -      | -       | -       | -     | -     | -       | -     | 2      | 2     |
| Internal Voltage Reference                                                                                                                                     |                  | -      | -       | -       | -     | -     | -       | -     | Y      | Y     |
| PDMA                                                                                                                                                           |                  | 2      | 2       | 2       | 2     | 2     | 2       | 2     | 2      | 2     |
| RTC                                                                                                                                                            |                  | -      | -       | -       | -     | -     | -       | -     | -      | -     |
| LCD                                                                                                                                                            |                  | -      | -       | -       | -     | -     | -       | -     | -      | -     |
| Connectivity                                                                                                                                                   | ISO 7816-3       | -      | 1       | 1       | 1     | 1     | 1       | 1     | 1      | 1     |
|                                                                                                                                                                | UART             | 2      | 2       | 2       | 2     | 2     | 2       | 2     | 2      | 2     |
|                                                                                                                                                                | SPI              | -      | 1       | 1       | 1     | 1     | 1       | 1     | 1      | 1     |
|                                                                                                                                                                | I <sup>2</sup> C | 1      | 2       | 2       | 2     | 2     | 2       | 2     | 2      | 2     |
| 12-bit SAR ADC                                                                                                                                                 |                  | 2      | 3       | 6       | 6     | 6     | 8       | 8     | 8      | 8     |
| Package                                                                                                                                                        |                  | MSOP10 | TSSOP14 | TSSOP20 | SOP20 | QFN20 | TSSOP28 | SOP28 | LQFP32 | QFN33 |
| Note:<br>1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.<br>2. ISO 7816-3 configurable as standard UART function. |                  |        |         |         |       |       |         |       |        |       |

**ML51 32KB Flash Series**

| Part Number                                                                                                                                                                                                                        |                  | ML51             |                  |        |       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------|------------------|--------|-------|
|                                                                                                                                                                                                                                    |                  | EC0AE            | UC0AE            | PC0AE  | TC0AE |
| Flash (KB)                                                                                                                                                                                                                         |                  | 32               | 32               | 32     | 32    |
| SRAM (KB)                                                                                                                                                                                                                          |                  | 2                | 2                | 2      | 2     |
| ISP ROM (KB)                                                                                                                                                                                                                       |                  | 4                | 4                | 4      | 4     |
| SPROM (bytes)                                                                                                                                                                                                                      |                  | 128              | 128              | 128    | 128   |
| System Frequency ( MHz)                                                                                                                                                                                                            |                  | 24               | 24               | 24     | 24    |
| GPIO                                                                                                                                                                                                                               |                  | 24               | 24               | 28     | 28    |
| 16-bit Timer                                                                                                                                                                                                                       |                  | 4                | 4                | 4      | 4     |
| PWM                                                                                                                                                                                                                                |                  | 6                | 6                | 6      | 6     |
| Analog Comparator                                                                                                                                                                                                                  |                  | 2                | 2                | 2      | 2     |
| Internal Voltage Reference                                                                                                                                                                                                         |                  | Y                | Y                | Y      | Y     |
| PDMA                                                                                                                                                                                                                               |                  | 2                | 2                | 2      | 2     |
| RTC                                                                                                                                                                                                                                |                  | -                | -                | -      | -     |
| LCD                                                                                                                                                                                                                                |                  | -                | -                | -      | -     |
| Connectivity                                                                                                                                                                                                                       | ISO 7816-3       | 1                | 1                | 1      | 1     |
|                                                                                                                                                                                                                                    | UART             | 2                | 2                | 2      | 2     |
|                                                                                                                                                                                                                                    | SPI              | 2 <sup>[3]</sup> | 2 <sup>[3]</sup> | 2      | 2     |
|                                                                                                                                                                                                                                    | I <sup>2</sup> C | 2                | 2                | 2      | 2     |
| 12-bit SAR ADC                                                                                                                                                                                                                     |                  | 8                | 8                | 8      | 8     |
| Package                                                                                                                                                                                                                            |                  | TSSOP28          | SOP28            | LQFP32 | QFN33 |
| <b>Note:</b><br>1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.<br>2. ISO 7816-3 configurable as standard UART function.<br>3. SPI0 and SPI1 share with same SS pin in 28pin package. |                  |                  |                  |        |       |

**ML51 64KB Flash Series**

| Part Number                                                                                                                                                           |                  | ML51    |         |         |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|---------|---------|
|                                                                                                                                                                       |                  | TD1AE   | LD1AE   | SD1AE   |
| Flash (KB)                                                                                                                                                            |                  | 64      | 64      | 64      |
| SRAM (KB)                                                                                                                                                             |                  | 4       | 4       | 4       |
| ISP ROM (KB)                                                                                                                                                          |                  | 4       | 4       | 4       |
| SPROM (bytes)                                                                                                                                                         |                  | 128     | 128     | 128     |
| System Frequency ( MHz)                                                                                                                                               |                  | 24      | 24      | 24      |
| GPIO                                                                                                                                                                  |                  | 28      | 43      | 56      |
| 16-bit Timer                                                                                                                                                          |                  | 4       | 4       | 4       |
| PWM                                                                                                                                                                   |                  | 6+2+2+2 | 6+2+2+2 | 6+2+2+2 |
| Analog Comparator                                                                                                                                                     |                  | 2       | 2       | 2       |
| Internal Voltage Reference                                                                                                                                            |                  | Y       | Y       | Y       |
| PDMA                                                                                                                                                                  |                  | 4       | 4       | 4       |
| RTC                                                                                                                                                                   |                  | Y       | Y       | Y       |
| LCD                                                                                                                                                                   |                  | -       | -       | -       |
| Connectivity                                                                                                                                                          | ISO 7816-3       | 2       | 2       | 2       |
|                                                                                                                                                                       | UART             | 2       | 2       | 2       |
|                                                                                                                                                                       | SPI              | 2       | 2       | 2       |
|                                                                                                                                                                       | I <sup>2</sup> C | 2       | 2       | 2       |
| 12-bit SAR ADC                                                                                                                                                        |                  | 9       | 10      | 14      |
| Package                                                                                                                                                               |                  | QFN33   | LQFP48  | LQFP64  |
| <b>Note:</b><br>1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.<br>2. ISO 7816-3 configurable as standard UART function. |                  |         |         |         |

**3.2.2 ML54 Series**

| Part Number                                                                                                                                                           |                  | ML54    |         |         |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|---------|---------|
|                                                                                                                                                                       |                  | MD1AE   | LD1AE   | SD1AE   |
| Flash (KB)                                                                                                                                                            |                  | 64      | 64      | 64      |
| SRAM (KB)                                                                                                                                                             |                  | 4       | 4       | 4       |
| ISP ROM (KB)                                                                                                                                                          |                  | 4       | 4       | 4       |
| SPROM (bytes)                                                                                                                                                         |                  | 128     | 128     | 128     |
| System Frequency ( MHz)                                                                                                                                               |                  | 24      | 24      | 24      |
| GPIO                                                                                                                                                                  |                  | 38      | 42      | 55      |
| 16-bit Timer                                                                                                                                                          |                  | 4       | 4       | 4       |
| PWM                                                                                                                                                                   |                  | 6+2+2+2 | 6+2+2+2 | 6+2+2+2 |
| Analog Comparator                                                                                                                                                     |                  | 2       | 2       | 2       |
| Internal Voltage Reference                                                                                                                                            |                  | Y       | Y       | Y       |
| PDMA                                                                                                                                                                  |                  | 4       | 4       | 4       |
| RTC                                                                                                                                                                   |                  | Y       | Y       | Y       |
| LCD                                                                                                                                                                   |                  | 8x17    | 8x18    | 8x28    |
|                                                                                                                                                                       |                  | 6x19    | 6x20    | 6x30    |
|                                                                                                                                                                       |                  | 4x21    | 4x22    | 4x32    |
| Connectivity                                                                                                                                                          | ISO 7816-3       | 2       | 2       | 2       |
|                                                                                                                                                                       | UART             | 2       | 2       | 2       |
|                                                                                                                                                                       | SPI              | 2       | 2       | 2       |
|                                                                                                                                                                       | I <sup>2</sup> C | 2       | 2       | 2       |
| 12-bit SAR ADC                                                                                                                                                        |                  | 10      | 10      | 14      |
| Package                                                                                                                                                               |                  | LQFP44  | LQFP48  | LQFP64  |
| <b>Note:</b><br>1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.<br>2. ISO 7816-3 configurable as standard UART function. |                  |         |         |         |

**3.2.3 ML56 Series**

| Part Number                                                                                                                                                                                                                |                  | ML56    |         |         |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|---------|---------|
|                                                                                                                                                                                                                            |                  | MD1AE   | LD1AE   | SD1AE   |
| Flash (KB)                                                                                                                                                                                                                 |                  | 64      | 64      | 64      |
| SRAM (KB)                                                                                                                                                                                                                  |                  | 4       | 4       | 4       |
| ISP ROM (KB)                                                                                                                                                                                                               |                  | 4       | 4       | 4       |
| SPROM (bytes)                                                                                                                                                                                                              |                  | 128     | 128     | 128     |
| System Frequency ( MHz)                                                                                                                                                                                                    |                  | 24      | 24      | 24      |
| GPIO                                                                                                                                                                                                                       |                  | 38      | 42      | 55      |
| 16-bit Timer                                                                                                                                                                                                               |                  | 4       | 4       | 4       |
| PWM                                                                                                                                                                                                                        |                  | 6+2+2+2 | 6+2+2+2 | 6+2+2+2 |
| Analog Comparator                                                                                                                                                                                                          |                  | 2       | 2       | 2       |
| Internal Voltage Reference                                                                                                                                                                                                 |                  | Y       | Y       | Y       |
| PDMA                                                                                                                                                                                                                       |                  | 4       | 4       | 4       |
| RTC                                                                                                                                                                                                                        |                  | Y       | Y       | Y       |
| LCD                                                                                                                                                                                                                        |                  | 8x17    | 8x18    | 8x28    |
|                                                                                                                                                                                                                            |                  | 6x19    | 6x20    | 6x30    |
|                                                                                                                                                                                                                            |                  | 4x21    | 4x22    | 4x32    |
| Touch Key                                                                                                                                                                                                                  |                  | 6+1     | 9+1     | 14+1    |
| Connectivity                                                                                                                                                                                                               | ISO 7816-3       | 2       | 2       | 2       |
|                                                                                                                                                                                                                            | UART             | 2       | 2       | 2       |
|                                                                                                                                                                                                                            | SPI              | 2       | 2       | 2       |
|                                                                                                                                                                                                                            | I <sup>2</sup> C | 2       | 2       | 2       |
| 12-bit SAR ADC                                                                                                                                                                                                             |                  | 10      | 10      | 14      |
| Package                                                                                                                                                                                                                    |                  | LQFP44  | LQFP48  | LQFP64  |
| <b>Note:</b><br>1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.<br>2. ISO 7816-3 configurable as standard UART function.<br>3.Touch key should define 1 key as reference pin. |                  |         |         |         |

**3.3 ML51/ML54/ML56 Series Selection Code**

| ML                   | 51        | F                       | B        | 9          | A       | E              |
|----------------------|-----------|-------------------------|----------|------------|---------|----------------|
| Core                 | Line      | Package                 | Flash    | SRAM       | Reserve | Temperature    |
| 1T 8051<br>Low power | 51: Base  | B: MSOP10 (3x3 mm)      | A: 8 KB  | 0: 2 KB    |         | E:-40 ~ 105° C |
|                      | 54: LCD   | D: TSSOP14 (4.4x5.0 mm) | B: 16 KB | 1: 4 KB    |         |                |
|                      | 56: Touch | E: TSSOP28 (4.4x9.7 mm) | C: 32 KB | 2: 8/12 KB |         |                |
|                      |           | F: TSSOP20 (4.4x6.5 mm) | D: 64 KB | 3: 16 KB   |         |                |
|                      |           | L: LQFP48 (7x7 mm)      |          | 6: 32 KB   |         |                |
|                      |           | M: LQFP44(10x10 mm)     |          | 8: 64 KB   |         |                |
|                      |           | O: SOP20 (300 mil)      |          | 9: 1 KB    |         |                |
|                      |           | P: LQFP32 (7x7 mm)      |          | A: 96 KB   |         |                |
|                      |           | S: LQFP64 (7x7 mm)      |          |            |         |                |
|                      |           | T: QFN33 (4x4 mm)       |          |            |         |                |
|                      |           | U: SOP28 (300 mil)      |          |            |         |                |
|                      |           | X: QFN20 (3x3mm)        |          |            |         |                |

## 4 PIN CONFIGURATION

### 4.1 Pin Configuration

Users can find pin configuration informations in chapter 4 or by using [NuTool - PinConfigure](#). The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

#### 4.1.1 ML51/ML54/ML56 Series Pin Diagram

##### 4.1.1.1 LQFP64 Package

Corresponding Part Number: ML51SD1AE/ ML54SD1AE / ML56SD1AE

##### ML51SD1AE

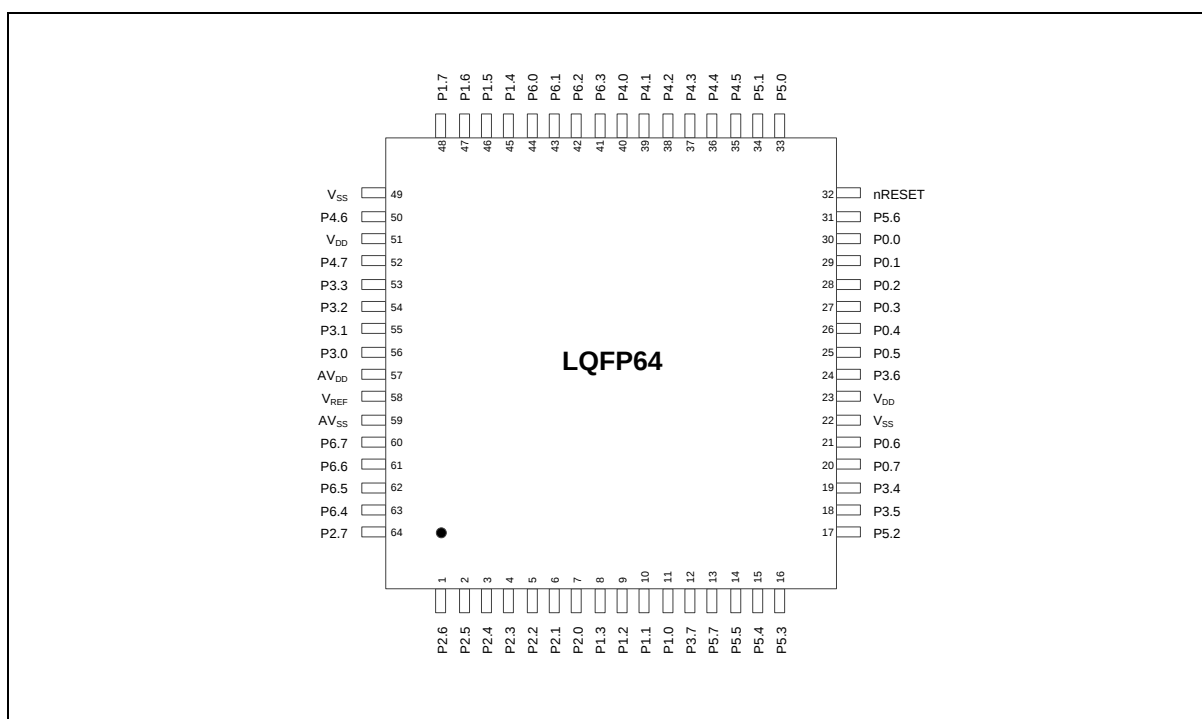


Figure 4.1-1 ML51SD1AE Pin Assignment

ML54SD1AE / ML56SD1AE

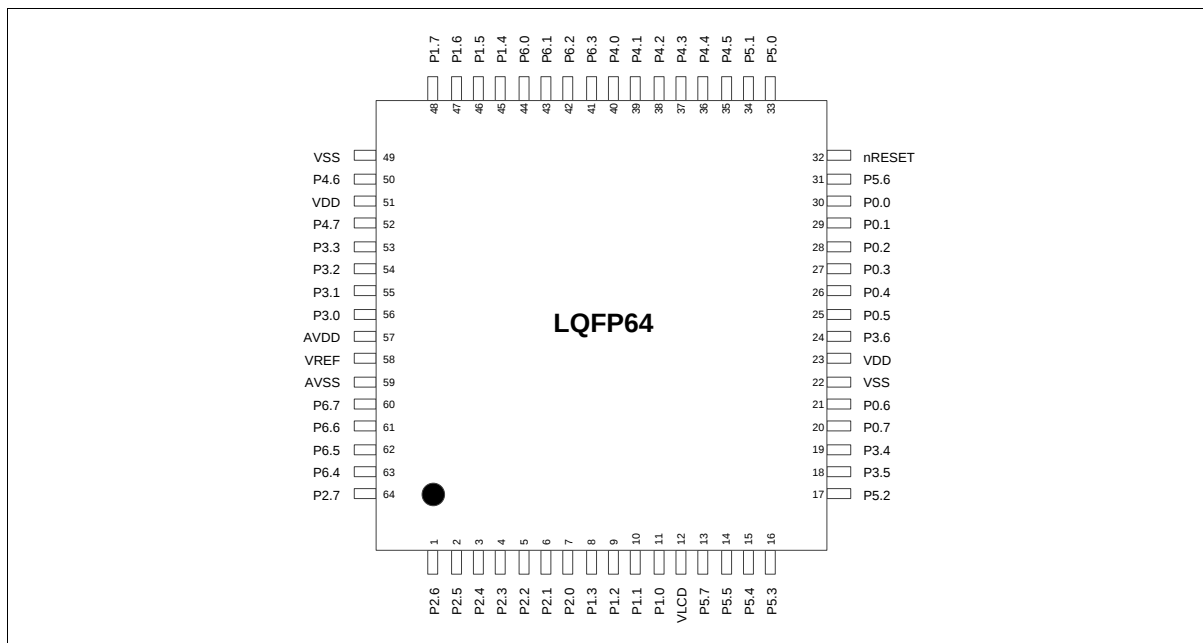


Figure 4.1-2 ML54SD1AE / ML56SD1AE Pin Assignment

4.1.1.2 LQFP48 Package

Corresponding Part Number: ML51LD1AE/ ML54LD1AE / ML56LD1AE

ML51LD1AE

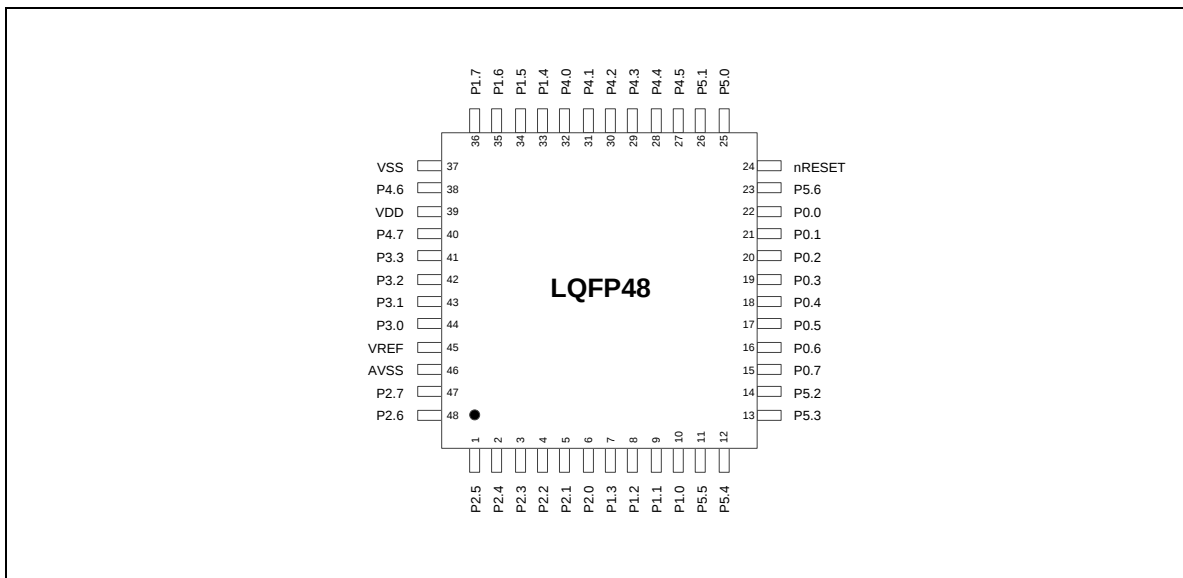


Figure 4.1-3 ML51LD1AE Pin Assignment

ML54LD1AE / ML56LD1AE

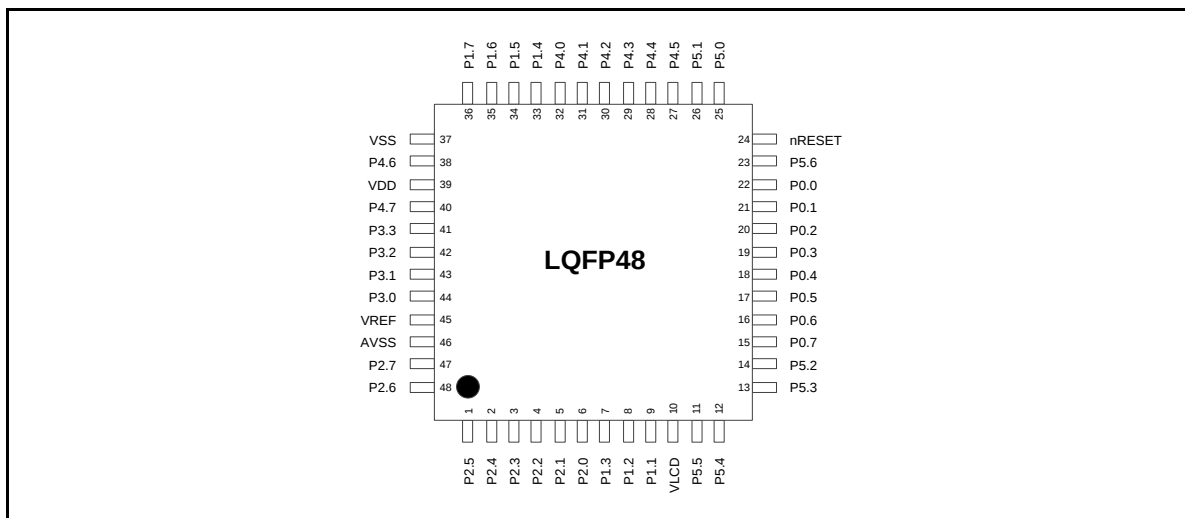


Figure 4.1-4 ML54LD1AE / ML56LD1AE Pin Assignment

4.1.1.3 LQFP44 Package

Corresponding Part Number: ML54MD1AE / ML56MD1AE

ML54MD1AE / ML56MD1AE

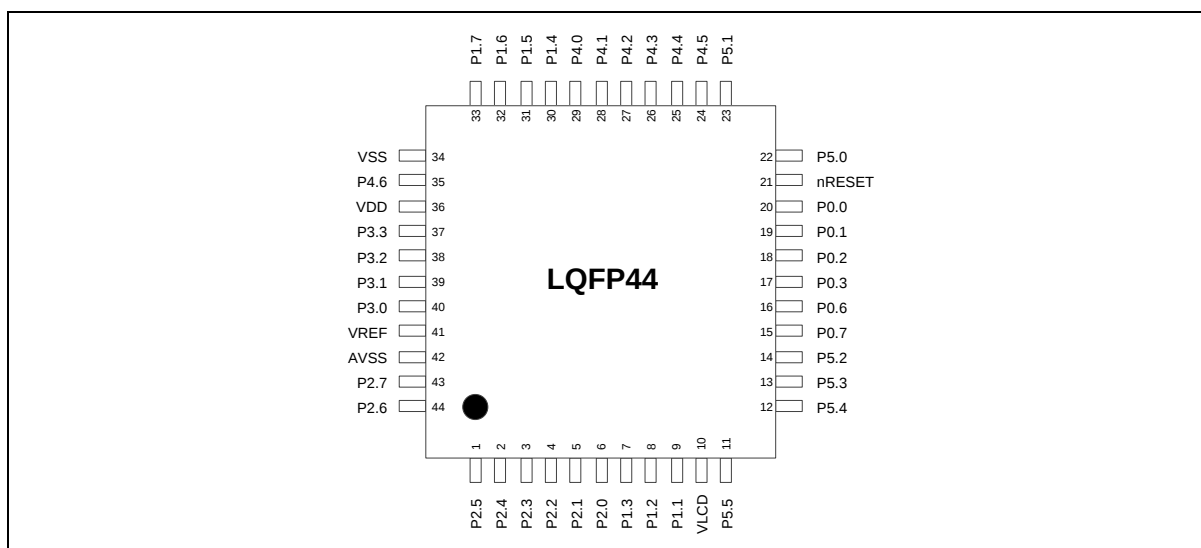


Figure 4.1-5 ML54MD1AE / ML56MD1AE Pin Assignment

#### 4.1.1.4 QFN33 Package

Corresponding Part Number: ML51TD1AE / ML51TC0AE / ML51TB9AE

#### ML51TD1AE / ML51TC0AE / ML51TB9AE

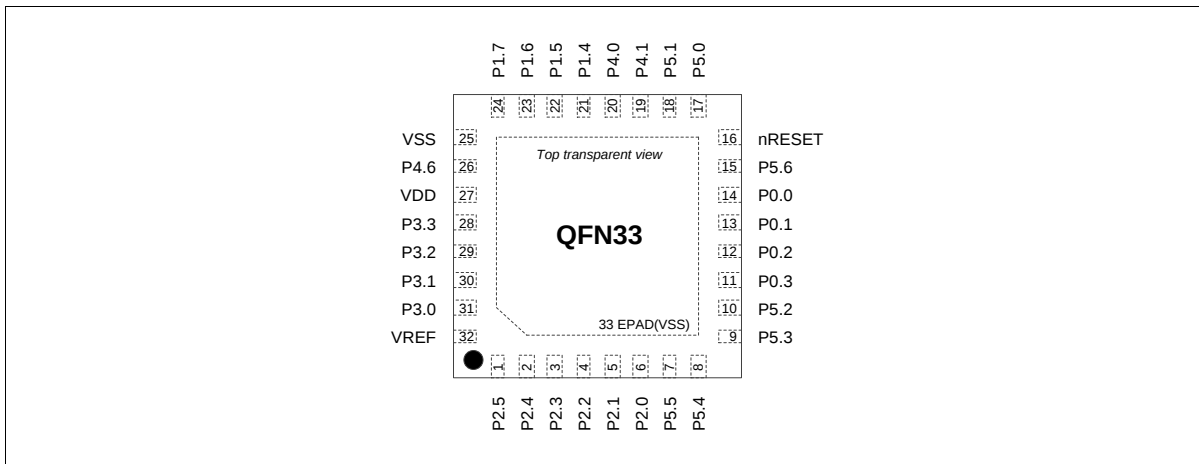


Figure 4.1-6 ML51TD1AE / ML51TC0AE / ML51TB9AE Pin Assignment

#### 4.1.1.5 LQFP32 Package

Corresponding Part Number: ML51PC0AE / ML51PB9AE

##### ML51PC0AE / ML51PB9AE

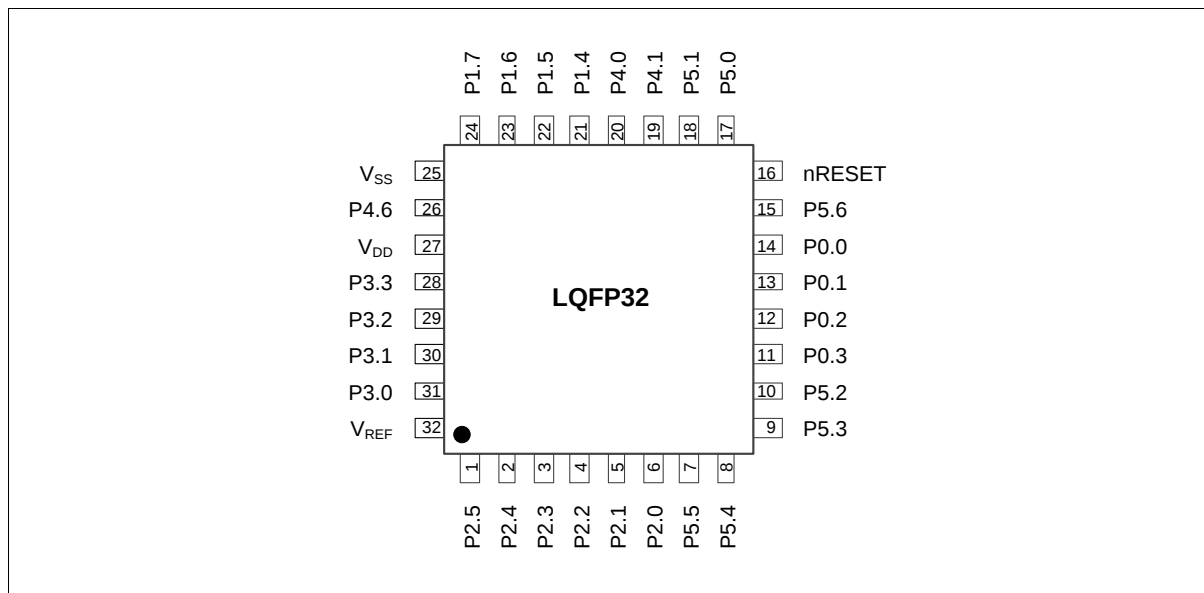


Figure 4.1-7 ML51PC0AE / ML51PB9AE Pin Assignment

#### 4.1.1.6 TSSOP28 Package

Corresponding Part Number: ML51EC0AE / ML51EB9AE

##### ML51EC0AE / ML51EB9AE

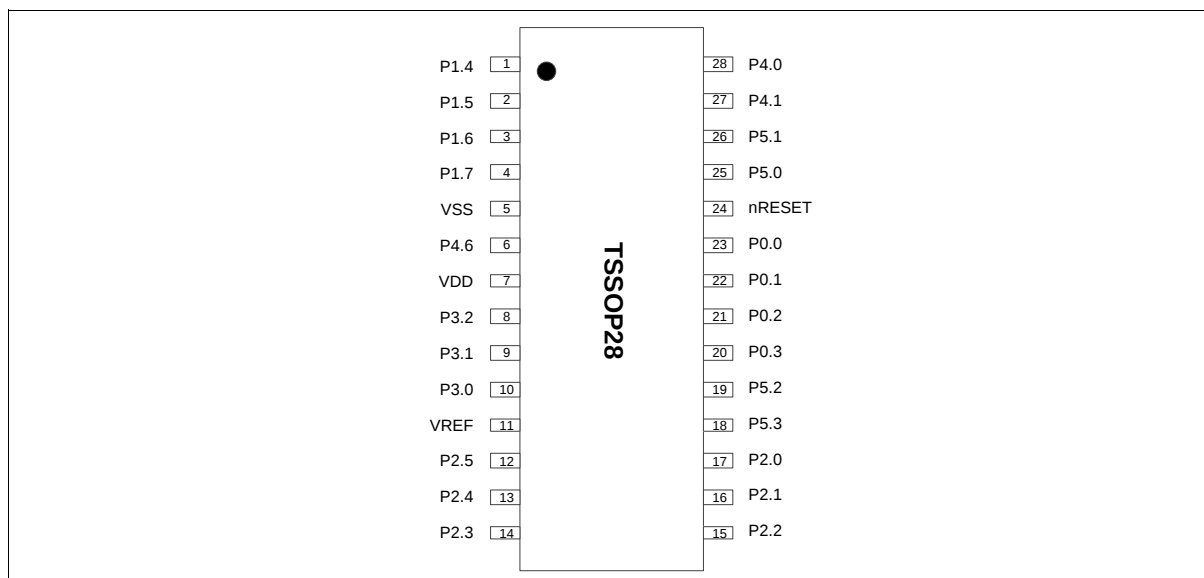


Figure 4.1-8 ML51EC0AE / ML51EB9AE Pin Assignment

#### 4.1.1.7 SOP28 Package

Corresponding Part Number: ML51UC0AE / ML51UB9AE

#### ML51UC0AE / ML51UB9AE

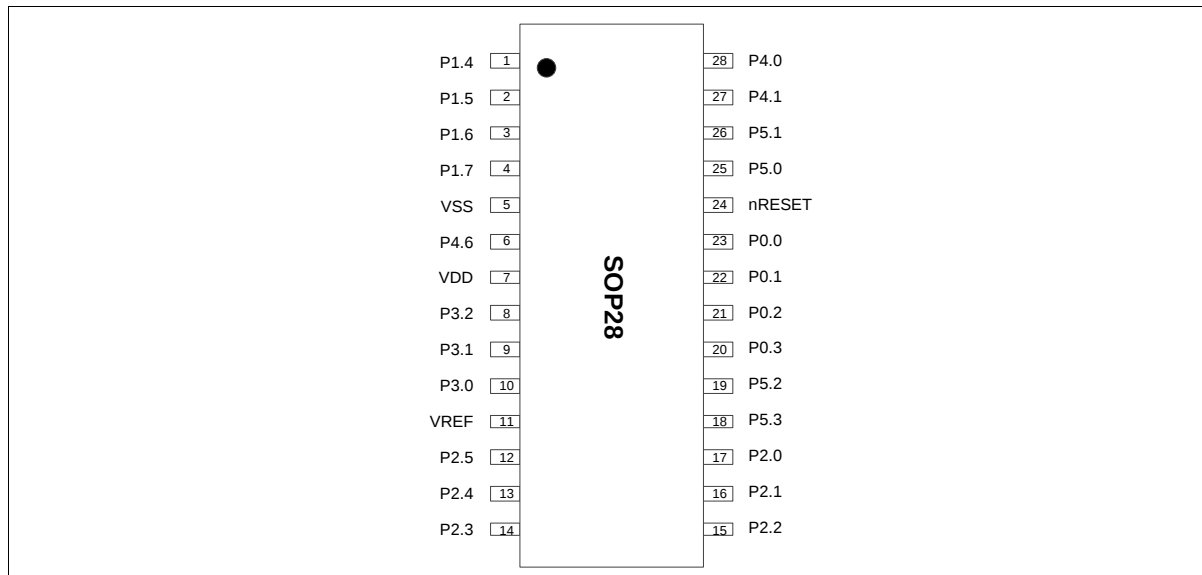


Figure 4.1-9 ML51UC0AE / ML51UB9AE Pin Assignment

#### 4.1.1.8 TSSOP20 Package

Corresponding Part Number: ML51FB9AE

#### ML51FB9AE

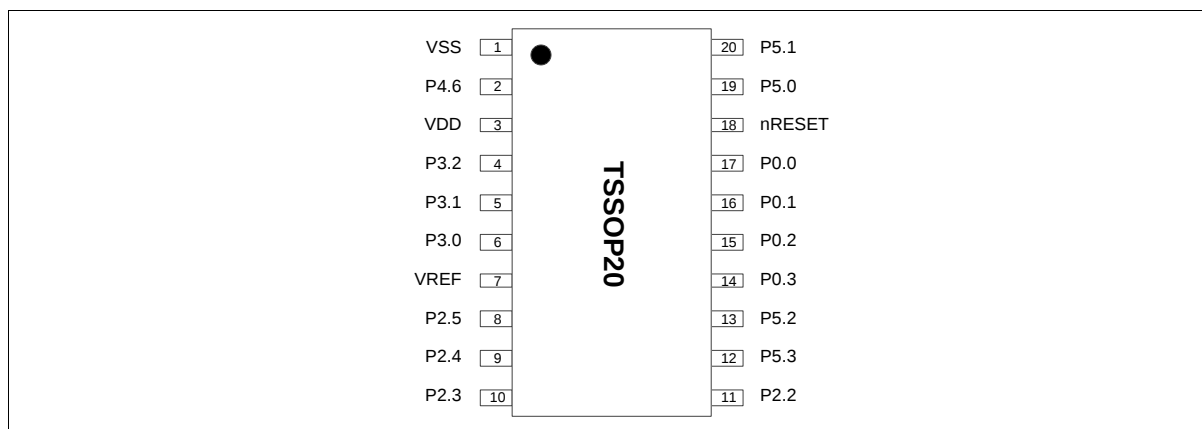


Figure 4.1-10 ML51FB9AE Pin Assignment

#### 4.1.1.9 SOP20 Package

Corresponding Part Number: ML51OB9AE

##### ML51OB9AE

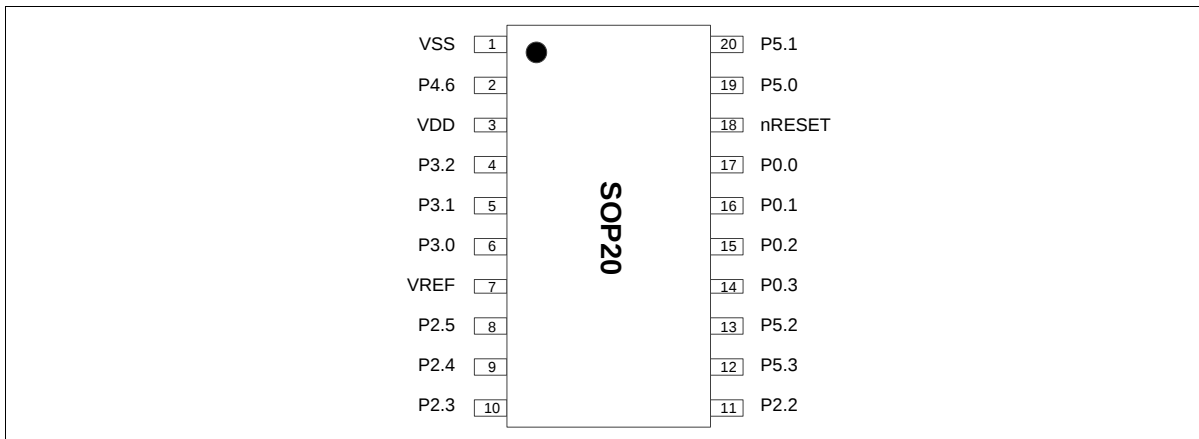


Figure 4.1-11 ML51OB9AE Pin Assignment

#### 4.1.1.10 QFN20 Package

Corresponding Part Number: ML51XB9AE

##### ML51XB9AE

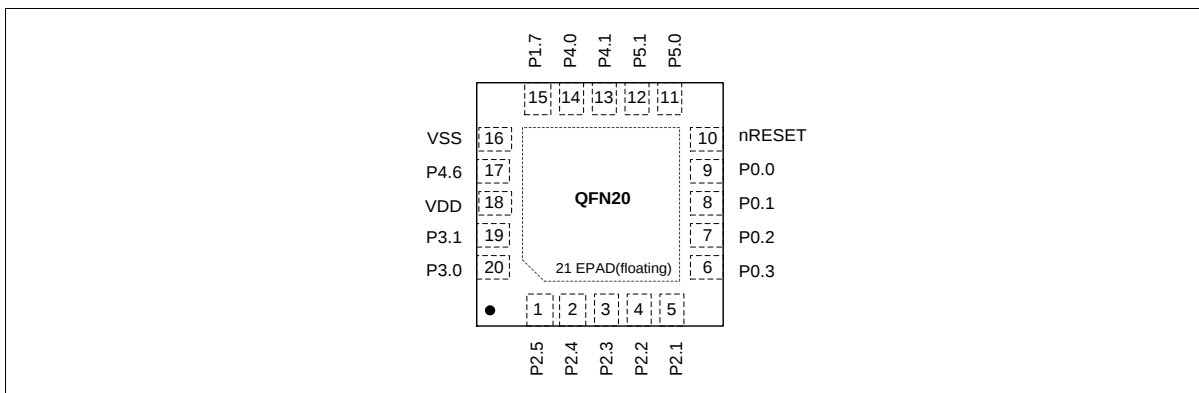


Figure 4.1-12 ML51XB9AE Pin Assignment

#### 4.1.1.11 TSSOP14 Package

Corresponding Part Number: ML51DB9AE

#### ML51DB9AE

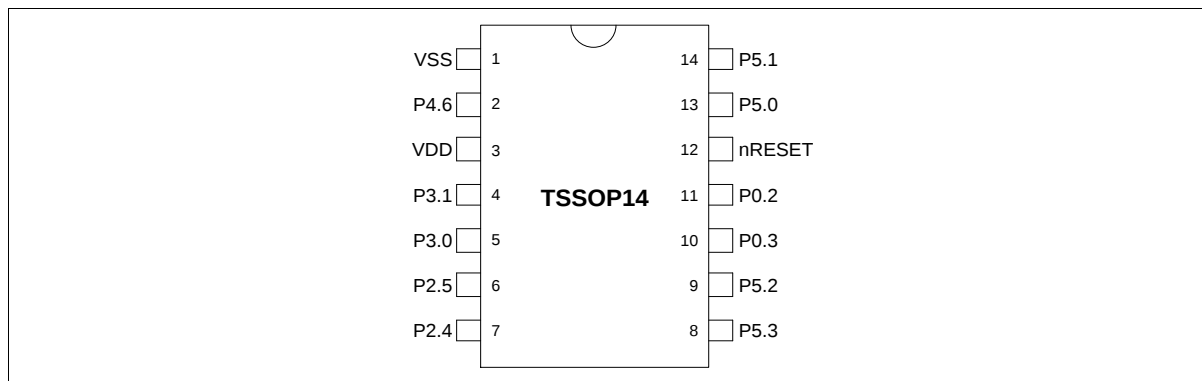


Figure 4.1-13 ML51DB9AE Pin Assignment

#### 4.1.1.12 MSOP10 Package

Corresponding Part Number: ML51BB9AE

#### ML51BB9AE

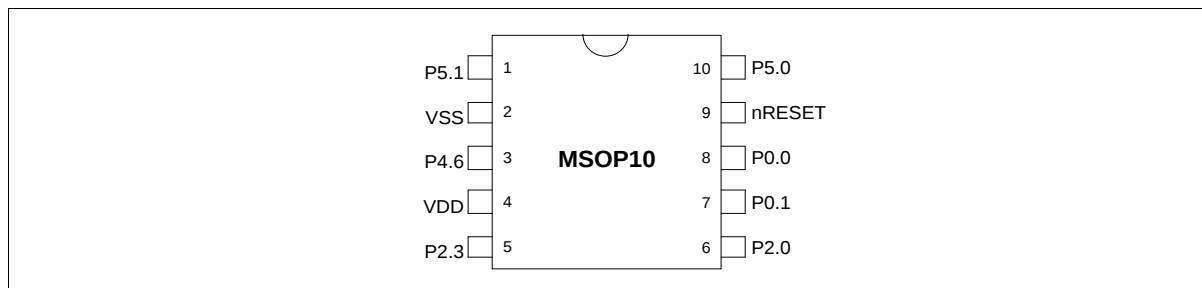


Figure 4.1-14 ML51BB9AE Pin Assignment

## 4.1.2 ML51/ML54/ML56 Series Multi Function Pin Diagram

### 4.1.2.1 LQFP64 Package

Corresponding Part Number: ML51SD1AE / ML54SD1AE / ML56SD1AE

#### ML51SD1AE Pin Function

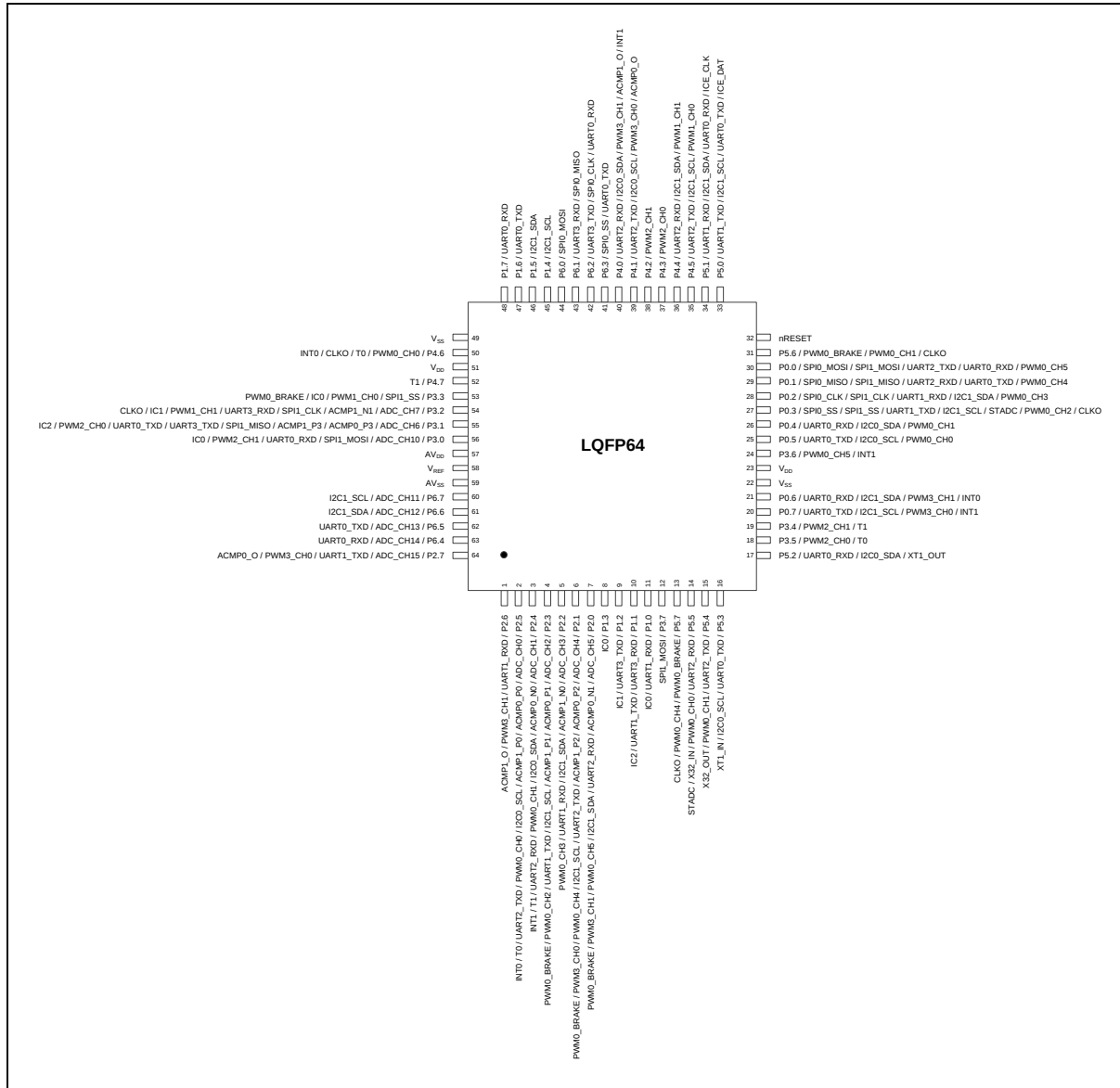


Figure 4.1-15 ML51SD1AE Multi-Function Pin assignment

| Pin | ML51SD1AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 1   | P2.6 / UART1_RXD / PWM3_CH1 / ACMP1_O                                               |
| 2   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 3   | P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 4   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |

| Pin | ML51SD1AE Pin Function                                                                         |
|-----|------------------------------------------------------------------------------------------------|
| 5   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3                                    |
| 6   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE |
| 7   | P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE            |
| 8   | P1.3 / IC0                                                                                     |
| 9   | P1.2 / UART3_TXD / IC1                                                                         |
| 10  | P1.1 / UART3_RXD / UART1_TXD / IC2                                                             |
| 11  | P1.0 / UART1_RXD / IC0                                                                         |
| 12  | P3.7 / SPI1_MOSI                                                                               |
| 13  | P5.7 / PWM0_BRAKE / PWM0_CH4 / CLKO                                                            |
| 14  | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                                                   |
| 15  | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                                                          |
| 16  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                           |
| 17  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                                          |
| 18  | P3.5 / PWM2_CH0 / T0                                                                           |
| 19  | P3.4 / PWM2_CH1 / T1                                                                           |
| 20  | P0.7 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1                                                  |
| 21  | P0.6 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0                                                  |
| 22  | V <sub>SS</sub>                                                                                |
| 23  | V <sub>DD</sub>                                                                                |
| 24  | P3.6 / PWM0_CH5 / INT1                                                                         |
| 25  | P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0                                                         |
| 26  | P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1                                                         |
| 27  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO                      |
| 28  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                                   |
| 29  | P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4                                |
| 30  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5                                |
| 31  | P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO                                                            |
| 32  | nRESET                                                                                         |
| 33  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                                              |
| 34  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                                              |
| 35  | P4.5 / UART2_TXD / I2C1_SCL / PWM1_CH0                                                         |
| 36  | P4.4 / UART2_RXD / I2C1_SDA / PWM1_CH1                                                         |

| Pin | ML51SD1AE Pin Function                                                                    |
|-----|-------------------------------------------------------------------------------------------|
| 37  | P4.3 / PWM2_CH0                                                                           |
| 38  | P4.2 / PWM2_CH1                                                                           |
| 39  | P4.1 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O                                          |
| 40  | P4.0 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1                                   |
| 41  | P6.3 / SPI0_SS / UART0_TXD                                                                |
| 42  | P6.2 / UART3_TXD / SPI0_CLK / UART0_RXD                                                   |
| 43  | P6.1 / UART3_RXD / SPI0_MISO                                                              |
| 44  | P6.0 / SPI0_MOSI                                                                          |
| 45  | P1.4 / I2C1_SCL                                                                           |
| 46  | P1.5 / I2C1_SDA                                                                           |
| 47  | P1.6 / UART0_TXD                                                                          |
| 48  | P1.7 / UART0_RXD                                                                          |
| 49  | V <sub>SS</sub>                                                                           |
| 50  | P4.6 / PWM0_CH0 / T0 / CLKO / INT0                                                        |
| 51  | V <sub>DD</sub>                                                                           |
| 52  | P4.7 / T1                                                                                 |
| 53  | P3.3 / SPI1_SS / PWM1_CH0 / IC0 / PWM0_BRAKE                                              |
| 54  | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO                  |
| 55  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2 |
| 56  | P3.0 / ADC_CH10 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0                                  |
| 57  | AV <sub>DD</sub>                                                                          |
| 58  | V <sub>REF</sub>                                                                          |
| 59  | AV <sub>SS</sub>                                                                          |
| 60  | P6.7 / ADC_CH11 / I2C1_SCL                                                                |
| 61  | P6.6 / ADC_CH12 / I2C1_SDA                                                                |
| 62  | P6.5 / ADC_CH13 / UART0_TXD                                                               |
| 63  | P6.4 / ADC_CH14 / UART0_RXD                                                               |
| 64  | P2.7 / ADC_CH15 / UART1_TXD / PWM3_CH0 / ACMP0_O                                          |

ML54SD1AE Pin Function

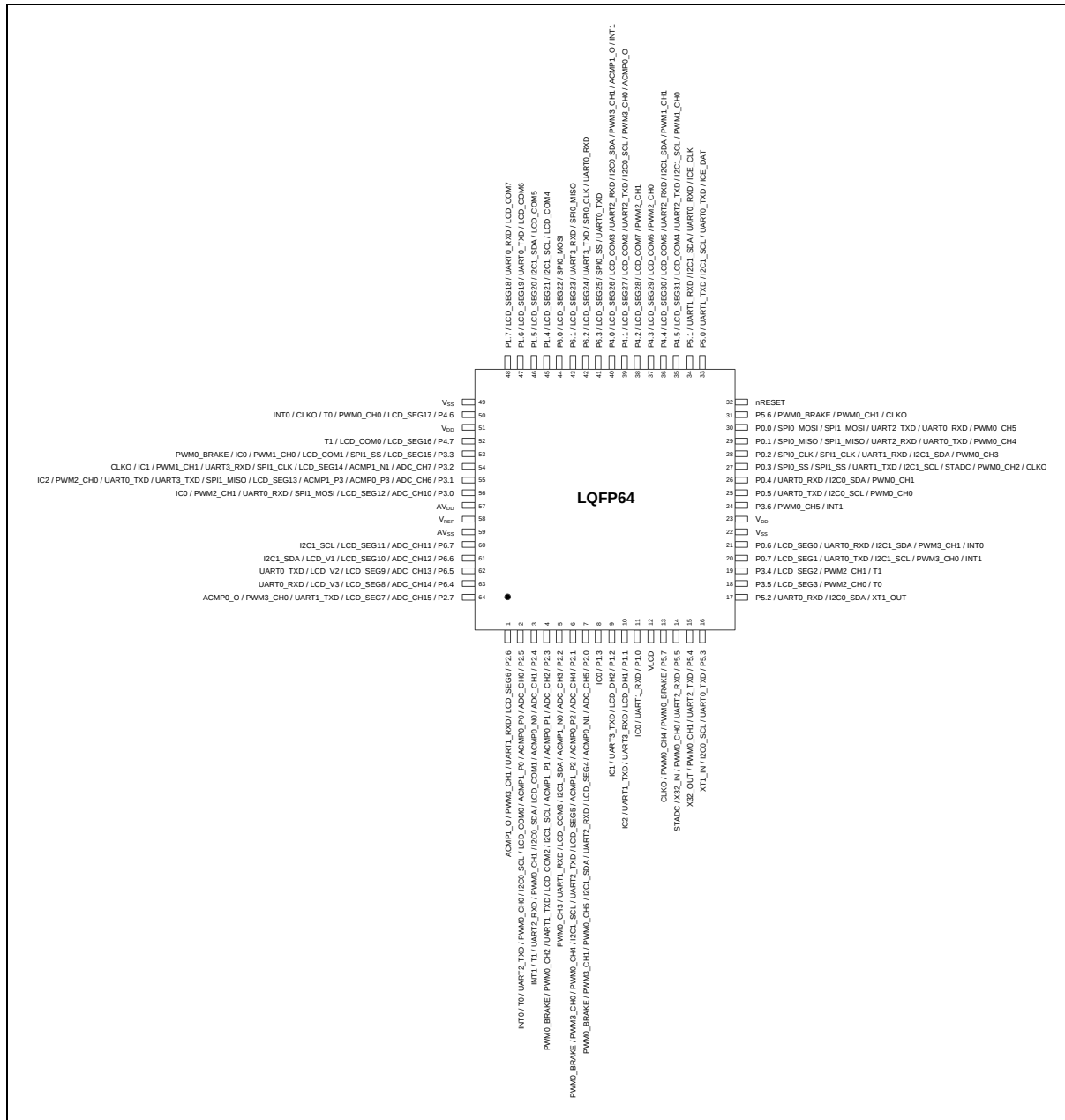


Figure 4.1-16 ML54SD1AE Multi-Function Pin assignment

| Pin | ML54SD1AE Pin Function                                                                         |
|-----|------------------------------------------------------------------------------------------------|
| 1   | P2.6 / LCD_SEG6 / UART1_RXD / PWM3_CH1 / ACMP1_O                                               |
| 2   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / LCD_COM0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INTO  |
| 3   | P2.4 / ADC_CH1 / ACMP0_N0 / LCD_COM1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 4   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / LCD_COM2 / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |

| Pin | ML54SD1AE Pin Function                                                                                    |
|-----|-----------------------------------------------------------------------------------------------------------|
| 5   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / LCD_COM3 / UART1_RXD / PWM0_CH3                                    |
| 6   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / LCD_SEG5 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE |
| 7   | P2.0 / ADC_CH5 / ACMP0_N1 / LCD_SEG4 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE            |
| 8   | P1.3 / IC0                                                                                                |
| 9   | P1.2 / LCD_DH2 / UART3_TXD / IC1                                                                          |
| 10  | P1.1 / LCD_DH1 / UART3_RXD / UART1_TXD / IC2                                                              |
| 11  | P1.0 / UART1_RXD / IC0                                                                                    |
| 12  | VLCD                                                                                                      |
| 13  | P5.7 / PWM0_BRAKE / PWM0_CH4 / CLKO                                                                       |
| 14  | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                                                              |
| 15  | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                                                                     |
| 16  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                                      |
| 17  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                                                     |
| 18  | P3.5 / LCD_SEG3 / PWM2_CH0 / T0                                                                           |
| 19  | P3.4 / LCD_SEG2 / PWM2_CH1 / T1                                                                           |
| 20  | P0.7 / LCD_SEG1 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1                                                  |
| 21  | P0.6 / LCD_SEG0 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0                                                  |
| 22  | V <sub>SS</sub>                                                                                           |
| 23  | V <sub>DD</sub>                                                                                           |
| 24  | P3.6 / PWM0_CH5 / INT1                                                                                    |
| 25  | P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0                                                                    |
| 26  | P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1                                                                    |
| 27  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO                                 |
| 28  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                                              |
| 29  | P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4                                           |
| 30  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5                                           |
| 31  | P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO                                                                       |
| 32  | nRESET                                                                                                    |
| 33  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                                                         |
| 34  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                                                         |
| 35  | P4.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL / PWM1_CH0                                             |

| Pin | ML54SD1AE Pin Function                                                                                |
|-----|-------------------------------------------------------------------------------------------------------|
| 36  | P4.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD / I2C1_SDA / PWM1_CH1                                         |
| 37  | P4.3 / LCD_SEG29 / LCD_COM6 / PWM2_CH0                                                                |
| 38  | P4.2 / LCD_SEG28 / LCD_COM7 / PWM2_CH1                                                                |
| 39  | P4.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O                               |
| 40  | P4.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1                        |
| 41  | P6.3 / LCD_SEG25 / SPI0_SS / UART0_TXD                                                                |
| 42  | P6.2 / LCD_SEG24 / UART3_TXD / SPI0_CLK / UART0_RXD                                                   |
| 43  | P6.1 / LCD_SEG23 / UART3_RXD / SPI0_MISO                                                              |
| 44  | P6.0 / LCD_SEG22 / SPI0_MOSI                                                                          |
| 45  | P1.4 / LCD_SEG21 / I2C1_SCL / LCD_COM4                                                                |
| 46  | P1.5 / LCD_SEG20 / I2C1_SDA / LCD_COM5                                                                |
| 47  | P1.6 / LCD_SEG19 / UART0_TXD / LCD_COM6                                                               |
| 48  | P1.7 / LCD_SEG18 / UART0_RXD / LCD_COM7                                                               |
| 49  | V <sub>SS</sub>                                                                                       |
| 50  | P4.6 / LCD_SEG17 / PWM0_CH0 / T0 / CLKO / INT0                                                        |
| 51  | V <sub>DD</sub>                                                                                       |
| 52  | P4.7 / LCD_SEG16 / LCD_COM0 / T1                                                                      |
| 53  | P3.3 / LCD_SEG15 / SPI1_SS / LCD_COM1 / PWM1_CH0 / IC0 / PWM0_BRAKE                                   |
| 54  | P3.2 / ADC_CH7 / ACMP1_N1 / LCD_SEG14 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO                  |
| 55  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / LCD_SEG13 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2 |
| 56  | P3.0 / ADC_CH10 / LCD_SEG12 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0                                  |
| 57  | AV <sub>DD</sub>                                                                                      |
| 58  | V <sub>REF</sub>                                                                                      |
| 59  | AV <sub>SS</sub>                                                                                      |
| 60  | P6.7 / ADC_CH11 / LCD_SEG11 / I2C1_SCL                                                                |
| 61  | P6.6 / ADC_CH12 / LCD_SEG10 / LCD_V1 / I2C1_SDA                                                       |
| 62  | P6.5 / ADC_CH13 / LCD_SEG9 / LCD_V2 / UART0_TXD                                                       |
| 63  | P6.4 / ADC_CH14 / LCD_SEG8 / LCD_V3 / UART0_RXD                                                       |
| 64  | P2.7 / ADC_CH15 / LCD_SEG7 / UART1_TXD / PWM3_CH0 / ACMP0_O                                           |

ML56SD1AE Pin Function

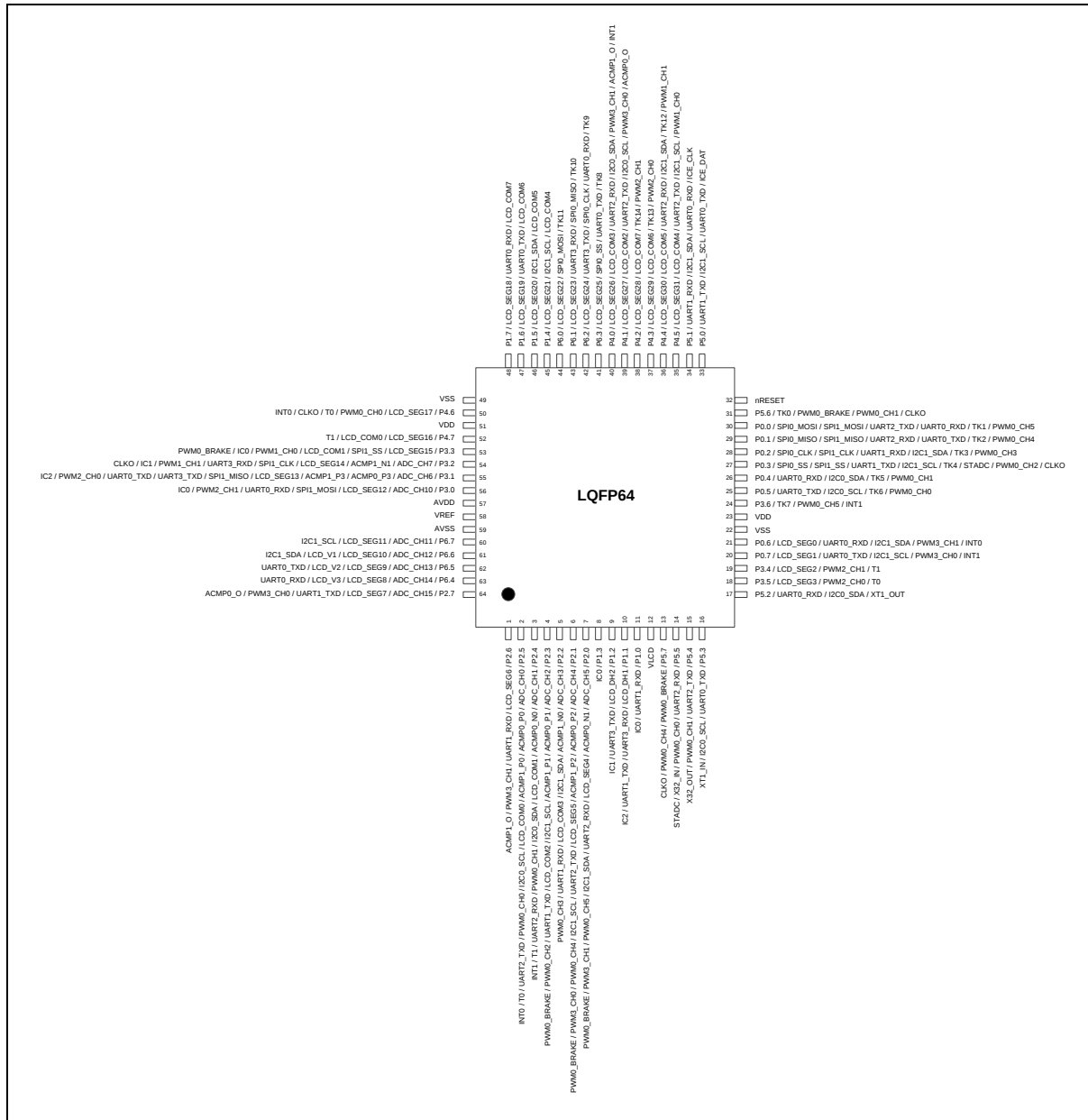


Figure 4.1-17 ML56SD1AE Multi-Function Pin assignment

| Pin | ML56SD1AE Pin Function                                                                  |
|-----|-----------------------------------------------------------------------------------------|
| 1   | P2.6/LCD_SEG6/UART1_RXD/PWM3_CH1/ACMP1_O                                                |
| 2   | P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0             |
| 3   | P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1                      |
| 4   | P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE          |
| 5   | P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3                              |
| 6   | P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE |

| Pin | ML56SD1AE Pin Function                                                         |
|-----|--------------------------------------------------------------------------------|
| 7   | P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE |
| 8   | P1.3/IC0                                                                       |
| 9   | P1.2/LCD_DH2/UART3_TXD/IC1                                                     |
| 10  | P1.1/LCD_DH1/UART3_RXD/UART1_TXD/IC2                                           |
| 11  | P1.0/UART1_RXD/IC0                                                             |
| 12  | VLCD                                                                           |
| 13  | P5.7/PWM0_BRAKE/PWM0_CH4/CLKO                                                  |
| 14  | P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC                                           |
| 15  | P5.4/UART2_TXD/PWM0_CH1/X32_OUT                                                |
| 16  | P5.3/UART0_TXD/I2C0_SCL/XT1_IN                                                 |
| 17  | P5.2/UART0_RXD/I2C0_SDA/XT1_OUT                                                |
| 18  | P3.5/LCD_SEG3/PWM2_CH0/T0                                                      |
| 19  | P3.4/LCD_SEG2/PWM2_CH1/T1                                                      |
| 20  | P0.7/LCD_SEG1/UART0_TXD/I2C1_SCL/PWM3_CH0/INT1                                 |
| 21  | P0.6/LCD_SEG0/UART0_RXD/I2C1_SDA/PWM3_CH1/INT0                                 |
| 22  | VSS                                                                            |
| 23  | VDD                                                                            |
| 24  | P3.6/TK7/PWM0_CH5/INT1                                                         |
| 25  | P0.5/UART0_TXD/I2C0_SCL/TK6/PWM0_CH0                                           |
| 26  | P0.4/UART0_RXD/I2C0_SDA/TK5/PWM0_CH1                                           |
| 27  | P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO                |
| 28  | P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3                         |
| 29  | P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4                      |
| 30  | P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5                      |
| 31  | P5.6/TK0/PWM0_BRAKE/PWM0_CH1/CLKO                                              |
| 32  | nRESET                                                                         |
| 33  | P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT                                      |
| 34  | P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK                                      |
| 35  | P4.5/LCD_SEG31/LCD_COM4/UART2_TXD/I2C1_SCL/PWM1_CH0                            |
| 36  | P4.4/LCD_SEG30/LCD_COM5/UART2_RXD/I2C1_SDA/TK12/PWM1_CH1                       |
| 37  | P4.3/LCD_SEG29/LCD_COM6/TK13/PWM2_CH0                                          |
| 38  | P4.2/LCD_SEG28/LCD_COM7/TK14/PWM2_CH1                                          |
| 39  | P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O                    |
| 40  | P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1               |

| Pin | ML56SD1AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 41  | P6.3/LCD_SEG25/SPI0_SS/UART0_TXD/TK8                                                |
| 42  | P6.2/LCD_SEG24/UART3_TXD/SPI0_CLK/UART0_RXD/TK9                                     |
| 43  | P6.1/LCD_SEG23/UART3_RXD/SPI0_MISO/TK10                                             |
| 44  | P6.0/LCD_SEG22/SPI0_MOSI/TK11                                                       |
| 45  | P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4                                                    |
| 46  | P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5                                                    |
| 47  | P1.6/LCD_SEG19/UART0_TXD/LCD_COM6                                                   |
| 48  | P1.7/LCD_SEG18/UART0_RXD/LCD_COM7                                                   |
| 49  | VSS                                                                                 |
| 50  | P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0                                                |
| 51  | VDD                                                                                 |
| 52  | P4.7/LCD_SEG16/LCD_COM0/T1                                                          |
| 53  | P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE                             |
| 54  | P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO                |
| 55  | P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2 |
| 56  | P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0                            |
| 57  | AV <sub>DD</sub>                                                                    |
| 58  | V <sub>REF</sub>                                                                    |
| 59  | AVSS                                                                                |
| 60  | P6.7/ADC_CH11/LCD_SEG11/I2C1_SCL                                                    |
| 61  | P6.6/ADC_CH12/LCD_SEG10/LCD_V1/I2C1_SDA                                             |
| 62  | P6.5/ADC_CH13/LCD_SEG9/LCD_V2/UART0_TXD                                             |
| 63  | P6.4/ADC_CH14/LCD_SEG8/LCD_V3/UART0_RXD                                             |
| 64  | P2.7/ADC_CH15/LCD_SEG7/UART1_TXD/PWM3_CH0/ACMP0_O                                   |

#### 4.1.2.2 LQFP48 Package

Corresponding Part Number: ML51LD1AE

#### ML51LD1AE Pin Function

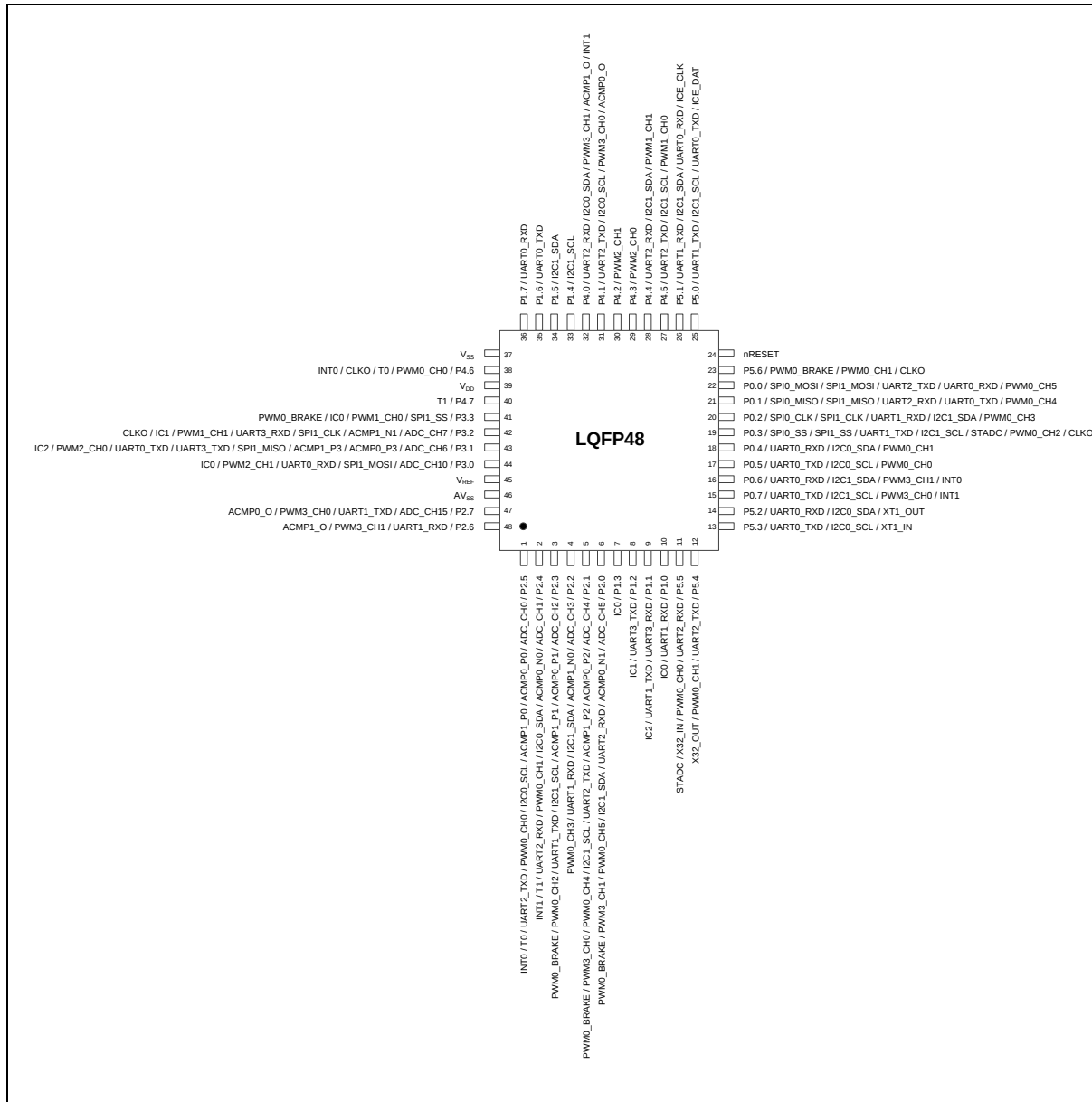


Figure 4.1-18 ML51LD1AE Multi-Function Pin assignment

| Pin | ML51LD1AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 1   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 2   | P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 3   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 4   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3                         |

| Pin | ML51LD1AE Pin Function                                                                         |
|-----|------------------------------------------------------------------------------------------------|
| 5   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE |
| 6   | P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE            |
| 7   | P1.3 / IC0                                                                                     |
| 8   | P1.2 / UART3_TXD / IC1                                                                         |
| 9   | P1.1 / UART3_RXD / UART1_TXD / IC2                                                             |
| 10  | P1.0 / UART1_RXD / IC0                                                                         |
| 11  | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                                                   |
| 12  | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                                                          |
| 13  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                           |
| 14  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                                          |
| 15  | P0.7 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1                                                  |
| 16  | P0.6 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0                                                  |
| 17  | P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0                                                         |
| 18  | P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1                                                         |
| 19  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLK0                      |
| 20  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                                   |
| 21  | P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4                                |
| 22  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5                                |
| 23  | P5.6 / PWM0_BRAKE / PWM0_CH1 / CLK0                                                            |
| 24  | nRESET                                                                                         |
| 25  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                                              |
| 26  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                                              |
| 27  | P4.5 / UART2_TXD / I2C1_SCL / PWM1_CH0                                                         |
| 28  | P4.4 / UART2_RXD / I2C1_SDA / PWM1_CH1                                                         |
| 29  | P4.3 / PWM2_CH0                                                                                |
| 30  | P4.2 / PWM2_CH1                                                                                |
| 31  | P4.1 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O                                               |
| 32  | P4.0 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1                                        |
| 33  | P1.4 / I2C1_SCL                                                                                |
| 34  | P1.5 / I2C1_SDA                                                                                |
| 35  | P1.6 / UART0_TXD                                                                               |
| 36  | P1.7 / UART0_RXD                                                                               |

| Pin | ML51LD1AE Pin Function                                                                    |
|-----|-------------------------------------------------------------------------------------------|
| 37  | VSS                                                                                       |
| 38  | P4.6 / PWM0_CH0 / T0 / CLKO / INT0                                                        |
| 39  | V <sub>DD</sub>                                                                           |
| 40  | P4.7 / T1                                                                                 |
| 41  | P3.3 / SPI1_SS / PWM1_CH0 / IC0 / PWM0_BRAKE                                              |
| 42  | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO                  |
| 43  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2 |
| 44  | P3.0 / ADC_CH10 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0                                  |
| 45  | V <sub>REF</sub>                                                                          |
| 46  | AV <sub>SS</sub>                                                                          |
| 47  | P2.7 / ADC_CH15 / UART1_TXD / PWM3_CH0 / ACMP0_O                                          |
| 48  | P2.6 / UART1_RXD / PWM3_CH1 / ACMP1_O                                                     |

# ML54LD1AE Pin Function

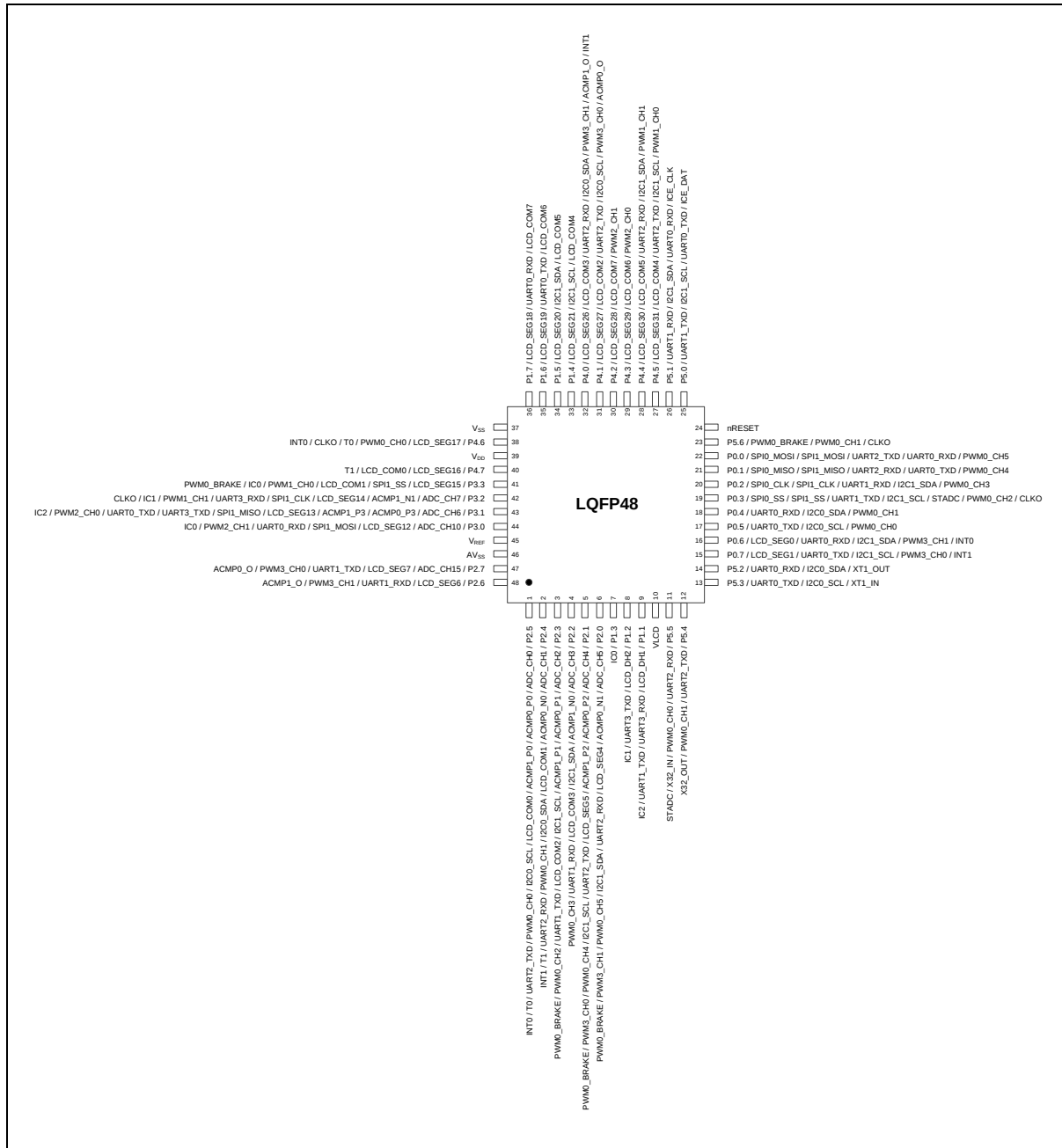


Figure 4.1-19 ML54LD1AE Multi-Function Pin assignment

| Pin | ML54LD1AE Pin Function                                                                         |
|-----|------------------------------------------------------------------------------------------------|
| 1   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / LCD_COM0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 2   | P2.4 / ADC_CH1 / ACMP0_N0 / LCD_COM1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 3   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / LCD_COM2 / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |

| Pin | ML54LD1AE Pin Function                                                                                    |
|-----|-----------------------------------------------------------------------------------------------------------|
| 4   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / LCD_COM3 / UART1_RXD / PWM0_CH3                                    |
| 5   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / LCD_SEG5 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE |
| 6   | P2.0 / ADC_CH5 / ACMP0_N1 / LCD_SEG4 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE            |
| 7   | P1.3 / IC0                                                                                                |
| 8   | P1.2 / LCD_DH2 / UART3_TXD / IC1                                                                          |
| 9   | P1.1 / LCD_DH1 / UART3_RXD / UART1_TXD / IC2                                                              |
| 10  | VLCD                                                                                                      |
| 11  | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                                                              |
| 12  | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                                                                     |
| 13  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                                      |
| 14  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                                                     |
| 15  | P0.7 / LCD_SEG1 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1                                                  |
| 16  | P0.6 / LCD_SEG0 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0                                                  |
| 17  | P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0                                                                    |
| 18  | P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1                                                                    |
| 19  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO                                 |
| 20  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                                              |
| 21  | P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4                                           |
| 22  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5                                           |
| 23  | P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO                                                                       |
| 24  | nRESET                                                                                                    |
| 25  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                                                         |
| 26  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                                                         |
| 27  | P4.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL / PWM1_CH0                                             |
| 28  | P4.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD / I2C1_SDA / PWM1_CH1                                             |
| 29  | P4.3 / LCD_SEG29 / LCD_COM6 / PWM2_CH0                                                                    |
| 30  | P4.2 / LCD_SEG28 / LCD_COM7 / PWM2_CH1                                                                    |
| 31  | P4.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O                                   |
| 32  | P4.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1                            |
| 33  | P1.4 / LCD_SEG21 / I2C1_SCL / LCD_COM4                                                                    |
| 34  | P1.5 / LCD_SEG20 / I2C1_SDA / LCD_COM5                                                                    |

| Pin | ML54LD1AE Pin Function                                                                                |
|-----|-------------------------------------------------------------------------------------------------------|
| 35  | P1.6 / LCD_SEG19 / UART0_TXD / LCD_COM6                                                               |
| 36  | P1.7 / LCD_SEG18 / UART0_RXD / LCD_COM7                                                               |
| 37  | VSS                                                                                                   |
| 38  | P4.6 / LCD_SEG17 / PWM0_CH0 / T0 / CLKO / INT0                                                        |
| 39  | V <sub>DD</sub>                                                                                       |
| 40  | P4.7 / LCD_SEG16 / LCD_COM0 / T1                                                                      |
| 41  | P3.3 / LCD_SEG15 / SPI1_SS / LCD_COM1 / PWM1_CH0 / IC0 / PWM0_BRAKE                                   |
| 42  | P3.2 / ADC_CH7 / ACMP1_N1 / LCD_SEG14 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO                  |
| 43  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / LCD_SEG13 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2 |
| 44  | P3.0 / ADC_CH10 / LCD_SEG12 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0                                  |
| 45  | V <sub>REF</sub>                                                                                      |
| 46  | AV <sub>SS</sub>                                                                                      |
| 47  | P2.7 / ADC_CH15 / LCD_SEG7 / UART1_TXD / PWM3_CH0 / ACMP0_O                                           |
| 48  | P2.6 / LCD_SEG6 / UART1_RXD / PWM3_CH1 / ACMP1_O                                                      |

# ML56LD1AE Pin Function

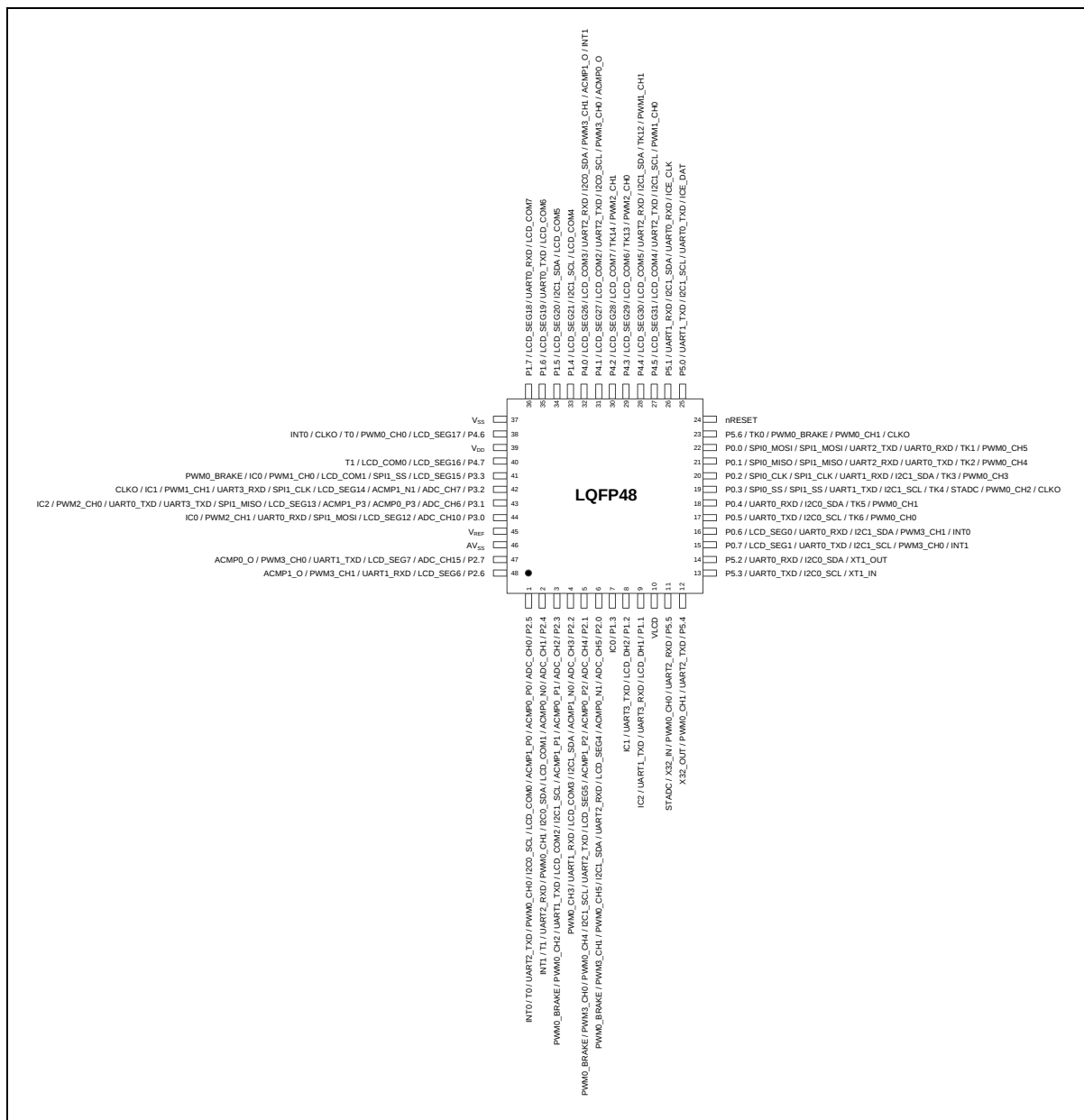


Figure 4.1-20 ML56LD1AE Multi-Function Pin assignment

| Pin | ML56LD1AE/ML56LC1AE Pin Function                                                        |
|-----|-----------------------------------------------------------------------------------------|
| 1   | P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0             |
| 2   | P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1                      |
| 3   | P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE          |
| 4   | P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3                              |
| 5   | P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE |
| 6   | P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE          |

| Pin | ML56LD1AE/ML56LC1AE Pin Function                                 |
|-----|------------------------------------------------------------------|
| 7   | P1.3/IC0                                                         |
| 8   | P1.2/LCD_DH2/UART3_TXD/IC1                                       |
| 9   | P1.1/LCD_DH1/UART3_RXD/UART1_TXD/IC2                             |
| 10  | VLCD                                                             |
| 11  | P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC                             |
| 12  | P5.4/UART2_TXD/PWM0_CH1/X32_OUT                                  |
| 13  | P5.3/UART0_TXD/I2C0_SCL/XT1_IN                                   |
| 14  | P5.2/UART0_RXD/I2C0_SDA/XT1_OUT                                  |
| 15  | P0.7/LCD_SEG1/UART0_TXD/I2C1_SCL/PWM3_CH0/INT1                   |
| 16  | P0.6/LCD_SEG0/UART0_RXD/I2C1_SDA/PWM3_CH1/INT0                   |
| 17  | P0.5/UART0_TXD/I2C0_SCL/TK6/PWM0_CH0                             |
| 18  | P0.4/UART0_RXD/I2C0_SDA/TK5/PWM0_CH1                             |
| 19  | P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO  |
| 20  | P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3           |
| 21  | P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4        |
| 22  | P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5        |
| 23  | P5.6/TK0/PWM0_BRAKE/PWM0_CH1/CLKO                                |
| 24  | nRESET                                                           |
| 25  | P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT                        |
| 26  | P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK                        |
| 27  | P4.5/LCD_SEG31/LCD_COM4/UART2_TXD/I2C1_SCL/PWM1_CH0              |
| 28  | P4.4/LCD_SEG30/LCD_COM5/UART2_RXD/I2C1_SDA/TK12/PWM1_CH1         |
| 29  | P4.3/LCD_SEG29/LCD_COM6/TK13/PWM2_CH0                            |
| 30  | P4.2/LCD_SEG28/LCD_COM7/TK14/PWM2_CH1                            |
| 31  | P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O      |
| 32  | P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1 |
| 33  | P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4                                 |
| 34  | P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5                                 |
| 35  | P1.6/LCD_SEG19/UART0_TXD/LCD_COM6                                |
| 36  | P1.7/LCD_SEG18/UART0_RXD/LCD_COM7                                |
| 37  | VSS                                                              |
| 38  | P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0                             |
| 39  | VDD                                                              |
| 40  | P4.7/LCD_SEG16/LCD_COM0/T1                                       |

| Pin | ML56LD1AE/ML56LC1AE Pin Function                                                    |
|-----|-------------------------------------------------------------------------------------|
| 41  | P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE                             |
| 42  | P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO                |
| 43  | P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2 |
| 44  | P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0                            |
| 45  | V <sub>REF</sub>                                                                    |
| 46  | AVSS                                                                                |
| 47  | P2.7/ADC_CH15/LCD_SEG7/UART1_TXD/PWM3_CH0/ACMP0_O                                   |
| 48  | P2.6/LCD_SEG6/UART1_RXD/PWM3_CH1/ACMP1_O                                            |

#### 4.1.2.3 LQFP44 Package

#### ML54MD1AE Pin Function

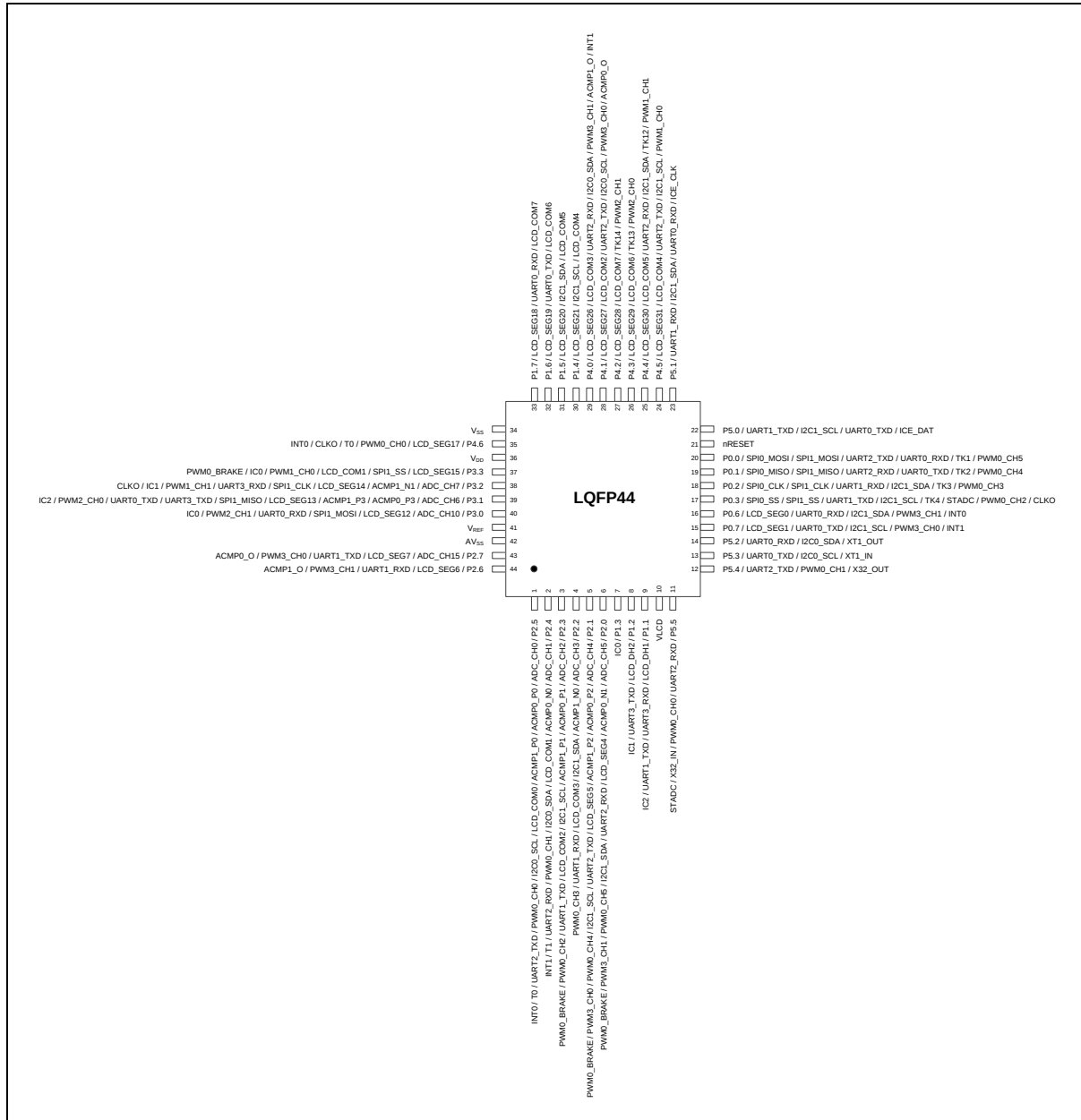


Figure 4.1-21 ML54MD1AE Multi-Function Pin assignment

| Pin | ML54MD1AE Pin Function                                                                         |
|-----|------------------------------------------------------------------------------------------------|
| 1   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / LCD_COM0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INTO  |
| 2   | P2.4 / ADC_CH1 / ACMP0_N0 / LCD_COM1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 3   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / LCD_COM2 / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |

| Pin | ML54MD1AE Pin Function                                                                                    |
|-----|-----------------------------------------------------------------------------------------------------------|
| 4   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / LCD_COM3 / UART1_RXD / PWM0_CH3                                    |
| 5   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / LCD_SEG5 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE |
| 6   | P2.0 / ADC_CH5 / ACMP0_N1 / LCD_SEG4 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE            |
| 7   | P1.3 / IC0                                                                                                |
| 8   | P1.2 / LCD_DH2 / UART3_TXD / IC1                                                                          |
| 9   | P1.1 / LCD_DH1 / UART3_RXD / UART1_TXD / IC2                                                              |
| 10  | VLCD                                                                                                      |
| 11  | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                                                              |
| 12  | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                                                                     |
| 13  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                                      |
| 14  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                                                     |
| 15  | P0.7 / LCD_SEG1 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1                                                  |
| 16  | P0.6 / LCD_SEG0 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0                                                  |
| 17  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLK0                                 |
| 18  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                                              |
| 19  | P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4                                           |
| 20  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5                                           |
| 21  | nRESET                                                                                                    |
| 22  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                                                         |
| 23  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                                                         |
| 24  | P4.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL / PWM1_CH0                                             |
| 25  | P4.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD / I2C1_SDA / PWM1_CH1                                             |
| 26  | P4.3 / LCD_SEG29 / LCD_COM6 / PWM2_CH0                                                                    |
| 27  | P4.2 / LCD_SEG28 / LCD_COM7 / PWM2_CH1                                                                    |
| 28  | P4.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O                                   |
| 29  | P4.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1                            |
| 30  | P1.4 / LCD_SEG21 / I2C1_SCL / LCD_COM4                                                                    |
| 31  | P1.5 / LCD_SEG20 / I2C1_SDA / LCD_COM5                                                                    |
| 32  | P1.6 / LCD_SEG19 / UART0_TXD / LCD_COM6                                                                   |
| 33  | P1.7 / LCD_SEG18 / UART0_RXD / LCD_COM7                                                                   |
| 34  | V <sub>SS</sub>                                                                                           |

| Pin | ML54MD1AE Pin Function                                                                                |
|-----|-------------------------------------------------------------------------------------------------------|
| 35  | P4.6 / LCD_SEG17 / PWM0_CH0 / T0 / CLKO / INT0                                                        |
| 36  | V <sub>DD</sub>                                                                                       |
| 37  | P3.3 / LCD_SEG15 / SPI1_SS / LCD_COM1 / PWM1_CH0 / IC0 / PWM0_BRAKE                                   |
| 38  | P3.2 / ADC_CH7 / ACMP1_N1 / LCD_SEG14 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO                  |
| 39  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / LCD_SEG13 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2 |
| 40  | P3.0 / ADC_CH10 / LCD_SEG12 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0                                  |
| 41  | V <sub>REF</sub>                                                                                      |
| 42  | AV <sub>SS</sub>                                                                                      |
| 43  | P2.7 / ADC_CH15 / LCD_SEG7 / UART1_TXD / PWM3_CH0 / ACMP0_O                                           |
| 44  | P2.6 / LCD_SEG6 / UART1_RXD / PWM3_CH1 / ACMP1_O                                                      |

ML56MD1AE Pin Function

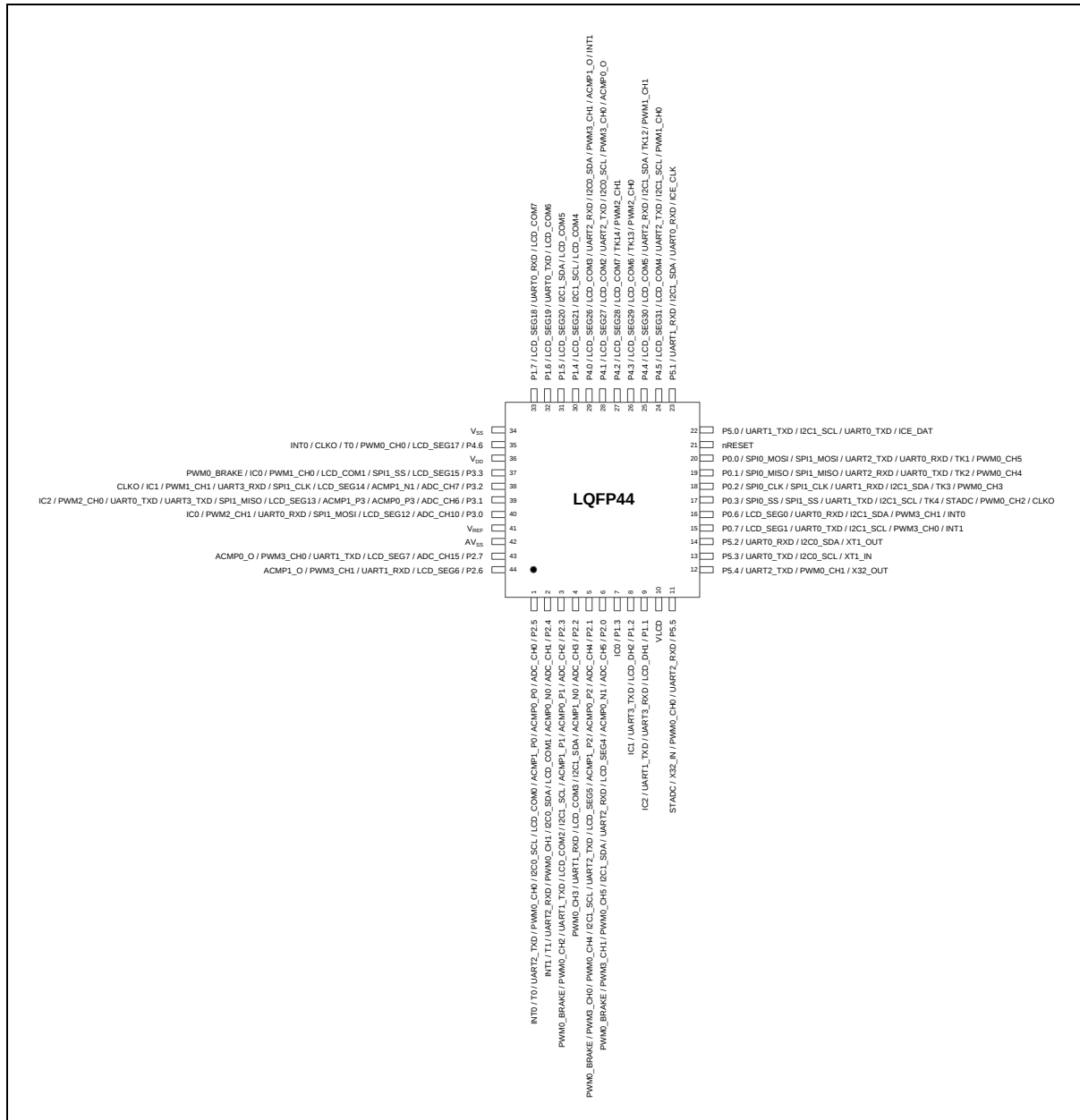


Figure 4.1-22 ML56MD1AE Multi-Function Pin assignment

| Pin | ML56MD1AE Pin Function                                                                  |
|-----|-----------------------------------------------------------------------------------------|
| 1   | P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0             |
| 2   | P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1                      |
| 3   | P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE          |
| 4   | P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3                              |
| 5   | P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE |

| Pin | ML56MD1AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 6   | P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE      |
| 7   | P1.3/IC0                                                                            |
| 8   | P1.2/LCD_DH2/UART3_TXD/IC1                                                          |
| 9   | P1.1/LCD_DH1/UART3_RXD/UART1_TXD/IC2                                                |
| 10  | VLCD                                                                                |
| 11  | P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC                                                |
| 12  | P5.4/UART2_TXD/PWM0_CH1/X32_OUT                                                     |
| 13  | P5.3/UART0_TXD/I2C0_SCL/XT1_IN                                                      |
| 14  | P5.2/UART0_RXD/I2C0_SDA/XT1_OUT                                                     |
| 15  | P0.7/LCD_SEG1/UART0_TXD/I2C1_SCL/PWM3_CH0/INT1                                      |
| 16  | P0.6/LCD_SEG0/UART0_RXD/I2C1_SDA/PWM3_CH1/INT0                                      |
| 17  | P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO                     |
| 18  | P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3                              |
| 19  | P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4                           |
| 20  | P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5                           |
| 21  | nRESET                                                                              |
| 22  | P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT                                           |
| 23  | P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK                                           |
| 24  | P4.5/LCD_SEG31/LCD_COM4/UART2_TXD/I2C1_SCL/PWM1_CH0                                 |
| 25  | P4.4/LCD_SEG30/LCD_COM5/UART2_RXD/I2C1_SDA/TK12/PWM1_CH1                            |
| 26  | P4.3/LCD_SEG29/LCD_COM6/TK13/PWM2_CH0                                               |
| 27  | P4.2/LCD_SEG28/LCD_COM7/TK14/PWM2_CH1                                               |
| 28  | P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O                         |
| 29  | P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1                    |
| 30  | P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4                                                    |
| 31  | P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5                                                    |
| 32  | P1.6/LCD_SEG19/UART0_TXD/LCD_COM6                                                   |
| 33  | P1.7/LCD_SEG18/UART0_RXD/LCD_COM7                                                   |
| 34  | VSS                                                                                 |
| 35  | P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0                                                |
| 36  | VDD                                                                                 |
| 37  | P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE                             |
| 38  | P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO                |
| 39  | P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2 |

| Pin | ML56MD1AE Pin Function                                   |
|-----|----------------------------------------------------------|
| 40  | P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0 |
| 41  | V <sub>REF</sub>                                         |
| 42  | AVSS                                                     |
| 43  | P2.7/ADC_CH15/LCD_SEG7/UART1_TXD/PWM3_CH0/ACMP0_O        |
| 44  | P2.6/LCD_SEG6/UART1_RXD/PWM3_CH1/ACMP1_O                 |

#### 4.1.2.4 QFN33 Package

#### ML51TD1AE Pin Function

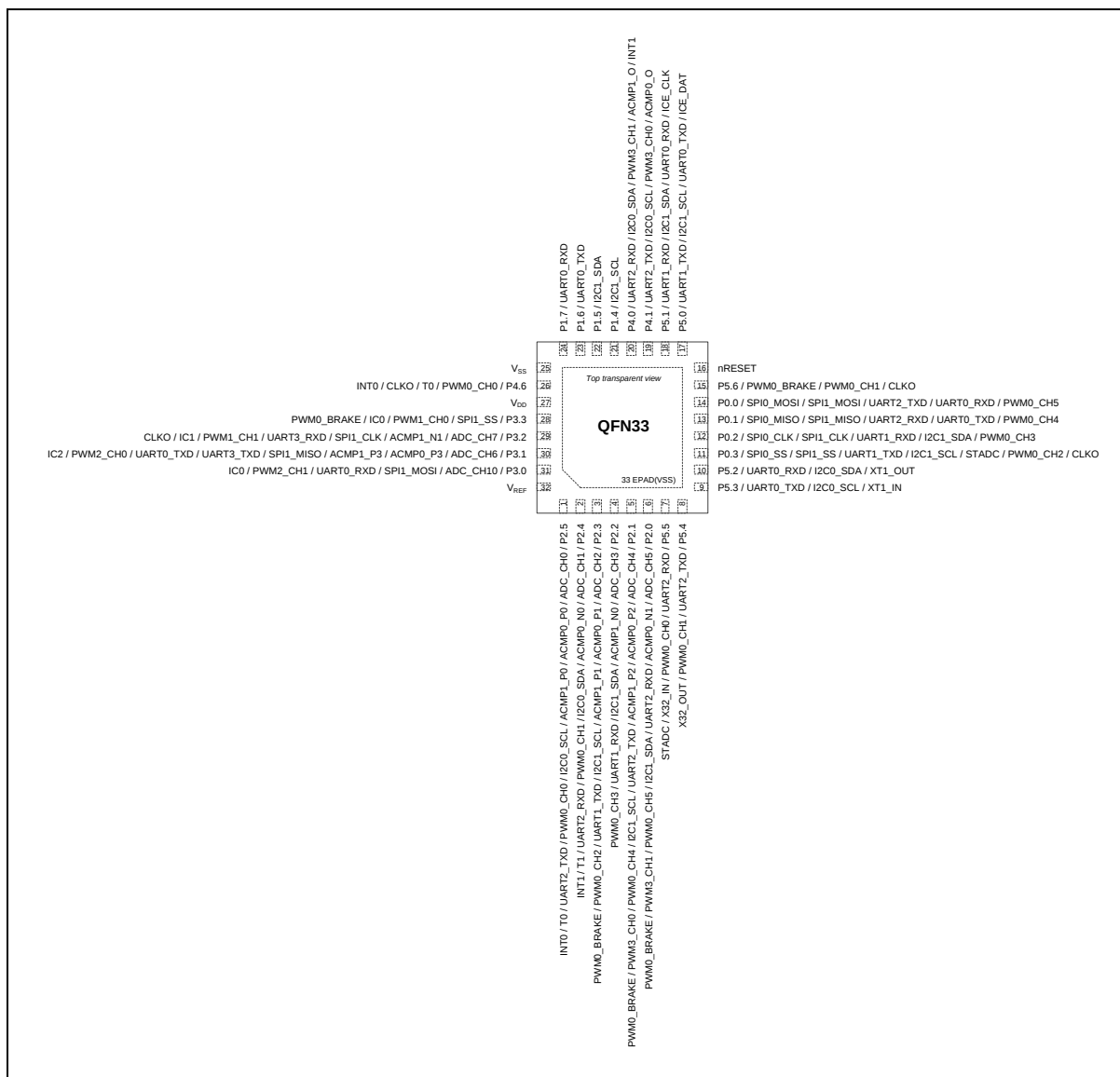


Figure 4.1-23 ML51TD1AE Multi-Function Pin assignment

| Pin | ML56TD1AE Pin Function                                                                  |
|-----|-----------------------------------------------------------------------------------------|
| 1   | P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0             |
| 2   | P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1                      |
| 3   | P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE          |
| 4   | P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3                              |
| 5   | P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE |
| 6   | P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE          |

| Pin | ML56TD1AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 7   | P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC                                                |
| 8   | P5.4/UART2_TXD/PWM0_CH1/X32_OUT                                                     |
| 9   | P5.3/UART0_TXD/I2C0_SCL/XT1_IN                                                      |
| 10  | P5.2/UART0_RXD/I2C0_SDA/XT1_OUT                                                     |
| 11  | P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO                     |
| 12  | P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3                              |
| 13  | P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4                           |
| 14  | P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5                           |
| 15  | P5.6/TK0/PWM0_BRAKE/PWM0_CH1/CLKO                                                   |
| 16  | nRESET                                                                              |
| 17  | P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT                                           |
| 18  | P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK                                           |
| 19  | P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O                         |
| 20  | P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1                    |
| 21  | P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4                                                    |
| 22  | P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5                                                    |
| 23  | P1.6/LCD_SEG19/UART0_TXD/LCD_COM6                                                   |
| 24  | P1.7/LCD_SEG18/UART0_RXD/LCD_COM7                                                   |
| 25  | VSS                                                                                 |
| 26  | P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0                                                |
| 27  | VDD                                                                                 |
| 28  | P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE                             |
| 29  | P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO                |
| 30  | P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2 |
| 31  | P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0                            |
| 32  | V <sub>REF</sub>                                                                    |
| 33  | EPAD(VSS)                                                                           |

ML51TC0AE / ML51TB9AE Pin Function

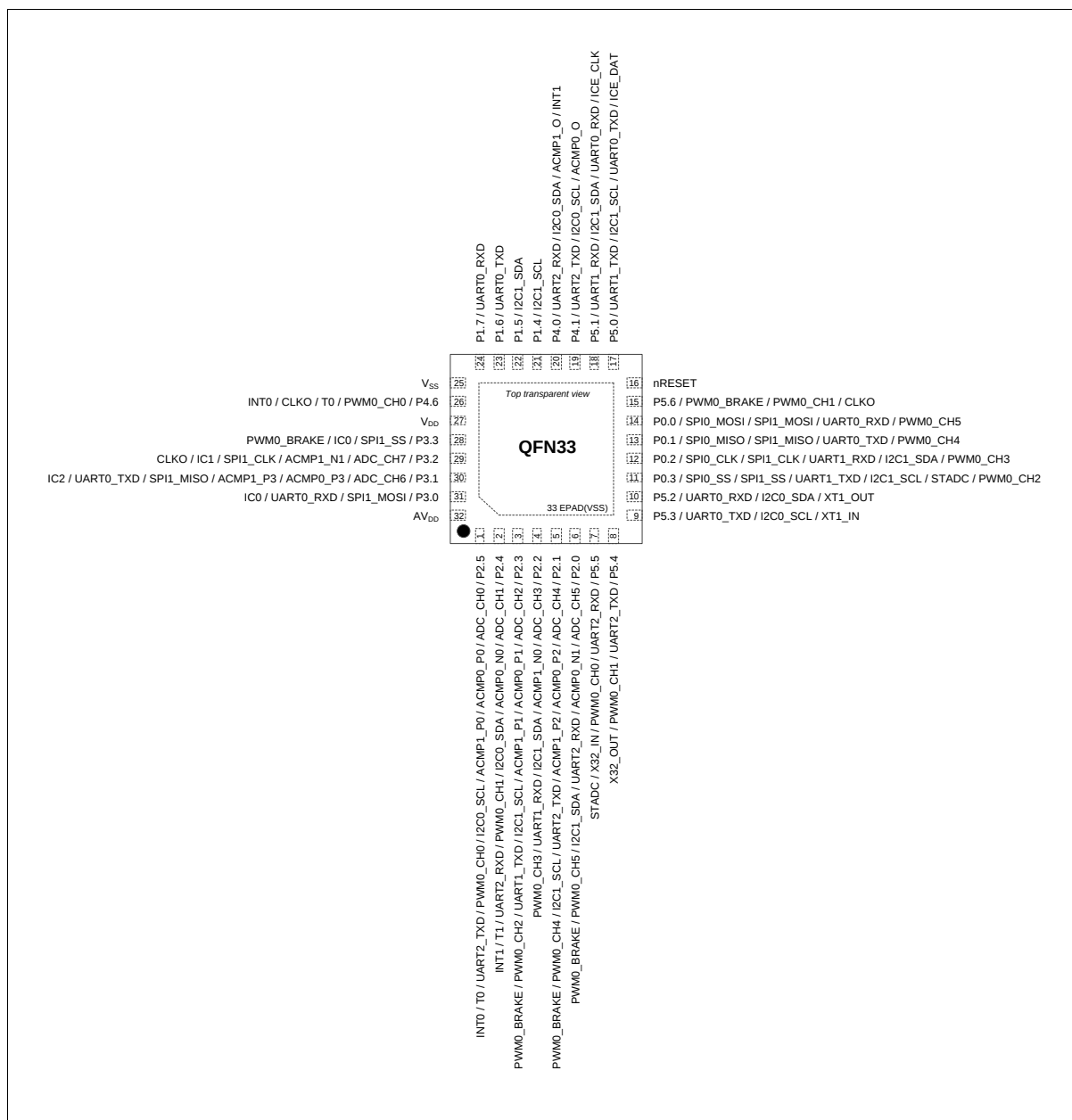


Figure 4.1-24 ML51TC0AE / ML51TB9AE Multi-Function Pin Assignment

| Pin | ML51TC0AE / ML51TB9AE Pin Function                                                  |
|-----|-------------------------------------------------------------------------------------|
| 1   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 2   | P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 3   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 4   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3                         |
| 5   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE |
| 6   | P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE            |

| Pin | ML51TC0AE / ML51TB9AE Pin Function                                 |
|-----|--------------------------------------------------------------------|
| 7   | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                       |
| 8   | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                              |
| 9   | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                               |
| 10  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                              |
| 11  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 |
| 12  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3       |
| 13  | P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4                |
| 14  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5                |
| 15  | P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO                                |
| 16  | nRESET                                                             |
| 17  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                  |
| 18  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                  |
| 19  | P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O                              |
| 20  | P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1                       |
| 21  | P1.4 / I2C1_SCL                                                    |
| 22  | P1.5 / I2C1_SDA                                                    |
| 23  | P1.6 / UART0_TXD                                                   |
| 24  | P1.7 / UART0_RXD                                                   |
| 25  | V <sub>SS</sub>                                                    |
| 26  | P4.6 / PWM0_CH0 / T0 / CLKO / INT0                                 |
| 27  | V <sub>DD</sub>                                                    |
| 28  | P3.3 / SPI1_SS / IC0 / PWM0_BRAKE                                  |
| 29  | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLKO                  |
| 30  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2 |
| 31  | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                 |
| 32  | AV <sub>DD</sub>                                                   |
| 33  | EPAD(VSS)                                                          |

4.1.2.5 LQFP32 Package

ML51PC0AE / ML51PB9AE Pin Function

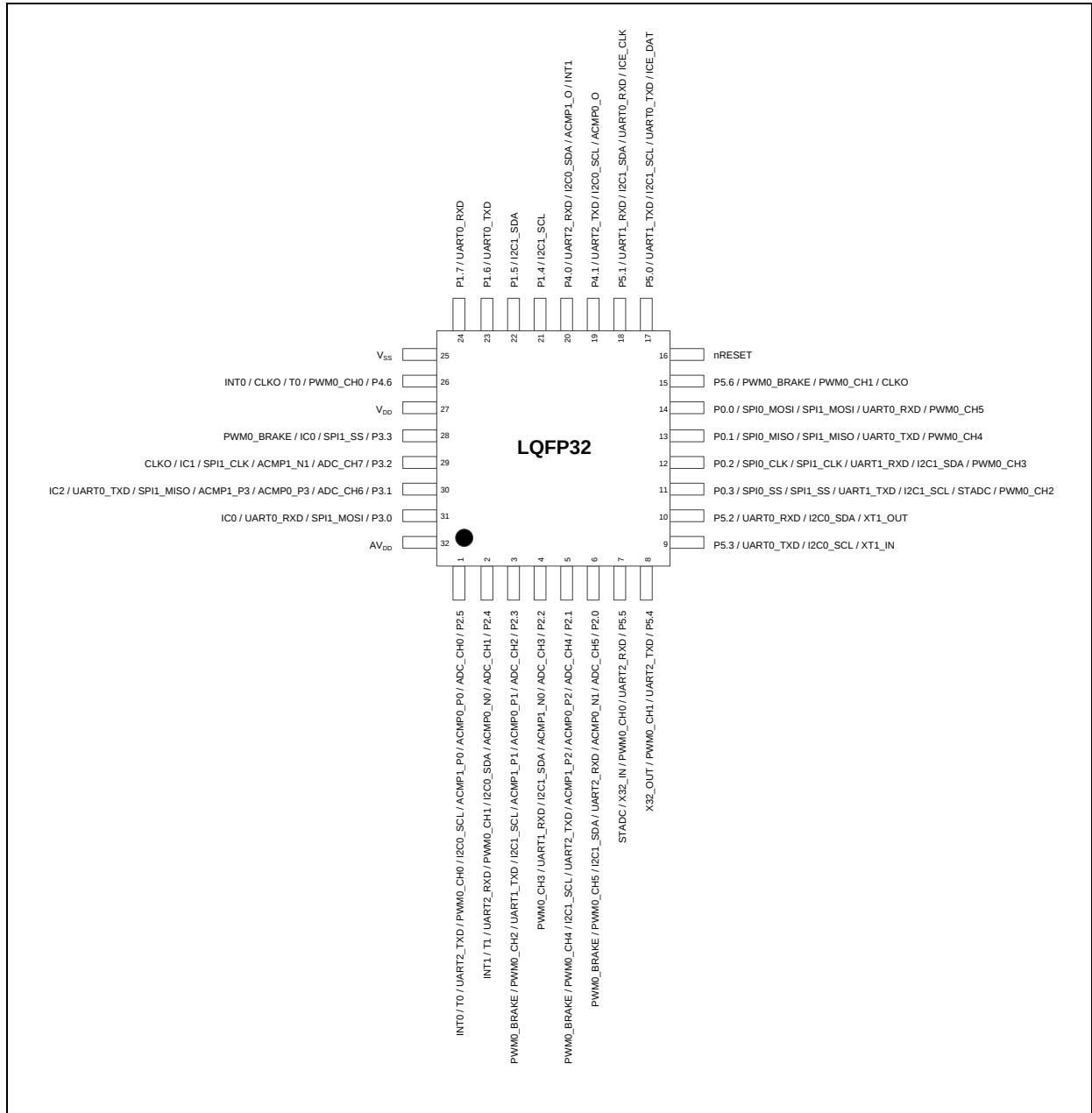


Figure 4.1-25 ML51PC0AE / ML51PB9AE Multi-Function Pin Assignment

| Pin | ML51PC0AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 1   | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 2   | P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 3   | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 4   | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3                         |

| Pin | ML51PC0AE Pin Function                                                              |
|-----|-------------------------------------------------------------------------------------|
| 5   | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE |
| 6   | P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE            |
| 7   | P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC                                        |
| 8   | P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT                                               |
| 9   | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                |
| 10  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                               |
| 11  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2                  |
| 12  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                        |
| 13  | P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4                                 |
| 14  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5                                 |
| 15  | P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO                                                 |
| 16  | nRESET                                                                              |
| 17  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                                   |
| 18  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                                   |
| 19  | P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O                                               |
| 20  | P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1                                        |
| 21  | P1.4 / I2C1_SCL                                                                     |
| 22  | P1.5 / I2C1_SDA                                                                     |
| 23  | P1.6 / UART0_TXD                                                                    |
| 24  | P1.7 / UART0_RXD                                                                    |
| 25  | V <sub>SS</sub>                                                                     |
| 26  | P4.6 / PWM0_CH0 / T0 / CLKO / INT0                                                  |
| 27  | V <sub>DD</sub>                                                                     |
| 28  | P3.3 / SPI1_SS / IC0 / PWM0_BRAKE                                                   |
| 29  | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLKO                                   |
| 30  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2                  |
| 31  | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                                  |
| 32  | AV <sub>DD</sub>                                                                    |

#### 4.1.2.6 TSSOP28 Package

#### ML51EC0AE / ML51EB9AE Pin Function

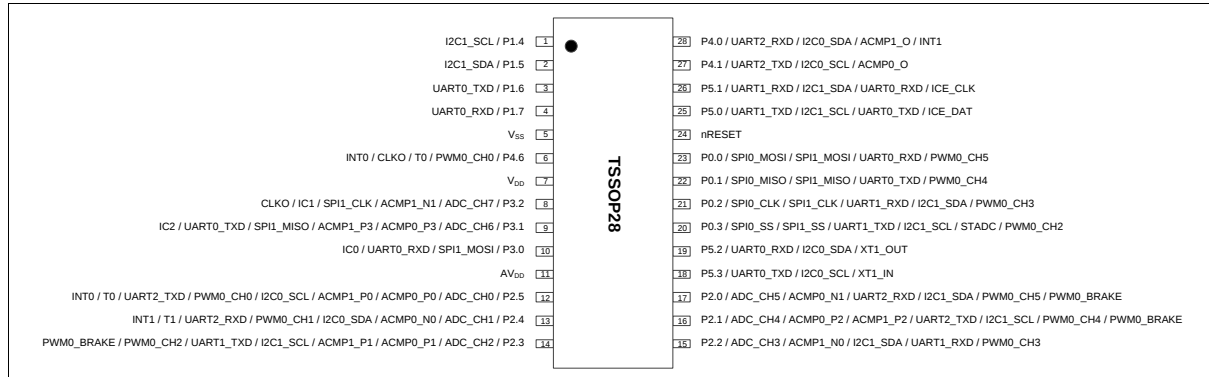


Figure 4.1-26 ML51EC0AE / ML51EB9AE Multi-Function Pin Assignment

| Pin | ML51EC0AE / ML51EB9AE Pin Function                                                  |
|-----|-------------------------------------------------------------------------------------|
| 1   | P1.4 / I2C1_SCL                                                                     |
| 2   | P1.5 / I2C1_SDA                                                                     |
| 3   | P1.6 / UART0_TXD                                                                    |
| 4   | P1.7 / UART0_RXD                                                                    |
| 5   | V <sub>SS</sub>                                                                     |
| 6   | P4.6 / PWM0_CH0 / T0 / CLK0 / INT0                                                  |
| 7   | V <sub>DD</sub>                                                                     |
| 8   | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLK0                                   |
| 9   | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2                  |
| 10  | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                                  |
| 11  | AV <sub>DD</sub>                                                                    |
| 12  | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 13  | P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 14  | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 15  | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3                         |
| 16  | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE |
| 17  | P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE            |
| 18  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                |
| 19  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                               |
| 20  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2                  |
| 21  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                        |

| Pin | ML51EC0AE / ML51EB9AE Pin Function                  |
|-----|-----------------------------------------------------|
| 22  | P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4 |
| 23  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5 |
| 24  | nRESET                                              |
| 25  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT   |
| 26  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK   |
| 27  | P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O               |
| 28  | P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1        |

4.1.2.7 SOP28 Package

Corresponding Part Number: ML51UC0AE / ML51UB9AE

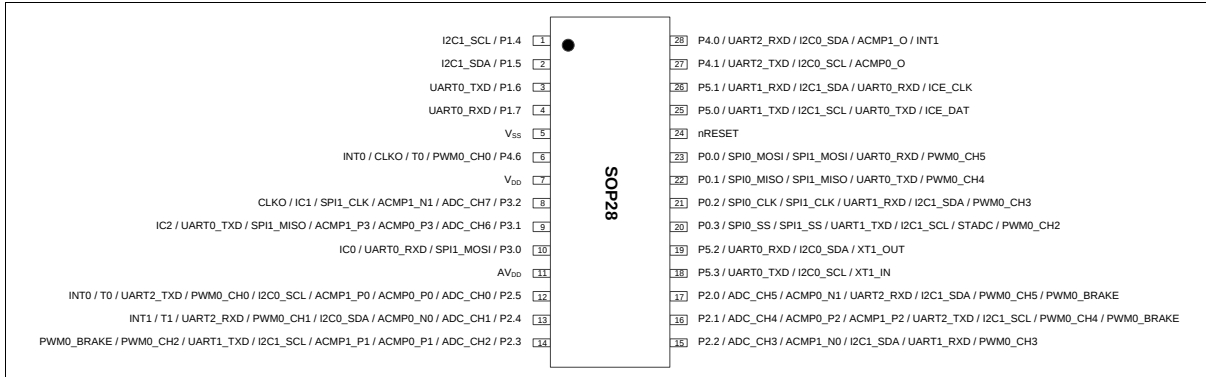


Figure 4.1-27 ML51UC0AE / ML51UB9AE Multi Function Pin Assignment

ML51UC0AE / ML51UB9AE Pin Function

| Pin | ML51UC0AE / ML51UB9AE Pin Function                                                  |
|-----|-------------------------------------------------------------------------------------|
| 1   | P1.4 / I2C1_SCL                                                                     |
| 2   | P1.5 / I2C1_SDA                                                                     |
| 3   | P1.6 / UART0_TXD                                                                    |
| 4   | P1.7 / UART0_RXD                                                                    |
| 5   | V <sub>SS</sub>                                                                     |
| 6   | P4.6 / PWM0_CH0 / T0 / CLK0 / INT0                                                  |
| 7   | V <sub>DD</sub>                                                                     |
| 8   | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLK0                                   |
| 9   | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2                  |
| 10  | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                                  |
| 11  | AV <sub>DD</sub>                                                                    |
| 12  | P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 13  | P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1             |
| 14  | P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 15  | P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3                         |
| 16  | P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE |
| 17  | P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE            |
| 18  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                                                |
| 19  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                                               |
| 20  | P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2                  |

| Pin | ML51UC0AE / ML51UB9AE Pin Function                           |
|-----|--------------------------------------------------------------|
| 21  | P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3 |
| 22  | P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4          |
| 23  | P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5          |
| 24  | nRESET                                                       |
| 25  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT            |
| 26  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK            |
| 27  | P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O                        |
| 28  | P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1                 |

#### 4.1.2.8 TSSOP20 Package

##### ML51FB9AE Pin Function

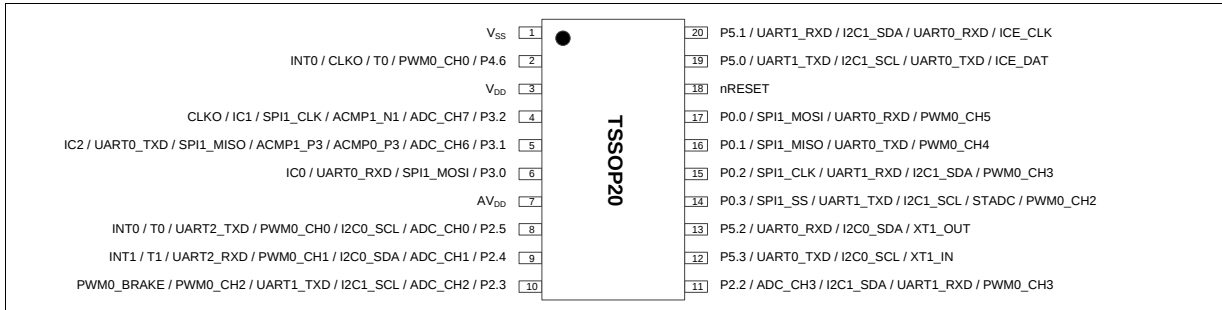


Figure 4.1-28 ML51FB9AE Multi Function Pin Assignment

| Pin | ML51FB9AE Pin Function                                             |
|-----|--------------------------------------------------------------------|
| 1   | V <sub>SS</sub>                                                    |
| 2   | P4.6 / PWM0_CH0 / T0 / CLKO / INT0                                 |
| 3   | V <sub>DD</sub>                                                    |
| 4   | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLKO                  |
| 5   | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2 |
| 6   | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                 |
| 7   | AV <sub>DD</sub>                                                   |
| 8   | P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0       |
| 9   | P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1       |
| 10  | P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE      |
| 11  | P2.2 / ADC_CH3 / I2C1_SDA / UART1_RXD / PWM0_CH3                   |
| 12  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                               |
| 13  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                              |
| 14  | P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2           |
| 15  | P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                  |
| 16  | P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4                            |
| 17  | P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5                            |
| 18  | nRESET                                                             |
| 19  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                  |
| 20  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                  |

#### 4.1.2.9 SOP20 Package

##### ML51OB9AE Pin Function

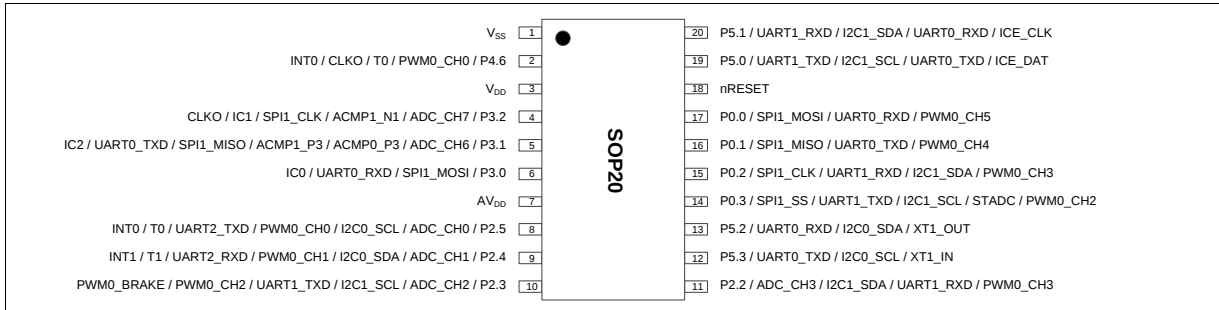


Figure 4.1-29 ML51OB9AE Multi Function Pin Assignment

| Pin | ML51OB9AE Pin Function                                             |
|-----|--------------------------------------------------------------------|
| 1   | V <sub>SS</sub>                                                    |
| 2   | P4.6 / PWM0_CH0 / T0 / CLKO / INT0                                 |
| 3   | V <sub>DD</sub>                                                    |
| 4   | P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLKO                  |
| 5   | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2 |
| 6   | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                 |
| 7   | AV <sub>DD</sub>                                                   |
| 8   | P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0       |
| 9   | P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1       |
| 10  | P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE      |
| 11  | P2.2 / ADC_CH3 / I2C1_SDA / UART1_RXD / PWM0_CH3                   |
| 12  | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                               |
| 13  | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                              |
| 14  | P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2           |
| 15  | P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                  |
| 16  | P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4                            |
| 17  | P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5                            |
| 18  | nRESET                                                             |
| 19  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                  |
| 20  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                  |

#### 4.1.2.10 QFN20 Package

#### ML51XB9AE Pin Function

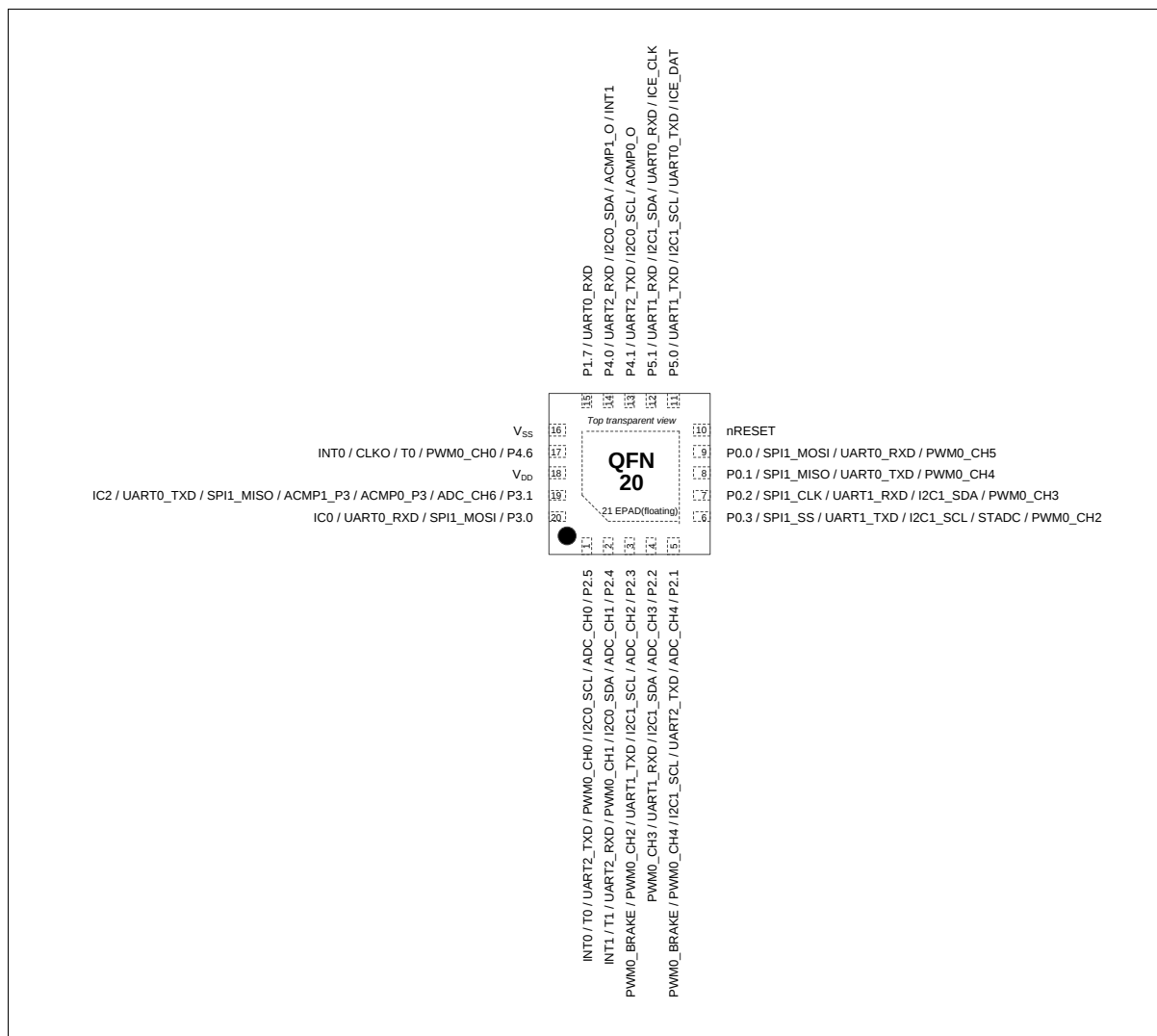


Figure 4.1-30 ML51XB9AE Multi Function Pin Assignment

| Pin | ML51XB9AE Pin Function                                        |
|-----|---------------------------------------------------------------|
| 1   | P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0  |
| 2   | P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1  |
| 3   | P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 4   | P2.2 / ADC_CH3 / I2C1_SDA / UART1_RXD / PWM0_CH3              |
| 5   | P2.1 / ADC_CH4 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE |
| 6   | P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2      |
| 7   | P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3             |
| 8   | P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4                       |

| Pin | ML51XB9AE Pin Function                                             |
|-----|--------------------------------------------------------------------|
| 9   | P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5                            |
| 10  | nRESET                                                             |
| 11  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                  |
| 12  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                  |
| 13  | P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O                              |
| 14  | P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1                       |
| 15  | P1.7 / UART0_RXD                                                   |
| 16  | V <sub>SS</sub>                                                    |
| 17  | P4.6 / PWM0_CH0 / T0 / CLK0 / INT0                                 |
| 18  | V <sub>DD</sub>                                                    |
| 19  | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2 |
| 20  | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                 |
| 21  | EPAD(floating)                                                     |

#### 4.1.2.11 TSSOP14 Package

##### ML51DB9AE Pin Function

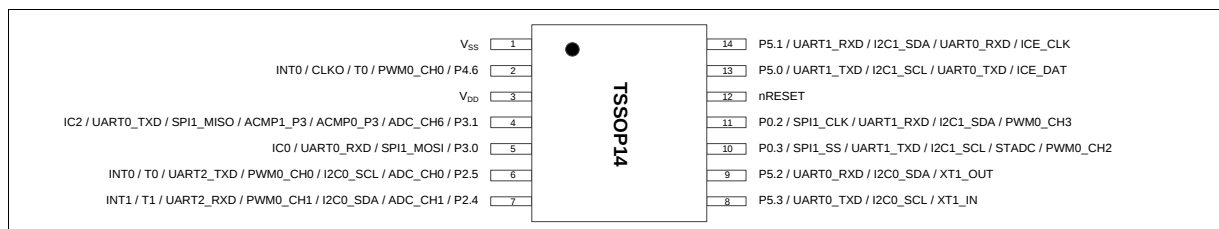


Figure 4.1-31 ML51DB9AE Multi Function Pin Assignment

| Pin | ML51DB9AE Pin Function                                             |
|-----|--------------------------------------------------------------------|
| 1   | V <sub>SS</sub>                                                    |
| 2   | P4.6 / PWM0_CH0 / T0 / CLK0 / INT0                                 |
| 3   | V <sub>DD</sub>                                                    |
| 4   | P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2 |
| 5   | P3.0 / SPI1_MOSI / UART0_RXD / IC0                                 |
| 6   | P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0       |
| 7   | P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1       |
| 8   | P5.3 / UART0_TXD / I2C0_SCL / XT1_IN                               |
| 9   | P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT                              |
| 10  | P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2           |
| 11  | P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3                  |
| 12  | nRESET                                                             |
| 13  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT                  |
| 14  | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK                  |

#### 4.1.2.12 MSOP10 Package

##### ML51BB9AE Pin Function

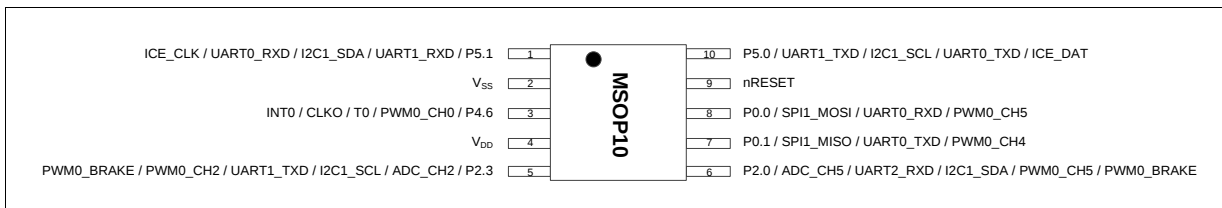


Figure 4.1-32 ML51BB9AE Pin Assignment

| Pin | ML51BB9AE Pin Function                                        |
|-----|---------------------------------------------------------------|
| 1   | P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK             |
| 2   | V <sub>SS</sub>                                               |
| 3   | P4.6 / PWM0_CH0 / T0 / CLK0 / INT0                            |
| 4   | V <sub>DD</sub>                                               |
| 5   | P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE |
| 6   | P2.0 / ADC_CH5 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE |
| 7   | P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4                       |
| 8   | P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5                       |
| 9   | nRESET                                                        |
| 10  | P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT             |

## 4.2 Pin Description

### 4.2.1 ML51/ML54/ML56 Series Pin Mapping

| Pin Number | ML54/ML56 |    |    | ML51  |    |       |    |    |       |    |    |
|------------|-----------|----|----|-------|----|-------|----|----|-------|----|----|
|            | 64        | 48 | 44 | 64    | 48 | 33/32 | 28 | 20 | QFN20 | 14 | 10 |
| AVDD       | 57        | 39 | 36 | 57    | 39 | 27    | 7  |    |       |    |    |
| AVSS       | 59        | 46 | 42 | 59    | 46 |       |    |    | 16    |    |    |
| VDD        | 23/51     | 39 | 36 | 23/51 | 39 | 27    | 7  | 3  | 18    | 3  | 4  |
| VSS        | 22/49     | 37 | 34 | 22/49 | 37 | 25/33 | 5  | 1  | 16    | 1  | 2  |
| nRESET     | 32        | 24 | 21 | 32    | 24 | 16    | 24 | 18 | 10    | 12 | 9  |
| VLCD       | 12        | 10 | 10 |       |    |       |    |    |       |    |    |
| VREF       | 58        | 45 | 41 | 58    | 45 | 32    | 11 | 7  |       |    |    |
| EPAD       |           |    |    |       |    | 33    |    |    | 21    |    |    |
| P0.0       | 30        | 22 | 20 | 30    | 22 | 14    | 23 | 17 | 9     |    | 8  |
| P0.1       | 29        | 21 | 19 | 29    | 21 | 13    | 22 | 16 | 8     |    | 7  |
| P0.2       | 28        | 20 | 18 | 28    | 20 | 12    | 21 | 15 | 7     | 11 |    |
| P0.3       | 27        | 19 | 17 | 27    | 19 | 11    | 20 | 14 | 6     | 10 |    |
| P0.4       | 26        | 18 |    | 26    | 18 |       |    |    |       |    |    |
| P0.5       | 25        | 17 |    | 25    | 17 |       |    |    |       |    |    |
| P0.6       | 21        | 16 | 16 | 21    | 16 |       |    |    |       |    |    |
| P0.7       | 20        | 15 | 15 | 20    | 15 |       |    |    |       |    |    |
| P1.0       | 11        |    |    | 11    | 10 |       |    |    |       |    |    |
| P1.1       | 10        | 9  | 9  | 10    | 9  |       |    |    |       |    |    |
| P1.2       | 9         | 8  | 8  | 9     | 8  |       |    |    |       |    |    |
| P1.3       | 8         | 7  | 7  | 8     | 7  |       |    |    |       |    |    |
| P1.4       | 45        | 33 | 30 | 45    | 33 | 21    | 1  |    |       |    |    |
| P1.5       | 46        | 34 | 31 | 46    | 34 | 22    | 2  |    |       |    |    |
| P1.6       | 47        | 35 | 32 | 47    | 35 | 23    | 3  |    |       |    |    |
| P1.7       | 48        | 36 | 33 | 48    | 36 | 24    | 4  |    | 15    |    |    |
| P2.0       | 7         | 6  | 6  | 7     | 6  | 6     | 17 |    |       |    | 6  |
| P2.1       | 6         | 5  | 5  | 6     | 5  | 5     | 16 |    | 5     |    |    |
| P2.2       | 5         | 4  | 4  | 5     | 4  | 4     | 15 | 11 | 4     |    |    |
| P2.3       | 4         | 3  | 3  | 4     | 3  | 3     | 14 | 10 | 3     |    | 5  |
| P2.4       | 3         | 2  | 2  | 3     | 2  | 2     | 13 | 9  | 2     | 7  |    |
| P2.5       | 2         | 1  | 1  | 2     | 1  | 1     | 12 | 8  | 1     | 6  |    |
| P2.6       | 1         | 48 | 44 | 1     | 48 |       |    |    |       |    |    |
| P2.7       | 64        | 47 | 43 | 64    | 47 |       |    |    |       |    |    |
| P3.0       | 56        | 44 | 40 | 56    | 44 | 31    | 10 | 6  | 20    | 5  |    |
| P3.1       | 55        | 43 | 39 | 55    | 43 | 30    | 9  | 5  | 19    | 4  |    |

|            | ML54/ML56 |    |    | ML51 |    |       |    |    |       |    |    |
|------------|-----------|----|----|------|----|-------|----|----|-------|----|----|
| Pin Number | 64        | 48 | 44 | 64   | 48 | 33/32 | 28 | 20 | QFN20 | 14 | 10 |
| P3.2       | 54        | 42 | 38 | 54   | 42 | 29    | 8  | 4  |       |    |    |
| P3.3       | 53        | 41 | 37 | 53   | 41 | 28    |    |    |       |    |    |
| P3.4       | 19        |    |    | 19   |    |       |    |    |       |    |    |
| P3.5       | 18        |    |    | 18   |    |       |    |    |       |    |    |
| P3.6       | 24        |    |    | 24   |    |       |    |    |       |    |    |
| P3.7       |           |    |    | 12   |    |       |    |    |       |    |    |
| P4.0       | 40        | 32 | 29 | 40   | 32 | 20    | 28 |    | 14    |    |    |
| P4.1       | 39        | 31 | 28 | 39   | 31 | 19    | 27 |    | 13    |    |    |
| P4.2       | 38        | 30 | 27 | 38   | 30 |       |    |    |       |    |    |
| P4.3       | 37        | 29 | 26 | 37   | 29 |       |    |    |       |    |    |
| P4.4       | 36        | 28 | 25 | 36   | 28 |       |    |    |       |    |    |
| P4.5       | 35        | 27 | 24 | 35   | 27 |       |    |    |       |    |    |
| P4.6       | 50        | 38 | 35 | 50   | 38 | 26    | 6  | 2  | 17    | 2  | 3  |
| P4.7       | 52        | 40 |    | 52   | 40 |       |    |    |       |    |    |
| P5.0       | 33        | 25 | 22 | 33   | 25 | 17    | 25 | 19 | 11    | 13 | 10 |
| P5.1       | 34        | 26 | 23 | 34   | 26 | 18    | 26 | 20 | 12    | 14 | 1  |
| P5.2       | 17        | 14 | 14 | 17   | 14 | 10    | 19 | 13 |       | 9  |    |
| P5.3       | 16        | 13 | 13 | 16   | 13 | 9     | 18 | 12 |       | 8  |    |
| P5.4       | 15        | 12 | 12 | 15   | 12 | 8     |    |    |       |    |    |
| P5.5       | 14        | 11 | 11 | 14   | 11 | 7     |    |    |       |    |    |
| P5.6       | 31        | 23 |    | 31   | 23 | 15    |    |    |       |    |    |
| P5.7       | 13        |    |    | 13   |    |       |    |    |       |    |    |
| P6.0       | 44        |    |    | 44   |    |       |    |    |       |    |    |
| P6.1       | 43        |    |    | 43   |    |       |    |    |       |    |    |
| P6.2       | 42        |    |    | 42   |    |       |    |    |       |    |    |
| P6.3       | 41        |    |    | 41   |    |       |    |    |       |    |    |
| P6.4       | 63        |    |    | 63   |    |       |    |    |       |    |    |
| P6.5       | 62        |    |    | 62   |    |       |    |    |       |    |    |
| P6.6       | 61        |    |    | 61   |    |       |    |    |       |    |    |
| P6.7       | 60        |    |    | 60   |    |       |    |    |       |    |    |

#### 4.2.2 ML51/ML54/ML56 Series Pin Functional Description

As default all GPIO type is defined as input mode. User should setting the GPIO Mode by PxMx register.

A: Analog suggest disable digial function O: output, I: input, I/O: bi-direction (Quasi)

| Group | Pin Name | Type | Description                               |
|-------|----------|------|-------------------------------------------|
| ACMP0 | ACMP0_N0 | A    | Analog comparator 0 negative input 0 pin. |
|       | ACMP0_N1 |      | Analog comparator 0 negative input 1 pin. |
|       | ACMP0_O  | O    | Analog comparator 0 output pin.           |
|       | ACMP0_P0 | A    | Analog comparator 0 positive input 0 pin. |
|       | ACMP0_P1 |      | Analog comparator 0 positive input 1 pin. |
|       | ACMP0_P2 |      | Analog comparator 0 positive input 2 pin. |
|       | ACMP0_P3 |      | Analog comparator 0 positive input 3 pin. |
| ACMP1 | ACMP1_N0 | A    | Analog comparator 1 negative input 0 pin. |
|       | ACMP1_N1 |      | Analog comparator 1 negative input 1 pin. |
|       | ACMP1_O  | O    | Analog comparator 1 output pin.           |
|       | ACMP1_P0 | A    | Analog comparator 1 positive input 0 pin. |
|       | ACMP1_P1 |      | Analog comparator 1 positive input 1 pin. |
|       | ACMP1_P2 |      | Analog comparator 1 positive input 2 pin. |
|       | ACMP1_P3 |      | Analog comparator 1 positive input 3 pin. |
| ADC   | ADC_CH0  | A    | ADC_ channel analog input.                |
|       | ADC_CH1  |      | ADC_ channel analog input.                |
|       | ADC_CH2  |      | ADC_ channel analog input.                |
|       | ADC_CH3  |      | ADC_ channel analog input.                |
|       | ADC_CH4  |      | ADC_ channel analog input.                |
|       | ADC_CH5  |      | ADC_ channel analog input.                |
|       | ADC_CH6  |      | ADC_ channel analog input.                |
|       | ADC_CH7  |      | ADC_ channel analog input.                |
|       | ADC_CH10 |      | ADC_ channel analog input.                |
|       | ADC_CH11 |      | ADC_ channel analog input.                |
|       | ADC_CH12 |      | ADC_ channel analog input.                |
|       | ADC_CH13 |      | ADC_ channel analog input.                |
|       | ADC_CH14 |      | ADC_ channel analog input.                |
|       | ADC_CH15 |      | ADC_ channel analog input.                |
| CLKO  | CLKO     | O    | Clock Out                                 |
| I2C0  | I2C0_SCL | I/O  | I2C0 clock pin.                           |
|       | I2C0_SDA | I/O  | I2C0 data input/output pin.               |
| I2C1  | I2C1_SCL | I/O  | I2C1 clock pin.                           |

| Group | Pin Name  | Type | Description                                                                                                      |
|-------|-----------|------|------------------------------------------------------------------------------------------------------------------|
|       | I2C1_SDA  | I/O  | I2C1 data input/output pin.                                                                                      |
| IC0   | IC0       | I/O  | Input Capture channel 0                                                                                          |
| IC1   | IC1       | I/O  | Input Capture channel 1                                                                                          |
| IC2   | IC2       | I/O  | Input Capture channel 2                                                                                          |
| ICE   | ICE_CLK   | I    | Serial wired debugger clock pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin |
|       | ICE_DAT   | O    | Serial wired debugger data pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin  |
| INT0  | INT0      | I    | External interrupt 0 input pin.                                                                                  |
| INT1  | INT1      | I    | External interrupt 1 input pin.                                                                                  |
| LCD   | LCD_COM0  | O    | LCD Common 0 output.                                                                                             |
|       | LCD_COM1  | O    | LCD Common 1 output.                                                                                             |
|       | LCD_COM2  | O    | LCD Common 2 output.                                                                                             |
|       | LCD_COM3  | O    | LCD Common 3 output.                                                                                             |
|       | LCD_COM4  | O    | LCD Common 4 output.                                                                                             |
|       | LCD_COM5  | O    | LCD Common 5 output.                                                                                             |
|       | LCD_COM6  | O    | LCD Common 6 output.                                                                                             |
|       | LCD_COM7  | O    | LCD Common 7 output.                                                                                             |
|       | LCD_DH1   | O    | LCD external capacitor pin of charge pump circuit.                                                               |
|       | LCD_DH2   | O    | LCD external capacitor pin of charge pump circuit.                                                               |
|       | LCD_SEG0  | O    | LCD segment 0 output                                                                                             |
|       | LCD_SEG1  | O    | LCD segment 1 output                                                                                             |
|       | LCD_SEG2  | O    | LCD segment 2 output                                                                                             |
|       | LCD_SEG3  | O    | LCD segment 3 output                                                                                             |
|       | LCD_SEG4  | O    | LCD segment 4 output                                                                                             |
|       | LCD_SEG5  | O    | LCD segment 5 output                                                                                             |
|       | LCD_SEG6  | O    | LCD segment 6 output                                                                                             |
|       | LCD_SEG7  | O    | LCD segment 7 output                                                                                             |
|       | LCD_SEG8  | O    | LCD segment 8 output                                                                                             |
|       | LCD_SEG9  | O    | LCD segment 9 output                                                                                             |
|       | LCD_SEG10 | O    | LCD segment 10 output                                                                                            |
|       | LCD_SEG11 | O    | LCD segment 11 output                                                                                            |
|       | LCD_SEG12 | O    | LCD segment 12 output                                                                                            |
|       | LCD_SEG13 | O    | LCD segment 13 output                                                                                            |

| Group  | Pin Name   | Type | Description                                                                                                                                                                                             |
|--------|------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        | LCD_SEG14  | O    | LCD segment 14 output                                                                                                                                                                                   |
|        | LCD_SEG15  | O    | LCD segment 15 output                                                                                                                                                                                   |
|        | LCD_SEG16  | O    | LCD segment 16 output                                                                                                                                                                                   |
|        | LCD_SEG17  | O    | LCD segment 17 output                                                                                                                                                                                   |
|        | LCD_SEG18  | O    | LCD segment 18 output                                                                                                                                                                                   |
|        | LCD_SEG19  | O    | LCD segment 19 output                                                                                                                                                                                   |
|        | LCD_SEG20  | O    | LCD segment 20 output                                                                                                                                                                                   |
|        | LCD_SEG21  | O    | LCD segment 21 output                                                                                                                                                                                   |
|        | LCD_SEG22  | O    | LCD segment 22 output                                                                                                                                                                                   |
|        | LCD_SEG23  | O    | LCD segment 23 output                                                                                                                                                                                   |
|        | LCD_SEG24  | O    | LCD segment 24 output                                                                                                                                                                                   |
|        | LCD_SEG25  | O    | LCD segment 25 output                                                                                                                                                                                   |
|        | LCD_SEG26  | O    | LCD segment 26 output                                                                                                                                                                                   |
|        | LCD_SEG27  | O    | LCD segment 27 output                                                                                                                                                                                   |
|        | LCD_SEG28  | O    | LCD segment 28 output                                                                                                                                                                                   |
|        | LCD_SEG29  | O    | LCD segment 29 output                                                                                                                                                                                   |
|        | LCD_SEG30  | O    | LCD segment 30 output                                                                                                                                                                                   |
|        | LCD_SEG31  | O    | LCD segment 31 output                                                                                                                                                                                   |
|        | LCD_V1     | I    | Output pin of the 1 <sup>st</sup> most positive LCD level for measurement.                                                                                                                              |
|        | LCD_V2     | I    | Output pin of the 2 <sup>nd</sup> most positive LCD level for measurement.                                                                                                                              |
|        | LCD_V3     | I    | Output pin of the 3 <sup>rd</sup> most positive LCD level for measurement.                                                                                                                              |
| nRESET | nRESET     | I    | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.<br><b>Note:</b> It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin. |
| PWM0   | PWM0_BRAKE | I    | PWM0 Brake input pin.                                                                                                                                                                                   |
|        | PWM0_CH0   | I/O  | PWM0 channel 0 output/capture input.                                                                                                                                                                    |
|        | PWM0_CH1   | I/O  | PWM0 channel 1 output/capture input.                                                                                                                                                                    |
|        | PWM0_CH2   | I/O  | PWM0 channel 2 output/capture input.                                                                                                                                                                    |
|        | PWM0_CH3   | I/O  | PWM0 channel 3 output/capture input.                                                                                                                                                                    |
|        | PWM0_CH4   | I/O  | PWM0 channel 4 output/capture input.                                                                                                                                                                    |
|        | PWM0_CH5   | I/O  | PWM0 channel 5 output/capture input.                                                                                                                                                                    |
| PWM1   | PWM1_CH0   | I/O  | PWM1 channel 0 output/capture input.                                                                                                                                                                    |
|        | PWM1_CH1   | I/O  | PWM1 channel 1 output/capture input.                                                                                                                                                                    |
| PWM2   | PWM2_CH0   | I/O  | PWM2 channel 0 output/capture input.                                                                                                                                                                    |
|        | PWM2_CH1   | I/O  | PWM2 channel 1 output/capture input.                                                                                                                                                                    |

| Group | Pin Name  | Type | Description                                                   |
|-------|-----------|------|---------------------------------------------------------------|
| PWM3  | PWM3_CH0  | I/O  | PWM3 channel 0 output/capture input.                          |
|       | PWM3_CH1  | I/O  | PWM3 channel 1 output/capture input.                          |
| SPI0  | SPI0_CLK  | I/O  | SPI0 serial clock pin.                                        |
|       | SPI0_MISO | I/O  | SPI0 MISO (Master In, Slave Out) pin.                         |
|       | SPI0_MOSI | I/O  | SPI0 MOSI (Master Out, Slave In) pin.                         |
|       | SPI0_SS   | I/O  | SPI0 slave select pin.                                        |
| SPI1  | SPI1_CLK  | I/O  | SPI1 serial clock pin.                                        |
|       | SPI1_MISO | I/O  | SPI1 MISO (Master In, Slave Out) pin.                         |
|       | SPI1_MOSI | I/O  | SPI1 MOSI (Master Out, Slave In) pin.                         |
|       | SPI1_SS   | I/O  | SPI1 slave select pin.                                        |
| STADC | STADC     | I    | ADC external trigger input.                                   |
| T0    | T0        | I/O  | External count input to Timer/Counter 0 or its toggle output. |
| T1    | T1        | I/O  | External count input to Timer/Counter 1 or its toggle output. |
| TK    | TK0       | A    | Touch Key 0.                                                  |
|       | TK1       | A    | Touch Key 1.                                                  |
|       | TK2       | A    | Touch Key 2.                                                  |
|       | TK3       | A    | Touch Key 3.                                                  |
|       | TK4       | A    | Touch Key 4.                                                  |
|       | TK5       | A    | Touch Key 5.                                                  |
|       | TK6       | A    | Touch Key 6.                                                  |
|       | TK7       | A    | Touch Key 7.                                                  |
|       | TK8       | A    | Touch Key 8.                                                  |
|       | TK9       | A    | Touch Key 9.                                                  |
|       | TK10      | A    | Touch Key 10.                                                 |
|       | TK11      | A    | Touch Key 11.                                                 |
|       | TK12      | A    | Touch Key 12.                                                 |
|       | TK13      | A    | Touch Key 13.                                                 |
|       | TK14      | A    | Touch Key 14.                                                 |
| UART0 | UART0_RXD | I    | UART0 data receiver input pin.                                |
|       | UART0_TXD | O    | UART0 data transmitter output pin.                            |
| UART1 | UART1_RXD | I    | UART1 data receiver input pin.                                |
|       | UART1_TXD | O    | UART1 data transmitter output pin.                            |
| UART2 | UART2_RXD | I    | UART2 data receiver input pin.                                |
|       | UART2_TXD | O    | UART2 data transmitter output pin.                            |
| UART3 | UART3_RXD | I    | UART3 data receiver input pin.                                |

| Group            | Pin Name  | Type           | Description                                                                                                                                  |
|------------------|-----------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------|
|                  | UART3_TXD | O              | UART3 data transmitter output pin.                                                                                                           |
| V <sub>REF</sub> | VREF      | A              | ADC reference voltage input.<br><b>Note:</b> This pin needs to be connected with a 1uF capacitor when use internal voltage reference output. |
| X32              | X32_IN    | I              | External 32.768 kHz crystal input pin.                                                                                                       |
|                  | X32_OUT   | O              | External 32.768 kHz crystal output pin.                                                                                                      |
| XT1              | XT1_IN    | I              | External 4~24 MHz (high speed) crystal input pin.                                                                                            |
|                  | XT1_OUT   | O              | External 4~24 MHz (high speed) crystal output pin.                                                                                           |
| EPAD             | EPAD      | VSS / Floating | Exposed pad connect to VSS or floating                                                                                                       |

## 5 BLOCK DIAGRAM

### 5.1 ML51/ML54/ML56 Series Full Function Block

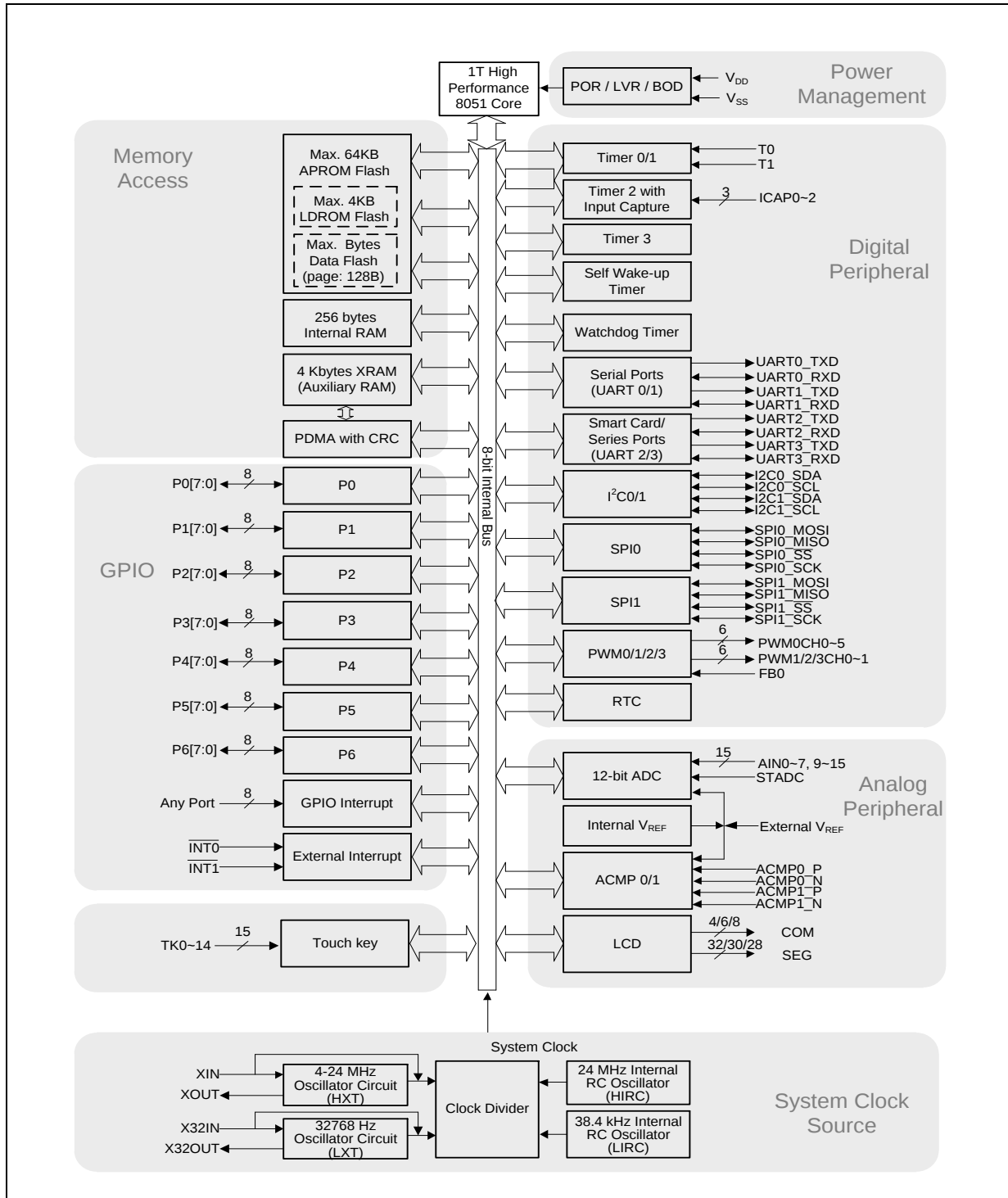


Figure 5.1-1 Functional Block Diagram

## 6 FUNCTIONAL DESCRIPTION

### 6.1 Memory Organization

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In ML51/ML54/ML56 Series, there are 256 bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the ML51/ML54/ML56 Series provides another on-chip 4 Kbytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded Flash, functioning as Program Memory, is divided into three blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 bytes. The Flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes.

## 6.2 System Manager

The ML51/ML54/ML56 Series has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. The ML51/ML54/ML56 Series provides five options of the system clock sources including internal oscillator, crystal/resonator, or external clock from  $X_{IN}$  pin via software. The ML51/ML54/ML56 Series is embedded with two internal oscillators: one 38.4 kHz low-speed and one 24 MHz high-speed, which is factory trimmed to  $\pm 2\%$  under all conditions. A clock divider CKDIV is also available on ML51/ML54/ML56 Series for adjustment of the flexibility between power consumption and operating performance.

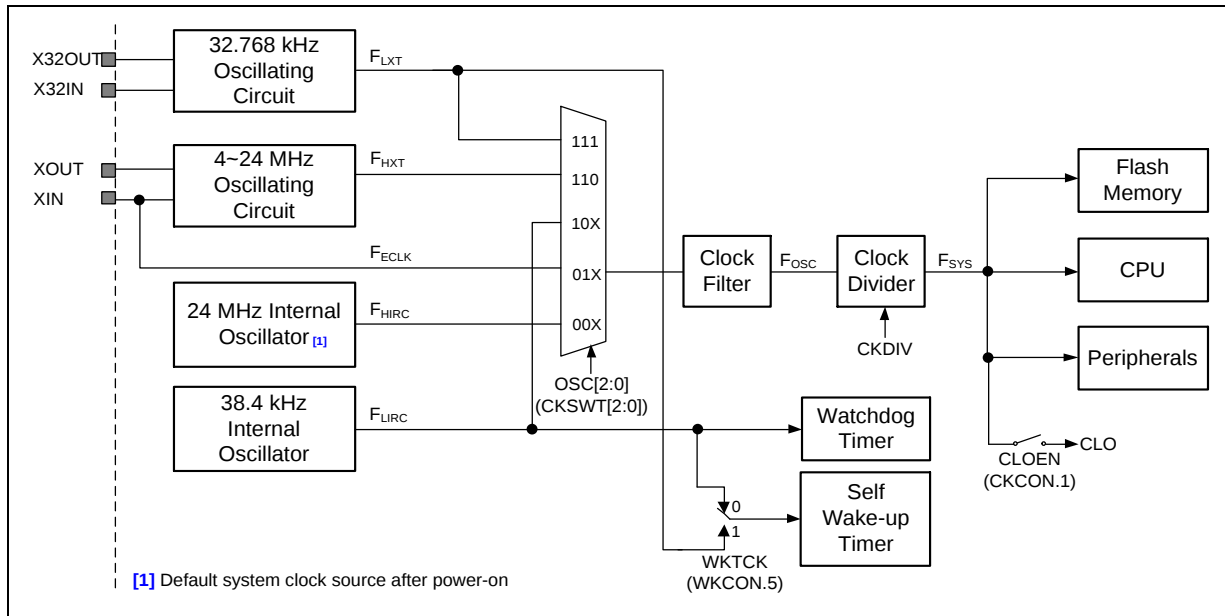


Figure 6.2-1 Clock System Block Diagram

## 6.3 Flash Memory Control

### 6.3.1 In-application-programming (IAP)

Unlike RAM's real-time operation, to update Flash data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read Flash data. The ML51/ML54/ML56 Series carried out the Flash operation with convenient mechanism to help user re-programming the Flash content by In-Application-Programming (IAP). IAP is an in-circuit electrical erasure and programming method through software.

After IAP enabling by setting IAPEN (CHPCON.0 with TA protected) and setting the enable bit in IAPUEN that allows the target block to be updated, user can easily fill the 16-bit target address in IAPAH and IAPAL, data in IAPFD, and command in IAPCN. Then the IAP is ready to begin by setting a triggering bit IAPGO (IAPTRG.0). Note that IAPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in IAP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. The erase and program time is internally controlled regardless of the operating voltage and frequency. Nominally, a page-erase time is 5 ms and a byte-program time is 23.5  $\mu$ s. After IAP action completed, the Program Counter continues to run the following instructions. The IAPGO bit will be automatically cleared. An IAP failure flag, IAPFF (CHPCON.6), can be check whether the previous IAP operation was successful or not. Through this progress, user can easily erase, program, and verify the Flash Memory by just taking care of pure software.

### 6.3.2 In-Circuit-Programming (ICP)

The Flash Memory can be programmed by "In-Circuit-Programming" (ICP). If the product is just under development or the end product needs firmware updating in the hand of an end customer, the hardware programming mode will make repeated programming difficult and inconvenient. ICP method makes it easy and possible without removing the microcontroller from the system. ICP mode also allows customers to manufacture circuit boards with un-programmed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a customized firmware.

There are three signal pins,  $\overline{\text{RST}}$ , ICPDA, and ICPCCK, involved in ICP function.  $\overline{\text{RST}}$  is used to enter or exit ICP mode. ICPDA is the data input and output pin. ICPCCK is the clock input pin, which synchronizes the data shifted in to or out from MCU under programming. User should leave these three pins plus  $V_{DD}$  and GND pins on the circuit board to make ICP possible.

Nuvoton provides ICP tool for ML51/ML54/ML56 Series, which enables user to easily perform ICP through Nuvoton ICP programmer. The ICP programmer developed by Nuvoton has been optimized according to the electric characteristics of MCU. It also satisfies the stability and efficiency during production progress. For more details, please visit Nuvoton 8-bit Microcontroller website: [Nuvoton 80C51 Microcontroller Technical Support](#).

### 6.3.3 On-Chip-Debugger (ICE)

The ML51/ML54/ML56 Series is embedded in an on-chip-debugger (OCD) providing developers with a low cost method for debugging user code, which is available on each package. The OCD gives debug capability of complete program flow control with eight hardware address breakpoints, single step, free running, and non-intrusive commands for memory access. The OCD system does not occupy any locations in the memory map and does not share any on-chip peripherals.

## 6.4 GPIO Port Structure and Operation

### 6.4.1 GPIO Mode

The ML51/ML54/ML56 Series has a maximum of 56 general purpose I/O pins which 40 bit-addressable general I/O pins grouped as 5 ports, P0 to P4, and 16 general I/O pins grouped as P5 and P6. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, where as a read gets the port pin logic state. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. The list below illustrates how to select the I/O mode of Px.n. Note that the default configuration of is input-only (high-impedance) after any reset.

| PnM1.X <sup>[1]</sup>         | PnM2.X <sup>[1]</sup> | I/O Type                    |
|-------------------------------|-----------------------|-----------------------------|
| 0                             | 0                     | Quasi-bidirectional         |
| 0                             | 1                     | Push-pull                   |
| 1                             | 0                     | Input-only (high-impedance) |
| 1                             | 1                     | Open-drain                  |
| <b>Note:</b> N = 0~5, x = 0~7 |                       |                             |

Table 6.4-1 Configuration for Different I/O Modes

All I/O pins can be selected as TTL level inputs or Schmitt triggered inputs by selecting corresponding bit in PxS register. Schmitt triggered input has better glitch suppression capability. All I/O pins also have bit-controllable, slew rate select ability via software. The Register Description are PxSR. By default, the slew rate is slow. If user would like to increase the I/O output speed, setting the corresponding bit in PxSR, the slew rate is selected in a faster level.

## 6.5 Timer

### 6.5.1 Overview

ML51/ML54/ML56 Series provides following 16-bit Timer. Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected. One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.

## 6.6 Watchdog Timer (WDT)

The ML51/ML54/ML56 Series provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

The Watchdog time-out interval is determined by the formula  $\frac{1}{F_{LIRC} \times \text{clock divider scalar}} \times 64$ , where  $F_{LIRC}$  is the frequency of internal 38.4 kHz oscillator. The following table shows an example of the Watchdog time-out interval with different pre-scales.

| WDPS.3 | WDPS.2 | WDPS.1 | WDPS.0 | Clock Divider Scale | WDT Time-Out Timing <sup>[1]</sup> |
|--------|--------|--------|--------|---------------------|------------------------------------|
| 0      | 0      | 0      | 0      | 1/1                 | 1.66 ms                            |
| 0      | 0      | 0      | 1      | 1/4                 | 6.64 ms                            |
| 0      | 0      | 1      | 0      | 1/8                 | 13.31 ms                           |
| 0      | 0      | 1      | 1      | 1/16                | 26.62 ms                           |
| 0      | 1      | 0      | 0      | 1/32                | 53.25 ms                           |
| 0      | 1      | 0      | 1      | 1/64                | 106.66 ms                          |
| 0      | 1      | 1      | 0      | 1/128               | 213.12 ms                          |
| 0      | 1      | 1      | 1      | 1/256               | 426.64 ms                          |
| 1      | 0      | 0      | 0      | 1/512               | 853.28ms                           |
| 1      | 0      | 0      | 1      | 1/1024              | 1706.56ms                          |
| 1      | 0      | 1      | 0      | 1/2048              | 3413.12ms                          |
| Others |        |        |        | 1/2048              | 3413.12ms                          |

**Note:** This is an approximate value since the deviation of LIRC.

Table 6.6-1 Watchdog Timer-out Interval Under Different Pre-scalars

Since the limitation of the maxima vaule of WDT timer delay. To wake up ML51/ML54/ML56 Series from idle mode or power down mode suggest use WKT function see Chapter 6.7 .

The WDT is implemented with a set of divider that divides the low-speed internal oscillator clock nominal 38.4 kHz. The divider output is selectable and determines the time-out interval. When the time-out interval is fulfilled, it will wake the system up from Idle or Power-down mode and an interrupt event will occur if WDT interrupt is enabled. If WDT is initialized as a time-out reset timer, a system reset will occur after a period of delay if without any software action.

## 6.7 Self Wake-up Timer (WKT)

### 6.7.1 Overview

The ML51/ML54/ML56 Series has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has two clock source, internal LIRC 38.4 kHz or LXT 32.768 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 16-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The RWK can reloadable when counter is count to overflow. The CWK can read current count value. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

## 6.8 Pulse Width Modulated (PWM)

### 6.8.1 Overview

The PWM (Pulse Width Modulation) signal is a useful control solution in wide application field. It can be used on motor driving, fan control, backlight brightness tuning, LED light dimming, or simulating as a simple digital to analog converter output through a low pass filter circuit.

The ML51/ML54/ML56 Series PWM0 is especially designed for motor control by providing three pairs, maximum 16-bit resolution of PWM0 output with programmable period and duty. The architecture makes user easy to drive the one-phase or three-phase brushless DC motor (BLDC), or three-phase AC induction motor. Each of six PWM can be configured as one of independent mode, complementary mode, or synchronous mode. If the complementary mode is used, a programmable dead-time insertion is available to protect MOS turn-on simultaneously. The PWM waveform can be edge-aligned or center-aligned with variable interrupt points.

The ML51/ML54/ML56 Series PWM1/2/3 provide individual configurable period and duty, maximum 16-bit resolution output. Each of two PWM1/2/3 can be configured as one of independent mode, complementary mode, or synchronous mode. The PWM1/2/3 waveform can be edge-aligned or center-aligned with variable interrupt points.

### 6.8.2 Features

- Up To 12 output pins can be selected
- Supports maximum clock source frequency up to 24 MHz
- Supports up to Three PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output
- Supports complementary mode for 3 complementary paired PWM output channels
- Dead-time insertion with 8-bit resolution
- Supports 16-bit resolution PWM counter
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
- Supports trigger ADC on the following events

## 6.9 Serial Port (UART0 & UART1)

### 6.9.1 Overview

The ML51/ML54/ML56 Series includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register.

### 6.9.2 Features

- Supports up to 2 UARTs: UART0, UART1
- Supports 2 Smart Card configuration as UART function as UART2 and UART3.
- UART baud rate clock from HIRC or HXT.
- Full-duplex asynchronous communications
- Programmable 9th bit.
- TXD and RXD pins of UART0 exchangeable via software.

## 6.10 Smart Card Interface (SC)

### 6.10.1 Overview

The ML51/ML54/ML56 Series provides Smart Card Interface controller (SC controller) with asynchronous protocol based on ISO/IEC 7816-3 standard. Software controls GPIO pins as the smartcard reset function and card detection function. This controller also provides UART emulation for high precision baud rate communication.

### 6.10.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- Programmable transmission clock frequency
- Programmable extra guard time selection
- Supports auto inverse convention function
- Supports UART mode
  - Full duplex, asynchronous communications
  - Supports programmable baud rate generator for each channel
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SCnEGT register
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1 or 2 stop bit generation

## **6.11 Serial Peripheral Interface (SPI)**

### **6.11.1 Overview**

The ML51/ML54/ML56 Series provides two Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between microcontrollers or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to  $F_{SYS}/4$ , transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

### **6.11.2 Features**

- 2 sets of SPI devices
- Supports Master or Slave mode operation
- Supports MSB first or LSB first transfer sequence
- Slave mode up to 12 Mhz

## 6.12 Inter-Integrated Circuit (I<sup>2</sup>C)

### 6.12.1 Overview

The ML51/ML54/ML56 Series provides two Inter-Integrated Circuit (I<sup>2</sup>C) bus to serves as an serial interface between the microcontrollers and the I<sup>2</sup>C devices such as EEPROM, LCD module, temperature sensor, and so on. The I<sup>2</sup>C bus used two wires design (a serial data line SDA and a serial clock line SCL) to transfer information between devices.

The I<sup>2</sup>C bus uses bi-directional data transfer between masters and slaves. There is no central master and the multi-master system is allowed by arbitration between simultaneously transmitting masters. The serial clock synchronization allows devices with different bit rates to communicate via one serial bus. The I<sup>2</sup>C bus supports four transfer modes including master transmitter, master receiver, slave receiver, and slave transmitter. The I<sup>2</sup>C interface only supports 7-bit addressing mode. A special mode General Call is also available. The I<sup>2</sup>C can meet both standard (up to 100kbps) and fast (up to 400k bps) speeds.

### 6.12.2 Features

- ◆ 2 sets of I<sup>2</sup>C devices
- ◆ Master/Slave mode
- ◆ Bidirectional data transfer between masters and slaves
- ◆ Multi-master bus (no central master)
- ◆ 7-bit addressing mode
- ◆ Standard mode (100 kbps) and Fast mode (400 kbps).
- ◆ Supports 8-bit time-out counter requesting the I<sup>2</sup>C interrupt if the I<sup>2</sup>C bus hangs up and timer-out counter overflows
- ◆ Multiple address recognition (four slave addresses with mask option)
- ◆ Supports hold time programmable

## **6.13 12-bit Analog-to-digital Converter (ADC)**

### **6.13.1 Overview**

The ML51/ML54/ML56 Series is embedded with a 12-bit SAR ADC. The ADC (analog-to-digital converter) allows conversion of an analog input signal to a 12-bit binary representation of that signal. The ML51/ML54/ML56 Series is selected as 8-channel inputs in single end mode. The internal band-gap voltage 0.814 V also can be the internal ADC input. The analog input, multiplexed into one sample and hold circuit, charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation and stores the result in the result registers. The ADC controller also supports DMA (direct memory access) function for ADC continuous conversion and storage result data into XRAM no need special enable PDMA module.

#### 6.14 Voltage Reference (VREF)

The  $V_{REF}$  pin is for analog multiplexer, such as ADC, ACMP. It default be used as an external source(set  $ENVRF = 0$ ). It also could be configurable as on-chip reference voltage generator ( $V_{REF\_IN}$ ) by setting  $ENVRF = 1$ . The output voltage is selectable by setting  $VRFSEL[2:0]$ . The maximum load of the  $V_{REF\_IN}$  must be less than 200  $\mu A$  to  $AV_{SS}$ . Set pre-load is to reduce stable time of  $V_{REF\_IN}$ . At first enable  $V_{REF\_IN}$  and turn on pre-load at the same time, the minimum stable time of pre-load on the  $V_{REF\_IN}$  must be greater than 3 ms. After the  $V_{REF\_IN}$  stable, user should be turn off pre-load to avoid any interference on analog multiplexer. Pre-load is only for internal  $V_{REF}$  use. For detailed electrical characteristics

## 6.15 Analog Comparator Controller (ACMP)

### 6.15.1 Overview

The ML51/ML54/ML56 Series contains two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. The comparator can be configured to generate an interrupt when the comparator output value changes.

### 6.15.2 Feature

- Analog input voltage range: 0 ~ AV<sub>DD</sub>(voltage of AV<sub>DD</sub> pin)
- Supports hysteresis function
- Supports wake-up function
- Selectable input sources of negative input
- Comparator ACMP0 supports
  - ◆ 4 positive source
    - P2.5 (ACMPn\_P0)
    - P2.3 (ACMPn\_P1)
    - P2.1 (ACMPn\_P2)
    - P3.1 (ACMPn\_P3)
  - ◆ 4 negative sources
    - P2.4 (ACMP0\_N0)
    - Comparator Reference Voltage (CRV)
    - VBG (BANDGAP voltage)
    - P2.0 (ACMP0\_N1)
- Comparator ACMP1 supports
  - ◆ 4 positive source
    - P2.5 (ACMPn\_P0)
    - P2.3 (ACMPn\_P1)
    - P2.1 (ACMPn\_P2)
    - P3.1 (ACMPn\_P3)
  - ◆ 4 negative sources
    - P2.2 (ACMP1\_N0)
    - Comparator Reference Voltage (CRV)
    - VBG (BANDGAP voltage)
    - P3.2 (ACMP1\_N1)

## **6.16 PDMA Controller (PDMA)**

### **6.16.1 Overview**

The ML51/ML54/ML56 Series provides peripheral direct memory access (PDMA) controller. The PDMA controller is used to provide high-speed data transfer between memory and peripherals or between memory and memory. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications.

### **6.16.2 Feature**

- ◆ Supports transfer data width of 8 bits
- ◆ Supports software and SPI and SMC/UART request
- ◆ Supports source and destination address increment size can be byte
- ◆ Supports transfer done and half done interrupt
- ◆ Supports using PDMA to write data to perform CRC operation

## 6.17 LCD Driver

### 6.17.1 Overview

The Liquid Crystal Displays (LCD) panel is widely used to meet the display need in applications. The ML54/ML56 series is equipped with LCD driver that can directly drive the LCD panel with 4 COM x 32 SEG, 6 COM x 30 SEG or 8 COM x 28 SEG. Use the corresponding COM and SEM according to the definition of multiple function pin. The LCD driver supports 1/4 duty, 1/6 duty, or 1/8 duty. The driving voltage supports 1/2 bias, 1/3 bias or 1/4 bias with waveform type A or Type B. The source of LCD clock is based on the choice of LIRC or LXT. The LCD display can keep display on or off during chip in power-down mode. The LCD power supply VLCD source is selectable from internal charge pump, external VLCD pin or analog power AV<sub>DD</sub>.

### 6.17.2 Features

- 1.8V to 5.5V LCD operating voltage.
- Selectable LCD clock source from LIRC or LXT
- 1/2, 1/3, 1/4 bias selectable
- Maximum 4 COM x 32 SEG, 6 COM x 30 SEG, 8 COM x 28 SEG
- Supports buffer mode for high current driving
- Support enhanced resistor mode for low power application
- Support external VLCD source or AV<sub>DD</sub> as LCD voltage source.
- Support programmable internal charge pump circuit for LCD voltage level is higher or lower than V<sub>DD</sub> application.
- Support blink function.
- Support display on or off during chip in power down mode

## **6.18 Real Time Clock (RTC)**

### **6.18.1 Overview**

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

### **6.18.2 Features**

- Supports real time counter and calendar counter for RTC time and calendar check.
- Supports alarm time and calendar settings
- Supports alarm time and calendar mask enable settings.
- Selectable 12-hour or 24-hour time scale setting.
- Supports Leap Year indication setting.
- Supports Day of the Week counter setting.
- Frequency of RTC clock source compensate by RTCFREQADJ0/1 register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.

## **6.19 Touch Key (TK)**

### **6.19.1 Overview**

The capacitive touch key sensing controller supports several programmable sensitivity levels for different applications to detect the finger touched or near the electrode covered by dielectric. It supports total 15 keys with single scan or programmable periodic key scans, and system can be waked up by any key for low power applications.

### **6.19.2 Features**

- Supports up to 14 touch keys + 1 reference
- Supports any CLKO pin as shielding and any TK pin as reference.
- Programmable sensitivity levels for each channel.
- Programmable scanning speed for different applications.
- Supports any touch key wake up for low power applications.
- Supports single key scan and programmable periodic key scan.
- Programmable interrupt options for key scan complete with/without threshold control.

## 6.20 Instruction Set

The ML51/ML54/ML56 Series executes all the instructions of the standard 80C51 family fully compatible with MCS-51. However, the timing of each instruction is different for it uses high performance 1T 8051 core. The architecture eliminates redundant bus states and implements parallel execution of fetching, decode, and execution phases. The ML51/ML54/ML56 Series uses one clock per machine-cycle. It leads to performance improvement of rate 8.1 (in terms of MIPS) with respect to traditional 12T 80C51 device working at the same clock frequency. However, the real speed improvement seen in any system will depend on the instruction mix.

All instructions are coded within an 8-bit field called an OPCODE. This single byte should be fetched from Program Memory. The OPCODE is decoded by the CPU. It determines what action the CPU will take and whether more operation data is needed from memory. If no other data is needed, then only one byte was required. Thus the instruction is called a one byte instruction. In some cases, more data is needed, which is two or three byte instructions.

## 7 APPLICATION CIRCUIT

### 7.1 Power Supply Scheme

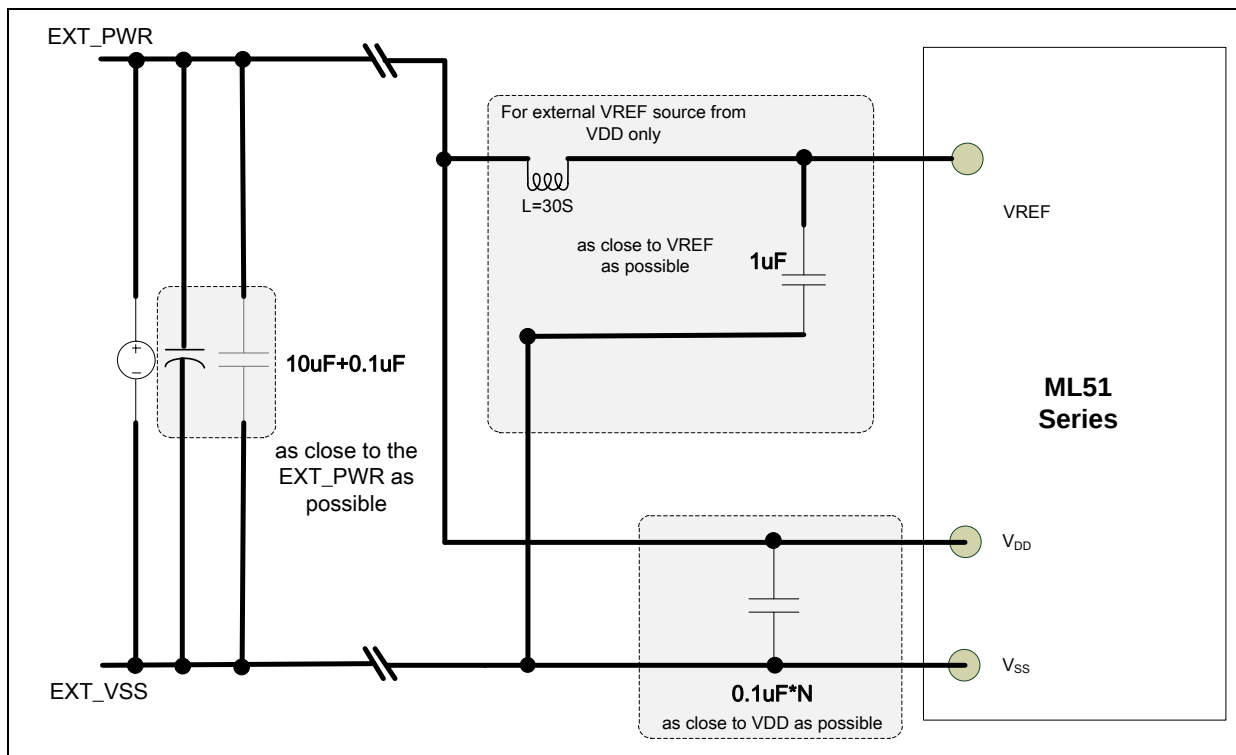


Figure 7.1-1 NuMicro® ML51/ML54/ML56 Series Power supply circuit

## 7.2 Peripheral Application Scheme

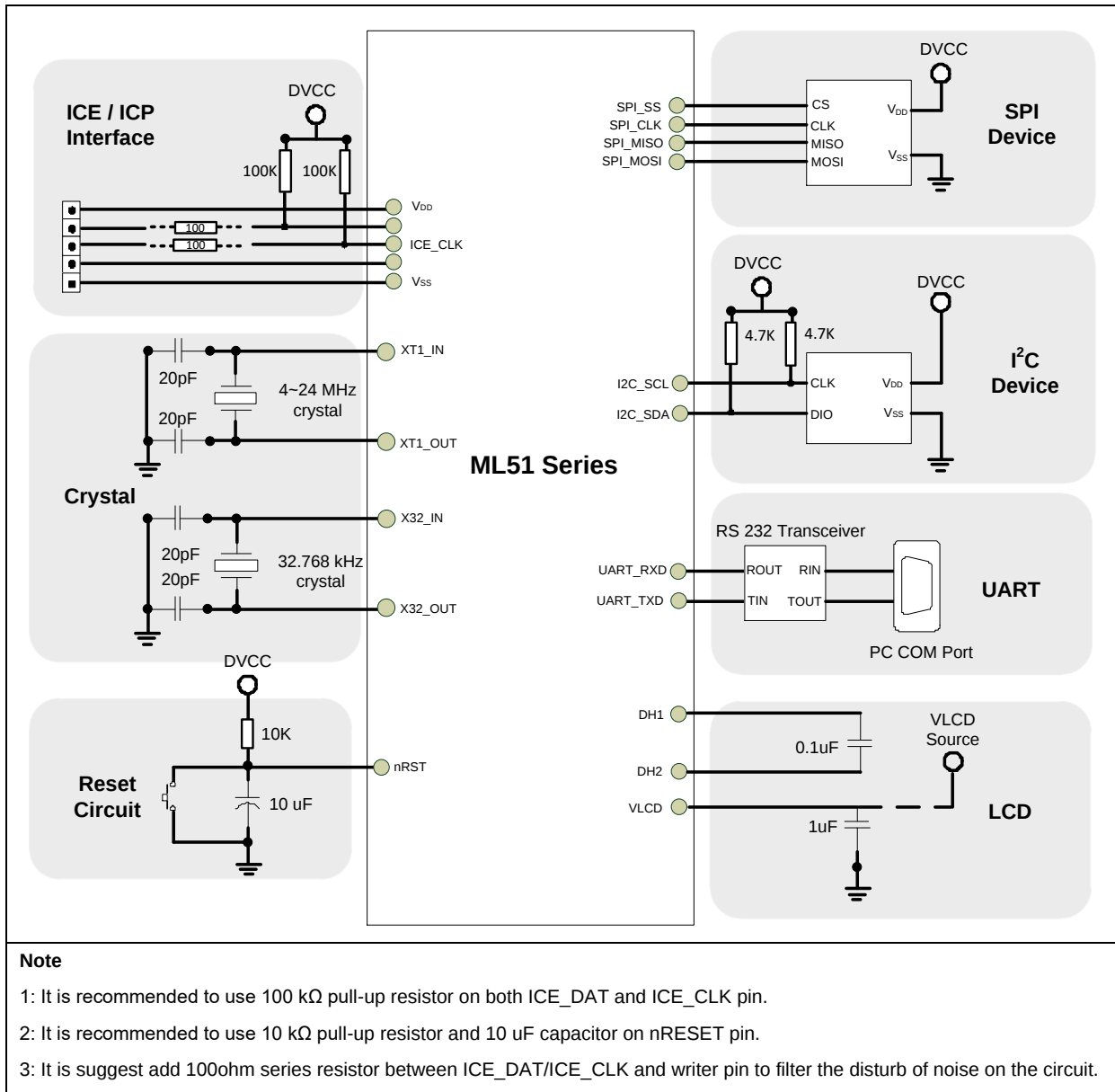


Figure 7.2-1 NuMicro® ML51/ML54/ML56 Series Peripheral interface circuit

## 8 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the ML51/ML54/ML56 series electrical characteristics.

### 8.1 General Operating Conditions

( $V_{DD}-V_{SS} = 1.8 \sim 5.5V$ ,  $T_A = 25^\circ C$ ,  $F_{sys} = 24\text{ MHz}$  unless otherwise specified.)

#### 8.1.1 ML51 32KB/16KB Flash Series

| Symbol                                                                                                                                                                                                                                                                                              | Parameter                | Min             | Typ | Max | Unit | Test Conditions |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-----------------|-----|-----|------|-----------------|
| T <sub>A</sub>                                                                                                                                                                                                                                                                                      | Temperature              | -40             | -   | 105 | °C   |                 |
| V <sub>DD</sub>                                                                                                                                                                                                                                                                                     | Operation voltage        | 1.8             | -   | 5.5 | V    |                 |
| AV <sub>DD</sub> <sup>[1]</sup>                                                                                                                                                                                                                                                                     | Analog operation voltage | V <sub>DD</sub> |     |     |      |                 |
| <b>Note:</b><br>1. It is recommended to power V <sub>DD</sub> and AV <sub>DD</sub> from the same source. A maximum difference of 0.3V between V <sub>DD</sub> and AV <sub>DD</sub> can be tolerated during power-on and power-off operation .<br>2.Based on characterization, tested in production. |                          |                 |     |     |      |                 |

Table 8.1-1 ML51 32KB/16KB Flash Series General Operating Conditions

#### 8.1.2 ML51 64KB Flash/ML54/ML56 Series

| Symbol                                                                                                                                                                                                                                                                                                       | Parameter                | Min             | Typ | Max | Unit | Test Conditions |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-----------------|-----|-----|------|-----------------|
| T <sub>A</sub>                                                                                                                                                                                                                                                                                               | Temperature              | -40             | -   | 105 | °C   |                 |
| V <sub>DD</sub>                                                                                                                                                                                                                                                                                              | Operation voltage        | 1.8             | -   | 3.6 | V    |                 |
| AV <sub>DD</sub> <sup>[1]</sup>                                                                                                                                                                                                                                                                              | Analog operation voltage | V <sub>DD</sub> |     |     |      |                 |
| <b>Note:</b><br><br>1. It is recommended to power V <sub>DD</sub> and AV <sub>DD</sub> from the same source. A maximum difference of 0.3V between V <sub>DD</sub> and AV <sub>DD</sub> can be tolerated during power-on and power-off operation .<br><br>2. Based on characterization, tested in production. |                          |                 |     |     |      |                 |

Table 8.1-2 ML56/ML54/ML51 64KB Flash Series General Operating Conditions

## 8.2 DC Electrical Characteristics

### 8.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

#### 8.2.1.1 ML51 32KB/16KB Flash Series

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for  $V_{DD} = 1.8V \sim 5.5V$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25^\circ C$  and  $V_{DD} = 3.3V$  unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock  $F_{sys}$ .
- Program run “while (1);” in flash.

#### Normal Run Mode

| Symbol              | Conditions                                                    | Fsys                            | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|---------------------|---------------------------------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                     |                                                               |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_RUN</sub> | Normal run mode, executed from Flash, all peripherals disable | 24 MHz (HIRC) <sup>[1]</sup>    | 2.40                   | 2.64                   | 2.87                   | 2.90                    | mA   |
|                     |                                                               | 24 MHz (HXT) <sup>[2][5]</sup>  | 2.52                   | 2.97                   | 3.10                   | 3.16                    |      |
|                     |                                                               | 12 MHz (HXT) <sup>[2][5]</sup>  | 1.56                   | 2.04                   | 2.13                   | 2.20                    |      |
|                     |                                                               | 4 MHz (HXT) <sup>[2][5]</sup>   | 0.91                   | 1.33                   | 1.39                   | 1.43                    |      |
|                     |                                                               | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.22                   | 0.29                   | 0.32                   | 0.35                    |      |
|                     |                                                               | 32.768 kHz (LXT) <sup>[4]</sup> | 0.24                   | 0.30                   | 0.32                   | 0.35                    |      |
|                     | Normal run mode, executed from Flash, all peripherals enable  | 24 MHz (HIRC) <sup>[1]</sup>    | 3.50                   | 3.78                   | 3.86                   | 3.89                    |      |
|                     |                                                               | 24 MHz (HXT) <sup>[2][5]</sup>  | 3.62                   | 4.11                   | 4.24                   | 4.31                    |      |
|                     |                                                               | 12 MHz (HXT) <sup>[2][5]</sup>  | 2.26                   | 2.74                   | 2.83                   | 2.92                    |      |
|                     |                                                               | 4 MHz (HXT) <sup>[2][5]</sup>   | 1.30                   | 1.74                   | 1.81                   | 1.83                    |      |
|                     |                                                               | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.37                   | 0.57                   | 0.59                   | 0.61                    |      |
|                     |                                                               | 32.768 kHz (LXT) <sup>[4]</sup> | 0.40                   | 0.58                   | 0.60                   | 0.62                    |      |

Notes:  
1. This value base on HIRC enable, HXT disable, LIRC enable, LXT enable  
2. This value base on HIRC disable, HXT enable, LIRC enable, LXT disable  
3. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable  
4. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable

| Symbol                                                                                  | Conditions | Fsys | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|-----------------------------------------------------------------------------------------|------------|------|------------------------|------------------------|------------------------|-------------------------|------|
|                                                                                         |            |      | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| 5. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values    |            |      |                        |                        |                        |                         |      |
| 6. AV <sub>DD</sub> = V <sub>DD</sub> = 3.3V, LVR17 enabled, POR enable and BOD enable. |            |      |                        |                        |                        |                         |      |
| 7. Based on characterization, not tested in production unless otherwise specified.      |            |      |                        |                        |                        |                         |      |

Table 8.2-1 ML51 32KB / 16KB Series Current Consumption In Normal Run Mode

**Low Power Run Mode**

| Symbol                                                                                   | Conditions                                                       | Fsys                            | Typ <sup>[3]</sup>     | Max <sup>[3][4]</sup>  |                        |                         | Unit |
|------------------------------------------------------------------------------------------|------------------------------------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                                                                                          |                                                                  |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_LPRUN</sub>                                                                    | Low power run mode, executed from Flash, all peripherals disable | 38.4 kHz (LIRC) <sup>[1]</sup>  | 15                     | 21                     | 42                     | 66                      | μA   |
|                                                                                          |                                                                  | 32.768 kHz (LXT) <sup>[2]</sup> | 19                     | 23                     | 44                     | 67                      |      |
|                                                                                          | Low power run mode, executed from Flash, all peripherals enable  | 38.4 kHz (LIRC) <sup>[1]</sup>  | 193                    | 307                    | 320                    | 344                     |      |
|                                                                                          |                                                                  | 32.768 kHz (LXT) <sup>[2]</sup> | 194                    | 308                    | 321                    | 345                     |      |
| Notes:                                                                                   |                                                                  |                                 |                        |                        |                        |                         |      |
| 1. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable                |                                                                  |                                 |                        |                        |                        |                         |      |
| 2. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable                 |                                                                  |                                 |                        |                        |                        |                         |      |
| 3. Based on characterization, not tested in production unless otherwise specified.       |                                                                  |                                 |                        |                        |                        |                         |      |
| 4. AV <sub>DD</sub> = V <sub>DD</sub> = 3.3V, LVR17 enabled, POR enable and BOD disable. |                                                                  |                                 |                        |                        |                        |                         |      |

Table 8.2-2 ML51 32KB/16KB Flash Series Current Consumption In Low Power Run Mode

**Idle Mode**

| Symbol               | Conditions                         | Fsys                            | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|----------------------|------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                      |                                    |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_IDLE</sub> | Idle mode, all peripherals disable | 24 MHz (HIRC) <sup>[1]</sup>    | 1.43                   | 1.58                   | 1.62                   | 1.64                    | mA   |
|                      |                                    | 24 MHz (HXT) <sup>[2][5]</sup>  | 1.52                   | 1.91                   | 2.00                   | 2.05                    |      |
|                      |                                    | 12 MHz (HXT) <sup>[2][5]</sup>  | 1.07                   | 1.44                   | 1.50                   | 1.56                    |      |
|                      |                                    | 4 MHz (HXT) <sup>[2][5]</sup>   | 0.76                   | 1.10                   | 1.15                   | 1.19                    |      |
|                      |                                    | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.20                   | 0.30                   | 0.32                   | 0.35                    |      |
|                      |                                    | 32.768 kHz (LXT) <sup>[4]</sup> | 0.22                   | 0.32                   | 0.34                   | 0.36                    |      |
|                      | Idle mode, all peripherals enable  | 24 MHz (HIRC) <sup>[1]</sup>    | 2.46                   | 2.72                   | 2.78                   | 2.80                    |      |
|                      |                                    | 24 MHz (HXT) <sup>[2][5]</sup>  | 2.55                   | 3.04                   | 3.15                   | 3.19                    |      |

| Symbol | Conditions | Fsys                            | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|--------|------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|        |            |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
|        |            | 12 MHz (HXT) <sup>[2][5]</sup>  | 1.67                   | 2.14                   | 2.22                   | 2.26                    |      |
|        |            | 4 MHz (HXT) <sup>[2][5]</sup>   | 1.08                   | 1.51                   | 1.57                   | 1.60                    |      |
|        |            | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.37                   | 0.57                   | 0.60                   | 0.61                    |      |
|        |            | 32.768 kHz (LXT) <sup>[4]</sup> | 0.38                   | 0.59                   | 0.61                   | 0.62                    |      |

Notes:

1. This value base on HIRC enable, HXT disable, LIRC enable, LXT enable
2. This value base on HIRC disable, HXT enable, LIRC enable, LXT disable
3. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable
4. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable
5. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values
6. Based on characterization, not tested in production unless otherwise specified.
7. AV<sub>DD</sub> = V<sub>DD</sub> = 3.3V, LVR17 enabled, POR enable and BOD enable.

Table 8.2-3 ML51 32KB/16KB Flash Series Current Consumption In Idle Mode

#### Low Power Idle Mode

| Symbol                 | Conditions                                                        | Fsys                            | Typ <sup>[3]</sup>     | Max <sup>[3][4]</sup>  |                        |                         | Unit |
|------------------------|-------------------------------------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                        |                                                                   |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_LPIDLE</sub> | Low power idle mode, executed from Flash, all peripherals disable | 38.4 kHz (LIRC) <sup>[1]</sup>  | 13                     | 19                     | 40                     | 63                      | μA   |
|                        |                                                                   | 32.768 kHz (LXT) <sup>[2]</sup> | 15                     | 20                     | 41                     | 65                      |      |
|                        | Low power idle mode, executed from Flash, all peripherals enable  | 38.4 kHz (LIRC) <sup>[1]</sup>  | 173                    | 304                    | 317                    | 341                     |      |
|                        |                                                                   | 32.768 kHz (LXT) <sup>[2]</sup> | 174                    | 306                    | 319                    | 342                     |      |

Notes:

1. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable
2. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable
3. Based on characterization, not tested in production unless otherwise specified.
4. AV<sub>DD</sub> = V<sub>DD</sub> = 3.3V, LVR17 enabled, POR enable and BOD enable.

Table 8.2-4 ML51 32KB/16KB Flash Series Current Consumption In Low Power Idle Mode

Power Down Mode

| Symbol             | Test Conditions                                                      | Typ <sup>[1]</sup>     | Max <sup>[2][3]</sup>  |                        |                         |    | Unit |
|--------------------|----------------------------------------------------------------------|------------------------|------------------------|------------------------|-------------------------|----|------|
|                    |                                                                      | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |    |      |
| I <sub>DD_PD</sub> | Power down mode, all peripherals disable@3.3V                        | 0.8                    | 1.6 <sup>[4]</sup>     | 18                     | 34                      | μA |      |
|                    | Power down mode, all peripherals disable@5.5V                        | 1.6                    | 2.5                    | 25                     | 50                      |    |      |
|                    | Power down mode, LVR enable all other peripherals disable            | 1.4                    | 3.2                    | 19                     | 36                      |    |      |
|                    | Power down mode, LVR enable BOD enable all other peripherals disable | 60                     | 80                     | 70                     | 100                     |    |      |
|                    | Power down mode, WDT / WKT enable all use LIRC, BOD disable          | 2.87                   | 5.2                    | 21                     | 37                      |    |      |
|                    | Power down mode, WDT use LIRC, WKT use LXT, BOD disable              | 2.42                   | 4.2                    | 20                     | 38                      |    |      |

Notes:

1. AV<sub>DD</sub> = V<sub>DD</sub> = 3.3V unless otherwise specified, LVR17 enabled, POR disabled and BOD disabled.

2. Based on characterization, not tested in production unless otherwise specified.

3. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

4. Based on characterization, tested in production.

Table 8.2-5 ML51 32KB/16KB Flash Series Chip Current Consumption in Power down mode

### 8.2.1.2 ML51 64KB Flash/ML54/ML56 Series

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for  $V_{DD} = 1.8V \sim 3.6V$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25^\circ C$  and  $V_{DD} = 3.3V$  unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock  $F_{sys}$ .
- Program run “while (1);” in flash.

### Normal Run Mode

| Symbol              | Conditions                                                    | Fsys                            | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|---------------------|---------------------------------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                     |                                                               |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_RUN</sub> | Normal run mode, executed from Flash, all peripherals disable | 24 MHz (HIRC) <sup>[1]</sup>    | 2.86                   | 3.67                   | 3.92                   | 4.15                    | mA   |
|                     |                                                               | 12 MHz (HIRC) <sup>[1]</sup>    | 1.98                   | 2.37                   | 2.6                    | 2.89                    |      |
|                     |                                                               | 1 MHz (HIRC) <sup>[1]</sup>     | 0.91                   | 1.14                   | 1.2                    | 1.32                    |      |
|                     |                                                               | 24 MHz (HXT) <sup>[2][5]</sup>  | 2.94                   | 3.76                   | 4.02                   | 4.23                    |      |
|                     |                                                               | 12 MHz (HXT) <sup>[2][5]</sup>  | 2.08                   | 2.47                   | 2.7                    | 2.98                    |      |
|                     |                                                               | 1 MHz (HXT) <sup>[2][5]</sup>   | 0.96                   | 1.2                    | 1.3                    | 1.48                    |      |
|                     |                                                               | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.23                   | 0.32                   | 0.34                   | 0.39                    |      |
|                     |                                                               | 32.768 kHz (LXT) <sup>[4]</sup> | 0.25                   | 0.35                   | 0.37                   | 0.42                    |      |
|                     | Normal run mode, executed from Flash, all peripherals enable  | 24 MHz (HIRC) <sup>[1]</sup>    | 4.50                   | 4.78                   | 4.86                   | 4.89                    |      |
|                     |                                                               | 12 MHz (HIRC) <sup>[1]</sup>    | 2.8                    | 3.4                    | 3.6                    | 3.98                    |      |
|                     |                                                               | 1 MHz (HIRC) <sup>[1]</sup>     | 1.17                   | 1.45                   | 1.6                    | 1.75                    |      |
|                     |                                                               | 24 MHz (HXT) <sup>[2][5]</sup>  | 4.9                    | 5.21                   | 5.46                   | 5.89                    |      |
|                     |                                                               | 12 MHz (HXT) <sup>[2][5]</sup>  | 2.67                   | 3.12                   | 3.33                   | 3.69                    |      |
|                     |                                                               | 1 MHz (HXT) <sup>[2][5]</sup>   | 1.21                   | 1.49                   | 1.75                   | 1.83                    |      |
|                     |                                                               | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.41                   | 0.61                   | 0.67                   | 0.72                    |      |
|                     |                                                               | 32.768 kHz (LXT) <sup>[4]</sup> | 0.42                   | 0.62                   | 0.69                   | 0.73                    |      |

Notes:

1. This value base on HIRC enable, HXT disable, LIRC enable, LXT enable

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Conditions | Fsys | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------|------------------------|------------------------|------------------------|-------------------------|------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |      | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| 2. This value base on HIRC disable, HXT enable, LIRC enable, LXT disable<br>3. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable<br>4. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable<br>5. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values<br>6. AV <sub>DD</sub> = V <sub>DD</sub> = 3.3V, LVR17 enabled, POR enable and BOD enable.<br>7. Based on characterization, not tested in production unless otherwise specified. |            |      |                        |                        |                        |                         |      |

Table 8.2-6 ML56/ML54/ML51 64KB Flash Series Current Consumption In Normal Run Mode

**Low Power Run Mode**

| Symbol                                                                             | Conditions                                                       | Fsys                            | Typ <sup>[3]</sup>     | Max <sup>[3][4]</sup>  |                        |                         | Unit |
|------------------------------------------------------------------------------------|------------------------------------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                                                                                    |                                                                  |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_LPRUN</sub>                                                              | Low power run mode, executed from Flash, all peripherals disable | 38.4 kHz (LIRC) <sup>[1]</sup>  | 19                     | 29                     | 52                     | 83                      | μA   |
|                                                                                    |                                                                  | 32.768 kHz (LXT) <sup>[2]</sup> | 21                     | 32                     | 55                     | 85                      |      |
|                                                                                    | Low power run mode, executed from Flash, all peripherals enable  | 38.4 kHz (LIRC) <sup>[1]</sup>  | 223                    | 314                    | 327                    | 351                     |      |
|                                                                                    |                                                                  | 32.768 kHz (LXT) <sup>[2]</sup> | 230                    | 326                    | 339                    | 362                     |      |
| Notes:                                                                             |                                                                  |                                 |                        |                        |                        |                         |      |
| 1. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable          |                                                                  |                                 |                        |                        |                        |                         |      |
| 2. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable           |                                                                  |                                 |                        |                        |                        |                         |      |
| 3. Based on characterization, not tested in production unless otherwise specified. |                                                                  |                                 |                        |                        |                        |                         |      |
| 4. AVDD = VDD = 3.3V, LVR17 enabled, POR enable and BOD disable.                   |                                                                  |                                 |                        |                        |                        |                         |      |

Table 8.2-7 ML56/ML54/ML51 64KB Flash Series Current Consumption In Low Power Run Mode

**Idle Mode**

| Symbol               | Conditions                         | Fsys                            | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|----------------------|------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                      |                                    |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_IDLE</sub> | Idle mode, all peripherals disable | 24 MHz (HIRC) <sup>[1]</sup>    | 1.8                    | 2.25                   | 2.43                   | 2.46                    | mA   |
|                      |                                    | 24 MHz (HXT) <sup>[2][5]</sup>  | 1.74                   | 1.91                   | 2.00                   | 2.05                    |      |
|                      |                                    | 12 MHz (HXT) <sup>[2][5]</sup>  | 1.07                   | 1.44                   | 1.50                   | 1.56                    |      |
|                      |                                    | 4 MHz (HXT) <sup>[2][5]</sup>   | 0.97                   | 1.10                   | 1.15                   | 1.19                    |      |
|                      |                                    | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.20                   | 0.30                   | 0.32                   | 0.35                    |      |
|                      |                                    | 32.768 kHz (LXT) <sup>[4]</sup> | 0.22                   | 0.32                   | 0.34                   | 0.36                    |      |

| Symbol                                                                               | Conditions                        | Fsys                            | Typ <sup>[6]</sup>     | Max <sup>[6][7]</sup>  |                        |                         | Unit |
|--------------------------------------------------------------------------------------|-----------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|------|
|                                                                                      |                                   |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |      |
|                                                                                      | Idle mode, all peripherals enable | 24 MHz (HIRC) <sup>[1]</sup>    | 2.46                   | 2.72                   | 2.78                   | 2.80                    |      |
|                                                                                      |                                   | 24 MHz (HXT) <sup>[2][5]</sup>  | 2.55                   | 3.04                   | 3.15                   | 3.19                    |      |
|                                                                                      |                                   | 12 MHz (HXT) <sup>[2][5]</sup>  | 1.67                   | 2.14                   | 2.22                   | 2.26                    |      |
|                                                                                      |                                   | 4 MHz (HXT) <sup>[2][5]</sup>   | 1.08                   | 1.51                   | 1.57                   | 1.60                    |      |
|                                                                                      |                                   | 38.4 kHz (LIRC) <sup>[3]</sup>  | 0.37                   | 0.57                   | 0.60                   | 0.61                    |      |
|                                                                                      |                                   | 32.768 kHz (LXT) <sup>[4]</sup> | 0.38                   | 0.59                   | 0.61                   | 0.62                    |      |
| Notes:                                                                               |                                   |                                 |                        |                        |                        |                         |      |
| 1. This value base on HIRC enable, HXT disable, LIRC enable, LXT enable              |                                   |                                 |                        |                        |                        |                         |      |
| 2. This value base on HIRC disable, HXT enable, LIRC enable, LXT disable             |                                   |                                 |                        |                        |                        |                         |      |
| 3. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable            |                                   |                                 |                        |                        |                        |                         |      |
| 4. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable             |                                   |                                 |                        |                        |                        |                         |      |
| 5. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values |                                   |                                 |                        |                        |                        |                         |      |
| 6. Based on characterization, not tested in production unless otherwise specified.   |                                   |                                 |                        |                        |                        |                         |      |
| 7. AVDD = VDD = 3.3V, LVR17 enabled, POR enable and BOD enable.                      |                                   |                                 |                        |                        |                        |                         |      |

Table 8.2-8 ML56/ML54/ML51 64KB Flash Series Current Consumption In Idle Mode

#### Low Power Idle Mode

| Symbol                 | Conditions                                                        | Fsys                            | Typ <sup>[3]</sup>     | Max <sup>[3][4]</sup>  |                        |                         |    | Unit |
|------------------------|-------------------------------------------------------------------|---------------------------------|------------------------|------------------------|------------------------|-------------------------|----|------|
|                        |                                                                   |                                 | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 85 °C | T <sub>A</sub> = 105 °C |    |      |
| I <sub>DD_LPIDLE</sub> | Low power idle mode, executed from Flash, all peripherals disable | 38.4 kHz (LIRC) <sup>[1]</sup>  | 17                     | 27                     | 50                     | 81                      | μA |      |
|                        |                                                                   | 32.768 kHz (LXT) <sup>[2]</sup> | 22                     | 32                     | 55                     | 87                      |    |      |
|                        | Low power idle mode, executed from Flash, all peripherals enable  | 38.4 kHz (LIRC) <sup>[1]</sup>  | 213                    | 302                    | 317                    | 340                     |    |      |
|                        |                                                                   | 32.768 kHz (LXT) <sup>[2]</sup> | 220                    | 312                    | 320                    | 342                     |    |      |

Notes:

5. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable

6. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable

7. Based on characterization, not tested in production unless otherwise specified.

8. AV<sub>DD</sub> = V<sub>DD</sub> = 3.3V , LVR17 enabled, POR enable and BOD enable.

Table 8.2-9 ML56/ML54/ML51 64KB Flash Series Current consumption in Low Power Idle mode

#### Power Down Mode

| Symbol | Test Conditions                               | Typ <sup>[1]</sup> | Max <sup>[2][3]</sup> |            |             | Unit |
|--------|-----------------------------------------------|--------------------|-----------------------|------------|-------------|------|
|        |                                               | TA = 25 °C         | TA = 25 °C            | TA = 85 °C | TA = 105 °C |      |
| IDD_PD | Power down mode, all peripherals disable@3.3V | 1.2                | 1.6 <sup>[4]</sup>    | 20         | 37          | μA   |
|        | Power down mode, all peripherals disable@5.5V | 1.7                | 2.6                   | 27         | 47          |      |

| Symbol                                                                                                                                                                                                                                                                                                                                                                              | Test Conditions                                                                       | Typ <sup>[1]</sup> | Max <sup>[2][3]</sup> |            |             | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|--------------------|-----------------------|------------|-------------|------|
|                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                       | TA = 25 °C         | TA = 25 °C            | TA = 85 °C | TA = 105 °C |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power down mode, LVR enable all other peripherals disable                             | 1.7                | 3.2                   | 25         | 42          |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power down mode, LVR enable, Low power BOD enable all other peripherals disable       | 4.8                | 10                    | 52         | 69          |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power down mode, LVR enable BOD enable all other peripherals disable                  | 61                 | 82                    | 98         | 110         |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power down mode, WDT / WKT enable all use LIRC, BOD disable                           | 3                  | 6.4                   | 44         | 52          |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power down mode, WDT use LIRC, WKT use LXT, BOD disable                               | 3.5                | 7.2                   | 48         | 68          |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power-down mode, RTC use LIRC, BOD disable, HIRC off / HXT off / LIRC on / LXT off    | 2.9                | 5.9                   | 32         | 49          |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power-down mode, RTC/TK use LIRC, BOD disable, HIRC off / HXT off / LIRC on / LXT off | 3.4                | 6.8                   | 42         | 56          |      |
|                                                                                                                                                                                                                                                                                                                                                                                     | Power-down mode, RTC use LXT, BOD disable, HIRC off / HXT off / LIRC off / LXT on     | 3.9                | 7.3                   | 48         | 77          |      |
| <b>Notes:</b><br>1. AVDD = VDD = 3.3V unless otherwise specified, LVR17 enabled, POR disabled and BOD disabled.<br>2. Based on characterization, not tested in production unless otherwise specified.<br>3. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.<br>4. Based on characterization, tested in production. |                                                                                       |                    |                       |            |             |      |

Table 8.2-10 ML56/ML54/ML51 64KB Flash Series Chip Current Consumption In Power Down Mode

**8.2.2 On-Chip Peripheral Current Consumption**

- The typical values for  $T_A = 25\text{ }^{\circ}\text{C}$  and  $V_{DD} = AV_{DD} = 3.3\text{ V}$  unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- The system clock = 24 MHz.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

| Peripheral           | I <sub>DD</sub> Base | I <sub>DD</sub> <sup>[1]</sup> | Unit |
|----------------------|----------------------|--------------------------------|------|
| ADC <sup>[2]</sup>   | 309.2                |                                | μA   |
| ACMP0 <sup>[3]</sup> | 1.0                  |                                |      |
| ACMP1 <sup>[3]</sup> | 1.1                  |                                |      |
| PWM0                 | 152.3                |                                |      |
| SPI0                 | 40.2                 |                                |      |
| SPI1                 | 44.2                 |                                |      |
| UART0                | 98.8                 | 1                              |      |
| UART1                |                      | 1                              |      |
| I2C0                 | 118.7                | 1                              |      |
| I2C1                 |                      | 1                              |      |
| SC0                  | 67.8                 |                                |      |
| PIN Interrupt        | 0.2                  |                                |      |
| TIMER 0              | 145                  | 4.1                            |      |
| TIMER 1              |                      | 3.9                            |      |
| TIMER 2              |                      | 4.4                            |      |
| TIMER 3              |                      | 10                             |      |
| INT0                 | 0.3                  |                                |      |
| INT1                 | 0.3                  |                                |      |
| WDT                  | 0.4                  |                                |      |
| WKT                  | 0.7                  |                                |      |
| PDMA0                | 13.4                 | 0.5                            |      |
| PDMA1                |                      | 0.5                            |      |
| PDMA2                |                      | 0.5                            |      |
| PDMA3                |                      | 0.5                            |      |
| CAPTURE0             | 145                  | 0.5                            |      |
| CAPTURE1             |                      | 0.3                            |      |
| CAPTURE2             |                      | 0.5                            |      |
| RTC                  | 1                    |                                |      |
| LCD                  | 23                   |                                |      |

| Peripheral                                                                                                                                                                                                                                                                           | I <sub>DD</sub> Base | I <sub>DD</sub> <sup>[1]</sup> | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------------------------|------|
| Notes:<br>1. Guaranteed by characterization results, not tested in production.<br>2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.<br>3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part. |                      |                                |      |

Table 8.2-11 Peripheral Current Consumption

### 8.2.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-12 Low-Power Mode Wakeup Timings is measured on a wakeup phase with a 24 MHz HIRC oscillator.

| Symbol                                | Parameter                   |                                       | Typ | Max  | Unit   |
|---------------------------------------|-----------------------------|---------------------------------------|-----|------|--------|
| t <sub>WU_IDLE</sub>                  | Wakeup from IDLE mode       |                                       | 5   | 6    | cycles |
| t <sub>WU_NPD</sub> <sup>[1][2]</sup> | Wakeup from Power down mode | Fsys = HIRC @5.5V                     | 7   | 20   | μs     |
|                                       |                             | Fsys = HIRC @3.6V                     | 10  | 20   | μs     |
|                                       |                             | Fsys = HIRC @1.8V                     | 13  | 20   | μs     |
|                                       |                             | Fsys = HXT@24MHz @5.5V <sup>[3]</sup> | 370 | -    | μs     |
|                                       |                             | Fsys = HXT@24MHz @3.6V <sup>[3]</sup> | 440 | -    |        |
|                                       |                             | Fsys = HXT@24MHz @1.8V <sup>[3]</sup> | 600 | -    | μs     |
|                                       |                             | Fsys = LIRC                           | 938 | 1500 | μs     |
|                                       |                             | Fsys = LXT@32.768KHz <sup>[4]</sup>   | 860 | -    | μs     |

Notes:

1. Based on test during characterization, not tested in production.

2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

3. Value variable based on extnerl Crystal stable time.

4 Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values, LXT not disabled when ML51/ML54/ML56 Series into Power down mode.

Table 8.2-12 Low-Power Mode Wakeup Timings

## 8.2.4 I/O DC Characteristics

### 8.2.4.1 GPIO Input Characteristics

| Symbol                             | Parameter                                                   | Min                     | Typ                 | Max                     | Unit | Test Conditions                                                                        |
|------------------------------------|-------------------------------------------------------------|-------------------------|---------------------|-------------------------|------|----------------------------------------------------------------------------------------|
| V <sub>IL</sub>                    | Input low voltage                                           | 0                       | -                   | 0.3*V <sub>DD</sub>     | V    |                                                                                        |
| V <sub>IL1</sub>                   | Input low voltage (I/O with TTL input)                      | V <sub>SS</sub> -0.3    | -                   | 0.2V <sub>DD</sub> -0.1 | V    |                                                                                        |
| V <sub>IH</sub>                    | Input high voltage                                          | 0.2V <sub>DD</sub> +0.9 | -                   | V <sub>DD</sub> +0.3    | V    |                                                                                        |
| V <sub>IH1</sub>                   | Input high voltage (I/O with Schmitt trigger input and Xin) | 0.7*V <sub>DD</sub>     | -                   | V <sub>DD</sub>         | V    |                                                                                        |
| V <sub>HY</sub> <sup>[1]</sup>     | Hysteresis voltage of schmitt input                         | -                       | 0.2*V <sub>DD</sub> | -                       | V    |                                                                                        |
| I <sub>LK</sub> <sup>[2]</sup>     | Input leakage current                                       | -1                      |                     | 1                       | μA   | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub> ,<br>Open-drain or input only mode |
|                                    |                                                             | -1                      |                     | 1                       |      | V <sub>DD</sub> < V <sub>IN</sub> < 5.5 V,<br>Open-drain or input only mode            |
| R <sub>PU</sub> <sup>[1] [3]</sup> | Pull up resistor                                            | 40                      | -                   | 60                      | kΩ   | V <sub>DD</sub> = 5.5 V, Quasi mode and Input mode with pull up enable                 |
|                                    |                                                             | 40                      | -                   | 60                      |      | V <sub>DD</sub> = 3.3 V, Quasi mode and Input mode with pull up enable                 |
|                                    |                                                             | 40                      | -                   | 70                      |      | V <sub>DD</sub> = 1.8 V, Quasi mode and Input mode pull up enable                      |
| R <sub>PD</sub> <sup>[1] [3]</sup> | Pull down resistor                                          | 40                      | -                   | 60                      | kΩ   | V <sub>DD</sub> = 5.5 V, Quasi mode and Input mode with pull up enable                 |
|                                    |                                                             | 40                      | -                   | 60                      |      | V <sub>DD</sub> = 3.3 V, Quasi mode and Input mode with pull up enable                 |
|                                    |                                                             | 40                      | -                   | 70                      |      | V <sub>DD</sub> = 1.8 V, Quasi mode and Input mode pull up enable                      |

Notes:

1.

Guaranteed by characterization result, not tested in production.

2.

Leakage could be higher than the maximum value, if abnormal injection happens.

3.

To sustain a voltage higher than V<sub>DD</sub> +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

4.

Test condition of V<sub>DD</sub> is base on the maximum value of V<sub>DD</sub>

Table 8.2-13 GPIO input characteristics

#### 8.2.4.2 GPIO Output Characteristics

The minimum and maximum values are obtained for  $V_{DD} = 1.8V \sim 5V$  for ML56/ML54/ML51 64KB Flash series and  $V_{DD} = 1.8V \sim 5.5V$  for ML51 32KB/16KB Flash series ML and temperature condition is  $T_A = 25^\circ C$  unless otherwise specified.

| Symbol            | Parameter                                                  | Min            | Typ | Max      | Unit    | Test Conditions                               |
|-------------------|------------------------------------------------------------|----------------|-----|----------|---------|-----------------------------------------------|
| $I_{SR}^{[1][2]}$ | Source current for quasi-bidirectional mode and high level | -7.4           | -   | -7.5     | $\mu A$ | $V_{DD} = 5.5V$<br>$V_{IN} = (V_{DD} - 0.4)V$ |
|                   |                                                            | -7.3           | -   | -7.5     | $\mu A$ | $V_{DD} = 3.3V$<br>$V_{IN} = (V_{DD} - 0.4)V$ |
|                   |                                                            | -7.3           | -   | -7.5     | $\mu A$ | $V_{DD} = 2.4V$<br>$V_{IN} = (V_{DD} - 0.4)V$ |
|                   |                                                            | -57.2          | -   | -58.3    | $\mu A$ | $V_{DD} = 5.5V$<br>$V_{IN} = 2.4V$            |
|                   | Source current for push-pull mode and high level           | -9             | -   | -9.6     | mA      | $V_{DD} = 5.5V$<br>$V_{IN} = (V_{DD} - 0.4)V$ |
|                   |                                                            | -6             | -   | -6.6     | mA      | $V_{DD} = 3.3V$<br>$V_{IN} = (V_{DD} - 0.4)V$ |
|                   |                                                            | -4.2           | -   | -4.9     | mA      | $V_{DD} = 2.7V$<br>$V_{IN} = (V_{DD} - 0.4)V$ |
|                   |                                                            | -18            | -   | -20      | mA      | $V_{DD} = 5.5V$<br>$V_{IN} = 2.4V$            |
| $I_{SK}^{[1][2]}$ | Sink current for push-pull mode and low level              | 18             | -   | 20       | mA      | $V_{DD} = 5.5V$<br>$V_{IN} = 0.4V$            |
|                   |                                                            | 16             | -   | 18       | mA      | $V_{DD} = 3.3V$<br>$V_{IN} = 0.4V$            |
|                   |                                                            | 9.7            | -   | 12.5     | mA      | $V_{DD} = 2.4V$<br>$V_{IN} = 0.4V$            |
| $V_{OH}^{[1]}$    | Output high level voltage for quasi-bidirectional mode     | $V_{DD} - 0.4$ | -   | $V_{DD}$ | V       | $I_{SR} = -7.3\mu A$                          |
|                   | Output high level voltage for push-pull mode               | $V_{DD} - 1.2$ | -   | $V_{DD}$ | V       | $V_{DD} \geq 4.5V$<br>$I_{SR} = -20mA$        |
|                   |                                                            |                |     |          | V       | $V_{DD} \geq 3.3V$<br>$I_{SR} = -13mA$        |
|                   |                                                            |                |     |          | V       | $V_{DD} \geq 2.7V$<br>$I_{SR} = -9mA$         |
|                   |                                                            | $V_{DD} - 0.4$ | -   | $V_{DD}$ | V       | $V_{DD} \geq 4.5V$<br>$I_{SR} = -9mA$         |
|                   |                                                            |                |     |          | V       | $V_{DD} \geq 3.3V$<br>$I_{SR} = -6mA$         |
|                   |                                                            |                |     |          | V       | $V_{DD} \geq 2.7V$<br>$I_{SR} = -4.2mA$       |

| Symbol                                                                                                                                                                                                                                                      | Parameter                                   | Min      | Typ | Max | Unit | Test Conditions                                              |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|----------|-----|-----|------|--------------------------------------------------------------|
| $V_{OL}^{[1]}$                                                                                                                                                                                                                                              | Output low level voltage for push-pull mode | $V_{SS}$ | -   | 1.2 | V    | $V_{DD} \geq 2.7\text{ V}$<br>$I_{SR} = 20\text{ mA (Max.)}$ |
|                                                                                                                                                                                                                                                             |                                             | $V_{SS}$ | -   | 0.4 | V    | $V_{DD} \geq 5.5\text{ V}$<br>$I_{SR} = 18\text{ mA}$        |
|                                                                                                                                                                                                                                                             |                                             |          |     |     | V    | $V_{DD} \geq 3.3\text{ V}$<br>$I_{SR} = 16\text{ mA}$        |
|                                                                                                                                                                                                                                                             |                                             |          |     |     | V    | $V_{DD} \geq 2.4\text{ V}$<br>$I_{SR} = 9.7\text{ mA}$       |
| $C_{IO}^{[1]}$                                                                                                                                                                                                                                              | I/O pin capacitance                         | -        | 5   | -   | pF   |                                                              |
| Notes:<br>1. Guaranteed by characterization result, not tested in production.<br>2. The $I_{SR}$ and $I_{SK}$ must always respect the absolute maximum current and the sum of I/O, CPU and peripheral must not exceed $\Sigma I_{DD}$ and $\Sigma I_{SS}$ . |                                             |          |     |     |      |                                                              |

Table 8.2-14 GPIO output characteristics

8.2.4.3 nRESET Pin Input Characteristics

| Symbol                                                                                            | Parameter                        | Min                 | Typ | Max                 | Unit | Test Conditions          |
|---------------------------------------------------------------------------------------------------|----------------------------------|---------------------|-----|---------------------|------|--------------------------|
| V <sub>ILR</sub>                                                                                  | Negative going threshold, nRESET | -                   | -   | 0.3*V <sub>DD</sub> | V    |                          |
| V <sub>IHR</sub>                                                                                  | Positive going threshold, nRESET | 0.7*V <sub>DD</sub> | -   | -                   | V    |                          |
| R <sub>RST</sub> <sup>[1]</sup>                                                                   | Internal nRESET pull up resistor | 45                  | -   | 60                  | KΩ   | V <sub>DD</sub> = 5.5 V  |
|                                                                                                   |                                  |                     |     |                     |      | V <sub>DD</sub> = 3.6 V  |
|                                                                                                   |                                  | 50                  | -   | 65                  |      | V <sub>DD</sub> = 1.8 V  |
| t <sub>FR</sub> <sup>[1]</sup>                                                                    | nRESET input response time       | -                   | 1.5 | -                   | μs   | Normal run and Idle mode |
|                                                                                                   |                                  | 10                  | -   | 25                  |      | Power-down mode          |
| Notes:                                                                                            |                                  |                     |     |                     |      |                          |
| 1. Guaranteed by characterization result, not tested in production.                               |                                  |                     |     |                     |      |                          |
| 2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable. |                                  |                     |     |                     |      |                          |

Table 8.2-15 nRESET Pin Input Characteristics

### 8.3 AC Electrical Characteristics

The maximum values are obtained for  $V_{DD} = 1.8 \text{ V} \sim 5.5 \text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.3 \text{ V}$  unless otherwise specified.  $V_{DD} = AV_{DD}$ .

#### 8.3.1 24 MHz Internal High Speed RC Oscillator (HIRC)

The 24 MHz RC oscillator is calibrated in production.

| Symbol.                                                                                                                                                          | Parameter                                    | Min               | Typ | Max              | Unit          | Test Conditions                                                                        |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|-------------------|-----|------------------|---------------|----------------------------------------------------------------------------------------|
| $V_{DD}$                                                                                                                                                         | Operating voltage                            | 1.8               | -   | 5.5              | V             |                                                                                        |
| $F_{HIRC}$                                                                                                                                                       | Oscillator frequency                         | 23.76             | 24  | 24.24            | MHz           | $T_A = 25^\circ\text{C}$ ,<br>$V_{DD} = 5\text{V}$                                     |
|                                                                                                                                                                  | Frequency drift over temperature and voltage | -1 <sup>[1]</sup> | -   | 1 <sup>[1]</sup> | %             | $T_A = 25^\circ\text{C}$ ,<br>$V_{DD} = 3.3\text{V}$                                   |
|                                                                                                                                                                  |                                              | -2 <sup>[2]</sup> | -   | 2 <sup>[2]</sup> | %             | $T_A = -20^\circ\text{C} \sim +105^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 5.5\text{V}$ |
|                                                                                                                                                                  |                                              | -5 <sup>[2]</sup> |     | 5 <sup>[2]</sup> | %             | $T_A = -40^\circ\text{C} \sim -20^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 5.5\text{V}$  |
| $I_{HIRC}^{[2]}$                                                                                                                                                 | Operating current                            | -                 | 490 | 550              | $\mu\text{A}$ |                                                                                        |
| $T_S^{[3]}$                                                                                                                                                      | Stable time                                  | -                 | 3   | 5                | $\mu\text{s}$ | $T_A = -40^\circ\text{C} \sim +105^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 5.5\text{V}$ |
| Notes:<br>1. Based on characterization, tested in production.<br>2. Guaranteed by characterization result, not tested in production.<br>3. Guaranteed by design. |                                              |                   |     |                  |               |                                                                                        |

Table 8.3-1 24 MHz Internal High Speed RC Oscillator(HIRC) Characteristic

### 8.3.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

| Symbol                                                                                                                                                                                                                               | Parameter                                    | Min                | Typ  | Max               | Unit          | Test Conditions                                                                                                       |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|--------------------|------|-------------------|---------------|-----------------------------------------------------------------------------------------------------------------------|
| $V_{DD}$                                                                                                                                                                                                                             | Operating voltage                            | 1.8                | -    | 5.5               | V             |                                                                                                                       |
| $F_{LRC}$                                                                                                                                                                                                                            | Oscillator frequency                         | -                  | 38.4 | -                 | kHz           |                                                                                                                       |
|                                                                                                                                                                                                                                      | Frequency drift over temperature and voltage | -2 <sup>[1]</sup>  | -    | 2 <sup>[1]</sup>  | %             | $T_A = 25\text{ }^{\circ}\text{C}$ ,<br>$V_{DD} = 5\text{V}$                                                          |
|                                                                                                                                                                                                                                      |                                              | -10 <sup>[2]</sup> | -    | 10 <sup>[2]</sup> | %             | $T_A = -40\sim 105\text{ }^{\circ}\text{C}$<br>$V_{DD} = 1.8\text{V}\sim 5.5\text{V}$<br>Without software calibration |
| $I_{LRC}^{[2]}$                                                                                                                                                                                                                      | Operating current                            | -                  | 0.85 | 1                 | $\mu\text{A}$ | $V_{DD} = 3.3\text{V}$                                                                                                |
| $T_S$                                                                                                                                                                                                                                | Stable time                                  | -                  | 500  | -                 | $\mu\text{s}$ | $T_A = -40\sim 105\text{ }^{\circ}\text{C}$<br>$V_{DD} = 1.8\text{V}\sim 5.5\text{V}$                                 |
| Notes:<br>1. Guaranteed by characterization, tested in production.<br>2. Guaranteed by characterization, not tested in production.<br>3. The 38.4 kHz low speed RC oscillator can be calibrated by user.<br>4. Guaranteed by design. |                                              |                    |      |                   |               |                                                                                                                       |

Table 8.3-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

### 8.3.3 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this section are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1\_IN and XT1\_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

| Symbol                                                                                                                                                                           | Parameter                  | Min <sup>[1]</sup> | Typ  | Max <sup>[1]</sup> | Unit | Test Conditions <sup>[2]</sup> |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|--------------------|------|--------------------|------|--------------------------------|
| V <sub>DD</sub>                                                                                                                                                                  | Operating voltage          | 1.8                | -    | 5.5                | V    |                                |
| R <sub>f</sub>                                                                                                                                                                   | Internal feedback resistor | -                  | 500  | -                  | kΩ   |                                |
| f <sub>HXT</sub>                                                                                                                                                                 | Oscillator frequency       | 4                  | -    | 24                 | MHz  |                                |
| I <sub>HXT</sub>                                                                                                                                                                 | Current consumption        | -                  | 80   | 180                | μA   | 4 MHz, Gain = L0               |
|                                                                                                                                                                                  |                            | -                  | 110  | 300                |      | 8 MHz, Gain = L1               |
|                                                                                                                                                                                  |                            | -                  | 180  | 500                |      | 12 MHz, Gain = L2              |
|                                                                                                                                                                                  |                            | -                  | 230  | 650                |      | 16 MHz, Gain = L3              |
|                                                                                                                                                                                  |                            | -                  | 360  | 975                |      | 24 MHz, Gain = L4              |
| T <sub>S</sub>                                                                                                                                                                   | Stable time <sup>[3]</sup> | -                  | 3500 | -                  | μs   | 4 MHz, Gain = L0               |
|                                                                                                                                                                                  |                            | -                  | 950  | -                  |      | 8 MHz, Gain = L1               |
|                                                                                                                                                                                  |                            | -                  | 700  | -                  |      | 12 MHz, Gain = L2              |
|                                                                                                                                                                                  |                            | -                  | 450  | -                  |      | 16 MHz, Gain = L3              |
|                                                                                                                                                                                  |                            | -                  | 400  | -                  |      | 24 MHz, Gain = L4              |
| D <sub>U<sub>HXT</sub></sub>                                                                                                                                                     | Duty cycle                 | 40                 | -    | 60                 | %    |                                |
| Notes:<br>1. Guaranteed by characterization, not tested in production.<br>2. L0 ~ L4 defined by SFR_XLTCON[6:4]_HXSG<br>3. Value variable based on external Crystal stable time. |                            |                    |      |                    |      |                                |

Table 8.3-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

#### Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

| CRYSTAL        | C1         | C2         | R1      |
|----------------|------------|------------|---------|
| 4 MHz ~ 24 MHz | 10 ~ 25 pF | 10 ~ 25 pF | without |

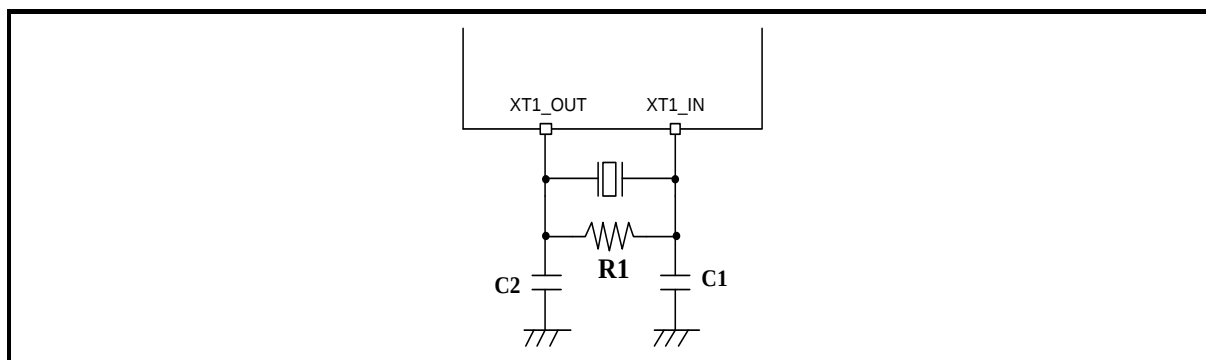


Table 8.3-4 Typical Crystal Application

### 8.3.4 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1\_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a waveform generator.

| Symbol                | Parameter                            | Min <sup>[1]</sup>        | Typ | Max <sup>[1]</sup>        | Unit | Test Conditions                         |
|-----------------------|--------------------------------------|---------------------------|-----|---------------------------|------|-----------------------------------------|
| $f_{\text{HXT\_ext}}$ | External user clock source frequency | 4                         | -   | 24                        | MHz  |                                         |
| $t_{\text{CHCX}}$     | Clock high time                      | 8                         | -   | -                         | ns   |                                         |
| $t_{\text{CLCX}}$     | Clock low time                       | 8                         | -   | -                         | ns   |                                         |
| $t_{\text{CLCH}}$     | Clock rise time                      | -                         | -   | 10                        | ns   | Low (10%) to high level (90%) rise time |
| $t_{\text{CHCL}}$     | Clock fall time                      | -                         | -   | 10                        | ns   | High (90%) to low level (10%) fall time |
| $Du_{\text{E\_HXT}}$  | Duty cycle                           | 40                        | -   | 60                        | %    |                                         |
| $V_{\text{IH}}$       | Input high voltage                   | $0.7 \cdot V_{\text{DD}}$ | -   | $V_{\text{DD}}$           | V    |                                         |
| $V_{\text{IL}}$       | Input low voltage                    | $V_{\text{SS}}$           | -   | $0.3 \cdot V_{\text{DD}}$ | V    |                                         |

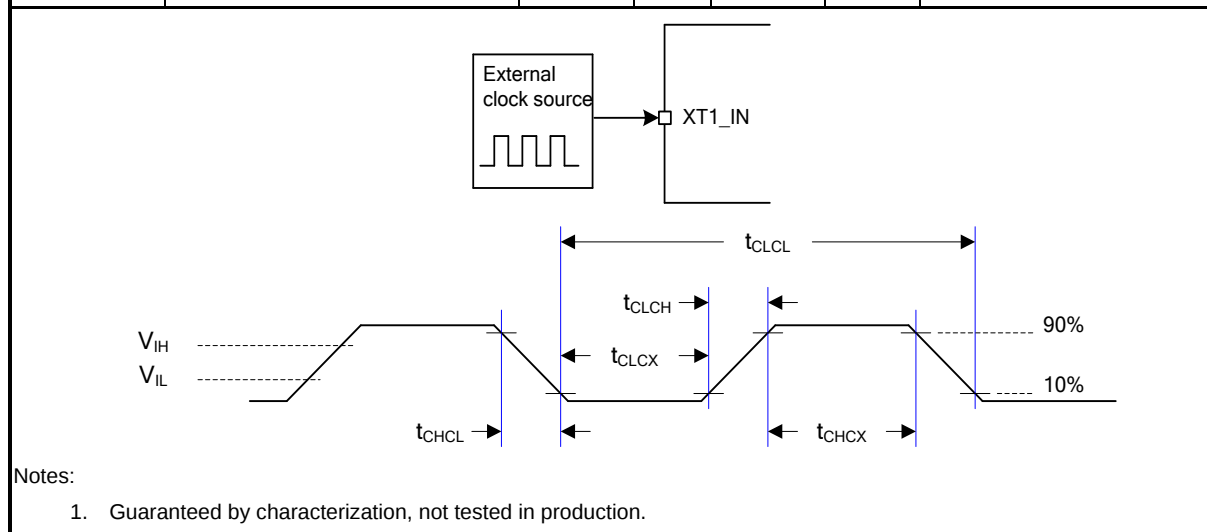


Table 8.3-5 External 4~24 MHz High Speed Clock Input Signal

### 8.3.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this section are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32\_OUT and X32\_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

| Symbol                       | Parameter                        | Min <sup>[1]</sup> | Typ | Max <sup>[1]</sup> | Unit | Test Conditions <sup>[2]</sup> |
|------------------------------|----------------------------------|--------------------|-----|--------------------|------|--------------------------------|
| V <sub>DD</sub>              | Operation voltage                | 1.8                | -   | 5.5                | V    |                                |
| T <sub>LXT</sub>             | Temperature range                | -40                | -   | 105                | °C   |                                |
| R <sub>f</sub>               | Internal feedback resistor       | -                  | 6   | -                  | MΩ   |                                |
| F <sub>LXT</sub>             | Oscillator frequency             | 32.768             |     |                    | kHz  |                                |
| I <sub>LXT</sub>             | Current consumption              | -                  | 1.3 | 3.7                | μA   | ESR=35 kΩ, Gain = L2           |
|                              |                                  | -                  | 1.6 | 6                  |      | ESR=70 kΩ, Gain = L3           |
| T <sub>S<sub>LXT</sub></sub> | Stable time <sup>[3]</sup>       | -                  | 2   | -                  | s    |                                |
| D <sub>u<sub>LXT</sub></sub> | Duty cycle                       | 30                 | -   | 70                 | %    |                                |
| R <sub>s</sub>               | Equivalent Series Resistor (ESR) | -                  | 35  | 70                 | kΩ   | Crystal @32.768 kHz            |

Notes:

1. Guaranteed by characterization, not tested in production.
2. L1 ~ L2 defined by SFR XLTCN[1:0] LXSG
3. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values, Value variable based on external Crystal stable time.

Table 8.3-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator Characteristics

#### Typical Crystal Application Circuits

| CRYSTAL                 | C1    | C2    | R1      |
|-------------------------|-------|-------|---------|
| 32.768 kHz, ESR < 70 kΩ | 20 pF | 20 pF | without |

Table 8.3-7 Typical 32.768 kHz Crystal Application Circuit

### 8.3.6 I/O AC Characteristics

| Symbol                  | Parameter                                                                            | Typ. | Max <sup>[1]</sup> | Unit | Test Conditions <sup>[2]</sup>                                                        |
|-------------------------|--------------------------------------------------------------------------------------|------|--------------------|------|---------------------------------------------------------------------------------------|
| $t_{r(I/O)out}$         | Normal mode <sup>[4]</sup> output high (90%) to low level (10%) falling time         | 4.6  | 5.1                | ns   | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 2.9  | 3.3                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 6.6  | 8                  |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 4.3  | 5                  |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 8.5  | 12.5               |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
|                         |                                                                                      | 8.0  | 10.7               |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
| $t_{f(I/O)out}$         | High slew rate mode <sup>[5]</sup> output high (90%) to low level (10%) falling time | 4.0  | 4.3                | ns   | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 2.1  | 2.5                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 4.9  | 5.8                |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 3.0  | 3.7                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 9.5  | 13.8               |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
|                         |                                                                                      | 5.4  | 7.4                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
| $t_{r(I/O)out}$         | Normal mode <sup>[4]</sup> output low (10%) to high level (90%) rising time          | 5.6  | 6.1                | ns   | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 3.4  | 3.7                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 8.1  | 9.4                |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 5.1  | 5.8                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 15.1 | 20.3               |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
|                         |                                                                                      | 9.6  | 12.4               |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
| $t_{f(I/O)out}$         | High slew rate mode <sup>[5]</sup> output low (10%) to high level (90%) rising time  | 4.8  | 5.2                | ns   | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 2.1  | 2.5                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 5.5 \text{ V}$                                   |
|                         |                                                                                      | 6.4  | 7.4                |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 3.0  | 3.7                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 3.3 \text{ V}$                                   |
|                         |                                                                                      | 12.7 | 16.9               |      | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
|                         |                                                                                      | 5.4  | 7.4                |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
| $f_{max(I/O)out}^{[3]}$ | I/O maximum frequency                                                                | 24   | 24                 | MHz  | $C_L = 30 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
|                         |                                                                                      |      |                    |      | $C_L = 10 \text{ pF}$ , $V_{DD} \geq 1.8 \text{ V}$                                   |
| $I_{DIO}^{[6]}$         | I/O dynamic current consumption                                                      | 2.77 | -                  | mA   | $C_L = 30 \text{ pF}$ , $V_{DD} = 3.3 \text{ V}$ ,<br>$f_{(I/O)out} = 24 \text{ MHz}$ |
|                         |                                                                                      | 1.19 | -                  |      | $C_L = 10 \text{ pF}$ , $V_{DD} = 3.3 \text{ V}$ ,<br>$f_{(I/O)out} = 24 \text{ MHz}$ |
|                         |                                                                                      | 0.69 | -                  |      | $C_L = 30 \text{ pF}$ , $V_{DD} = 3.3 \text{ V}$ ,<br>$f_{(I/O)out} = 6 \text{ MHz}$  |
|                         |                                                                                      | 0.3  | -                  |      | $C_L = 10 \text{ pF}$ , $V_{DD} = 3.3 \text{ V}$ ,<br>$f_{(I/O)out} = 6 \text{ MHz}$  |

|                                                                                                             |
|-------------------------------------------------------------------------------------------------------------|
| Notes:                                                                                                      |
| 1. Guaranteed by characterization result, not tested in production.                                         |
| 2. C <sub>L</sub> is a external capacitive load to simulate PCB and device loading.                         |
| 3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$ .                         |
| 4. PxSR.n bit value = 0, Normal output slew rate                                                            |
| 5. PxSR.n bit value = 1, high speed output slew rate                                                        |
| 6. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$ |

Table 8.3-8 I/O AC characteristics

## 8.4 Analog Characteristics

### 8.4.1 Reset and Power Control Block Characteristics

The maximum values are obtained for  $V_{DD} = 1.8V \sim 5.5V$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25^\circ C$  and  $V_{DD} = 3.3V$ . The parameters in below table are derived from tests performed under ambient temperature unless otherwise specified.

| Symbol                                                       | Parameter                                | Min  | Typ  | Max  | Unit | Test Conditions         |
|--------------------------------------------------------------|------------------------------------------|------|------|------|------|-------------------------|
| I <sub>POR</sub> <sup>[1]</sup>                              | POR Operating Current                    | -    | 60   | 100  | μA   | AV <sub>DD</sub> = 5.5V |
| I <sub>LVR</sub> <sup>[1]</sup>                              | LVR Operating Current                    | -    | 30   | 80   |      | AV <sub>DD</sub> = 5.5V |
|                                                              | LVR Low Power Run Mode Operating Current |      | 0.5  | 1    |      | AV <sub>DD</sub> = 5.5V |
| I <sub>BOD</sub> <sup>[1]</sup>                              | BOD Operating Current                    | -    | 0.5  | 2.9  |      | AV <sub>DD</sub> = 5.5V |
| V <sub>POR</sub>                                             | POR Reset Voltage                        | 1.45 | 1.55 | 1.65 | V    | -                       |
| V <sub>LVR</sub>                                             | LVR Reset Voltage                        | 1.55 | 1.63 | 1.70 |      | -                       |
| V <sub>BOD</sub>                                             | BOD Brown-Out Detect Voltage             | 1.7  | 1.8  | 2    |      |                         |
|                                                              |                                          | 1.9  | 2    | 2.2  |      |                         |
|                                                              |                                          | 2.3  | 2.4  | 2.5  |      |                         |
|                                                              |                                          | 2.55 | 2.7  | 2.8  |      |                         |
|                                                              |                                          | 2.85 | 3    | 3.2  |      |                         |
|                                                              |                                          | 3.55 | 3.7  | 3.9  |      |                         |
|                                                              |                                          | 4.2  | 4.4  | 4.5  |      |                         |
| T <sub>LVR_SU</sub> <sup>[1]</sup>                           | LVR Startup Time                         | -    | 1    | 2    | μs   | -                       |
| T <sub>LVR_RE</sub> <sup>[1]</sup>                           | LVR Respond Time                         | -    | 15   | 20   |      | -                       |
|                                                              | LVR Low Power Run Mode Respond Time      | -    | 20   | 30   |      | -                       |
| T <sub>BOD_SU</sub> <sup>[1]</sup>                           | BOD Startup Time                         | -    | 250  | 350  |      | -                       |
| T <sub>BOD_RE</sub> <sup>[1]</sup>                           | BOD Respond Time                         | -    | 19   | 30   |      | -                       |
| Notes:                                                       |                                          |      |      |      |      |                         |
| 1. Guaranteed by characterization, not tested in production. |                                          |      |      |      |      |                         |
| 2. Design for specified applicaiton.                         |                                          |      |      |      |      |                         |

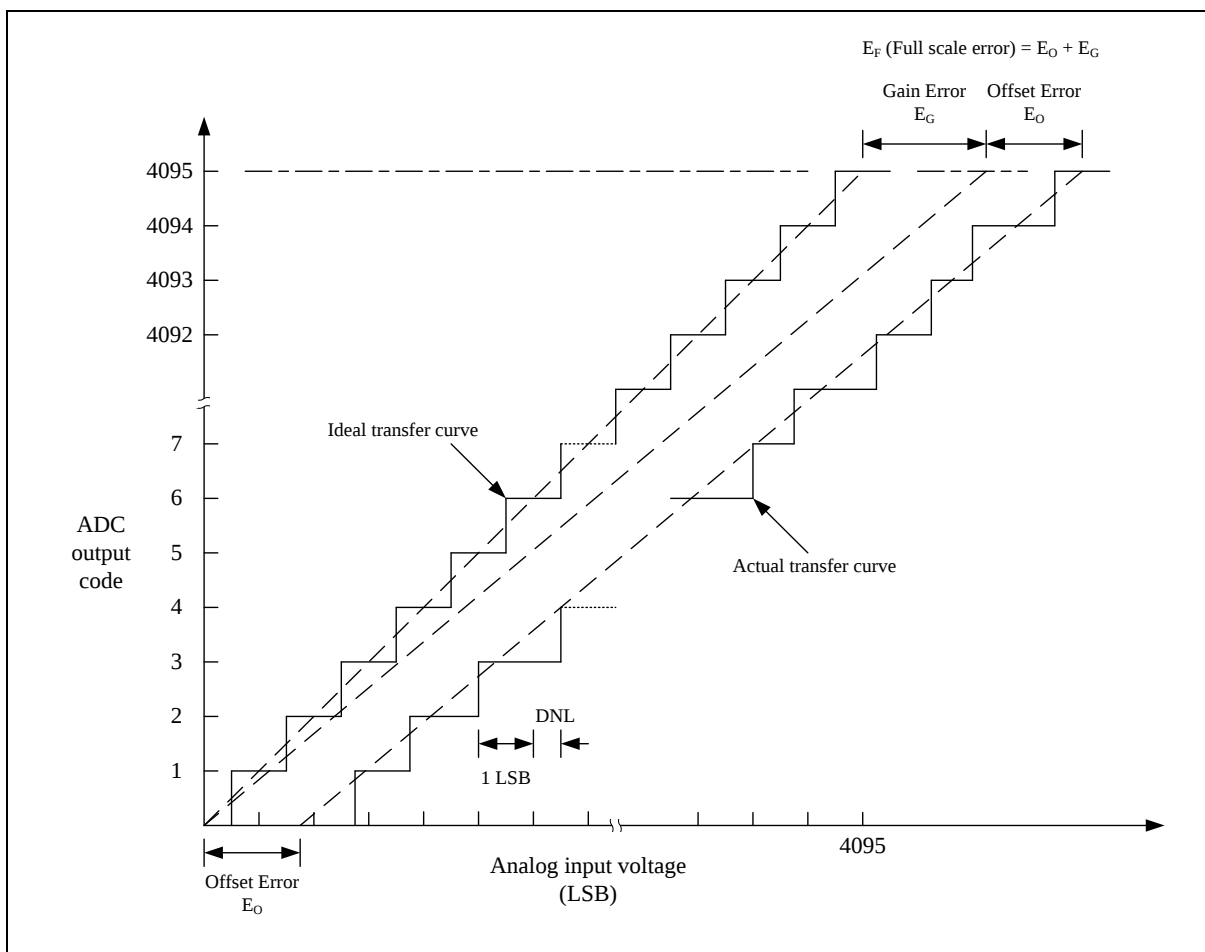
Table 8.4-1 Reset And Power Control Unit

### 8.4.2 12-bit SAR ADC

The maximum values are obtained for  $V_{DD} = 1.8V \sim 5.5V$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25^\circ C$  and  $V_{DD} = 3.3V$ . The parameters in below table are derived from tests performed under ambient temperature unless otherwise specified.

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Parameter                                        | Min           | Typ | Max       | Unit       | Test Conditions                                                                        |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|---------------|-----|-----------|------------|----------------------------------------------------------------------------------------|
| $T_A$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Temperature                                      | -40           | -   | 105       | $^\circ C$ |                                                                                        |
| $AV_{DD}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Analog operating voltage                         | 1.8           | -   | $V_{DD}$  | V          | $V_{DD} = AV_{DD}$                                                                     |
| $V_{REF}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Reference voltage                                | 1.8           | -   | $AV_{DD}$ | V          | $AV_{DD} - V_{REF} < 1.2V$                                                             |
| $V_{IN}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | ADC channel input voltage                        | 0             | -   | $V_{REF}$ | V          |                                                                                        |
| $I_{ADC}^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Operating current ( $AV_{DD} + V_{REF}$ current) | -             | -   | 418       | $\mu A$    | $AV_{DD} = V_{DD} = V_{REF} = 5.5V$<br>$F_{ADC} = 500kHz$<br>$T_{CONV} = 17 * T_{ADC}$ |
| $N_R$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Resolution                                       | 12            |     |           | Bit        |                                                                                        |
| $F_{ADCEC}^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Encoding Rate                                    | 500           |     |           | kHz        | This value is fixed by ADC module                                                      |
| $T_{ADCEC}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Encoding Time                                    | 2             |     |           | $\mu s$    | This value is fixed by ADC module                                                      |
| $F_{ADCSMP}^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | ADC Sampling Clock frequency                     | $F_{SYS}/128$ |     | $F_{SYS}$ | kHz        | base on ADCDIV (ADCCON1[5:4])                                                          |
| $T_{SMP}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Sampling Time <sup>[3]</sup>                     | 0.417         | -   | 202       | $\mu s$    |                                                                                        |
| $F_{ADCCOV}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Conversion Rate $F_{ADCCOV} = 1/T_{ADCCOV}$      | 2.417         |     | 204       | $\mu s$    | $F_{SYS} = 24MHz$ ;                                                                    |
| $T_{ADCCOV}^{[2]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Conversion Time $T_{ADC} = T_{SMP} + T_{ADCEC}$  | 4.9           |     | 413       | kHz        | $F_{SYS} = 24MHz$ ;                                                                    |
| $T_{EN}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Enable to ready time                             | 20            | -   | -         | $\mu s$    |                                                                                        |
| $INL^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Integral Non-Linearity Error                     | -3            | -   | +3        | LSB        | $V_{REF} = AV_{DD} = V_{DD}$                                                           |
| $DNL^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Differential Non-Linearity Error                 | -2            | -   | +4        | LSB        | $V_{REF} = AV_{DD} = V_{DD}$                                                           |
| $E_G^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Gain error                                       | -3.5          | -   | +0.4      | LSB        | $V_{REF} = AV_{DD} = V_{DD}$                                                           |
| $E_O^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Offset error                                     | -2            | -   | +2.8      | LSB        | $V_{REF} = AV_{DD} = V_{DD}$                                                           |
| $E_A^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Absolute Error                                   | -7            |     | +7        | LSB        | $V_{REF} = AV_{DD} = V_{DD}$                                                           |
| $R_S$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Input Channel Equivalent Resistance              |               | 0.5 | 2.5       | k $\Omega$ |                                                                                        |
| $C_{IN}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Input Equivalent Capacitance                     |               | 2.5 |           | pF         |                                                                                        |
| <p>1. Guaranteed by characterization result, not tested in production.</p> <p>2. ADC Conversion time <math>T_{ADCCOV} = \text{ADC Sampling Time } (T_{SMP}) + \text{ADC Encoding Time } (T_{ADCEC})</math>.</p> <p>3. <math>\text{ADC Sampling Time} = \frac{4 * \text{ADCAQT} + 10}{F_{ADC}}</math> (FADC Base on ADCDIV (ADCSR[3:1]))</p> <p>ADC Sampling Time Minimum condition <math>\frac{10}{24MHz}</math> . (ADCAQT = 0, ADCDIV = 0)</p> <p>ADC Sampling Time Maximum condition <math>\frac{4 * 7 + 10}{24MHz / 128}</math> (ADCAQT = 7, ADCDIV = 7 )</p> |                                                  |               |     |           |            |                                                                                        |

Table 8.4-2 ADC Characteristics



**Note:** The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

### 8.4.3 Analog Comparator Controller (ACMP)

The maximum values are obtained for  $V_{DD} = 5.5\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^{\circ}\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol                                                                                 | Parameter                              | Min  | Typ           | Max             | Unit               | Test Conditions                        |
|----------------------------------------------------------------------------------------|----------------------------------------|------|---------------|-----------------|--------------------|----------------------------------------|
| $AV_{DD}$                                                                              | Analog supply voltage                  | 1.8  | -             | 5.5             | V                  | $V_{DD} = AV_{DD}$                     |
| $T_A$                                                                                  | Temperature                            | -40  | -             | 105             | $^{\circ}\text{C}$ |                                        |
| $I_{DD}$                                                                               | Operating current                      | -    | 2             | 5               | $\mu\text{A}$      |                                        |
| $V_{CM}^{[2]}$                                                                         | Input common mode voltage range        | 0.35 | $1/2 AV_{DD}$ | $AV_{DD} - 0.3$ |                    |                                        |
| $V_{DI}^{[2]}$                                                                         | Differential input voltage sensitivity | 10   | 20            | -               | mV                 | Hysteresis disable                     |
| $V_{offset}^{[2]}$                                                                     | Input offset voltage                   | -    | 10            | 20              | mV                 | Hysteresis disable                     |
| $V_{hys}^{[2]}$                                                                        | Hysteresis window                      | -    | 10            | 20              | mV                 |                                        |
| $A_v^{[1]}$                                                                            | DC voltage Gain                        | 45   | 65            | 75              | dB                 |                                        |
| $T_d^{[2]}$                                                                            | Propagation delay                      | -    | -             | 5               | $\mu\text{S}$      |                                        |
| $T_{Stable}^{[2]}$                                                                     | Stable time                            | -    | -             | 5               | $\mu\text{S}$      |                                        |
| $A_{CRV}^{[2]}$                                                                        | CRV output voltage                     | -5   | -             | 5               | %                  | $AV_{DD} \times (1/6 + CRVCTL/24)$     |
| $R_{CRV}^{[2]}$                                                                        | Unit resistor value                    | -    | 4.5           | -               | k $\Omega$         |                                        |
| $T_{SETUP\_CRV}^{[2]}$                                                                 | Stable time                            | -    | -             | 2               | $\mu\text{S}$      | CRV output voltage settle to $\pm 5\%$ |
| $I_{DD\_CRV}^{[2]}$                                                                    | Operating current                      | -    | 2             | -               | $\mu\text{A}$      |                                        |
| Notes:                                                                                 |                                        |      |               |                 |                    |                                        |
| 1. Guaranteed by design, not tested in production                                      |                                        |      |               |                 |                    |                                        |
| 2. Guaranteed by characteristic, not tested in production. unless otherwise specified. |                                        |      |               |                 |                    |                                        |

Table 8.4-3 ACMP Characteristics

#### 8.4.4 Internal Voltage Reference

The maximum values are obtained for  $V_{DD} = 5.5$  V and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25$  °C and  $V_{DD} = 3.3$  V unless otherwise specified.

| Symbol           | Parameter                             | Min.  | Typ.  | Max.      | Unit | Test Conditions                                                                                                                                   |
|------------------|---------------------------------------|-------|-------|-----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{REF\_EXT}$   | External Analog reference voltage     | 1.8   | -     | $AV_{DD}$ |      |                                                                                                                                                   |
| $V_{REF\_INT}$   | Internal reference voltage            | 1.49  | 1.538 | 1.59      | V    | $AV_{DD} \geq 2.0$ V, $T_A = 25^\circ\text{C}$<br>Internal analog reference voltage<br>$V_{REFSEL}[2:0] = 000$ <sup>[2]</sup>                     |
|                  |                                       | 2.018 | 2.048 | 2.078     |      | $AV_{DD} \geq 2.4$ V, $T_A = 25^\circ\text{C}$<br>Internal Analog reference voltage<br>$V_{REFSEL}[2:0] = 001$ <sup>[2]</sup><br>Test in product. |
|                  |                                       | 2.48  | 2.560 | 2.64      |      | $AV_{DD} \geq 2.9$ V, $T_A = 25^\circ\text{C}$<br>Internal analog reference voltage<br>$V_{REFSEL}[2:0] = 010$ <sup>[2]</sup>                     |
|                  |                                       | 3.042 | 3.072 | 3.102     |      | $AV_{DD} \geq 3.4$ V, $T_A = 25^\circ\text{C}$ Internal<br>Analog reference voltage<br>$V_{REFSEL}[2:0] = 011$ <sup>[2]</sup><br>Test in product. |
|                  |                                       | 3.97  | 4.096 | 4.22      |      | $AV_{DD} \geq 4.5$ V, $T_A = 25^\circ\text{C}$<br>Internal analog reference voltage<br>$V_{REFSEL}[2:0] = 100$ <sup>[2]</sup>                     |
| $V_{BG}$         | Band-gap voltage                      | 0.793 | 0.814 | 0.835     | V    | $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$ , Test in product.                                                                               |
| $T_s$            | Stable time                           | -     | 24    | 180       | mS   | $C_L = 1$ uF, $V_{REF}$ initial=0, Preload is enabled.                                                                                            |
|                  |                                       | -     | 2     | 2.6       | mS   | $C_L = 1$ uF, $V_{REF}$ initial=5.5, Preload is enabled.                                                                                          |
| $I_{VREF\_INT}$  | $V_{REF\_INT}$ operating current      | -     | -     | 1         | mA   |                                                                                                                                                   |
| $I_{VREF\_LOAD}$ | $V_{REF\_INT}$ output loading current | -     | -     | 1         | mA   |                                                                                                                                                   |

**Note:**

1. Guaranteed by characterization, not tested in production

Table 8.4-4 Voltage Reference Character

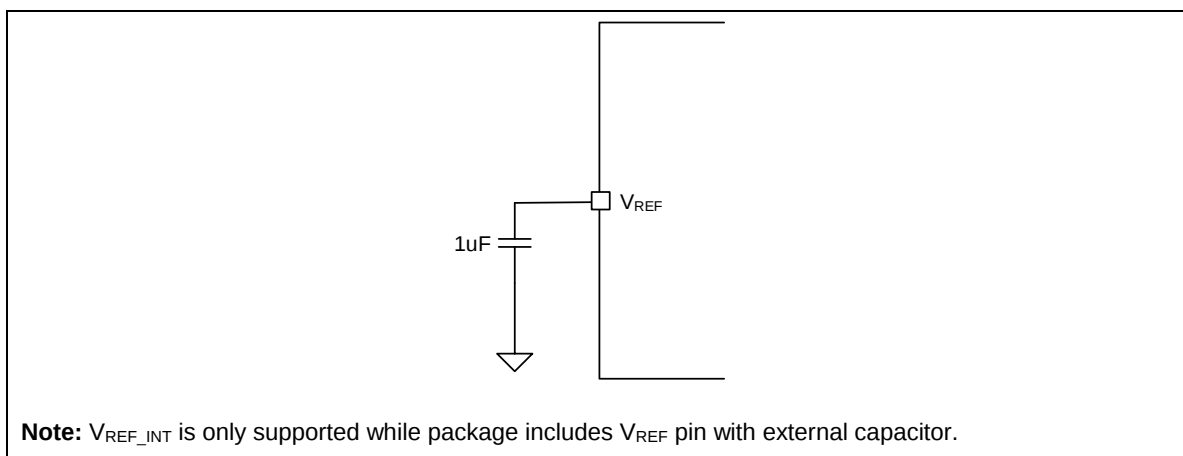


Figure 8.4-1 Typical Connection With Internal Voltage Reference

#### 8.4.5 Temperature Sensor

The maximum values are obtained for  $V_{DD} = 1.8 \sim 5.5$  V and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25$  °C and  $V_{DD} = 3.3$  V unless otherwise specified.

| Symbol                                                                                                                                                                                                                                           | Parameter                            | Min. | Typ. | Max. | Unit  | Test Conditions |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|------|------|------|-------|-----------------|
| $V_{TEMP\_OS}^{[1]}$                                                                                                                                                                                                                             | Temperature sensor offset voltage    | 645  | 675  | 705  | mV    |                 |
| $T_C^{[1]}$                                                                                                                                                                                                                                      | Temperature Coefficient              | 1.74 | 1.83 | 1.9  | mV/°C | $T_J = 25$ °C   |
| $I_{TEMP}^{[1]}$                                                                                                                                                                                                                                 | Temperature sensor operating current | -    | 16   | 30   | μA    |                 |
| <b>Note:</b> <ol style="list-style-type: none"> <li>1. Guaranteed by characterization, not tested in production</li> <li>2. <math>V_{TEMP}</math> (mV) = <math>T_C</math> (mV/°C) x Temperature (°C) + <math>V_{TEMP\_OS}</math> (mV)</li> </ol> |                                      |      |      |      |       |                 |

Table 8.4-5 Temperature Sensor Character

### 8.4.6 LCD Controller

The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^{\circ}\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol          | Parameter                                                              | Min     | Typ           | Max | Unit          | Test Conditions                                                         |
|-----------------|------------------------------------------------------------------------|---------|---------------|-----|---------------|-------------------------------------------------------------------------|
| $V_{LCD}$       | LCD external pin voltage                                               | 1.8     | -             | 5.5 | V             |                                                                         |
| $V_{LCDDDD}$    | VLCD Power Supply voltage                                              | 1.8     | -             | 3.6 | V             | LCD Power source is $AV_{DD}$                                           |
| $V_{LCDCP}$     | LCD internal Charge Pump Voltage Output Value                          | -       | 5.4           | -   | V             | VCP_SEL[5:0]=000000                                                     |
|                 |                                                                        | -       | 5.2           | -   |               | VCP_SEL[5:0]=000101                                                     |
|                 |                                                                        | -       | 5.0           | -   |               | VCP_SEL[5:0]=001010                                                     |
|                 |                                                                        | -       | 4.8           | -   |               | VCP_SEL[5:0]=001110                                                     |
|                 |                                                                        | -       | 4.6           | -   |               | VCP_SEL[5:0]=010011                                                     |
|                 |                                                                        | -       | 4.4           | -   |               | VCP_SEL[5:0]=011000                                                     |
|                 |                                                                        | -       | 4.2           | -   |               | VCP_SEL[5:0]=011101                                                     |
|                 |                                                                        | -       | 4.0           | -   |               | VCP_SEL[5:0]=100010                                                     |
|                 |                                                                        | -       | 3.8           | -   |               | VCP_SEL[5:0]=100111                                                     |
|                 |                                                                        | -       | 3.6           | -   |               | VCP_SEL[5:0]=101100                                                     |
|                 |                                                                        | -       | 3.4           | -   |               | VCP_SEL[5:0]=110000                                                     |
|                 |                                                                        | -       | 3.2           | -   |               | VCP_SEL[5:0]=110101                                                     |
|                 |                                                                        | -       | 3.0           | -   |               | VCP_SEL[5:0]=111010                                                     |
|                 |                                                                        | -       | 2.8           | -   |               | VCP_SEL[5:0]=111111                                                     |
| $C_{LCD}$       | VLCD pin external pin capacitor <sup>[2]</sup>                         | 1       |               |     | $\mu\text{F}$ | Withtout charge pump mode                                               |
|                 |                                                                        | 1       |               | 10  |               | With charge pump mode                                                   |
| $C_{DH1-DH2}$   | External charge-pump capacitor <sup>[2]</sup>                          | Without |               |     | $\mu\text{F}$ | Withtout charge pump mode                                               |
|                 |                                                                        | 0.1     |               | 1   |               | With charge pump mode                                                   |
| $C_{VX}$        | V1/V2/V3 external capacitance                                          | Without |               |     | $\mu\text{F}$ | Internal embedded with capacitor                                        |
| $V_{3/4}$       | COM/SEG 3/4 $V_{LCD}$ (1/4 Bias)                                       | -       | $3/4 V_{LCD}$ | -   | V             |                                                                         |
| $V_{2/4}$       | COM/SEG 2/4 $V_{LCD}$ (1/4 Bias)                                       | -       | $2/4 V_{LCD}$ | -   | V             |                                                                         |
| $V_{1/4}$       | COM/SEG 1/4 $V_{LCD}$ (1/4 Bias)                                       | -       | $1/4 V_{LCD}$ | -   | V             |                                                                         |
| $V_{2/3}$       | COM/SEG 2/3 $V_{LCD}$ (1/3 Bias)                                       | -       | $2/3 V_{LCD}$ | -   | V             |                                                                         |
| $V_{1/3}$       | COM/SEG 1/3 $V_{LCD}$ (1/3 Bias)                                       | -       | $1/3 V_{LCD}$ | -   | V             |                                                                         |
| $R_{R\_MODE}$   | Resistor Mode total internal Resistor Value                            | -       | 240           | -   | K $\Omega$    |                                                                         |
| $R_{RE\_MODE}$  | Resistor Enhance Mode total internal Resistor Value                    |         | 6             |     | M $\Omega$    |                                                                         |
| $I_{LCD}^{[3]}$ | Supply current from $V_{DD}$ with built-in charge pump and buffer mode | -       | 18            | -   | $\mu\text{A}$ | $V_{DD}=1.8$ , $V_{LCD}=V_{CP}=3.2$ , Buffer Mode, all LCD display on   |
|                 |                                                                        |         | 31            |     |               | $V_{DD}=1.8$ , $V_{LCD}=V_{CP}=3.2$ , Resistor Mode, all LCD display on |
|                 |                                                                        | -       | 5.5           | -   |               | $V_{DD}=1.8$ , $V_{LCD}=V_{CP}=3.2$ , Resistor                          |

| Symbol                                                                                                                                              | Parameter                                                         | Min | Typ | Max | Unit | Test Conditions                                                                                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|-----|-----|-----|------|------------------------------------------------------------------------------------------------|
|                                                                                                                                                     |                                                                   |     |     |     |      | Enhance Mode, all LCD display on                                                               |
|                                                                                                                                                     |                                                                   | -   | 24  | -   |      | V <sub>DD</sub> =3.3, V <sub>LCD</sub> =V <sub>CP</sub> =5.4, Buffer Mode, all LCD display on  |
|                                                                                                                                                     |                                                                   | -   | 1.8 | -   |      | V <sub>DD</sub> =1.8, V <sub>LCD</sub> =V <sub>CP</sub> =3.2, Buffer Mode, all LCD display off |
| I <sub>VLCD</sub> <sup>[3]</sup>                                                                                                                    | Supply current from V <sub>LCD</sub> without Built-In Charge Pump | -   | 7   | -   | μA   | V <sub>DD</sub> =1.8, V <sub>LCD</sub> =3.3, Buffer Mode, all LCD display on                   |
|                                                                                                                                                     |                                                                   |     | 14  |     |      | V <sub>DD</sub> =1.8, V <sub>LCD</sub> =3.3, Resistor Mode, all LCD display on                 |
|                                                                                                                                                     |                                                                   |     | 0.8 |     |      | V <sub>DD</sub> =1.8, V <sub>LCD</sub> =3.3, Resistor Enhance Mode, all LCD display on         |
|                                                                                                                                                     |                                                                   | -   | 9.2 | -   |      | V <sub>DD</sub> =1.8, V <sub>LCD</sub> =5.4, Buffer Mode, all LCD display on                   |
|                                                                                                                                                     |                                                                   | -   | 7   | -   |      | V <sub>DD</sub> =3.3, V <sub>LCD</sub> =3.3, Buffer Mode, all LCD display on                   |
|                                                                                                                                                     |                                                                   | -   | 9   | -   |      | V <sub>DD</sub> =1.8, V <sub>LCD</sub> =5.4, Buffer Mode, all LCD display off                  |
| Notes:                                                                                                                                              |                                                                   |     |     |     |      |                                                                                                |
| 1. All condition not special defined is guaranteed by design, not tested in production                                                              |                                                                   |     |     |     |      |                                                                                                |
| 2. C <sub>DH1-DH2</sub> value should be 1/10 C <sub>LCD</sub>                                                                                       |                                                                   |     |     |     |      |                                                                                                |
| 3. LCD COM/SEG is set to clock source is LIRC, 1/8 duty, 1/4 bias, type B 64 Hz frame rate, all pixels active, waveform, without LCD panel loading. |                                                                   |     |     |     |      |                                                                                                |

Table 8.4-6 LCD Digital Characteristics

#### LCD Voltage Source From Internal Charge Pump

| Symbol                          | Parameter                                                                         | LCD Status | V <sub>DD</sub> | V <sub>LCD</sub> | Typ.        |     |     |               |     |     |                       |     |     | Unit |
|---------------------------------|-----------------------------------------------------------------------------------|------------|-----------------|------------------|-------------|-----|-----|---------------|-----|-----|-----------------------|-----|-----|------|
|                                 |                                                                                   |            |                 |                  | Buffer Mode |     |     | Resistor Mode |     |     | Resistor Enhance Mode |     |     | °C   |
|                                 |                                                                                   |            |                 |                  | -20         | 25  | 85  | -20           | 25  | 85  | -20                   | 25  | 85  |      |
| I <sub>LCD CPPD</sub><br>(LIRC) | VDD Supply Current in Power Down Mode with LIRC, VLCD source internal Charge Pump | LCD On     | 1.8V            | 3.2V             | 17          | 18  | 24  | 30            | 31  | 36  | 5.1                   | 5.5 | 10  | μA   |
|                                 |                                                                                   |            | 3.3V            | 3.2V             | 20          | 22  | 29  | 37            | 39  | 44  | 6                     | 6.3 | 6   |      |
|                                 |                                                                                   |            |                 | 5.4V             | 22          | 24  | 31  | 49            | 52  | 58  | 7                     | 7   | 6   |      |
|                                 |                                                                                   | LCD Off    | 1.8V            | 3.2V             | 1.6         | 1.6 | 5   | 1.6           | 1.6 | 5   | 1.6                   | 1.6 | 5   |      |
|                                 |                                                                                   |            | 3.3V            | 3.2V             | 1.8         | 2   | 5.7 | 1.8           | 2   | 5.7 | 1.8                   | 2   | 5.7 |      |
|                                 |                                                                                   |            |                 | 5.4V             | 1.8         | 2   | 5.7 | 1.8           | 2   | 5.7 | 1.8                   | 2   | 5.7 |      |
| I <sub>LCD CPPD</sub><br>(LXT)  | VDD Supply Current in Power Down Mode with LXT, VLCD source internal Charge       | LCD On     | 1.8V            | 3.2V             | 17          | 18  | 25  | 30            | 32  | 37  | 5.5                   | 6   | 11  |      |
|                                 |                                                                                   |            | 3.3V            | 3.2V             | 21          | 22  | 30  | 37            | 40  | 45  | 6                     | 6.5 | 16  |      |
|                                 |                                                                                   |            |                 | 5.4V             | 22          | 24  | 32  | 50            | 52  | 59  | 7                     | 7.5 | 17  |      |
|                                 |                                                                                   | LCD        | 1.8V            | 3.2V             | 1.6         | 1.6 | 5   | 1.6           | 1.6 | 5   | 1.6                   | 1.6 | 5   |      |
|                                 |                                                                                   |            |                 |                  |             |     |     |               |     |     |                       |     |     |      |

| Symbol | Parameter | LCD Status | V <sub>DD</sub> | V <sub>LCD</sub> | Typ.        |    |     |               |    |     |                       |    |     | Unit |
|--------|-----------|------------|-----------------|------------------|-------------|----|-----|---------------|----|-----|-----------------------|----|-----|------|
|        |           |            |                 |                  | Buffer Mode |    |     | Resistor Mode |    |     | Resistor Enhance Mode |    |     |      |
|        |           |            |                 |                  | -20         | 25 | 85  | -20           | 25 | 85  | -20                   | 25 | 85  | °C   |
|        | Pump      | Off        | 3.3V            | 3.2V             | 1.8         | 2  | 5.7 | 1.8           | 2  | 5.7 | 1.8                   | 2  | 5.7 |      |
|        |           |            |                 | 5.4V             | 1.8         | 2  | 5.7 | 1.8           | 2  | 5.7 | 1.8                   | 2  | 5.7 |      |

Notes:  
1. All condition not special defined is guaranteed by design, not tested in production  
2. The values are obtained for TA= 25 °C and VDD = 3.3 V unless otherwise specified.  
3. LCD COM/SEG is set as 1/8 duty, 1/4 bias, type B 64 Hz frame rate, all pixels active, without LCD panel loading.

Table 8.4-7 Current Consumption In Power Down Mode With LCD Voltage Source From Internal Charge Pump

#### LCD Voltage Source From AV<sub>DD</sub>

| Symbol                          | Parameter                                                                  | LCD Status | V <sub>LCD</sub><br>(AV <sub>DD</sub> ) | Typ.        |     |      |               |      |      |                       |     |     | Unit |
|---------------------------------|----------------------------------------------------------------------------|------------|-----------------------------------------|-------------|-----|------|---------------|------|------|-----------------------|-----|-----|------|
|                                 |                                                                            |            |                                         | Buffer Mode |     |      | Resistor Mode |      |      | Resistor Enhance Mode |     |     |      |
|                                 |                                                                            |            |                                         | -20         | 25  | 85   | -20           | 25   | 85   | -20                   | 25  | 85  | °C   |
| I <sub>LCDVDDP</sub><br>D(LIRC) | VDD Supply Current in Power Down Mode with LIRC, VLCD source internal AVDD | LCD On     | 1.8V                                    | 6.2         | 6.8 | 13   | 9             | 9.2  | 13   | 2.1                   | 2.4 | 6   | μA   |
|                                 |                                                                            |            | 3.3V                                    | 9           | 9.5 | 15   | 16            | 16.4 | 21   | 2.6                   | 3   | 7   |      |
|                                 |                                                                            | LCD Off    | 1.8V                                    | 5.2         | 6   | 11   | 8             | 8.3  | 12   | 1.2                   | 1.4 | 5   |      |
|                                 |                                                                            |            | 3.3V                                    | 8           | 8.5 | 13.5 | 14.2          | 14.6 | 19   | 1.6                   | 1.8 | 6   |      |
| I <sub>LCDVDDP</sub><br>D(LXT)  | VDD Supply Current in Power Down Mode with LXT, VLCD source internal AVDD  | LCD On     | 1.8V                                    | 6.6         | 7.5 | 5.2  | 9.6           | 10   | 12.1 | 2.7                   | 3   | 4.8 |      |
|                                 |                                                                            |            | 3.3V                                    | 9           | 10  | 6.2  | 16.8          | 14.5 | 19.2 | 3.2                   | 3.5 | 5.8 |      |
|                                 |                                                                            | LCD Off    | 1.8V                                    | 5.2         | 6   | 11   | 8             | 8.3  | 12   | 1.2                   | 1.4 | 5   |      |
|                                 |                                                                            |            | 3.3V                                    | 8           | 8.5 | 13.5 | 14.2          | 14.6 | 19   | 1.6                   | 1.8 | 6   |      |

Notes:  
1. All condition not special defined is guaranteed by design, not tested in production  
2. The values are obtained for TA= 25 °C unless otherwise specified.  
3. LCD COM/SEG is set to 1/8 duty, 1/4 bias, 128 Hz frame rate, all pixels active, type B waveform, no LCD panel loading.

Table 8.4-8 Current Consumption In Power Down Mode With LCD Voltage Source From AV<sub>DD</sub>

LCD Voltage Source From External VLCD Pin

| Symbol                                                                                                                   | Parameter                                                                       | LCD Status | V <sub>LCD</sub> | Typ.        |     |     |               |    |      |                       |     |     | Unit |
|--------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|------------|------------------|-------------|-----|-----|---------------|----|------|-----------------------|-----|-----|------|
|                                                                                                                          |                                                                                 |            |                  | Buffer Mode |     |     | Resistor Mode |    |      | Resistor Enhance Mode |     |     |      |
|                                                                                                                          |                                                                                 |            |                  | -20         | 25  | 85  | -20           | 25 | 85   | -20                   | 25  | 85  | °C   |
| I <sub>LCDVLCDD(LIRC)</sub>                                                                                              | VLCD Supply Current in Power Down Mode with LIRC, VLCD source External VLCD pin | LCD On     | 3.3              | 6.5         | 7   | 9   | 13.5          | 14 | 15   | 0.7                   | 0.8 | 1.2 | μA   |
|                                                                                                                          |                                                                                 |            | 5.4V             | 8.6         | 9.2 | 11  | 22            | 23 | 24   | 1.2                   | 1.2 | 2   |      |
|                                                                                                                          |                                                                                 | LCD Off    | 3.3V             | 6.5         | 7   | 8.5 | 14            | 14 | 14.5 | 0.5                   | 0.6 | 1   |      |
|                                                                                                                          |                                                                                 |            | 5.4V             | 8.3         | 9   | 11  | 22            | 23 | 23.5 | 0.9                   | 1   | 2   |      |
| I <sub>LCDVLCDD(LXT)</sub>                                                                                               | Supply Current in Power Down Mode with LXT, VLCD source External VLCD pin       | LCD On     | 3.3              | 6.5         | 7   | 9   | 13.5          | 14 | 15   | 0.7                   | 0.8 | 1.2 |      |
|                                                                                                                          |                                                                                 |            | 5.4V             | 8.6         | 9.2 | 11  | 22            | 23 | 24   | 1.2                   | 1.2 | 2   |      |
|                                                                                                                          |                                                                                 | LCD Off    | 3.3V             | 6.5         | 7   | 8.5 | 14            | 14 | 14.5 | 0.5                   | 0.6 | 1   |      |
|                                                                                                                          |                                                                                 |            | 5.4V             | 8.3         | 9   | 11  | 22            | 23 | 23.5 | 0.9                   | 1   | 2   |      |
| Notes:                                                                                                                   |                                                                                 |            |                  |             |     |     |               |    |      |                       |     |     |      |
| 1. All condition not special defined is guaranteed by design, not tested in production                                   |                                                                                 |            |                  |             |     |     |               |    |      |                       |     |     |      |
| 2. The values are obtained for TA= 25 °C and VDD = 3.3 V unless otherwise specified.                                     |                                                                                 |            |                  |             |     |     |               |    |      |                       |     |     |      |
| 3. LCD COM/SEG is set to 1/8 duty, 1/4 bias, 128 Hz frame rate, all pixels active, type B waveform, no LCD panel loading |                                                                                 |            |                  |             |     |     |               |    |      |                       |     |     |      |

Table 8.4-9 Current Consumption In Power Down Mode With LCD Voltage Source From External VLCD pin

## 8.5 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

| Symbol                                                               | Parameter       | Min     | Typ | Max | Unit                  | Test Condition                                   |
|----------------------------------------------------------------------|-----------------|---------|-----|-----|-----------------------|--------------------------------------------------|
| V <sub>FLA</sub> <sup>[1]</sup>                                      | Supply voltage  | -       | 1.5 | -   | V                     | T <sub>A</sub> = 25°C                            |
| T <sub>ERASE</sub>                                                   | Page erase time | -       | 5   | -   | ms                    |                                                  |
| T <sub>PROG</sub>                                                    | Program time    | -       | 10  | -   | μs                    |                                                  |
| I <sub>DD1</sub>                                                     | Read current    | -       | 4   | -   | mA                    |                                                  |
| I <sub>DD2</sub>                                                     | Program current | -       | 4   | -   | mA                    |                                                  |
| I <sub>DD3</sub>                                                     | Erase current   | -       | 12  | -   | mA                    |                                                  |
| N <sub>ENDUR</sub>                                                   | Endurance       | 100,000 | -   |     | cycles <sup>[2]</sup> | T <sub>J</sub> = -40°C~125°C                     |
| T <sub>RET</sub>                                                     | Data retention  | 50      | -   | -   | year                  | 100 kcycle <sup>[3]</sup> T <sub>A</sub> = 55°C  |
|                                                                      |                 | 25      | -   | -   | year                  | 100 kcycle <sup>[3]</sup> T <sub>A</sub> = 85°C  |
|                                                                      |                 | 10      | -   | -   | year                  | 100 kcycle <sup>[3]</sup> T <sub>A</sub> = 105°C |
| Notes:                                                               |                 |         |     |     |                       |                                                  |
| 1. V <sub>FLA</sub> is source from chip internal LDO output voltage. |                 |         |     |     |                       |                                                  |
| 2. Number of program/erase cycles.                                   |                 |         |     |     |                       |                                                  |
| 3. Guaranteed by design.                                             |                 |         |     |     |                       |                                                  |

Table 8.5-1 Flash Memory Characteristics

## 8.6 Absolute Maximum Ratings

Voltage Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

### 8.6.1 Voltage Characteristics

#### 8.6.1.1 ML51 32KB/16KB Flash Series

| Symbol                                                                                                                              | Description                                           | Min          | Max | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|--------------|-----|------|
| $V_{DD}-V_{SS}^{[1]}$                                                                                                               | DC power supply                                       | -0.3         | 6.5 | V    |
| $\Delta V_{DD}$                                                                                                                     | Variations between different power pins               | -            | 50  | mV   |
| $ V_{DD}-AV_{DD} $                                                                                                                  | Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ | -            | 50  | mV   |
| $\Delta V_{SS}$                                                                                                                     | Variations between different ground pins              | -            | 50  | mV   |
| $ V_{SS}-AV_{SS} $                                                                                                                  | Allowed voltage difference for $V_{SS}$ and $AV_{SS}$ | -            | 50  | mV   |
| $V_{IN}$                                                                                                                            | Input voltage on I/O                                  | $V_{SS}-0.3$ | 6.5 | V    |
| Notes:                                                                                                                              |                                                       |              |     |      |
| 1. All main power ( $V_{DD}$ , $AV_{DD}$ ) and ground ( $V_{SS}$ , $AV_{SS}$ ) pins must be connected to the external power supply. |                                                       |              |     |      |

Table 8.6-1 ML51 32KB/16KB Flash Series Voltage Characteristics

#### 8.6.1.2 ML51 64KB Flash/ML54/ML56 Series

| Symbol                                                                                                                              | Description                                           | Min          | Max | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|--------------|-----|------|
| $V_{DD}-V_{SS}^{[1]}$                                                                                                               | DC power supply                                       | -0.3         | 4.0 | V    |
| $\Delta V_{DD}$                                                                                                                     | Variations between different power pins               | -            | 50  | mV   |
| $ V_{DD}-AV_{DD} $                                                                                                                  | Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ | -            | 50  | mV   |
| $\Delta V_{SS}$                                                                                                                     | Variations between different ground pins              | -            | 50  | mV   |
| $ V_{SS}-AV_{SS} $                                                                                                                  | Allowed voltage difference for $V_{SS}$ and $AV_{SS}$ | -            | 50  | mV   |
| $V_{IN}$                                                                                                                            | Input voltage on I/O                                  | $V_{SS}-0.3$ | 3.6 | V    |
| Notes:                                                                                                                              |                                                       |              |     |      |
| 2. All main power ( $V_{DD}$ , $AV_{DD}$ ) and ground ( $V_{SS}$ , $AV_{SS}$ ) pins must be connected to the external power supply. |                                                       |              |     |      |

Table 8.6-2 ML51 64KB Flash/ML54/ML56 Series Voltage Characteristics

### 8.6.2 Current Characteristics

| Symbol                                                                                                                                                                                                                                                                     | Description                                              | Min | Max | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-----|-----|------|
| $\Sigma I_{DD}^{[1]}$                                                                                                                                                                                                                                                      | Maximum current into $V_{DD}$                            | -   | 150 | mA   |
| $\Sigma I_{SS}$                                                                                                                                                                                                                                                            | Maximum current out of $V_{SS}$                          | -   | 150 |      |
| $I_{IO}$                                                                                                                                                                                                                                                                   | Maximum current sunk by a I/O Pin                        | -   | 22  |      |
|                                                                                                                                                                                                                                                                            | Maximum current sourced by a I/O Pin                     | -   | 10  |      |
|                                                                                                                                                                                                                                                                            | Maximum current sunk by total I/O Pins <sup>[2]</sup>    | -   | 100 |      |
|                                                                                                                                                                                                                                                                            | Maximum current sourced by total I/O Pins <sup>[2]</sup> | -   | 100 |      |
| $I_{INJ(PIN)}^{[3]}$                                                                                                                                                                                                                                                       | Maximum injected current by a I/O Pin                    | -   | ±5  |      |
| $\Sigma I_{INJ(PIN)}^{[3]}$                                                                                                                                                                                                                                                | Maximum injected current by total I/O Pins               | -   | ±25 |      |
| <b>Note:</b>                                                                                                                                                                                                                                                               |                                                          |     |     |      |
| 1. Maximum allowable current is a function of device maximum power dissipation.                                                                                                                                                                                            |                                                          |     |     |      |
| 2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.                                                                                     |                                                          |     |     |      |
| 3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$ . $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin. |                                                          |     |     |      |

Table 8.6-3 Current Characteristics

### 8.6.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$

- $T_A$  = ambient temperature (°C)
- $\theta_{JA}$  = thermal resistance junction-ambient (°C/Watt)
- $P_D$  = sum of internal and I/O power dissipation

| Symbol                                                                                                             | Description                                                     | Min | Typ | Max | Unit    |
|--------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|-----|-----|-----|---------|
| $T_A$                                                                                                              | Operating ambient temperature                                   | -40 | -   | 105 | °C      |
| $T_J$                                                                                                              | Operating junction temperature                                  | -40 | -   | 125 |         |
| $T_{ST}$                                                                                                           | Storage temperature                                             | -65 | -   | 150 |         |
| $\theta_{JA}^{[1]}$                                                                                                | Thermal resistance junction-ambient<br>10-pin MSOP(3x3 mm)      | -   | 160 | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>14-pin TSSOP( 4.4x5 mm)  | -   | 100 | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>20-pin QFN(3x3 mm)       | -   | 68  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>20-pin TSSOP(4.4x6.5 mm) | -   | 38  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>20-pin SOP(300mil)       | -   | 60  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>28-pin TSSOP(4.4x9.7 mm) | -   | 30  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>28-pin SOP(300 mil)      | -   | 55  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>32-pin LQFP(7x7 mm)      | -   | 62  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>33-pin QFN(4x4 mm)       | -   | 28  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>44-pin LQFP(10x10 mm)    | -   | 49  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>48-pin LQFP(7x7 mm)      | -   | 60  | -   | °C/Watt |
|                                                                                                                    | Thermal resistance junction-ambient<br>64-pin LQFP(7x7 mm)      | -   | 50  | -   | °C/Watt |
| <b>Note:</b><br>1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions |                                                                 |     |     |     |         |

Table 8.6-4 Thermal Characteristics

#### 8.6.4 EMC Characteristics

##### 8.6.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

##### 8.6.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

##### 8.6.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

##### 8.6.4.4 EMC Character Table

#### ML51 32KB/16KB Flash Series

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Description                                               | Min   | Typ | Max   | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|-------|-----|-------|------|
| $V_{HBM}^{[1]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Electrostatic discharge,human body mode                   | -8000 | -   | +8000 | V    |
| $V_{CDM}^{[2]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Electrostatic discharge,charge device model               | -1000 | -   | +1000 |      |
| $LU^{[3]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Pin current for latch-up <sup>[3]</sup> @ $V_{DD} = 5.5V$ | -150  | -   | +150  | mA   |
| $V_{EFT}^{[*4][*5]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Fast transient voltage burst                              | -4.4  | -   | +4.4  | kV   |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level</li> <li>2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.</li> <li>3. Determined according to JEDEC EIA/JESD78 standard.</li> <li>4. Determined according to IEC 61000-4-4 Electrical fast transient/burst immunity test.</li> <li>5. The performace cretia class is 4A.</li> </ol> |                                                           |       |     |       |      |

Table 8.6-5 ML51 32KB/16KB Flash Series EMC Characteristics

#### ML51 64KB Flash/ML54/ML56 Series

| Symbol          | Description                                               | Min   | Typ | Max   | Unit |
|-----------------|-----------------------------------------------------------|-------|-----|-------|------|
| $V_{HBM}^{[1]}$ | Electrostatic discharge,human body mode                   | -7000 | -   | +7000 | V    |
| $V_{CDM}^{[2]}$ | Electrostatic discharge,charge device model               | -1000 | -   | +1000 |      |
| $LU^{[3]}$      | Pin current for latch-up <sup>[3]</sup> @ $V_{DD} = 3.6V$ | -200  | -   | +200  | mA   |

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Description                  | Min  | Typ | Max  | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|------|------|
| $V_{EFT}^{[*4] [*5]}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Fast transient voltage burst | -4.4 | -   | +4.4 | kV   |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level</li> <li>2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.</li> <li>3. Determined according to JEDEC EIA/JESD78 standard.</li> <li>4. Determined according to IEC 61000-4-4 Electrical fast transient/burst immunity test.</li> <li>5. The performance criteria class is 4A.</li> </ol> |                              |      |     |      |      |

Table 8.6-6 ML51 64KB Flash/ML54/ML56 Series EMC Characteristics

### 8.6.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

| Pacakge                                                        | MSL   |
|----------------------------------------------------------------|-------|
| 10-pin MSOP(3x3 mm) <sup>[1]</sup>                             | MSL 3 |
| 14-pin TSSOP( 4.4x5 mm) <sup>[1]</sup>                         | MSL 3 |
| 20-pin QFN(3x3 mm) <sup>[1]</sup>                              | MSL 3 |
| 20-pin TSSOP(4.4x6.5 mm) <sup>[1]</sup>                        | MSL 3 |
| 20-pin SOP(300mil) <sup>[1]</sup>                              | MSL 3 |
| 28-pin TSSOP(4.4x9.7 mm) <sup>[1]</sup>                        | MSL 3 |
| 28-pin SOP(300 mil) <sup>[1]</sup>                             | MSL 3 |
| 32-pin LQFP(7x7 mm) <sup>[1]</sup>                             | MSL 3 |
| 33-pin QFN(4x4 mm) <sup>[1]</sup>                              | MSL 3 |
| 44-pin LQFP(10x10 mm)                                          | MSL 3 |
| 48-pin LQFP(7x7 mm) <sup>[1]</sup>                             | MSL 3 |
| 64-pin LQFP(7x7 mm) <sup>[1]</sup>                             | MSL 3 |
| <b>Note:</b><br>1. Determined according to IPC/JEDEC J-STD-020 |       |

Table 8.6-7 Package Moisture Sensitivity(MSL)

### 8.6.6 Soldering Profile

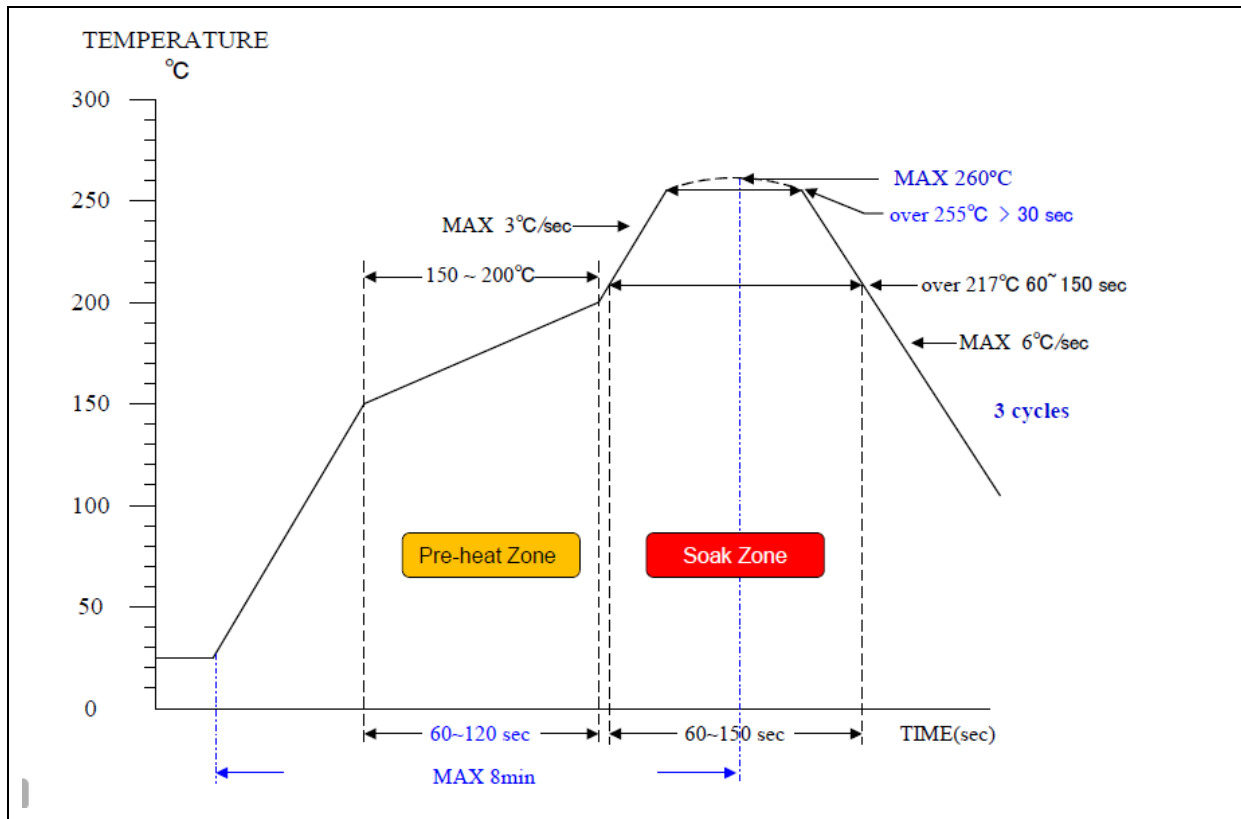


Figure 8.6-1 Soldering Profile From J-STD-020C

| Profile Feature                                       | Pb Free Package     |
|-------------------------------------------------------|---------------------|
| Average ramp-up rate (217°C to peak)                  | 3°C/sec. max        |
| Preheat temperature 150°C ~200°C                      | 60 sec. to 120 sec. |
| Temperature maintained above 217°C                    | 60 sec. to 150 sec. |
| Time with 5°C of actual peak temperature              | > 30 sec.           |
| Peak temperature range                                | 260°C               |
| Ramp-down rate                                        | 6°C/sec ax.         |
| Time 25°C to peak temperature                         | 8 min. max          |
| <b>Note:</b><br>1. Determined according to J-STD-020C |                     |

Table 8.6-8 Soldering Profile

## 9 PACKAGE DIMENSIONS

### 9.1 LQFP 64L-pin (7.0 x 7.0 x 1.4 mm)

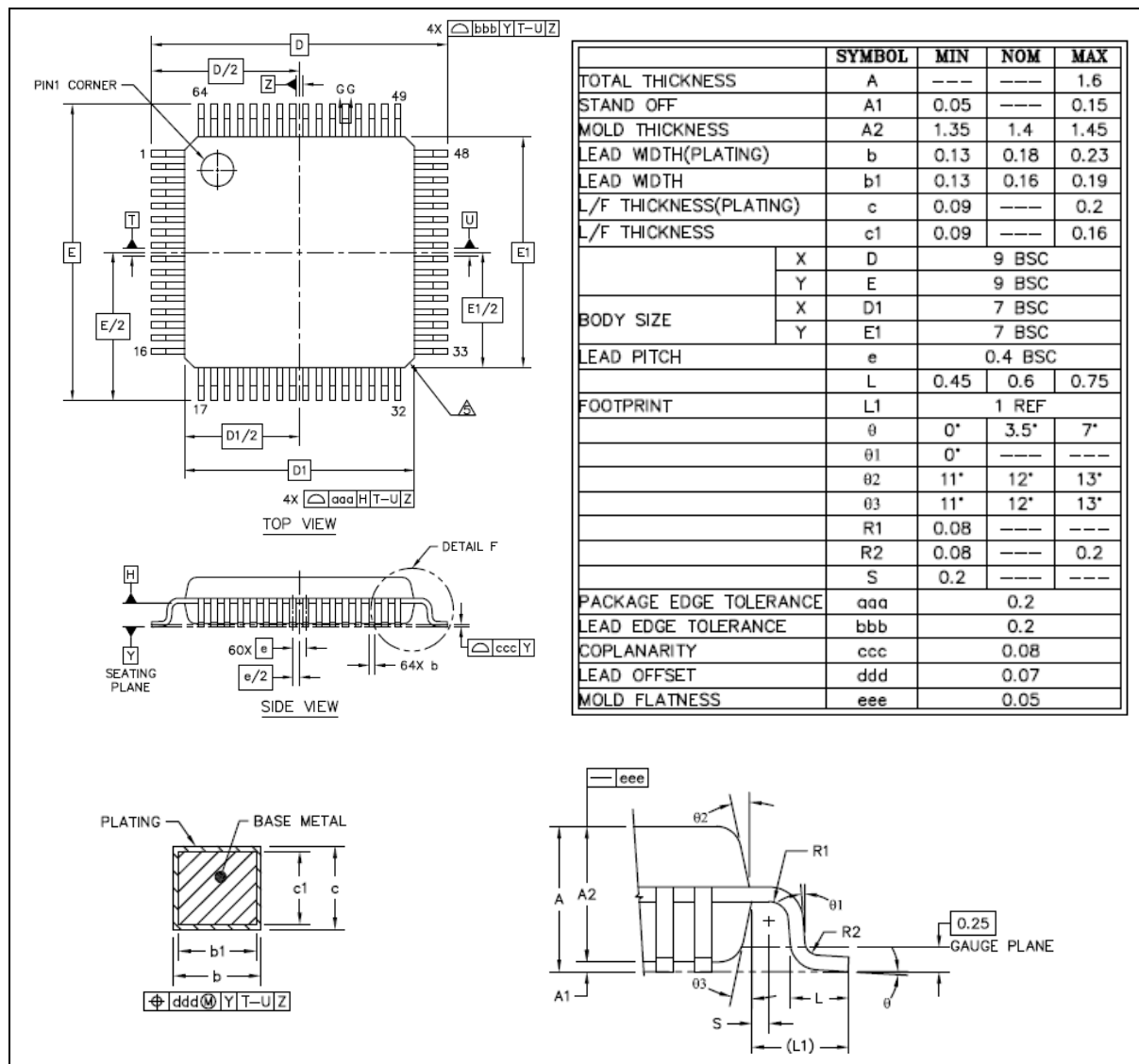


Figure 9.1-1 LQFP 64L Package Dimension

## 9.2 LQFP 48-pin (7.0 x 7.0 x 1.4 mm)

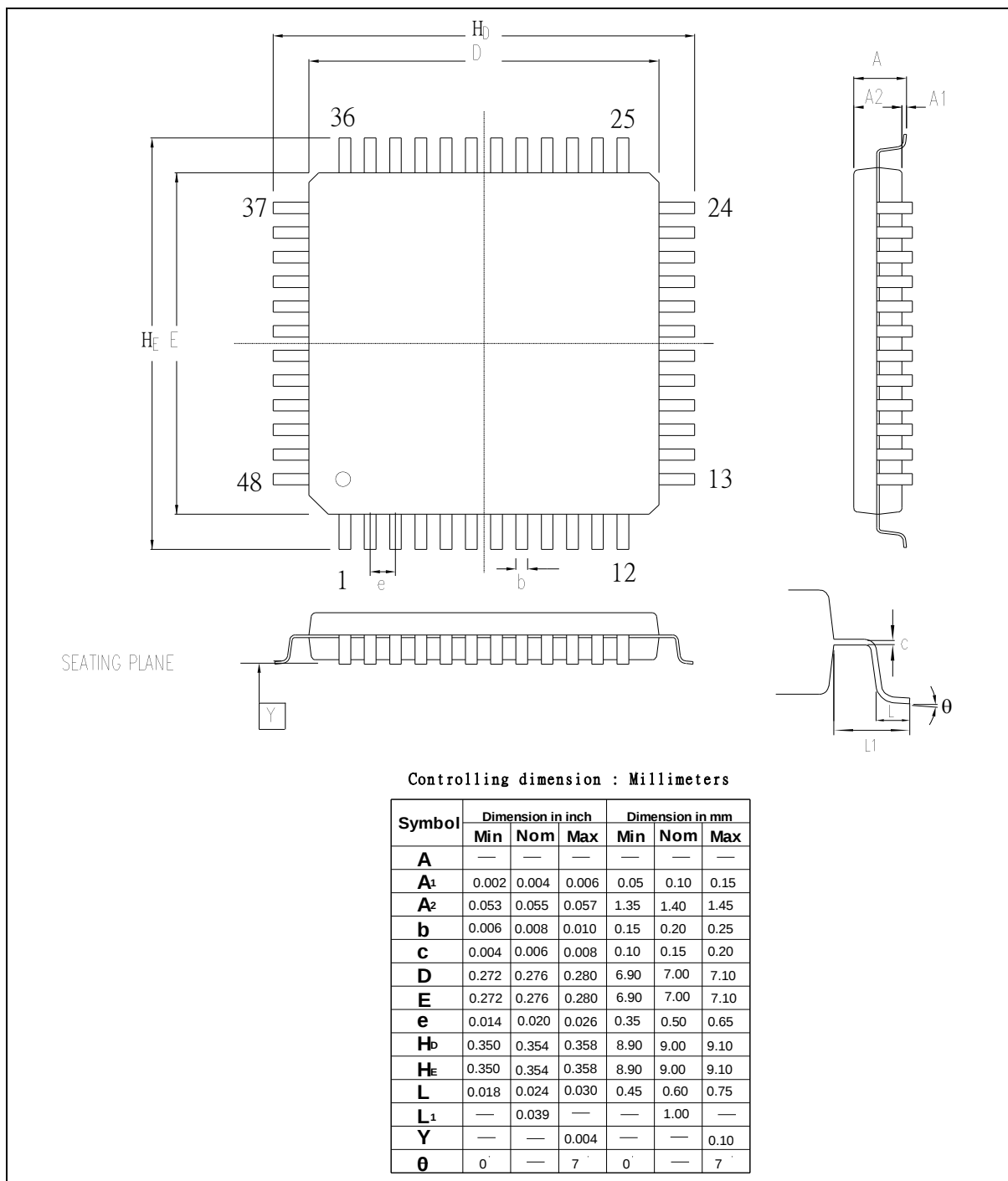


Figure 9.2-1 LQFP-48 Package Dimension

9.3 LQFP 44-pin (10 x 10 x 1.4mm

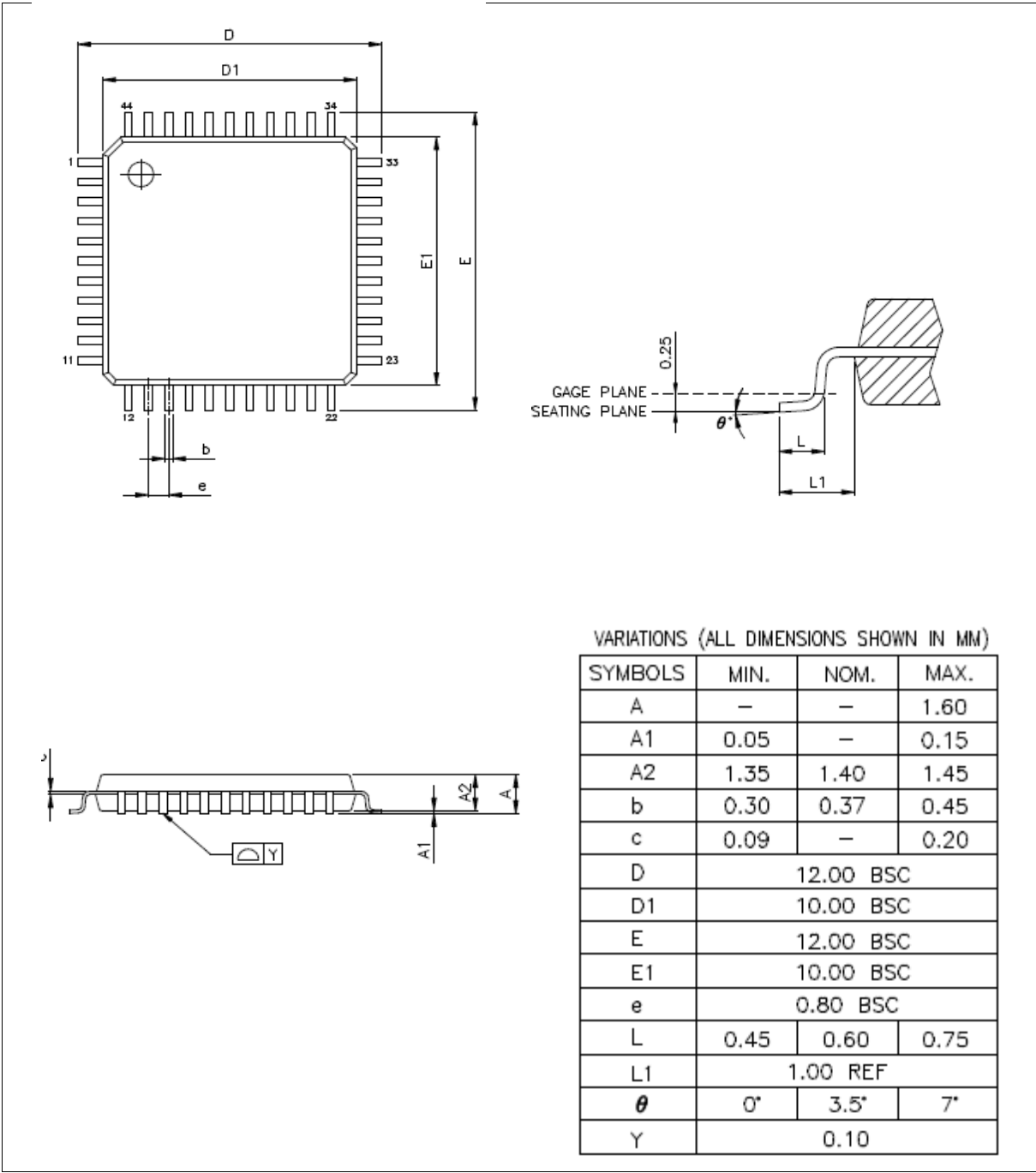


Figure 9.3-1 LFP44 Package Dimension

9.4 QFN 33-pin (4.0 x 4.0 x 0.8 mm)

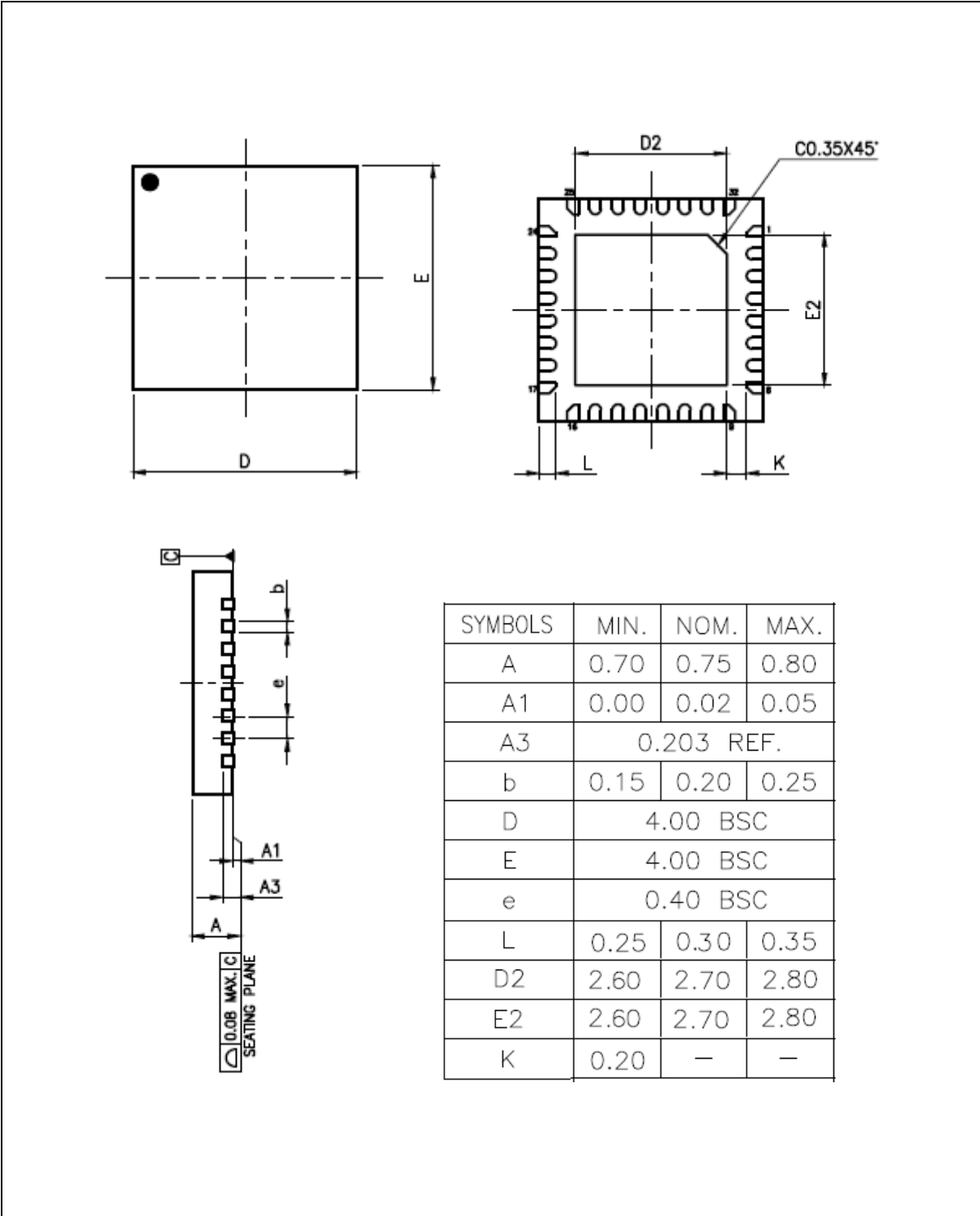


Figure 9.4-1 QFN-33 Package Dimension

9.5 LQFP 32-pin (7.0 x 7.0 x 1.4 mm)

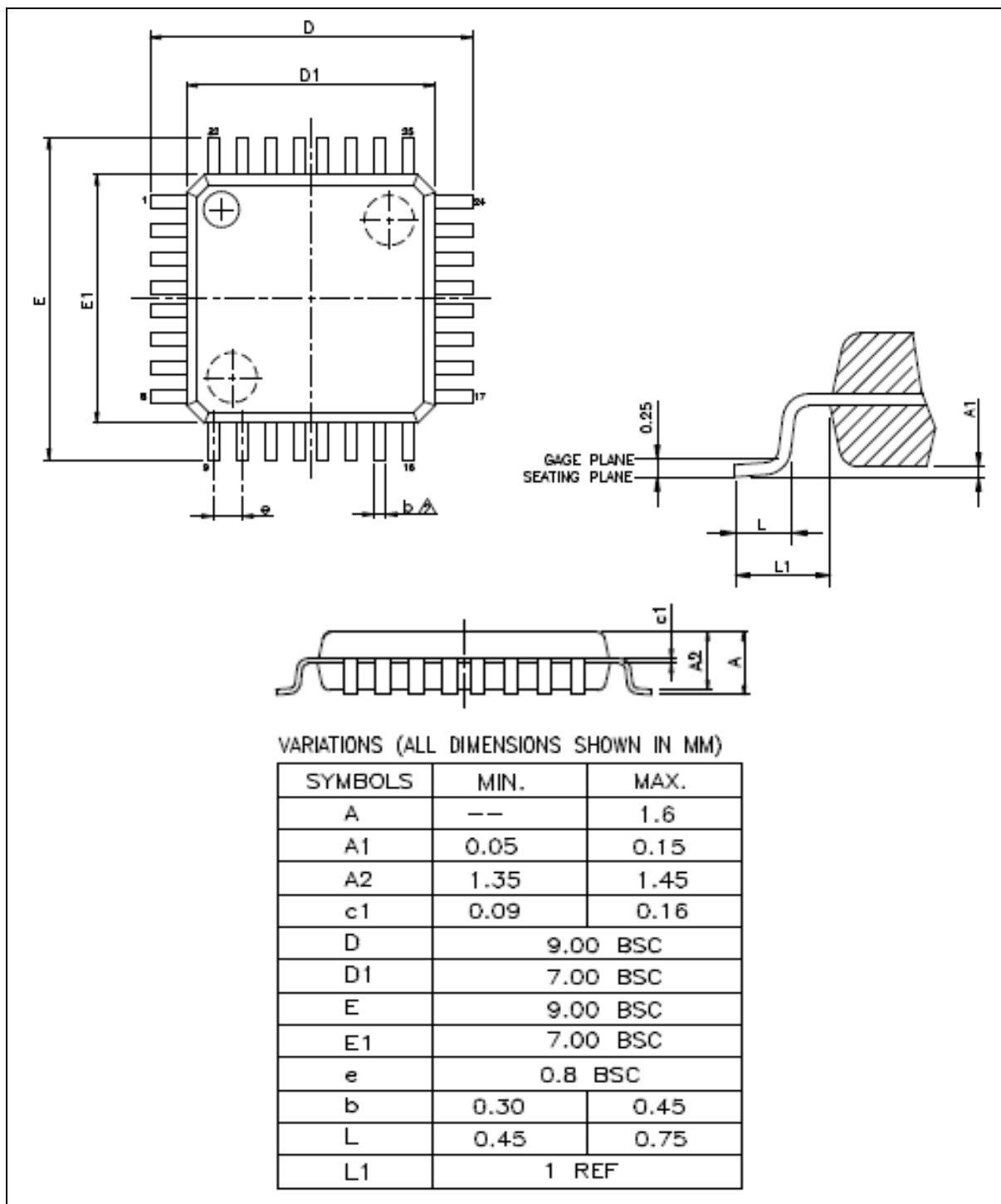


Figure 9.5-1 LQFP-32 Package Dimension

9.6 TSSOP 28-pin (4.4 x 9.7 x 1.0 mm)

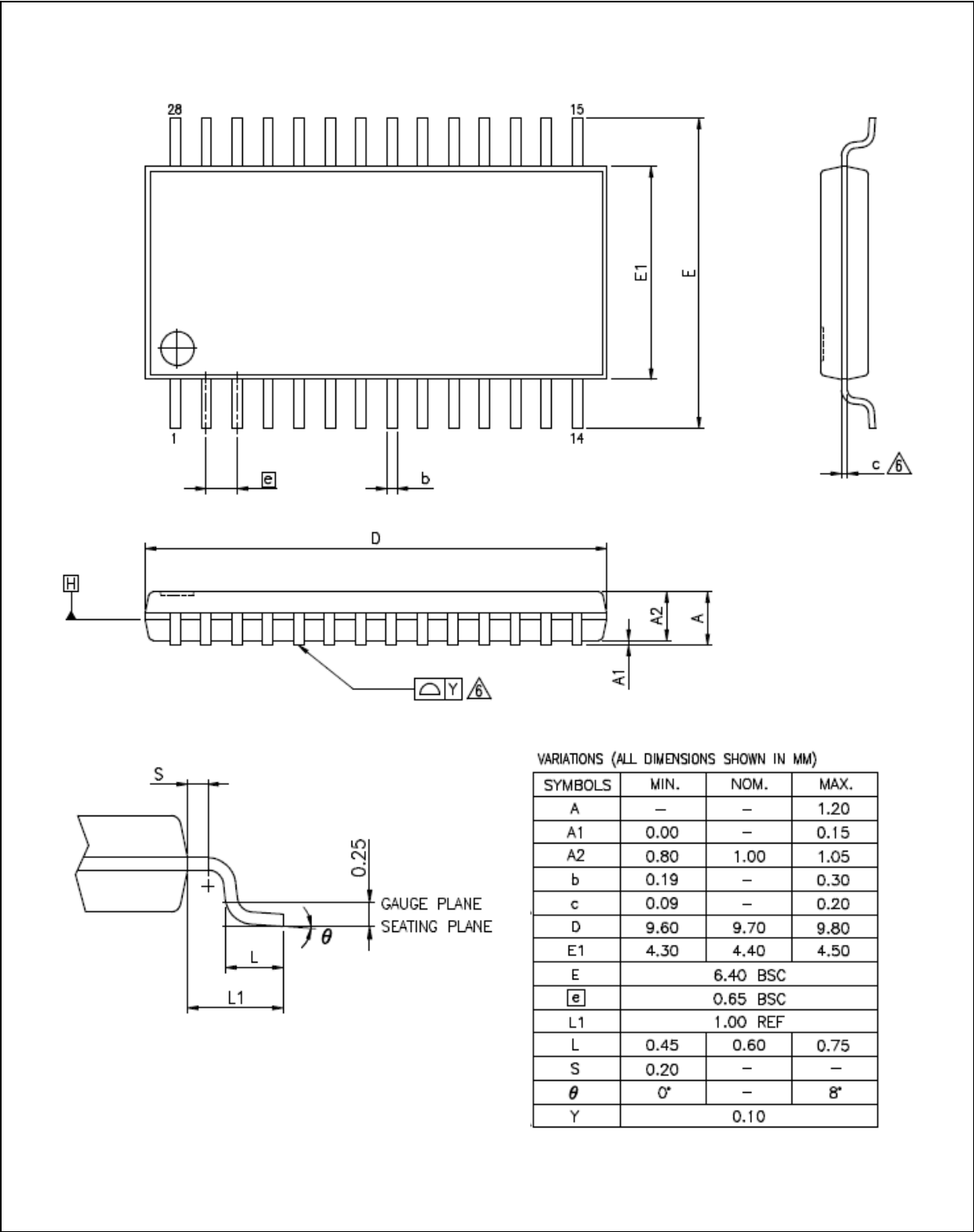


Figure 9.6-1 TSSOP-28 Package Dimension

### 9.7 SOP 28-pin (300mil)

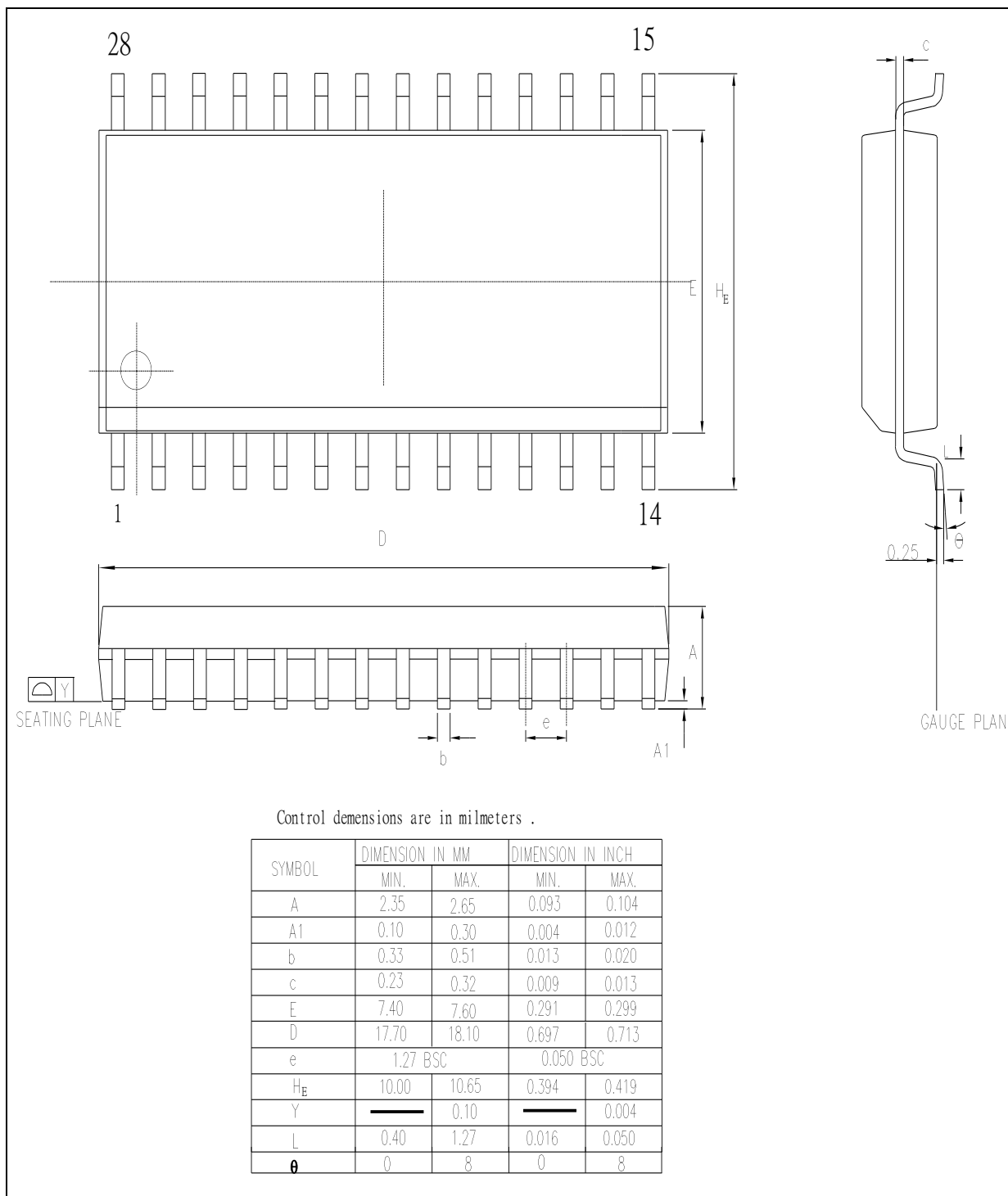


Figure 9.7-1 SOP-28 Package Dimension

9.8 TSSOP 20-pin (4.4 x 6.5 x 0.9 mm)

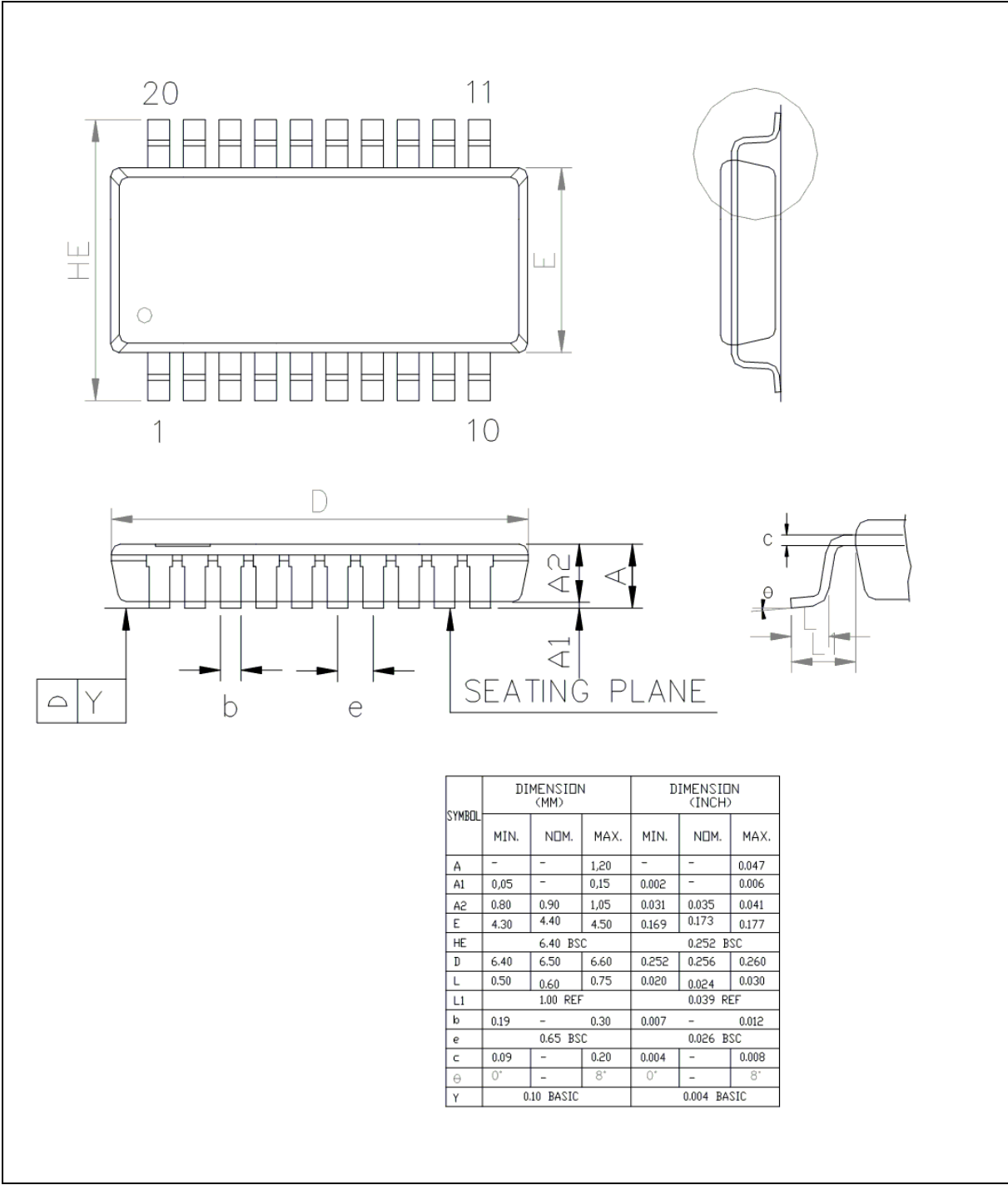


Figure 9.8-1 TSSOP-20 Package Dimension

### 9.9 SOP 20-pin (300 mil)

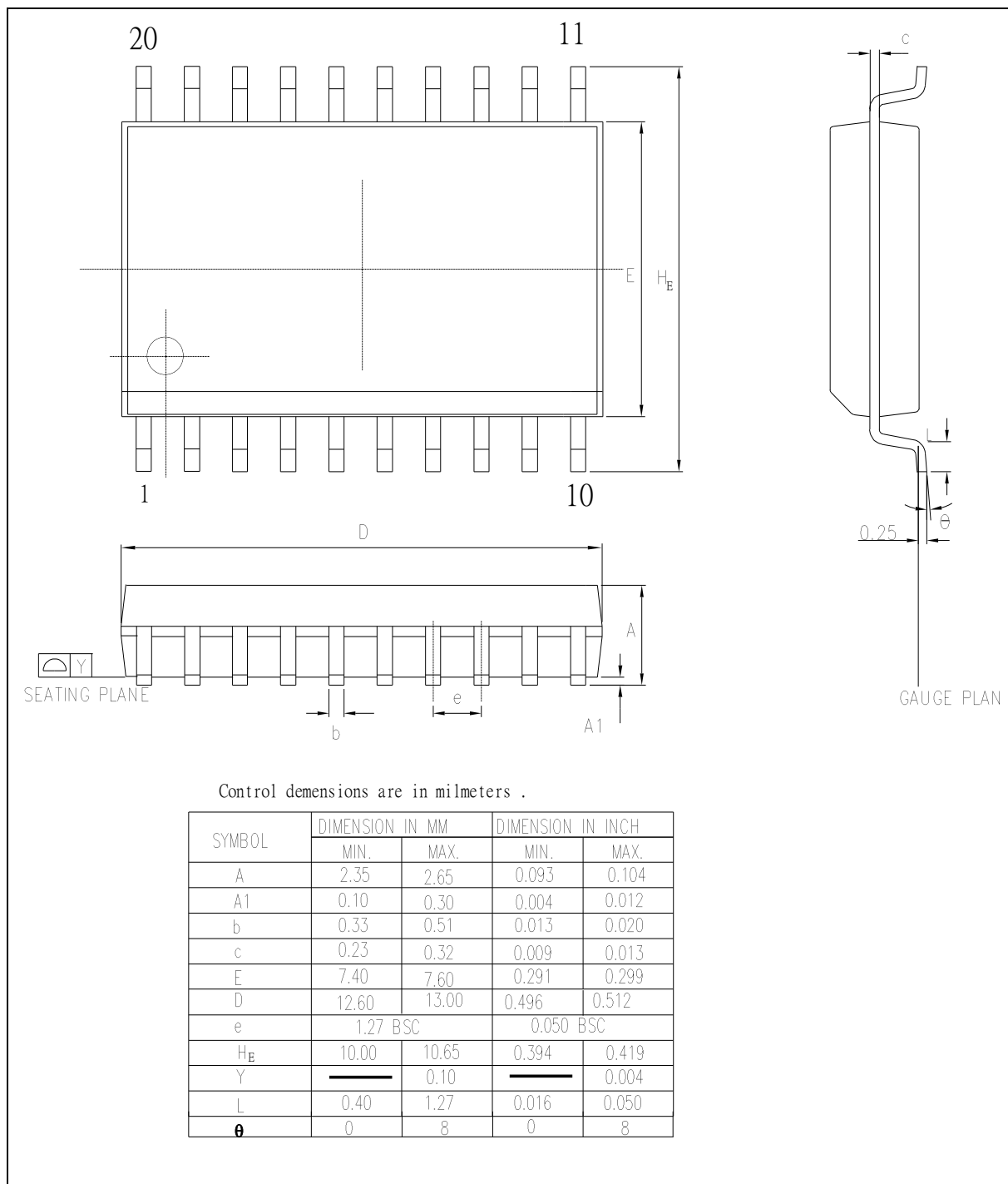


Figure 9.9-1 SOP-20 Package Dimension

9.10 QFN 20-pin ( 3.0 x 3.0 x 0.8 mm )

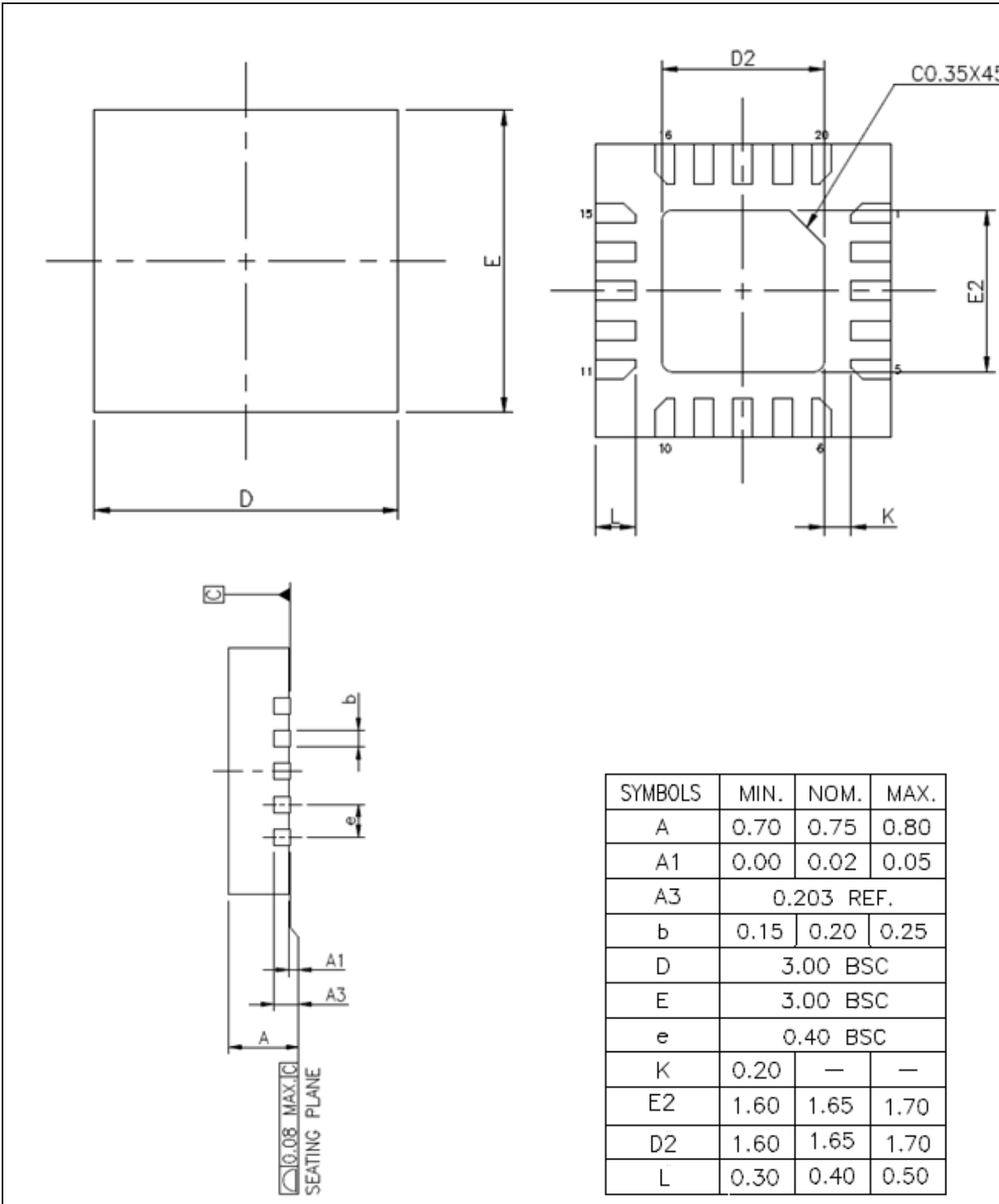


Figure 9.10-1 QFN-20 Package Dimension

### 9.11 TSSOP 14-pin (4.4 x 5.0 x 0.9 mm)

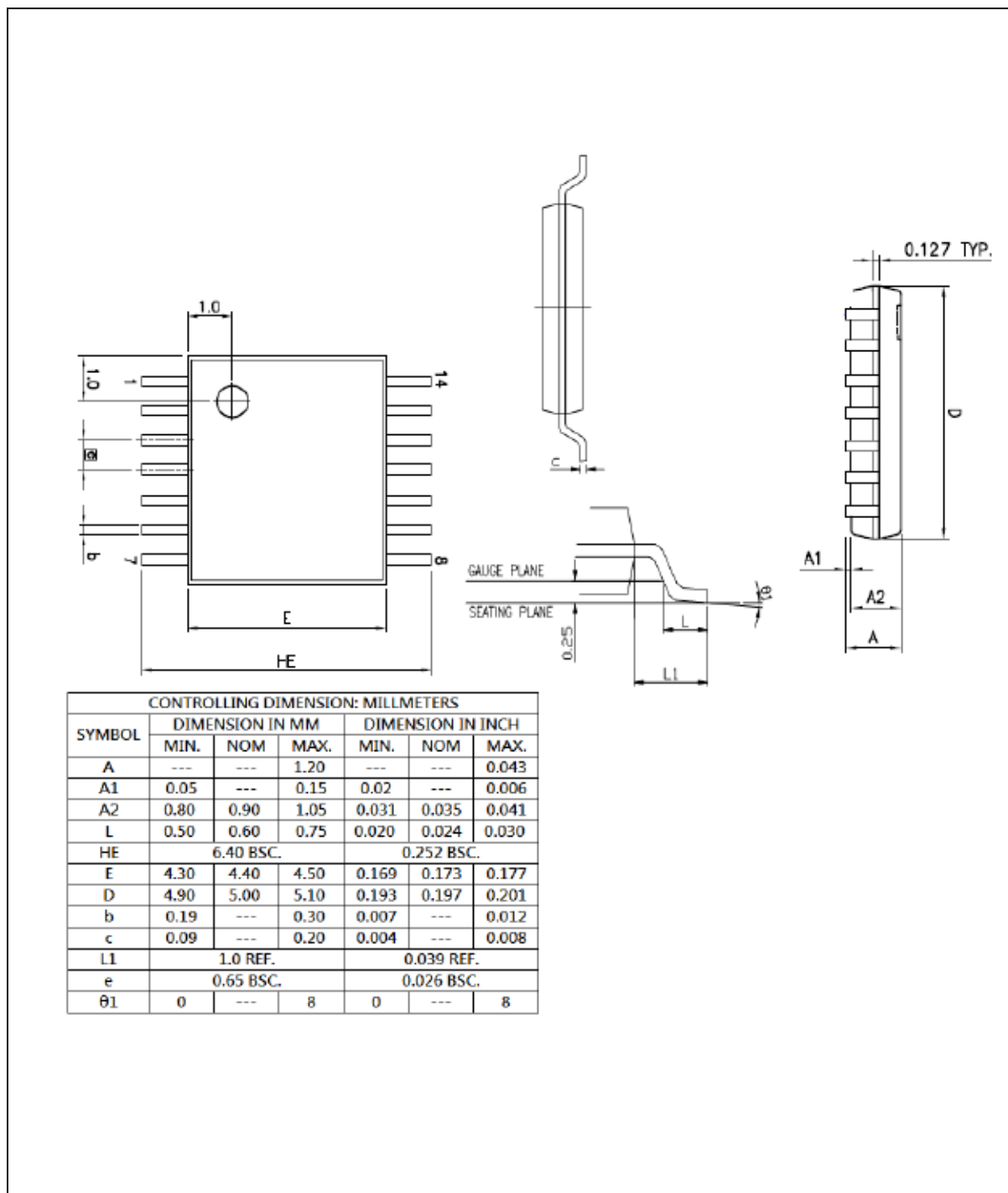


Figure 9.11-1 TSSOP-14 Package Dimension

9.12 MSOP 10-pin (3.0 x 3.0 x 0.85 mm)

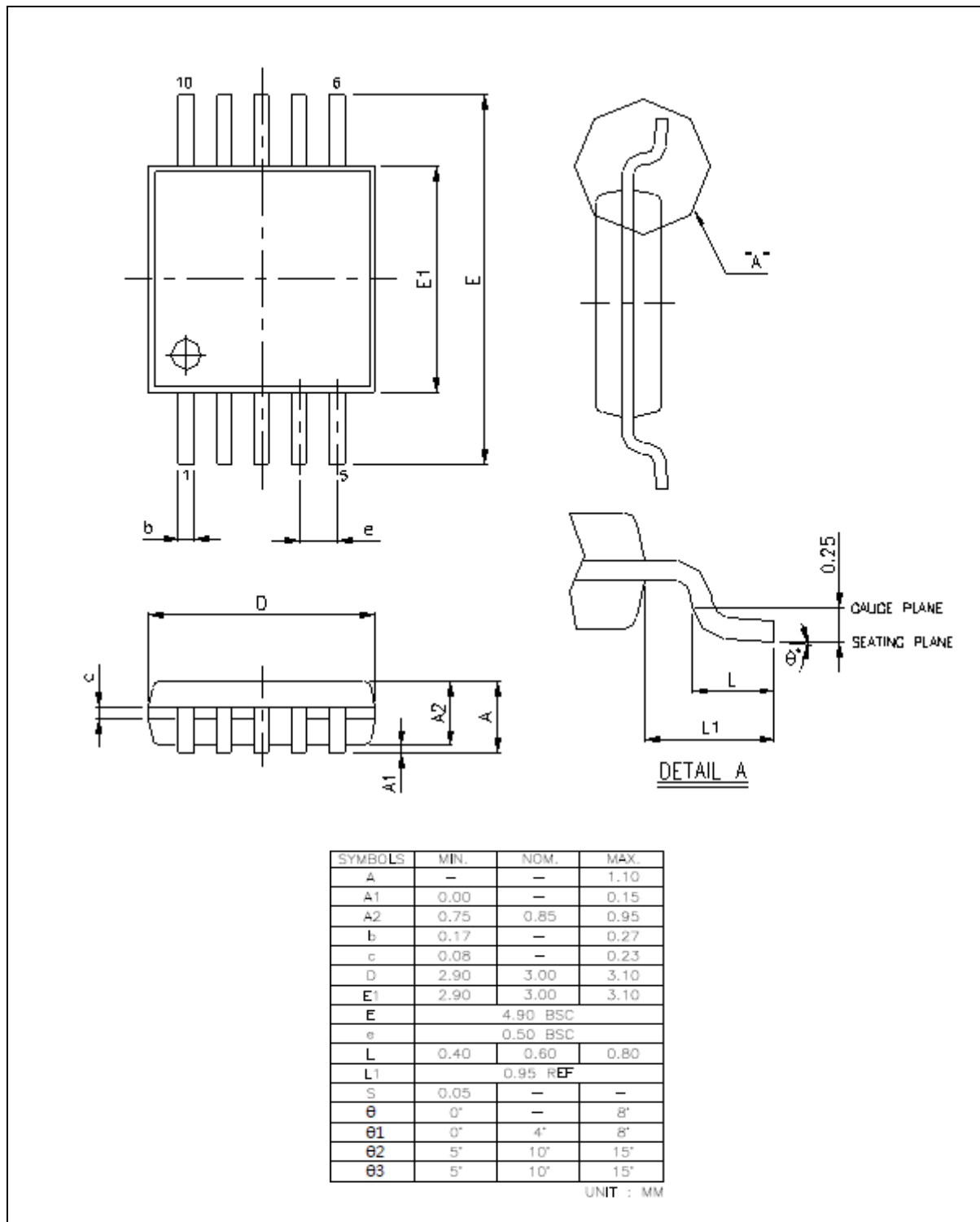


Figure 9.12-1 MSOP-10 Package Dimension

## 10 ABBREVIATIONS

### 10.1 Abbreviations

| Acronym | Description                                    |
|---------|------------------------------------------------|
| ADC     | Analog-to-Digital Converter                    |
| BOD     | Brown-out Detection                            |
| GPIO    | General-Purpose Input/Output                   |
| Fsys    | Frequency of system clock                      |
| HIRC    | 12 MHz Internal High Speed RC Oscillator       |
| IAP     | In Application Programming                     |
| ICP     | In Circuit Programming                         |
| ISP     | In System Programming                          |
| LCD     | Liquid Crystal Displays                        |
| LDO     | Low Dropout Regulator                          |
| LIRC    | 10 kHz internal low speed RC oscillator (LIRC) |
| LVR     | Low Voltage \$reset                            |
| PDMA    | Peripheral Direct Memory Access                |
| POR     | Power On Reset                                 |
| PWM     | Pulse Width Modulation                         |
| RTC     | Real Time Clock                                |
| SPI     | Serial Peripheral Interface                    |
| TK      | Touch Key                                      |
| UART    | Universal Asynchronous Receiver/Transmitter    |
| UCID    | Unique Customer ID                             |
| WKT     | Wakeup Timer                                   |
| WDT     | Watchdog Timer                                 |

Table 10.1-1 List of Abbreviations

## 11 REVISION HISTORY

| Date       | Revision | Chapter         | Description                                                                                                                |
|------------|----------|-----------------|----------------------------------------------------------------------------------------------------------------------------|
| 2018.12.05 | 1.00     |                 | Initial release.                                                                                                           |
| 2019.09.03 | 1.01     | Section 3.1     | Added package type table                                                                                                   |
|            |          | Section 4.2.2   | Added Multi-function summary table                                                                                         |
|            |          | Section 6.2     | Added ICP connect circuit                                                                                                  |
|            |          | Section 7.2.4   | Modified ISR value                                                                                                         |
|            |          | Section 7.3     | Removed 32.768kHz external clock input and deviation figure.                                                               |
|            |          | Section 7.4.1   | Modified POR/LVR/BOD operating current value                                                                               |
|            |          | Section 7.6.1   | Modified DC power supply item                                                                                              |
|            |          | Section 8.6     | Modified TSSOP20 package dimension in title                                                                                |
| 2020.03.11 | 1.02     | Section 37.6    | Modified TSSOP20 package value                                                                                             |
|            |          | Section 6.2     | Added note in application circuit                                                                                          |
|            |          | Section 7.4.2   | Added RS and CIN value in table                                                                                            |
|            |          | Section 7.4.4   | Added section 7.4.4. Moved internal voltage character table to this section                                                |
| 2020.06.29 | 1.03     | Section 8.1     | Modified QFN33 package L value to 0.3                                                                                      |
|            |          | Section 7.6.2   | Modified Maximum current to 150mA                                                                                          |
|            |          | Section 7.6.4   | Modified Pin current for latch-up value to 150mA<br>Modified Fast transient voltage burst value to 4.4kV                   |
|            |          | Section 7.4.2   | Modified ADC conversion rate and sampling timing description.                                                              |
| 2020.09.01 | 2.00     |                 | Added ML51 64KB/ML54/ML56 Series description.                                                                              |
| 2021.02.20 | 2.01     | Section 8.2.4.3 | Added GPIO Output Characteristics table                                                                                    |
|            |          | Section 8.4.2   | Updated ADC sampling timing value                                                                                          |
|            |          | Section 8.5     | Modified Supply voltage typical value to 1.5                                                                               |
| 2022.03.07 | 2.02     | Section 3.2.1   | Updated ML51 series selection guide table.                                                                                 |
|            |          | Section 4.2     | Added QFN package EPAD exposed pad description.                                                                            |
|            |          | Section 8.2.4.2 | Modified I <sub>SK</sub> Maximum value from 11mA to 12.5 mA.<br>Added R <sub>PU</sub> and R <sub>PD</sub> Resistor value   |
|            |          | Section 8.3.6   | Added description for I/O dynamic current consumption.                                                                     |
|            |          | Section 8.4.2   | Updated ADC sampling and convert rate table description.                                                                   |
|            |          | Section 8.4.6   | Updated LCD operating temperature to -40~105.<br>Updated LCD Power down current table condition from temperature 0 to -20. |
|            |          | Section 8.4.6   | Modified VLCD pin and external charge pump capacitor value.<br>Updated the V1/V2/V3 external capacitor description.        |

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