Description

The P9415 is a highly-integrated single-chip wireless power transmitter/receiver IC (TRx). The device can be configured to receive or transmit an AC power signal through magnetic induction.

When the device is configured as a wireless power transmitter, it uses an on-chip full/half-bridge inverter, a PWM generator, a modulator/demodulator for communication, and micro controller to produce an AC power signal to drive external L-C tank. As a receiver, the device receives an AC power signal from a wireless transmitter and converts it into rectified output voltage, which can be used to power devices or supply the charger input in mobile applications. The P9415 integrates a high efficiency Synchronous Full Bridge Rectifier and control circuitry to modulate the load to send message packets to the Transmitter (Tx) to optimize power delivery.

The P9415 features Multiple-time programmable (MTP) non-volatile memory to easily update control firmware and device functions.

The device includes over-temperature and voltage protection. Fault conditions associated with power transfer are managed by an industry-leading 32-bit ARM® Cortex®-M0 processor offering high level of programmability while consuming extremely low standby power. The processor can also control GPIOs to indicate operating and fault modes. The P9415 is available in an ultra-small 53-WLCSP package.

Typical Applications

- Wireless power solution for mobile applications

Features

- Single-chip medium power wireless solution
- 24kB Multiple-time programmable (MTP) non-volatile memory for expanded feature support
- WPC 1.2.4 compatible
- Delivers up to 30W as a receiver
- WattShare™ TRx mode with up to 5W Tx capability
- Embedded 32-bit ARM® Cortex®-M0 processor
- Reliable over voltage clamping
- Proprietary Rx-to-Tx modulation/demodulation for two-way communication
- High-performance LDO
- Tx-to-Rx (backchannel) communication
- Supports proprietary mode magnetic induction wireless power solutions
- Supports I2C 400kHz standard interface and GPIOs
- Package: 6 × 9 ball array, 2.82 × 4.22 × 0.50 mm, 53-WLCSP with 0.40mm ball pitch

Typical Applications Schematic

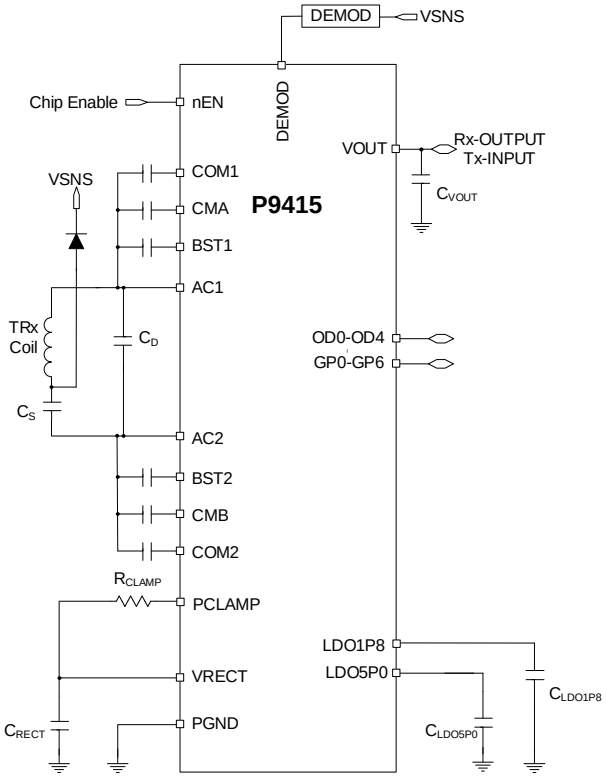

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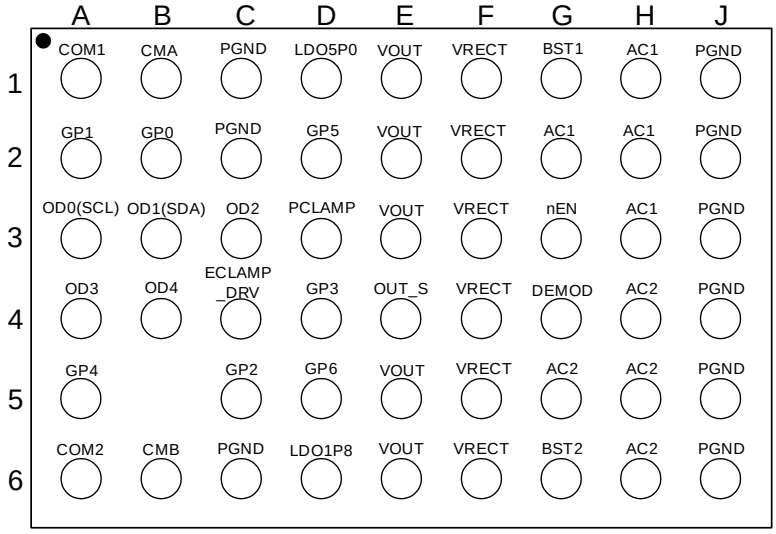
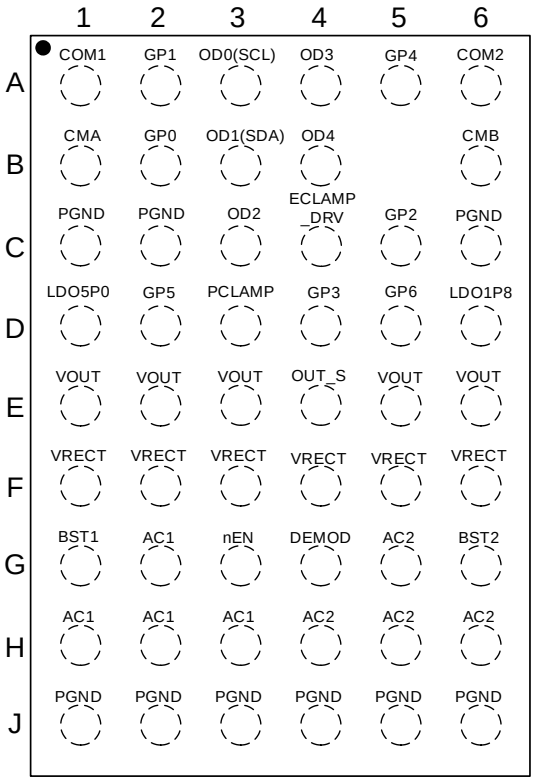
Figure 1. Pin Assignments



IDTP9415 CSP-53 (Ball View)



IDTP9415 CSP-53 (Top View)

2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
A1	COM1	O	High-voltage open-drain modulation FET. Connect a capacitor from AC1 to COM1.
A2	GP1	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
A3	OD0	I/O	Clock for I2C Serial Interface with AP (SCL). Connect a pull-up resistor to the system I/O supply.
A4	OD3	I/O	General Purpose Open Drain I/O, referenced to LDO1P8. This pin can be floating if not used.
A5	GP4	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
A6	COM2	O	High-voltage open-drain modulation FET. Connect a capacitor from AC2 to COM2.
B1	CMA	O	High-voltage open-drain modulation FET. Connect a capacitor from AC1 to CMA.
B2	GP0	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
B3	OD1	I/O	Data for I2C Serial Interface with AP (SDA). Connect a pull-up resistor to the system I/O supply.
B4	OD4	I/O	General Purpose Open Drain I/O, referenced to LDO1P8. This pin can be floating if not used.
B6	CMB	O	High-voltage open-drain modulation FET. Connect a capacitor from AC2 to CMB.
C3	OD2	I/O	General Purpose Open Drain I/O, referenced to LDO1P8. This pin can be floating if not used.
C4	ECLAMP_DRV	O	Push-Pull output driver for External Power Clamp FET gate control (Connect a resistor from Vrect to the external FET to GND). This pin can be floating if not used.
C5	GP2	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
D1	LDO5P0	O	Internal 5V LDO for chip power only (always On when Vrect is powered). Connect a capacitor to ground.
D2	GP5	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
D3	PCLAMP	I	High voltage open drain input for linear clamping during OVP events. Connect a resistor from this pin to VRECT for > 5W operation. Short directly to VRECT for 5W or lower power applications.
D4	GP3	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
D5	GP6	I/O	General Purpose Push-Pull I/O, referenced to LDO1P8. This pin can be floating if not used.
D6	LDO1P8	O	1.8V LDO for Internal Core (always on when Vrect is powered). Connect a capacitor to ground.
E1, E2, E3, E5, E6	VOUT	O	Main LDO output pin. Connect a capacitor to ground.

Pin Number	Name	Type	Description
E4	OUT_S	I	Input current positive input when operating in Tx mode with external current sense resistor. If external current sense resistor is not used, connect this pin to VOUT pins.
F1, F2, F3, F4, F5, F6	VRECT	O	Filter cap for the internal rectifier output. Connect a capacitor to ground.
G1	BST1	O	Bootstrap capacitor for driving high side N-MOSFET of the internal rectifier. Connect a capacitor from AC1 to BST1.
G2, H1, H2, H3	AC1	I/O	AC1 power input. Connect to RX LC tank (due to symmetry may connect to Rx coil or Resonance Capacitor).
G3	nEN	I	Active-low enable pin. When it is pulled-up High by the AP GPIO, the rectifier will be set in Diode mode without ASK signal modulation. While it is pulled-down Low, the rectifier can be set in any predefined modes.
G5, H4, H5, H6	AC2	I/O	AC2 power input. Connect to RX LC tank (due to symmetry may connect to Rx coil or Resonance Capacitor).
G4	DEMOD	I	Tx mode Communication Demodulator input. Connect to LC node via diode and DEMOD filter.
G6	BST2	O	Bootstrap capacitor for driving the high side N-MOSFET of the internal rectifier. Connect a capacitor from AC2 to BST2.
C1, C2, C6, J1, J2, J3, J4, J5, J6	PGND	GND	Power Ground. All PGND pins must be connected together externally.

[a] Note - 'I' = Input (Digital or Analog), 'O' = Output (Digital).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the P9415 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol/Pins	Parameter	Minimum	Maximum	Units
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	°C
HBM	ESD – Human Body Model	-	2000	V
CDM	ESD – Charged Device Model	-	500	V
CMA, CMB, COM1, COM2, PCLAMP, VRECT, AC1, AC2	Maximum voltage	-0.3	26.5	V
BST1, BST2	Maximum voltage	-0.3	AC1+5, AC2+5	V
LDO1P8, GP0-GP6	Maximum voltage	-0.3	2	V
LDO5P0, DEMOD, nEN, ECLAMP_DRV, OD0-OD4	Maximum voltage	-0.3	6	V
PGND	Maximum voltage	-0.3	0.3	V
VOUT	Maximum voltage	-0.3	21	V
CMA, CMB, COM1, COM2	Maximum RMS current		500	mA
AC1, AC2	Maximum RMS current		2	A
VOUT Output Current	Maximum RMS current		1.9	A

4. Thermal Characteristics

Table 3. Thermal Characteristics[a][b][c][d]

Symbol	Parameter	Value	Units
θ_{JA}	Theta JA. Junction to ambient.	45	°C/W
θ_{JB}	Theta JB. Junction to board.	4.36	°C/W
θ_{JC}	Theta JC. Junction to case.	0.2	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)	MSL 1	-

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3” x 4.5” in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

[d] For the WLCSP (AWQ53) package, connecting 8 PGND balls and at least two other CSP balls (10 thermal balls total) to internal/external ground planes from top to bottom sides of the PCB is recommended for improving the overall thermal performance.

5. Electrical Characteristics Table

V_{RECT} = 5.5 V[a], C_{LDO1P8_OUT} = C_{LDO5P0_OUT} = 2.2µF, C_{MLDO_VOUT} = 10 µF, nEN = 0V, unless otherwise noted. T_J =-5°C to 125°C, Typical values are at 25°C.

Table 4. Device Characteristics

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
V_{RECT} and Under-voltage Lock-out (Rx Mode)						
$V_{IN\_VRECT\_Rx}$[b][e]	V_{RECT} Input Operating Voltage Range Rx		3.5		23.5	V
$V_{UVLO\_RISING\_Rx}$	UVLO Rising Rx	Rising voltage on VRECT, no load		2.55	2.8	V
$V_{UVLO\_HYS\_Rx}$	UVLO Hysteresis Rx	Falling hysteresis voltage on VRECT (LDO shutdown)		150		mV
Over-voltage Protection						
V_{OVP}	Over-voltage Protection	OVP interrupt rising voltage on VRECT (Default setting 24.7V)	23.6	24.7	26.4	V
$V_{OVP\text{-}HYS}$	Over-voltage Hysteresis			1.5		V
V_{PCLAMP}	Pclamp Over-voltage Protection	Pre-clamp OVP, rising voltage on V_{RECT}		23.4		V
Quiescent Current						
$I_{RECT\text{-}ACTIVE}$	I_{RECT} Active Current	No external load on VRECT, LDO5P0, LDO1P8; Rectifier not switching		6	15	mA
LDO1P8 Drop Out Regulator (For Internal Usage Only)[f]						
V_{LDO1P8}[f]	LDO1P8 output voltage		1.62	1.8	1.98	V
I_{LDO1P8_LMT}	Current Limit			60		mA
$\Delta V_{LDO1P8\_OUT\_LINE}$	Line Regulation	V_{RECT} = 3.5V to 23.5V, I_{OUT} = 10mA	-5		+5	%
$\Delta V_{LDO1P8\_OUT\_LOAD}$	Load Regulation	I_{OUT} = 1mA to 40mA	-5		+5	%
LDO5P0[c] Drop Out Regulator (For Internal Use Only)						
V_{LDO5P0}	LDO5P0 Output voltage		4.5	5	5.5	V
Main Low-Drop-Out Regulator (VOUT)						
V_{MLDO}	Regulated Output Voltage on VOUT	V_{RECT} = 5.5V, I_{OUT} = 1.33A	4.80	5	5.20	V
		V_{RECT} = 9.5V, I_{OUT} = 1.33A	8.80	9	9.20	V
		V_{RECT} = 15.5V, I_{OUT} = 1.33A	14.75	15	15.25	V
		V_{RECT} = 19.5V, I_{OUT} = 1.33A	18.70	19	19.30	V
		V_{RECT} = 20.5V, I_{OUT} = 1.33A	19.60	20	20.40	V
V_{MLDO_STEP}	MLDO Output Voltage Step			100		mV

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
$\Delta V_{MLDO\_VOUT\_LINE}$	Line Regulation	VRECT = 5.5V to 20.5V, V_{OUT} = 5V, I_{OUT} = 20mA		10	100	mV
$\Delta V_{MLDO\_VOUT\_LOAD}$	Load Regulation	I_{OUT} = 20mA to 1.33A, V_{OUT} = 5V		30	90	mV
I_{OUT_MAX}	Maximum IOUT V_{OUT} = 5V to 20V	I_{MLDO_ILMT} = 1.9A[d][h]	1.6			A
FET RDS_{ON}						
R_{DSON_MLDO}	Main LDO			40		mΩ
R_{DSON_RECT}	Rectifier			50		mΩ
$R_{DSON\_CMA/CMB/COM1/COM2}$	Communication A/B/1/2			1		Ω
Input Supplies and UVLO (Tx Mode, V_{IN_VOUT} = 7.5V)						
$V_{IN\_VOUT\_Tx}$[b][e]	V_{OUT} Input Operating Voltage Range Tx		4.5	7.5	12	V
$V_{IN\_UVLO\_Tx}$	Under-Voltage Lockout Tx	V_{IN} Rising, power into VOUT pin		3.1	3.4	V
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			67.5		kSa/s
$V_{IN,FS}$[g]	Full scale Input voltage			2.1		V
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		140		°C
		Threshold Falling		130		°C
Enable Input nEN						
V_{IH}	Input Threshold High		1.6			V
V_{IL}	Input Threshold Low				0.25	V
I_{nEN_LKG}	nEN Leakage Current	V_{nEN} = 0V	-1		1	µA
		V_{nEN} = 5.0V		2.5		µA
Open Drain Inputs/Outputs (SCL, SDA, OD2, OD3, OD4)						
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.5	V
I_{LKG}	Input Leakage Current	V = 0V and 5V; Digital or ADC input mode.	-1		1	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA			0.36	V

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
Push-Pull General Purpose Inputs/Outputs (GP0, GP1, GP2, GP3, GP4, GP5, GP6)						
V_{IH}	Input High Voltage		1.4			V
V_{IL}	Input Low Voltage				0.65	V
I_{LKG}	Input Leakage Current	V = 0V and 1.8V; Digital or ADC input mode	-1.5		1.5	µA
V_{OH}	Output High Voltage	I_{OH} = 8mA (for all combined GPIOs)	1.44			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA (for all combined GPIOs)			0.4	V
ECLAMP_DRV Output						
V_{OH}	Output High Voltage	I_{OH} = 8 mA	4.0	4.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.6		V
SCL, SDA (I^2C Interfaces SCL (OD0), SDA (OD1)						
f_{SCL}	Clock Frequency				400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line			150		pF
C_I	SCL, SDA Input Capacitance			5		pF

[a] V_{RECT} may exceed 23.5V but the device EC table limits are not guaranteed under this condition.

[b] Input Voltage Operating Range is dependent upon the type of Transmitter Power Stage (full-bridge, half-bridge) and Transmitting Coil Inductance. WPC Specifications should be consulted for appropriate input voltage ranges by end product type.

[c] Do not externally load. For internal biasing only.

[d] Guaranteed by design and not subject to 100% production testing.

[e] Full power transfer will not occur at the minimum IC operating specification.

[f] LDO1P8 pin can only be loaded as shown in reference schematics.

[g] Any open-drain GPIO pin (SCL, SDA, OD2, OD3, OD4) that is connected as an input to the ADC should stay below 2.1V to prevent saturation of the ADC, and any push-pull GPIO pin (GP0, GP1, GP2, GP3, GP4, GP5, GP6) connected to the ADC, the voltage must be ≤ LDO1P8 to avoid interference with the LDO1P8 power supply.

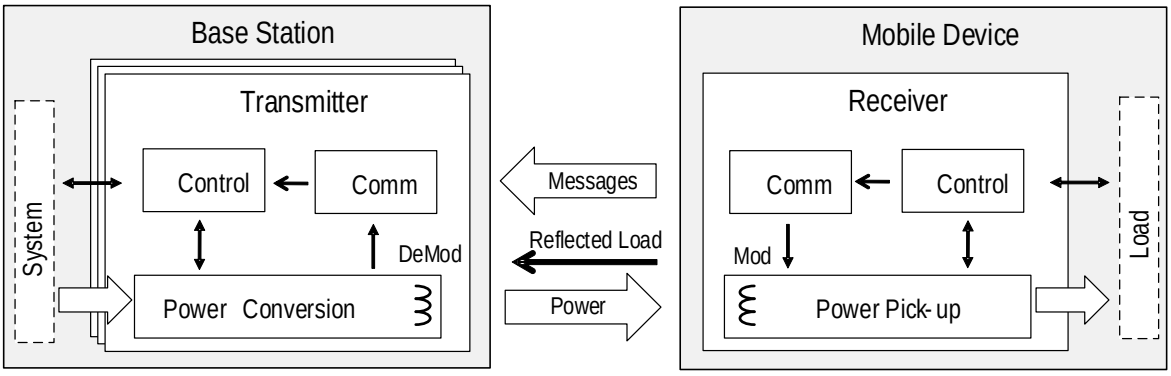
[h] The test condition is up to 55°C.

6. Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s), and transmit the power over a strongly-coupled inductor pair (magnetic induction) or over a loosely-coupled inductor pair (magnetic resonance) to a receiver in a mobile device. A WPC[1] system uses near field magnetic induction between coils and can be a free-positioning or magnetically-guided type of system.

In WPC systems, the amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The bit rate for Rx-to-Tx communication link is 2kbps for WPC receivers and is amplitude modulated (ASK) on top of the power link that exists.

Figure 2. Block Diagram of WPC System

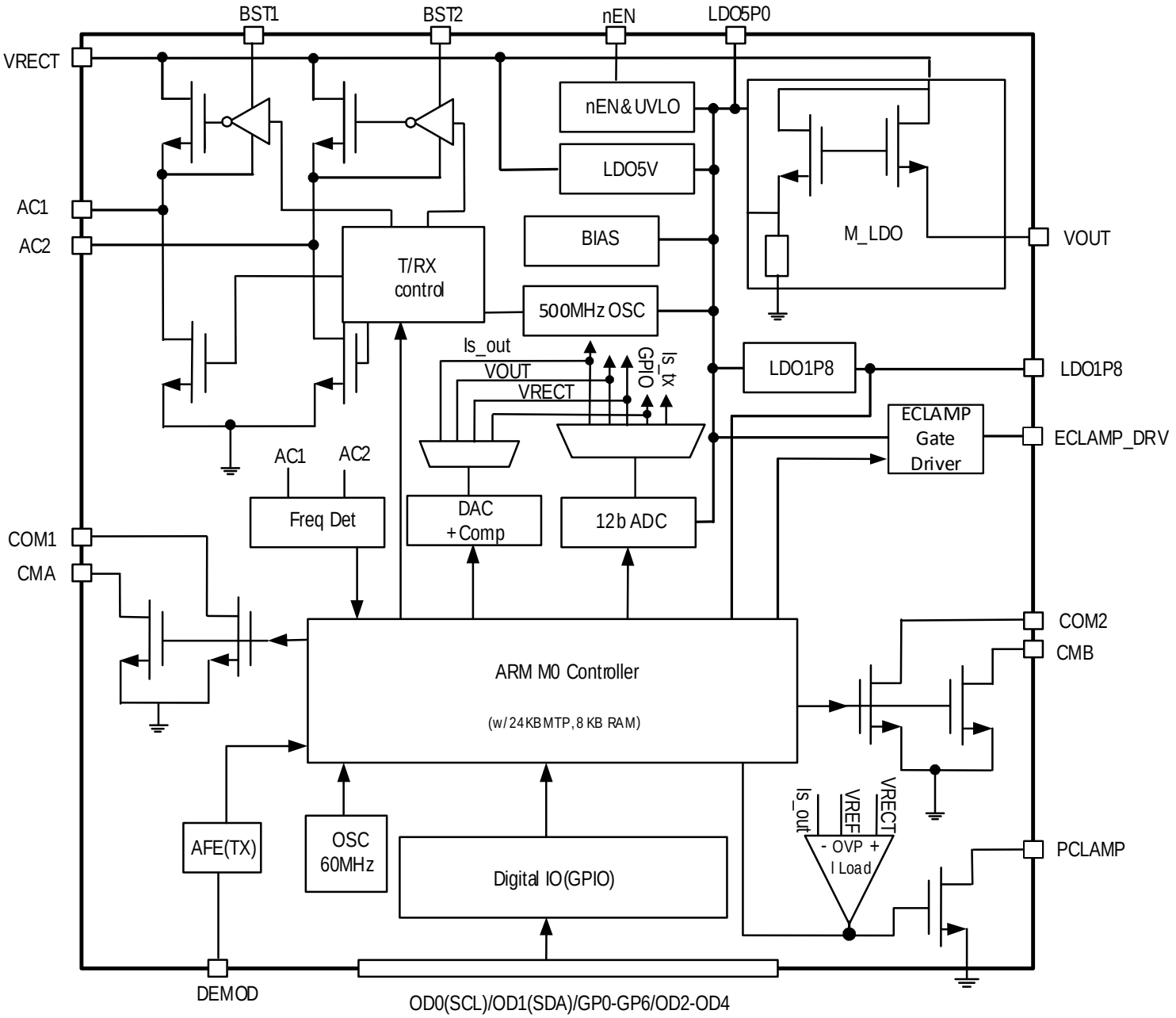


[1] For the most current information, see the WPC specification at http://www.wirelesspowerconsortium.com/.

7. Theory of Operation

The P9415 is a highly-integrated wireless power receiver IC for mobile devices. The device can receive up to 30W wirelessly using near-field magnetic induction. The P9415 Rx will operate in WPC mode when the digital ping frequency is below 190 kHz from the transmitter.

Figure 3. Internal Block Diagram



7.1 Overview

The simplified internal block diagram of the P9415 is shown in Figure 3. External Rx coil(s) and CS capacitor(s) as shown in Figure 1 transfer energy wirelessly using the P9415 AC1 and AC2 pins to be full-wave-rectified (AC-to-DC).

The wireless power is stored on a capacitor(s) connected to VRECT. Until the voltage across the VRECT capacitor exceeds the UVLO threshold, the rectification is performed by the body diodes of the Synchronous Full Bridge Rectifier FETs. After the internal biasing circuit is enabled, the Driver and Control block operate the MOSFET switches of the rectifier in various modes to maintain reliable connections at optimal efficiency. An internal ADC monitors the voltage at VRECT and the load current, the P9415 sends instructions to the wireless power transmitter to increase or decrease the amount of power transferred or to terminate power transmission based on these readings. The voltage at the output of the P9415 Main Low-Drop-Out (LDO) regulator is programmed up to 20V using I2C commands. The internal temperature is continuously monitored to ensure proper operation.

The voltage at VRECT and the current through the rectifier are sampled periodically and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the internal control logic, which decides whether the loading conditions on VRECT indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at VRECT below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at VRECT is higher than its target, the transmitter is instructed to increase its frequency. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO's load current increases.

7.2 WPC Mode Characteristics

7.2.1 Startup

When a mobile device containing the P9415 is placed on a WPC "Qi" charging pad, it responds to the transmitter's "ping" signal by rectifying the AC power from the transmitter and storing it on a capacitor connected to VRECT. During the "Ping" phase, once the rectifier provides voltage at the VRECT pin above the UVLO threshold, the digital section of the P9415 enables communication. The control loop of the P9415 adjusts the rectifier voltage by sending error packets to the transmitter before and after it enables the VOUT LDO.

The VOUT LDO is enabled when the power transfer mode is initiated and the voltage at VRECT, the output of the full-wave synchronous rectifier reaches the target voltage that includes headroom in addition to the LDO VOUT target voltage. For example, if the VOUT voltage target is 12V, the target VRECT voltage is VOUT + headroom, where headroom is a function of the output current.

7.2.2 Power Transfer

Once the "identification and configuration" phase is completed and successful "negotiation and calibration" is made, then the transmitter initiates power transfer mode. The P9415 control circuit measures the rectifier voltage and sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the main LDO linear regulator and to notify the Tx of the current Rectified Power Packet for Foreign Object Detection (FOD) to guarantee safe efficient power transfer. The P9415 is compatible with WPC (latest specification) and can use compatible Rx coils. Each receiver coil type has a unique inductance value. As such, a unique resonant capacitor (C_S) is used for a given type of receiver coil.

7.2.3 Advanced Foreign Object Detection (FOD) WPC MODE

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of parasitic metal objects are coins, keys, paperclips, etc. The amount of heating depends on the amplitude and frequency of the magnetic field coupled, as well as on the characteristics of the object such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduced power transfer efficiency. Moreover, if no appropriate measures are taken, the heating could lead to unsafe situations if the objects reach high temperatures.

WPC power transmitters and receivers also need to compensate for the power loss due to parasitic metals intentionally designed into the final product: i.e., metals that are neither part of the power transmitter, nor of the power receiver, but which absorb power from magnetic field coupling during power transfer, such as Li-ion batteries, metallic cases, etc.

The P9415 uses advanced FOD techniques to detect foreign objects placed on or near the transmitter base station. The FOD algorithm includes values that are programmable through either the I²C interface or MTP (Multi-Time Programmable) bits. Programmability is necessary so that the FOD settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the Tx and Rx coils, battery, shielding, and case materials under no load to full load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

The P9415 FOD values need to be tuned prior to production for WPC compliance using final production hardware and coils.

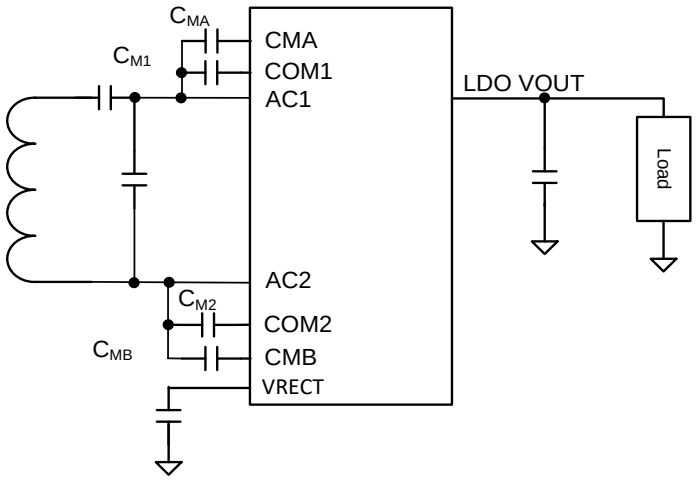
7.2.4 Status/Interrupt Output

When the power transfer connection is established and stable, the VOUT LDO is enabled. GPOD and GPIO pins can be connected to the AP to perform status and interrupt commands.

7.2.5 WPC Modulation/Communication

The P9415 operates in WPC using a single LC tank Rx coil and requires AC modulation capacitor connections for WPC communication. The LC tank also should be tuned to achieve maximum efficiency (C_{MA}, C_{MB}, C_{M1}, C_{M2} connected to pins CMA, CMB COM1, COM2) in order to accomplish WPC modulation.

Figure 4. Rx Modulation Components



Receiver-to-transmitter communication is completed by modulating the load applied to the receiver's inductor. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. Modulation is done with AC Modulation, using internal switches to connect external capacitors from AC1 and AC2 to ground.

The P9415 communicates with the base via communication packets or decodes messages sent by WPC Rx's. Each communication packet has the following structure:

Figure 5. Communication Packet Structure

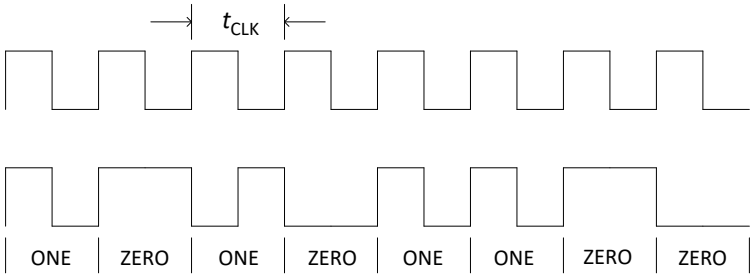
Preamble	Header	Message	Checksum

According to the WPC specification, the power receiver communicates with the power transmitter using backscatter modulation. The load seen by the power transmitter's inductor is modulated on the receiver side to send packets. The power transmitter demodulates these signals as a modulation of coil current/voltage to decode and receive packets.

7.2.6 Bit Encoding Scheme

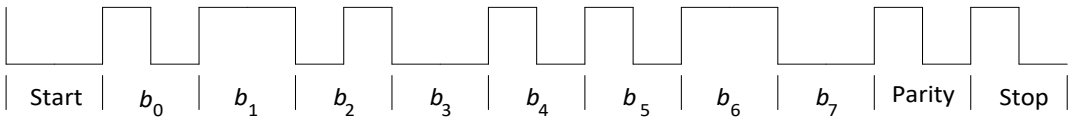
As required by the WPC, the P9415 uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using two wider transitions as shown below:

Figure 6. Bit Encoding Scheme



Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown below:

Figure 7. Byte Encoding Scheme

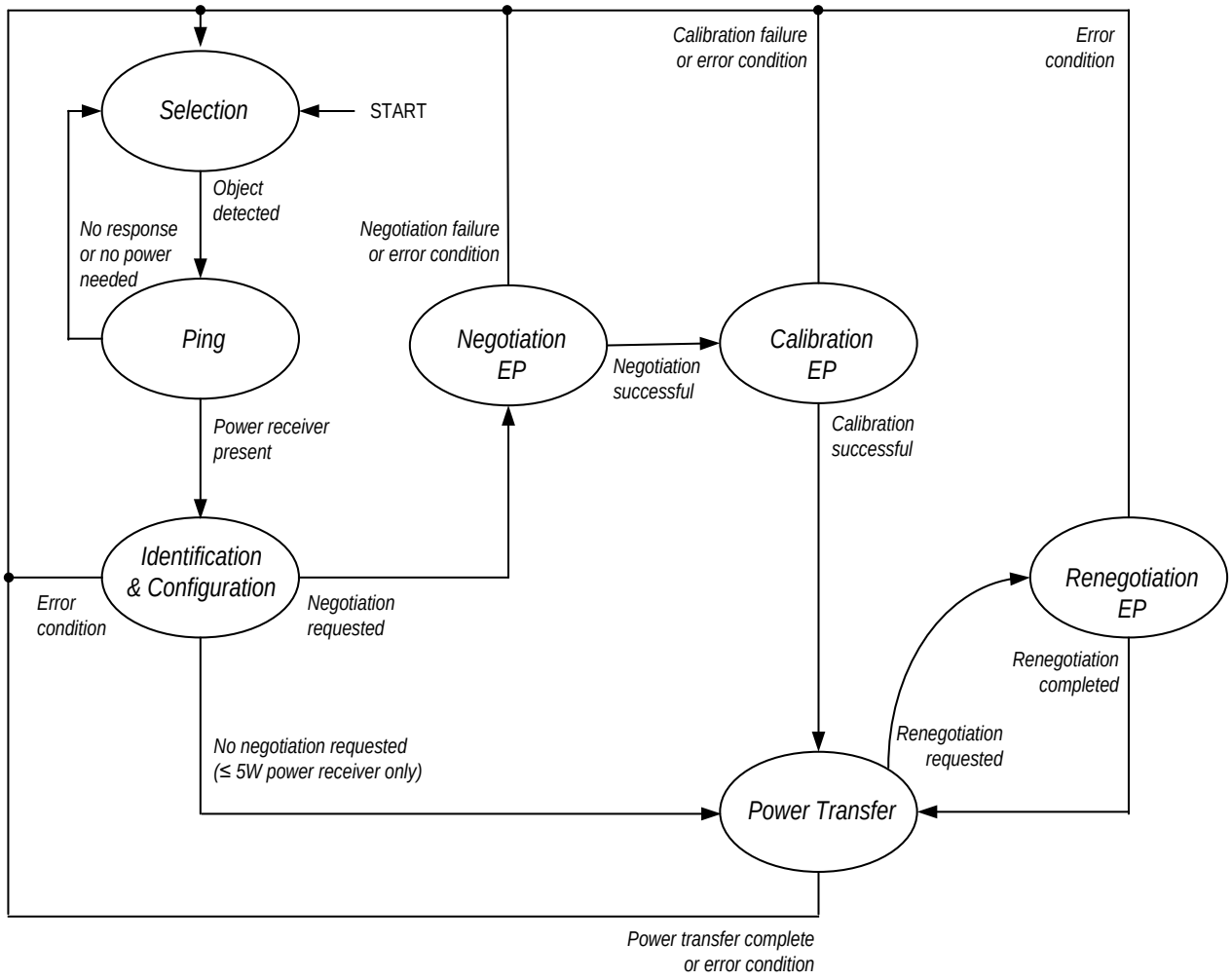


Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

7.2.7 System Feedback Control

The P9415 is fully compatible with WPC (latest specification) and has all necessary circuitry to communicate with the base station or with a receiver via WPC communication packets. The overall WPC system behavior between the transmitter and receiver follows the state machine in Figure 8.

Figure 8. WPC System Feedback Control



The P9415 goes through six phases: Selection, Ping, Identification & Configuration, Negotiation, Calibration, and Power Transfer.

7.2.8 Selection

In this phase, the P9415 senses or delivers the wireless power and proceeds to the Ping state. It monitors the rectified voltage or DEMOD signal, and when the voltage is above the V_{UVLO_rising} threshold, the P9415 prepares to communicate with the base station or enter power Ping mode.

7.2.9 Ping

In this phase, the P9415 transmits a Signal Strength Packet as the first communication packet to instruct the base to keep the power signal ON (or the P9415 detects a Signal Strength Packet). After sending/receiving the Signal Strength Packet, the P9415 proceeds to the Identification and Configuration phase. If, instead, an End of Power Packet is sent or an invalid response is sent, then it remains in the Ping phase.

In this phase, the P9415 sends/expects the following packets:

- Signal Strength Packet
- End of Power Packet

7.2.10 Identification and Configuration (ID and Config)

In this phase, the P9415 sends or expects the following packets:

- Identification Packet
- Configuration Packet

After the transmission of the Configuration Packet, the P9415 proceeds to the Negotiation phase.

7.2.11 Negotiation

The Power Receiver negotiates with the Power Transmitter to fine-tune the Power Transfer Contract. For this purpose, the Power Receiver sends negotiation requests to the Power Transmitter, where the Power Transmitter can grant or deny.

7.2.12 Calibration

The Power Receiver provides its Received Power back to the Power Transmitter.

7.2.13 Power Transfer

In this phase, the P9415 controls the power transfer by means of the following Control Data Packets:

- Control Error Packets
- Rectified Power Packet
- End Power Transfer Packet

7.2.14 Renegotiation

In this phase, the Power Receiver can make adjustments to the Power Transfer Contract, if required. If necessary, this phase can be aborted prematurely without changing the Power Transfer Contract.

7.2.15 End of Power Transfer (EPT)

In the event of EPT, the device turns off the LDO only after the AP instructs the P9415 to continuously send End of Power (EPT) packets until the transmitter removes the power and the rectifier voltage on the receiver side drops below the UVLO threshold.

7.3 Rx Mode Functions

7.3.1 Status and Interrupt Indicators

The P9415 has five General Purpose Open Drain (GPOD) pins and seven General Purpose Input Output (GPIO) pins. These GP pins can be configured to meet a wide variety of signaling and sensing requirements to meet end application requirements. The GPIO pins can be push-pull input/outputs, and the GPOD pins can be open-drain inputs/outputs. These digital pins are internally biased or referenced to one of the 1.8V and 5V voltage rail. The GPIO pins must not be directly connected to GND to avoid overcurrent conditions forced upon the output. Resistive pull-downs on the GPIO pins should be ≥ 2 kΩ. When any of the GPOD or GPIO pins are used for analog voltage measurements using the internal ADC, the voltage should be limited to < 1.8 V in order to avoid saturating the ADC or forcing a voltage above the reference voltage rail.

7.3.2 Multiple-Time Programming Memory

The P9415 includes MTP or “pseudo-flash” capability with re-programming up to 1000 times. This offers the advantage of re-programming during pre-production phase to optimize performance and/or re-programming for field upgrades when required. The device contains 24 KB of MTP memory. The MTP programming voltage range is based on the “On-the-Go” (OTG) specification of 5V power (±10%) applied to VRECT via the VOUT pin.

7.3.3 Synchronous Rectifier

The efficiency of the full-bridge rectifier in the P9415 is increased by implementing it as a synchronous rectifier. The rectifier comprises four internally-driven switches that work in a full synchronous mode of operation when the load applied to VOUT is higher than the programmed threshold value. Below that threshold, the rectifier works in half-synchronous rectification mode. In half-synchronous rectification mode, only the low-side N-MOSFETs are driven and the high-side N-MOSFETs are forced into diode mode. At power-up, when the voltage is below the UVLO threshold, the rectifier works by using the body diodes associated with the NMOS transistors. The BST capacitors are used to provide power to drive the gates of high-side NMOS switches.

7.3.4 Rectifier and VRECT Level

Once VRECT powers up to greater than UVLO, the full-bridge rectifier switches to half synchronous or full synchronous mode (depending on the loading conditions) to efficiently transfer energy from the transmitter to the load applied to VOUT. The control loop of the P9415 maintains the rectifier voltage between 5V and 23.5V, depending on the output current (I_{OUT}) and the programmed output voltage. VRECT must not be directly loaded.

7.3.5 Over-voltage Protection

In the event that the VRECT voltage increases above the OVP voltage set point, the control loop sends an interrupt to the appropriate system AP, initiates internal self-clamping, and sends error packets/frequency increment commands to the transmitter in an attempt to bring the rectifier voltage back to a safe operating voltage level while simultaneously clamping the incoming energy using internal clamping circuitry. The clamp is released when the VRECT voltage falls below the V_{OVP} hysteresis falling level. If the condition persists an End of Power request is made to the transmitter.

7.3.6 Over Current Protection, Over Temperature Protection, and Thermal Shutdown

The P9415 uses over-current (OC) protection and over-temperature (OT) protection by sending an interrupt to the appropriate system AP. Thermal shutdown (TSD) is also supported with End Power Transfer packets sent by the P9415 to the transmitter.

The current limit level is set by firmware, and is dependent upon the maximum output current needed. If the MLDO output current exceeds the programmed current limit then an OC condition exists and an interrupt is sent to the AP. The MLDO will attempt to limit the output current to the over-current setpoint by reducing the output voltage proportionally to the amount of current being consumed above the OCP limit. Operating the P9415 in OCP mode will cause VOUT to decrease, which will create a voltage difference between Vrect and VOUT and the device temperature will increase.

The internal device temperature is monitored, and the P9415 reports an over-temperature condition interrupt to the AP if the temperature exceeds 130°C typically (Internally fixed level). The P9415 will generate another interrupt when the temperature falls below approximately 130°C. If the temperature exceeds 140°C typically, a thermal shutdown condition exists and the receiver will start sending “End Power Transfer” packets with an “over-temperature condition” code until the transmitter removes the power. Power will resume when the transmitter reapplies the ping and the process will repeat.

7.3.7 Enable Input

The P9415 can be disabled by applying a logic high to the nEN pin. When the nEN pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active. The P9415 should not be disabled at any time during power transfer. In order to utilize the /EN pin function, wireless power should be terminated via and EPT command, then once power is removed, /EN high may be asserted.

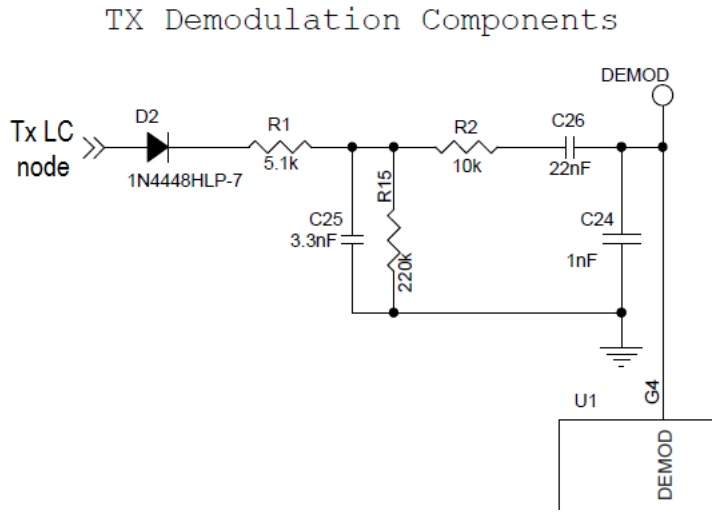
7.3.8 LDO Regulators

The P9415 has three LDOs. The Main LDO (VOUT pin) is programmable from 5V to 20V and LDO5P0 are powered by VRECT. LDO1P8 is powered by LDO5P0. Both LDO5P0 and LDO1P8 are used for supplying power to internal low voltage blocks. The LDOs must have local ceramic bypass capacitors placed near the P9415.

7.4 Tx Mode

Power is transmitted using the VOUT pins as the input; this is the same node as the Rx output when in WPC Rx Mode (mobile device). In Tx Mode (base station), the Rx is now the Tx and sends instructions that are filtered using the DEMOD filter shown in Figure 9, and decoded internally using a dithered PWM controller for high resolution voltage modulation decoding. Based on the received packet, the P9415 will adjust the operating frequency to match the transmitted power level to the required receiver power level for reliable and efficient wireless power transfer.

Figure 9. Tx DEMOD Filter and AC Coupling



8. Applications Information

8.1 External Components

The P9415 requires a minimum number of external components for proper operation. See Figure 11 and Table 5 of this document, and *AN-998 Determining critical component values for Wireless Power Receivers*.

8.2 Rx Wireless Power Coil

The Rx coil is dependent on customer requirements and most are custom designs. IDT recommends the following measured values for Rx-only coils:

- Ls = 8 to 10µH
- DCR = < 0.3Ω
- ACR = < 0.4Ω

8.3 Resonance Capacitors

The series resonance capacitors (C32, C33, C34, C36, and C37) are critical components and must be chosen carefully. All current that flows to the load flows through these components plus any current lost in the rectifier AC to DC conversion. The recommended capacitor is the 100nF Murata (GRM155C71H104KE19, X7S, 50V, or GRM155R61H104KE19, X5R, 50V), which have an ESR < 0.1ohms at 100kHz. The GRM155C71H104KE19 capacitor is the best choice based on ESR value and DC bias effects. If another capacitor is chosen, inspecting the ESR vs. Frequency curve of the manufacturer's capacitor datasheet is necessary to compare ESR characteristics as well as the DC bias effects on the capacitor value. Adding an additional non-populated (NP) component placement (C37) is advised if additional capacitance is needed for a particular Rx coil.

8.4 Input Capacitor (VRECT Capacitors)

The LDO input capacitors (VRECT capacitors) should be located as close as possible to the VRECT pins and ground (PGND). Ceramic capacitors are recommended for their low ESR and small profile.

8.5 Output Capacitor (VOUT Capacitors)

The output capacitor connection to the ground pins (PGND) should be made as short as practical for maximum device performance. Because the LDO is designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance. For better transient response, the total amount of output capacitance should be increased to meet the output voltage variation target of the application (VRECT capacitance might need to be increased as well).

8.6 LDO1P8 Capacitor

The P9415 has an internal LDO regulator that must have at least a 1µF to 2.2µF capacitor connected from the LDO1P8 pin to PGND. This capacitor should be as close as possible to the LDO1P8 pin with a close GND connection. A 0.1µF capacitor in a 0201 or 0402 size package can be added for improved high-frequency decoupling of the LDO1P8 power rail because this voltage powers the internal ARM Cortex-M0 processor.

8.7 LDO5P0 Capacitor

The P9415 has an internal LDO regulator that must have at least a 1µF to 2.2µF capacitor connected from the LDO5P0 pin to PGND. This capacitor should be as close as possible to the LDO5P0 pin with a close PGND connection. A 0.1µF capacitor in a 0201 or 0402 size package can be added for improved high frequency decoupling of the LDO5P0 power rail because this voltage powers the internal ADC and UVLO circuits.

For additional power savings at higher input voltages, an external 5V supply should be connected to supply power to the P9415 via the LDO5P0 pin. The applied voltage to this pin must be > LDO5P0 regular output voltage in order to power the low-voltage circuitry from the external 5V supply, the external 5V supply should be between 5.2V to 5.5V.

8.8 PCLAMP Connection

The P9415 has an internal automatic DC clamping feature to protect the device from events that cause high voltages to occur on the AC or DC side of the rectifier. The clamping engages by the VRECT connection to the PCLAMP pin. The VRECT node must be connected to the PCLAMP pin at all times during Rx mode operation. For greater than 5W operation, the VRECT node is connected to the PCLAMP pin using a 50Ω to 100Ω resistor with greater than 1/4W rating with 2.5x or greater over-power surge capability. For space constrained designs, the PCLAMP pin can be directly connected to the VRECT node for 5W or lower power operation.

In addition, there is an option for external FET and resistor clamping by use of the ECLAMP_DRV pin. This out is synchronized with the internal PCLAMP signal and is capable of 5V drive level.

8.9 Transient Voltage Suppressors

The Transient Voltage Suppressor (TVS) is an active device that will direct high voltages from the input to ground, thus protecting the wireless power device or other downstream ICs from being exposed to high voltages.

Transient Voltage Suppressor diodes should be added to the design from the AC1 and AC2 nodes to GND or from AC1 to AC2. These components are useful to rapidly limit incoming ESD surges or situations when the TX incoming power exceeds the expected power and VRECT voltage rises above target and over Overvoltage Protection threshold in less than 10µs to aid in voltage limiting the incoming AC waveforms in conjunction with the PCLAMP power limiting circuitry.

A balance in Reverse Standoff Voltage (VRWM), Clamping Voltage (VCL), Break-down Voltage (VBR) relative to the expected Vrect operating voltage Vrect (be sure minimum VBR is less than maximum operating Vrect value and that VCL is less than Vrect Absolute maximum voltage) should be reached.

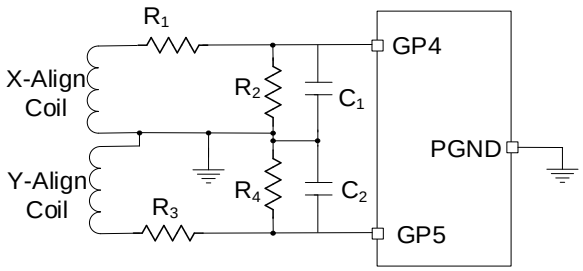
Table 5. Transient Voltage Suppressors (TVS) Recommendations

V_{MLDO} = 15V CDS0D323-T18C	V_{MLDO} = 20V D20V0L1B2LP
VRWM = 18V maximum	VRWM = 20V maximum
VBR = 20V minimum at 5mA	VBR = 21V minimum at 1mA
VCL = 29V maximum at 1A pp	VCL = 30V maximum at 1A pp

8.10 XY Alignment

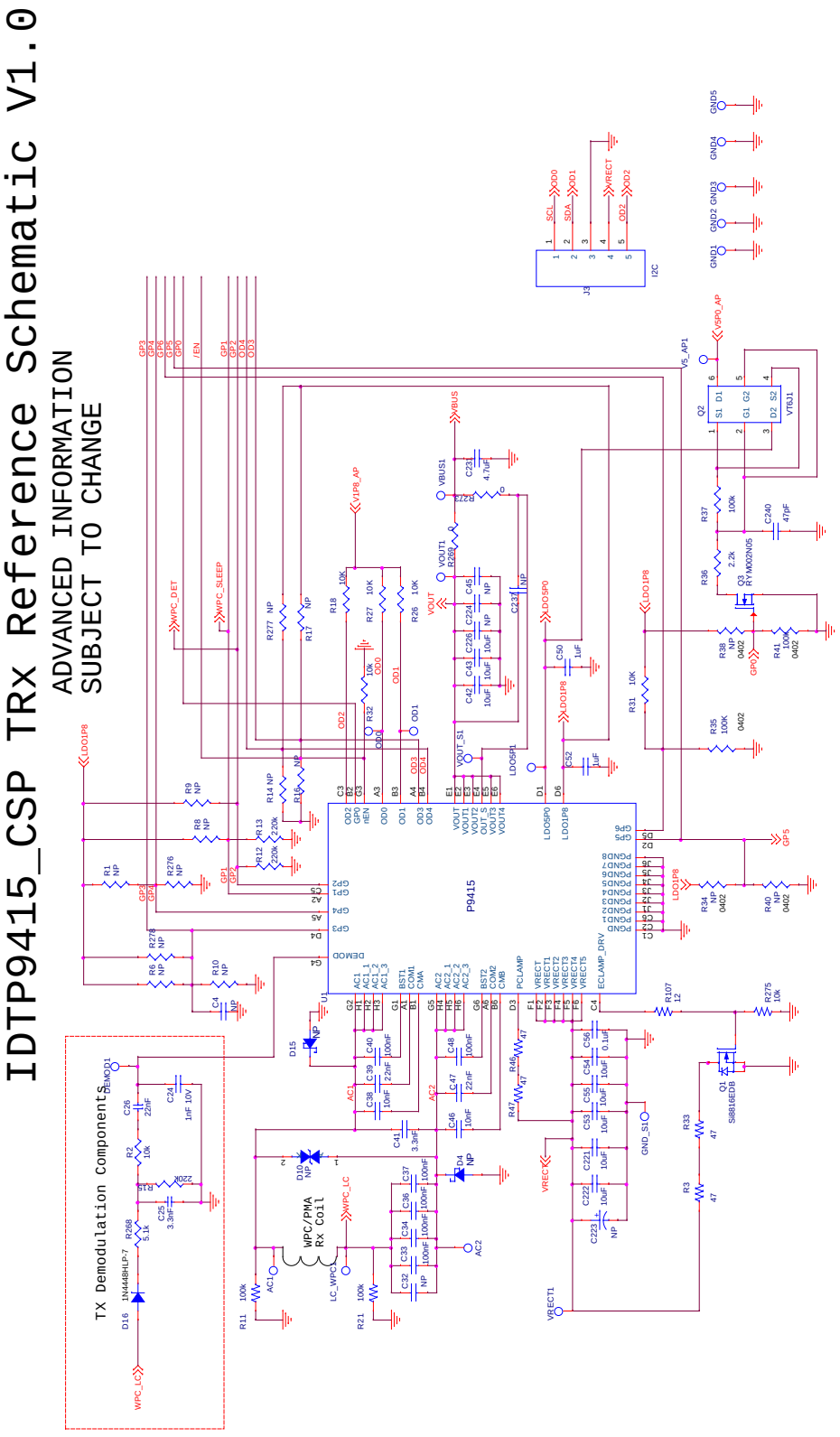
The P9415 has integrated XY alignment coil data receive circuitry that should be used to monitor XY alignment coils integrated with the WPC TRx coil. The XY alignment feature allows the device to sense its relative position to the Tx coil magnetic field center and enables FOD compensation to be applied based on the position of the Rx to increase spatial freedom. When used, the XY alignment coils should be connected to pins GP4 (X-alignment coil input) and GP5 (Y-alignment coil input).

Figure 10. Typical XY Align Coil Schematic Level Connection Guide



8.11 Applications Schematics

Figure 11. Typical TRx Applications Schematic



8.12 PCB Layout Considerations

For optimum device performance and lowest output noise, the following guidelines should be observed. Please contact IDT for Gerber files that contain the recommended board layout and application note *AN1043 P9415 TRx Layout Guide*.

An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Signal traces not related to the P9415 should be routed away from the IC as much as possible to avoid blocking thermal dissipation paths from the IC to the PCB. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs because the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques should be used to remove the heat due to device power dissipation.

The following general guidelines should be helpful with designing a board layout for lowest thermal resistance:

1. PC board traces with large cross-sectional areas remove more heat. For optimum results, use large-area PCB patterns with wide copper traces, placed on the P9415 side of the PCB.
2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
3. Thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

8.13 Special Notes

Package assembly:

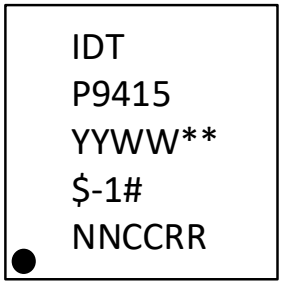
- Unopened Dry Packaged Parts have a one-year shelf life.
- The HIC indicator card for newly-opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

9. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/awq53-package-outline-drawing-2820-x-4220-x-0500-mm-body-040mm-pitch-dsbga

10. Marking Diagram



Line 1. The manufacturer.
Line 2. The part number.
Line 3. “YYWW” is the last 2 digits of the year and week that the part was assembled. “**” denotes sequential lot number.
Line 4. “$” denotes assembly mark code. ”#” denotes stepping code.
Line 5. “NN” is the wafer number; “CC” is the column or X- coordinate of the wafer; “RR” is the row or Y-coordinate of the wafer.

11. Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Ambient Temperature	Firmware[a]
P9415-0AWQI8	AWQ53 WLCSP-53 2.82 × 4.22 × 0.50 mm with 0.4mm pitch	MSL 1	Tape and Reel	-40° to +85°C	Blank
P9415-1AWQI8	AWQ53 WLCSP-53 2.82 × 4.22 × 0.50 mm with 0.4mm pitch	MSL 1	Tape and Reel	-40° to +85°C	Core FW

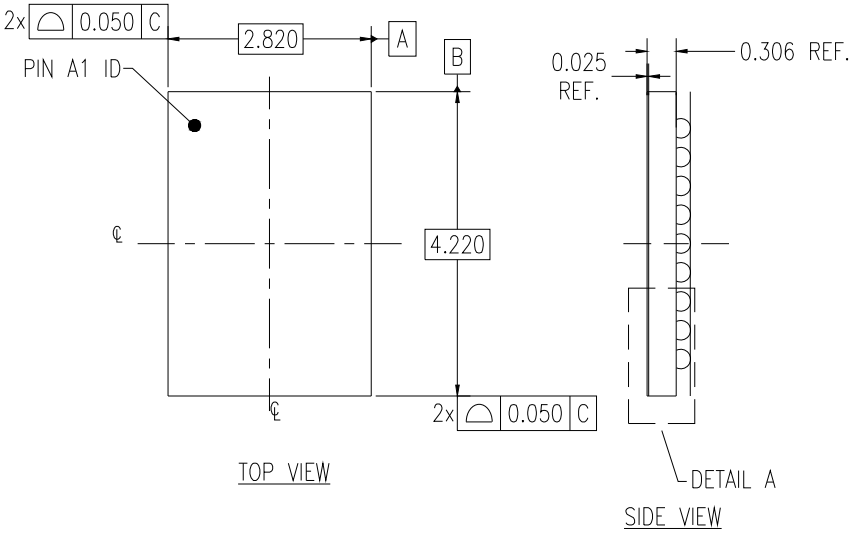
[a] This field is a custom value that is specific to each customer application. Please contact your local sales team for your particular value for this field.

12. Revision History

Revision Date	Description of Change
December 19, 2019	▪ Added ordering information for chip with core firmware ▪ Added spec to the EC table for VOUT = 20V ▪ Updated some of the EC table min/typ/max values based on final characterization data ▪ Removed duplicate I2C pin VIH/VOL/Leakage spec (since it's covered with other OD pin specs)
November 1, 2019	▪ Increased the maximum ratings for CMA, CMB, COM1, COM2, PCLAMP, VRECT, AC1, and AC2 in Table 2 ▪ Updated the electrical characteristics for $V_{IN\_VRECT\_Rx}$, V_{OVP}, and V_{PCLAMP} in Table 4
October 9, 2019	Initial release.

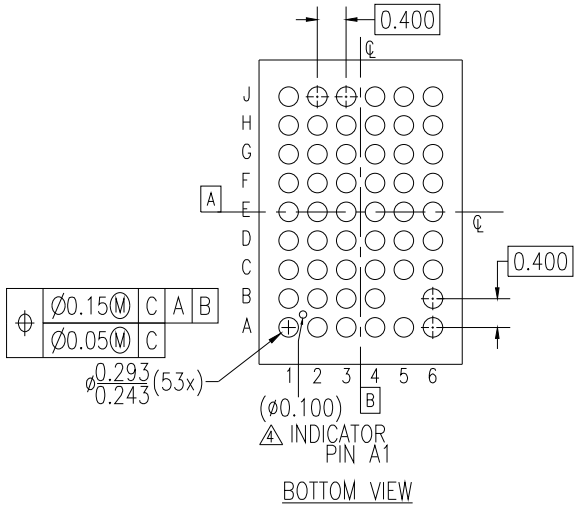
DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
4/3/19	00	INITIAL RELEASE	JH
5/7/19	01	CHANGE CODE AZQ53 TO AWQ53	JH
NOTE: REFER TO AGILE FOR OFFICIAL RELEASE DATE			

NOTES:
1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE CONTACT POINTS OF THREE OR MORE SOLDER BALLS THAT SUPPORT THE DEVICE WHEN PLACED ON A TOP OF A PLANAR SURFACE.
4. BOTTOM PIN#1 INDICATOR OPTIONAL.
5. BALL SIZE BEFORE REFLOW IS 0.25MM.
6. WAFER SCRIBE LINE WIDTH 90UM, KERF WIDTH 40UM.

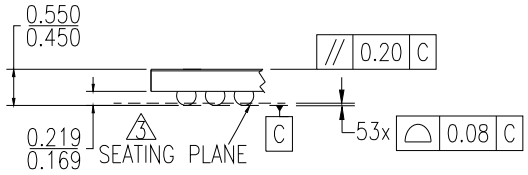


TOP VIEW

SIDE VIEW



BOTTOM VIEW



DETAIL A
(ROTATED 90 DEG CW)

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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San Jose, CA 95138
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE: AWQ53 Package Outline Drawing
2.820 x 4.220 x 0.500 mm Body,
0.40mm Pitch DSBGA

SIZE	DRAWING No.	REV
C	PSC-4798	01

DO NOT SCALE DRAWING | SHEET 1 OF 2

DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
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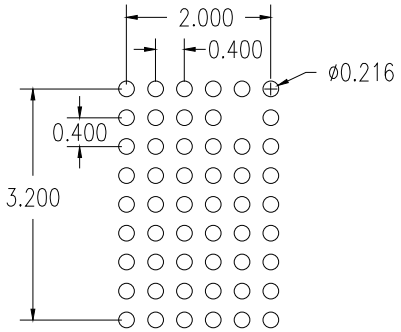
5/7/19	01	CHANGE CODE AZQ53 TO AWQ53	JH
NOTE: REFER TO AGILE FOR OFFICIAL RELEASE DATE			



RECOMMENDED LAND PATTERN DIMENSION

NOTE:
1. ALL DIMENSIONS ARE IN MM, ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEW ON PCB.
3. NSMD LAND PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION AS PER IDT DSBGA APPLICATION NOTE.

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

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5/7/19	01	CHANGE CODE AZQ53 TO AWQ53	JH
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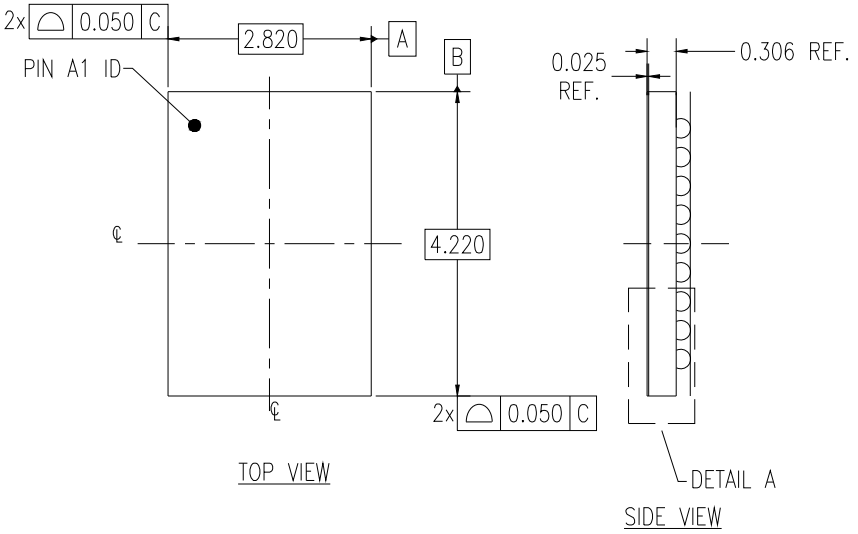

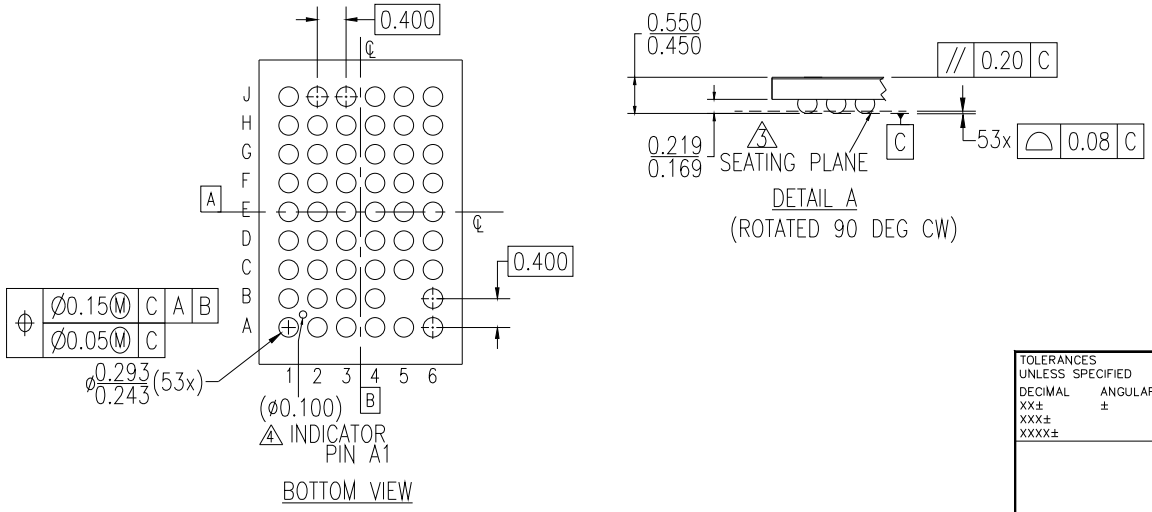

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

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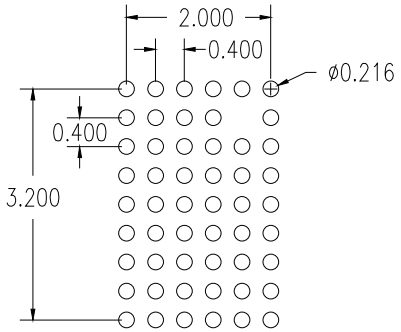
TITLE: AWQ53 Package Outline Drawing
2.820 x 4.220 x 0.500 mm Body,
0.40mm Pitch DSBGA

SIZE	DRAWING No.	REV
C	PSC-4798	01

DO NOT SCALE DRAWING | SHEET 1 OF 2

DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
4/3/19	00	INITIAL RELEASE	JH
5/7/19	01	CHANGE CODE AZQ53 TO AWQ53	JH
NOTE: REFER TO AGILE FOR OFFICIAL RELEASE DATE			



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1. ALL DIMENSIONS ARE IN MM, ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEW ON PCB.
3. NSMD LAND PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION AS PER IDT DSBGA APPLICATION NOTE.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
	TITLE: AWQ53 Package Outline Drawing 2.820 x 4.220 x 0.500 mm Body, 0.40mm Pitch DSBGA	
	SIZE: C DRAWING No.: PSC-4798 REV: 01	
	DO NOT SCALE DRAWING	SHEET 2 OF 2

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