

DATA SHEET

74ALVCHS16830

18-bit to 36-bit address driver
with bus hold (3-State)

Product data
Supersedes data of 2001 Sep 07

2002 Mar 15

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

FEATURES

- Diodes on inputs clamp overshoot
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors
- Packaged in thin very small-outline package (TVSOP) — 0.4 mm pitch
- Optimized for use with PCK953 in SDRAM module applications
- Low noise, low skew

DESCRIPTION

The ALVCHS16830 address driver is designed for 2.3 V to 3.6 V V_{CC} operation.

Diodes to V_{CC} have been added on the inputs to clamp overshoot.

The bus hold feature retains the inputs' last state whenever the input bus goes to high impedance. This prevents floating inputs and eliminates the need for pull up or pull down resistors.

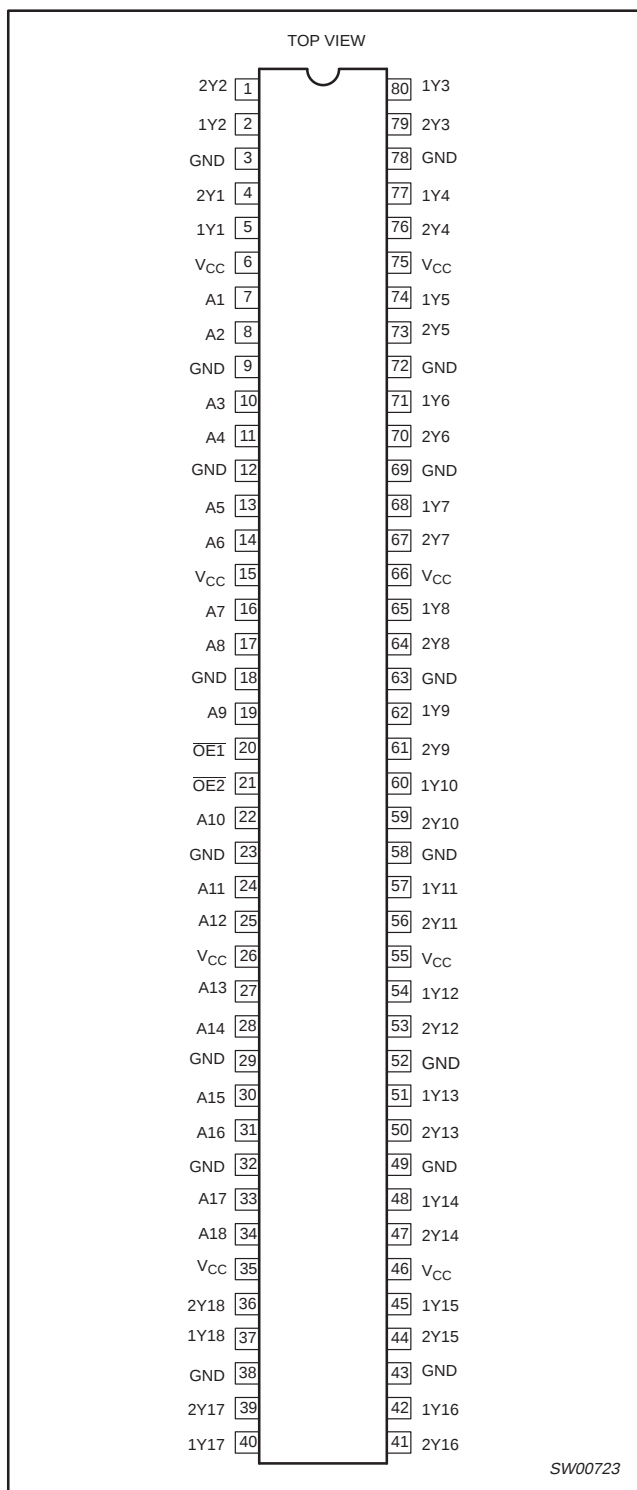
To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The 74ALVCHS16830 is characterized for operation from -40 to $+85$ °C.

FUNCTION TABLE

Inputs			Outputs	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

PIN CONFIGURATION



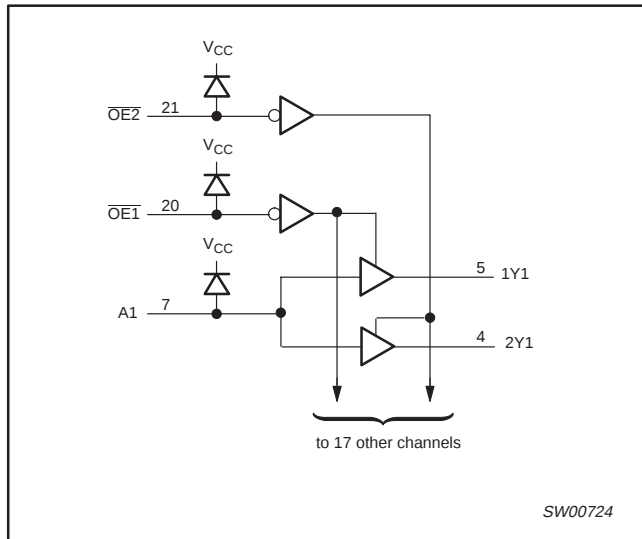
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
80-pin plastic thin very small outline (TVSOP)	-40 to $+85$ °C	74ALVCHS16830DGB	SOT647-1

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

LOGIC DIAGRAM (POSITIVE LOGIC)



PIN DESCRIPTION

PIN(S)	SYMBOL	FUNCTION
6, 15, 26, 35, 46, 55, 66, 75	V _{CC}	Supply voltage
7, 8, 10, 11, 13, 14, 16, 17, 19, 22, 24, 25, 27, 28, 30, 31, 33, 34	A _n	Inputs
1, 2, 4, 5, 36, 37, 39, 40, 41, 42, 44, 45, 47, 48, 50, 51, 53, 54, 56, 57, 59, 60, 61, 62, 64, 65, 67, 68, 70, 71, 73, 74, 76, 77, 79, 80	1Y _n , 2Y _n	Outputs
20, 21	$\overline{\text{OE}}1$, $\overline{\text{OE}}2$	Output enable
3, 9, 12, 18, 23, 29, 32, 38, 43, 49, 52, 58, 63, 69, 72, 78	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Over recommended operating free-air temperature range (unless otherwise noted).¹

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	Supply voltage range		−0.5 to +4.6	V
V _I	Input voltage range	See Note 2	−0.5 to +4.6	V
V _O	Output voltage range	See Notes 2 and 3	−0.5 to V _{CC} +0.5	V
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current		± 50	mA
I _{CC} , I _{GND}	Continuous current through each V _{CC} or GND		± 100	mA
Θ _{JA}	Package thermal impedance	See Note 4	106	°C/W
T _{stg}	Storage temperature range		−65 to +150	°C

NOTES:

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 4.6 V maximum.
- The package thermal impedance is calculated in accordance with JESD 51.

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

RECOMMENDED OPERATING CONDITIONSAll unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	—	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	—	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	—	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	—	0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3 \text{ V}$	—	−12	mA
		$V_{CC} = 2.7 \text{ V}$	—	−12	
		$V_{CC} = 3 \text{ V}$	—	−24	
I_{OL}	Low-level output current	$V_{CC} = 2.3 \text{ V}$	—	12	mA
		$V_{CC} = 2.7 \text{ V}$	—	12	
		$V_{CC} = 3 \text{ V}$	—	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		—	10	ns/V
T_{amb}	Operating free-air temperature		−40	+85	°C

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	LIMITS			UNIT
				MIN	TYP ¹	MAX	
V_{IK}		$I_I = -18 \text{ mA}$	2.3 V	—	—	-1.2	V
		$I_I = 18 \text{ mA}$	2.3 V	—	—	$V_{CC}+1.2$	
V_{OH}		$I_{OH} = -100 \mu\text{A}$	2.3 V to 3.6 V	$V_{CC}-0.2$	—	—	V
		$I_{OH} = -4 \text{ mA}, V_{IH} = 1.7 \text{ V}$	2.3 V	1.9	—	—	
		$I_{OH} = -6 \text{ mA}, V_{IH} = 1.7 \text{ V}$	2.3 V	1.7	—	—	
		$I_{OH} = -8 \text{ mA}, V_{IH} = 2 \text{ V}$	2.7 V	2.4	—	—	V
		$I_{OH} = -12 \text{ mA}, V_{IH} = 2 \text{ V}$	3 V	2	—	—	V
		$I_{OH} = -24 \text{ mA}, V_{IH} = 2 \text{ V}$	3 V	2	—	—	
V_{OL}		$I_{OL} = 100 \mu\text{A}$	2.3 V to 3.6 V	—	—	0.2	V
		$I_{OL} = 4 \text{ mA}, V_{IL} = 0.7 \text{ V}$	2.3 V	—	—	0.4	
		$I_{OL} = 6 \text{ mA}, V_{IL} = 0.7 \text{ V}$	2.3 V	—	—	0.55	
		$I_{OL} = 8 \text{ mA}, V_{IL} = 0.8 \text{ V}$	2.7 V	—	—	0.55	V
		$I_{OL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}$	3 V	—	—	0.6	V
		$I_{OL} = 24 \text{ mA}, V_{IL} = 0.8 \text{ V}$	3 V	—	—	0.8	
I_I		$V_I = V_{CC}$ or GND	3.6 V	—	—	± 5	μA
$I_{I(\text{hold})}$		$V_I = 0.7 \text{ V}$	2.3 V	45	—	—	μA
		$V_I = 1.7 \text{ V}$	2.3 V	-45	—	—	
		$V_I = 0.8 \text{ V}$	3 V	75	—	—	
		$V_I = 2 \text{ V}$	3 V	-75	—	—	
		$V_I = 0$ to 3.8 V^2	3.6 V	—	—	± 500	
I_{OZ}		$V_O = V_{CC}$ or GND	3.6 V	—	—	± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	—	—	40	μA
ΔI_{CC}		One input at $V_{CC} - 0.8 \text{ V}$, Other inputs at V_{CC} or GND	3 V to 3.6 V	—	—	750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V	—	3.62	—	pF
	Data inputs			—	8.21	—	
C_o	Outputs	$V_O = V_{CC}$ or GND	3.3 V	—	3.53	—	pF

NOTES:

1. All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
2. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.2	3.8	—	4	1.7	3.5	ns
t_{en}	$\overline{OE}$	Y	1	5.7	—	5.7	1	4.8	ns
t_{dis}	$\overline{OE}$	Y	1	4.9	—	5.4	1.7	5.2	ns
$t_{sk(o)}^1$	Output skew	—	—	—	—	—	—	500	ps

NOTE:

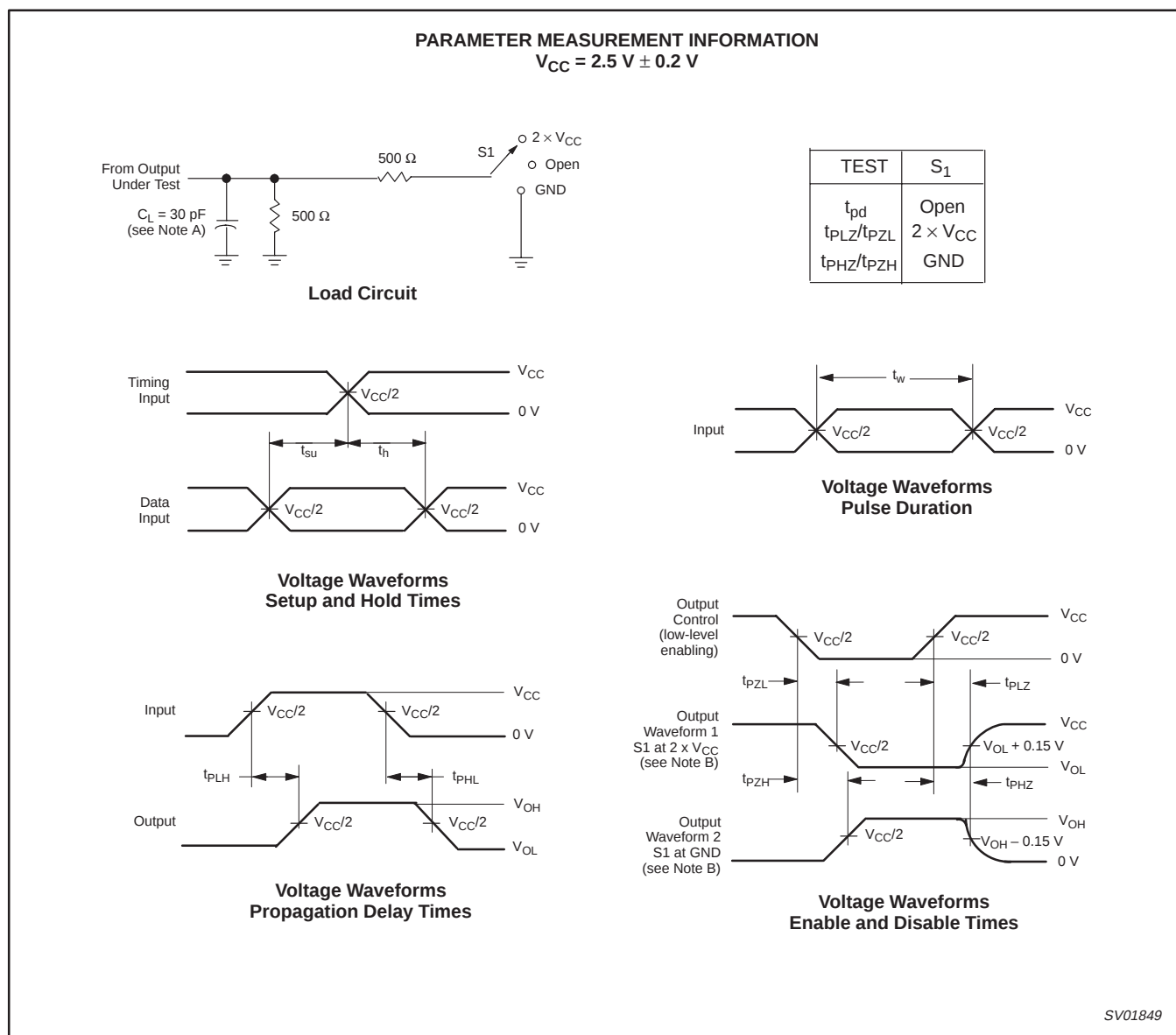
1. Output skew between any 2 outputs of same part switching in the same direction.

OPERATING CHARACTERISTICS, $T_{amb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance per driver	All outputs enabled	$C_L = 0$, $f = 10\text{ MHz}$	49	53	pF
		All outputs disabled		6	7.5	

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

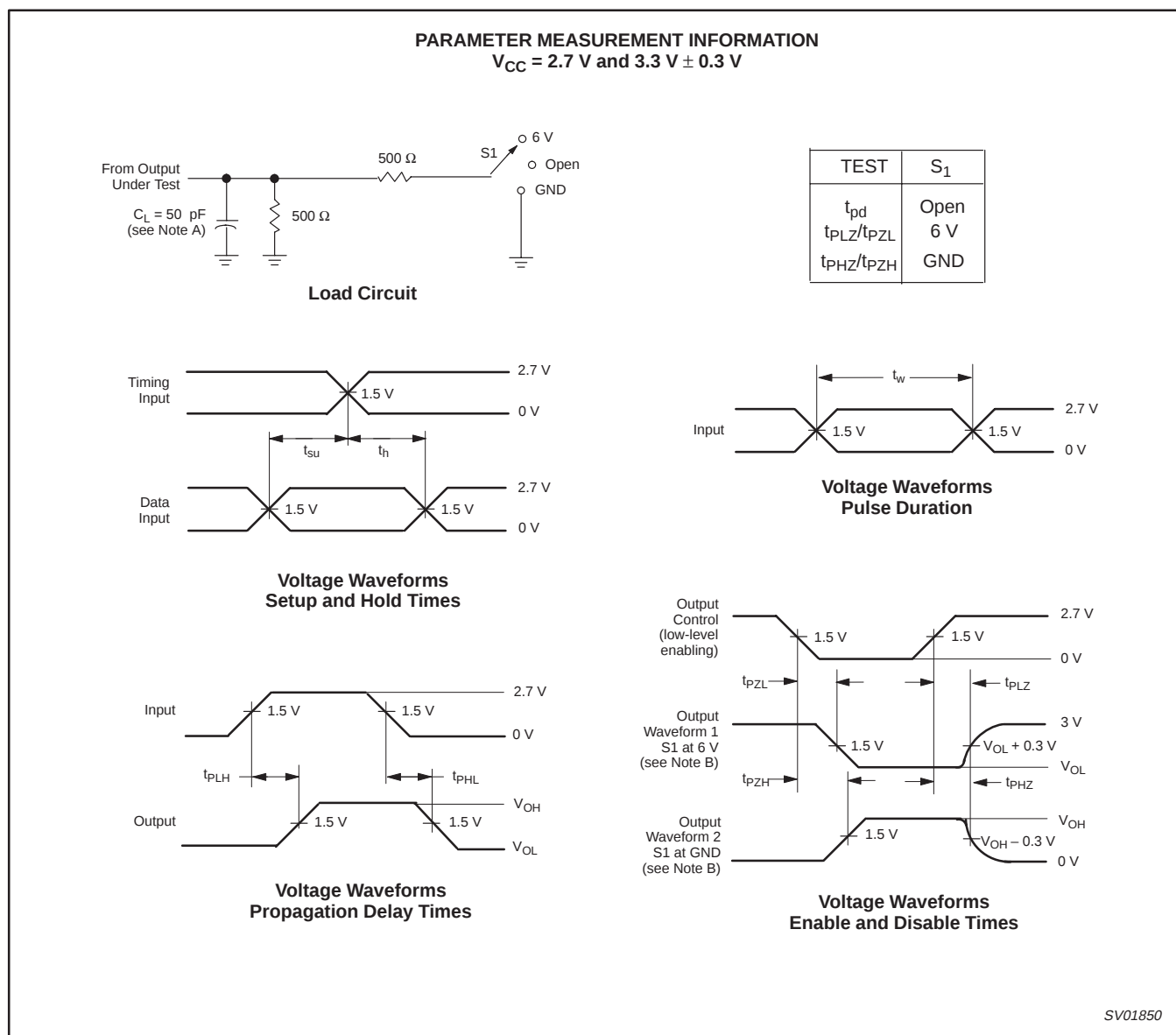
**NOTES:**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load circuit and voltage waveforms

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

**NOTES:**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

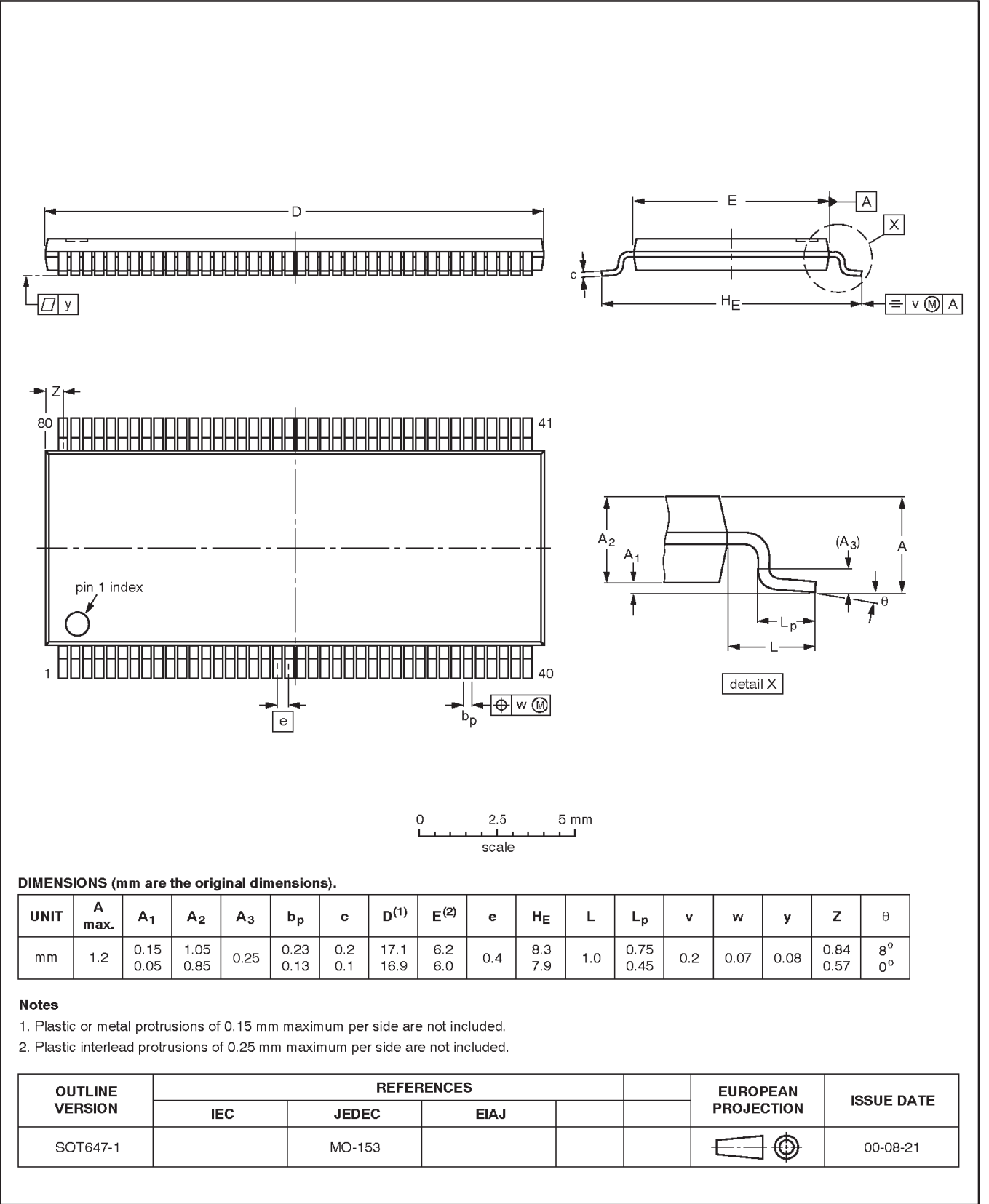
Figure 2. Load circuit and voltage waveforms

18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

TSSOP80: plastic thin shrink small outline package; 80 leads; body width 6.1 mm

SOT647-1



18-bit to 36-bit address driver with bus hold (3-State)

74ALVCHS16830

Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

© Koninklijke Philips Electronics N.V. 2002
 All rights reserved. Printed in U.S.A.

Date of release: 03-02

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

Document order number:

9397 750 09605

Let's make things better.