



Advance Information

PLL Tuning Circuit with 1.3 GHz Prescaler and D/A Converters for Automatic Tuner Alignment

The MC44864 is a tuning circuit for TV applications. This device contains a PLL section and a DAC section and is MCU controlled through an I²C Bus.

The PLL section contains all the functions required to control the VCO of a TV tuner. The IC generates the tuning voltage and the additional control signals, such as band switching voltages.

The D/A section generates three additional varactor voltages to feed all of the varactors of the tuner with individually optimized control voltages (automatic tuner adjustment). The MC44864 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSIAC™ (Motorola Oxide Self-Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control
- Selectable +8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Programmable Reference Divider
- 3-State Phase/Frequency Comparator
- Operational Amplifier for Direct Varactor Control with Low Saturation Voltage
- Four Output Buffers (15 mA)
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- The HF Input is Symmetrical
- Three 6 Bit DACs for Automatic Tuner Adjustment Allowing Use of Non-Matched Varactors
- Better Tuner Performances Through Optimum Filter Response
- I²C Bus Controlled
- Four Chip Addresses for the PLL Section
- Four Chip Addresses for the D/A Section
- ESD Protected to MIL-STD-883C, Method 3015.7 (2,000 V, 1.5 kΩ, 150 pF)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

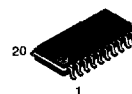
Rating	Pin	Value	Unit
Power Supply Voltage (V _{CC1})	9	6.0	V
Band Buffer "Off" Voltage	14 – 17	15	V
Band Buffer "On" Current	14 – 17	20	mA
Operational Amplifier Power Supply Voltage (V _{CC2})	4	36	V
Operational Amplifier Short Circuit Duration (0 to V _{CC2})	5 – 8	Continuous	S
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	0 to +70	°C

NOTE: ESD data available upon request.

MC44864

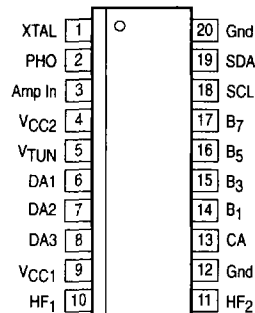
PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND D/A CONVERTERS

SEMICONDUCTOR TECHNICAL DATA



M SUFFIX
PLASTIC PACKAGE
CASE 967
(EIAJ-20)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44864M	T _A = 0° to +70°C	EIAJ-20

9

9



9

MC44864

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 32 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V _{CC1} Supply Voltage Range	9	4.5	5.0	5.5	V
V _{CC1} Supply Current (V _{CC1} = 5.0 V)(1)(2)	9	–	50	70	mA
V _{CC2} Supply Voltage Range	4	25	30	35	V
V _{CC2} Supply Current (Output Open)	4	–	1.3	2.5(4)	mA
Band Buffer Leakage Current when “Off” at 12 V	14 – 17	–	0.01	1.0	μA
Band Buffer Saturation Voltage when “On” at 15 mA	14 – 17	–	1.8	2.0	V
Data/Clock Current at 0 V	18, 19	–10	–	0	μA
Clock Current at 5.0 V	18	0	–	1.0	μA
Data Current at 5.0 V Acknowledge “Off”	19	0	–	1.0	μA
Data Saturation Voltage at 15 mA Acknowledge “On”	19	–	1.2	–	V
Data/Clock Input Voltage Low	18, 19	–	–	1.5	V
Data/Clock Input Voltage High	18, 19	3.0	–	–	V
Clock Frequency Range	18	–	–	100	kHz
Phase Detector Current in High Impedance State	2	–15	–	15	nA
Oscillator Frequency Range	1, 2	3.5	4.0	4.1	MHz
Phase Detector High–State Source Current (@ 1.5 V)	2	–2.5	–	–0.5	mA
Phase Detector Low–State Sink Current (@ 4.0 V)	2	0.5	–	2.5	mA
Operational Amplifier Internal Reference Voltage	–	2.0	2.5	3.0	V
Operational Amplifier Input Current	3	–15	–	15	nA
DC Open Loop Gain	–	2000	–	–	V/V
Gain Bandwidth Product	–	–	0.2	–	MHz
Phase Margin	–	–	50	–	Deg.
V _{out} Low, Sinking 50 μA	6 – 8	–	0.2	0.5	V
V _{out} High, Sourcing 50 μA (V _{CC2} – V _{out} High)	6 – 8	–	–	1.5	V
Tuning Voltage (DC)	5 – 8	–	–	30	V
D/A Converters Step Size(3)	6 – 8	0.5	–	1.5	LSB
D/A Converters Temperature Drift	6 – 8	–	1.0	–	LSB
DAC Offset at V _{TUN} = 2.5 V	–	–50	–	50	mV
DAC Offset at V _{TUN} = 25 V	–	–700	–	700	mV
DAC Voltages (DC)	6 – 8	–	–	33	V

NOTES: 1. When prescaler “Off”, typical supply current is decreased by 10 mA.

2. Band Buffers “Off”, 2.4 mA more when one buffer is on.

3. For definition of the LSB, see Figure 9 in the D/A section.

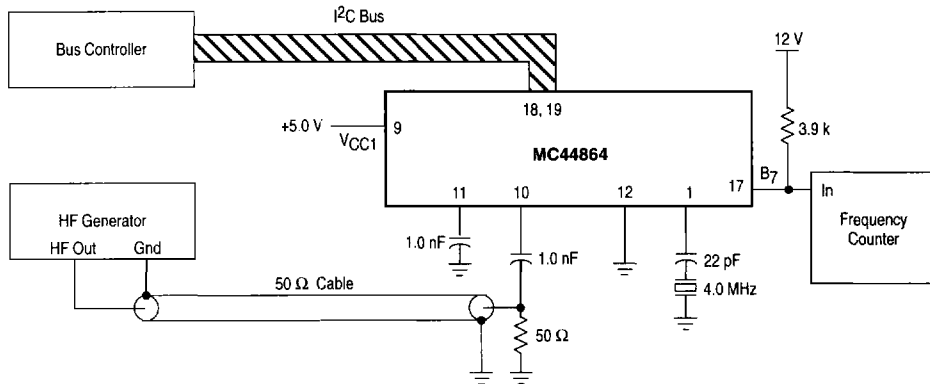
4. 2.5 mA as long as the analog outputs are not in saturation high, which means V_{TUN}, V_{DAC} (Pins 5, 6, 7, 8) lower than V_{CC2} – 1.5 V. When all outputs are in saturation high the maximum V_{CC2} current is 5.0 mA.

MC44864

HF CHARACTERISTICS (See Figure 1)

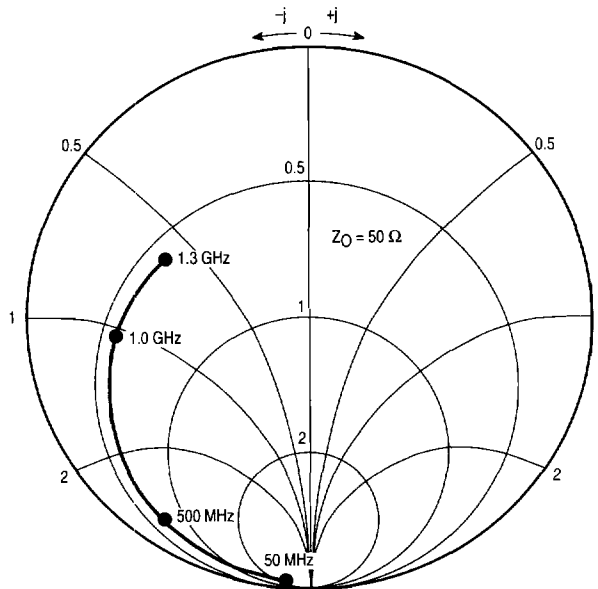
Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	10, 11	—	1.55	—	V
Input Voltage Range					mVrms
10–150 MHz (Prescaler "Off")	10, 11	20	—	315	
80–1000 MHz	10, 11	20	—	315	
1000–1300 MHz	10, 11	50	—	315	

Figure 1. HF Sensitivity Test Circuit



Device is in test mode: B7 is "On", R2 = 1 and R3 = 0 (see Bus section).
Sensitivity is the level of the HF generator on 50 Ω load (without MC44864 load).

Figure 2. Typical HF Input Impedance



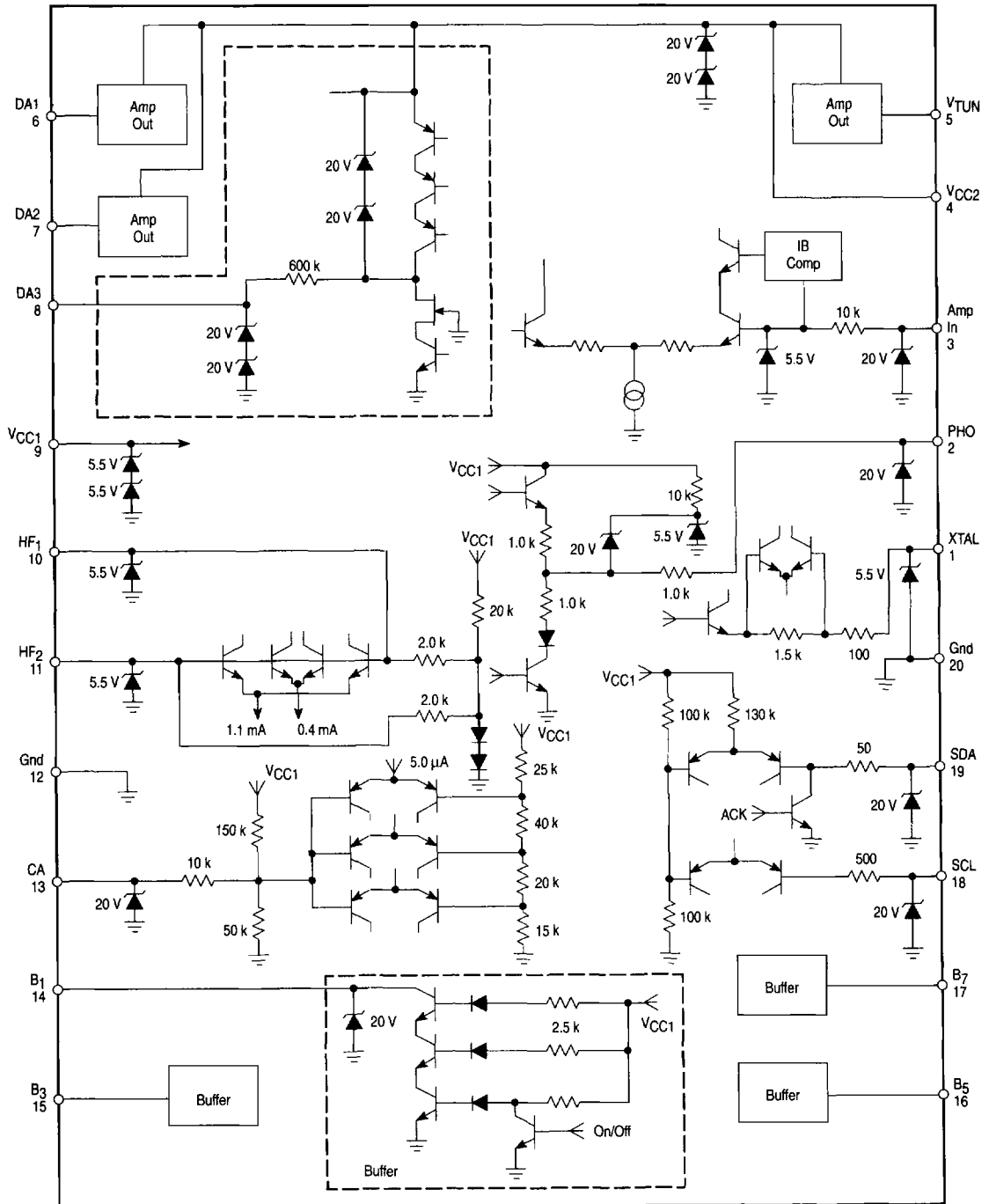
MC44864

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
6, 7, 8	DA1, DA2, DA3	D/A output control voltages
9	V _{CC1}	Positive supply of the circuit (except DACs)
10, 11	HF ₁ , HF ₂	HF input from local oscillator
12, 20	Gnd	Ground
13	CA	Chip Address
14, 15, 16, 17	B ₁ , B ₃ , B ₅ , B ₇	Band buffer output can drive 15 mA
18	SCL	Clock input (supplied by the microprocessor via Bus)
19	SDA	Data input (bus)
1	XTAL	Crystal oscillator (typically 4.0 MHz)
2	PHO	Phase comparator output
3	Amp In	Negative operational amplifier input
4	V _{CC2}	Operational amplifier positive supply
5	V _{TUN}	Operational amplifier output which provides the tuning voltage

MC44864

Figure 3. Pin Circuit Schematic



MC44864

FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion of the features and function of the internal blocks is given below.

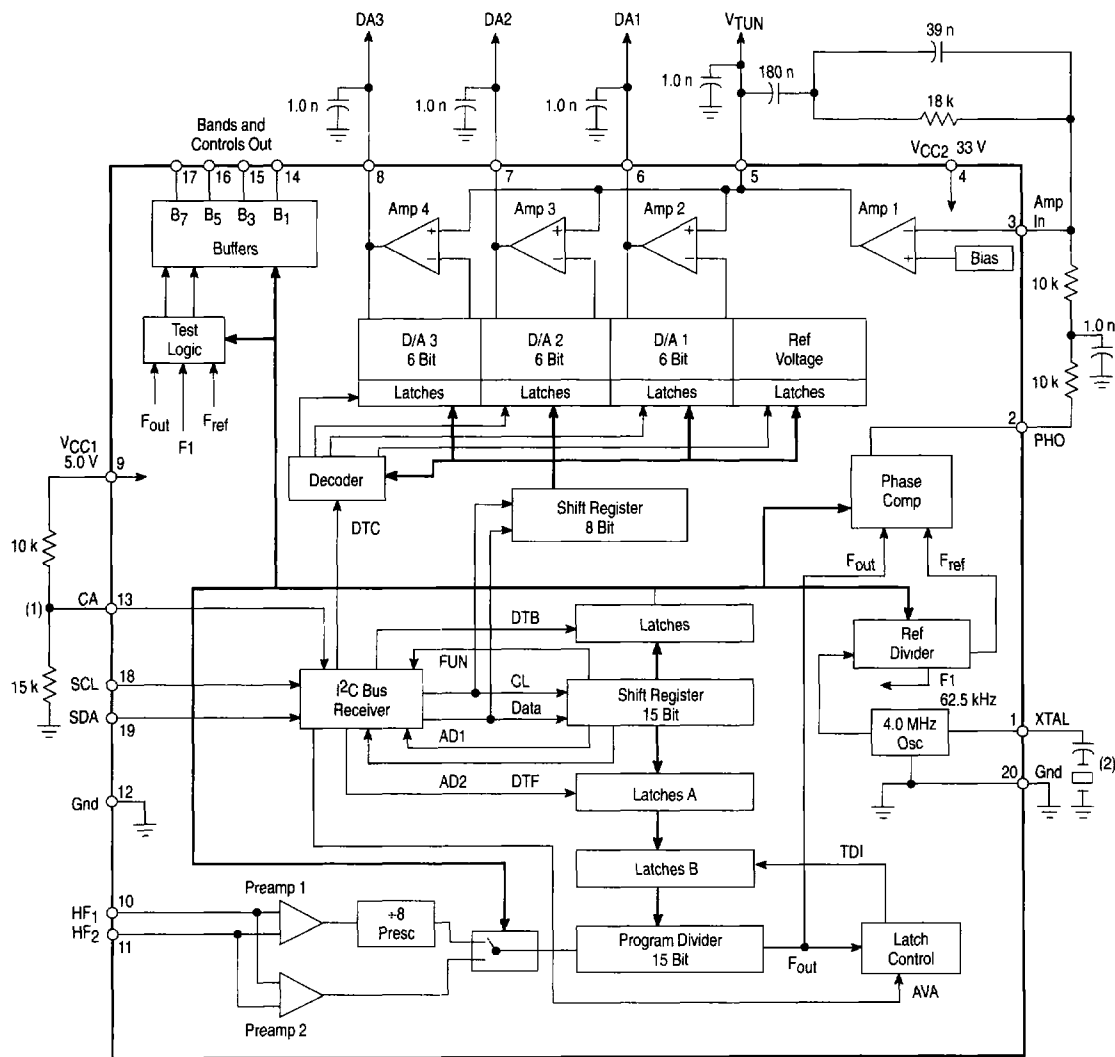
Automatic Tuner Alignment

The circuit generates the tuning voltage through the PLL. The output voltages of the D/A converters are equal to the tuning voltage plus a positive or negative offset of up to 31 steps. During the automatic alignment one first lets the PLL lock to the appropriate frequency and then searches for the

optimum value of the other varactor voltages. The digital word for each voltage value is stored in a nonvolatile memory (NVM). Hence, for each frequency point to be adjusted, three times 6 bits of information have to be stored (plus 2 bits for the DAC range).

The information stored in the NVM reflects the characteristic of the individual tuner. For this reason, the NVM is preferably situated inside the tuner and is also controlled by the I²C Bus.

Figure 4. Block Diagram



NOTES: 1. Pin 13: Short to V_{CC}
Resistors ±10%
Open or 1.0 nF to Gnd
Short to Gnd
for addresses CC, CE
for addresses C8, CA (values 10 k and 15 k) for test only
for addresses C4, C6
for addresses C0, C2

2. The crystal may be connected to Pin 20 with no connection to external Gnd.

MC44864

Figure 5. TV Tuner for Automatic Alignment

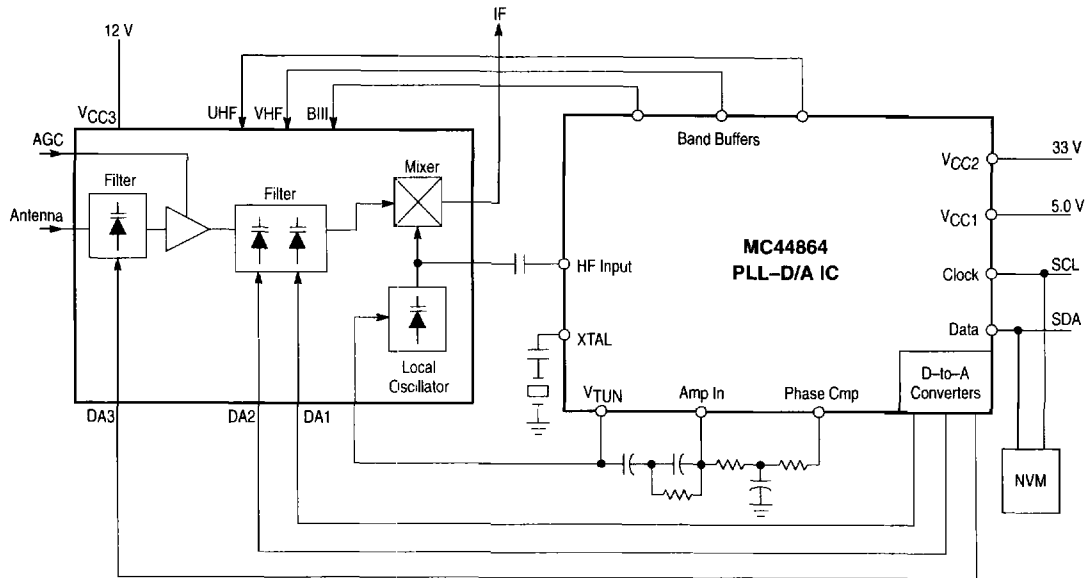


Figure 6. Definition of Bytes

CA1_PLL Chip Address	1	1	0	0	A ₃	A ₂	A ₁	A ₀ = 0	ACK
CO_Control Information	1	R ₆	T	P	R ₃	R ₂	R ₁	R ₀	ACK
BA_Band Information	B ₇	X	B ₅	X	B ₃	X	B ₁	X	ACK
FM_Frequency Information (with MSB)	0	N ₁₄	N ₁₃	N ₁₂	N ₁₁	N ₁₀	N ₉	N ₈	ACK
FL_Frequency Information (with LSB)	N ₇	N ₆	N ₅	N ₄	N ₃	N ₂	N ₁	N ₀	ACK

Chip Addresses

The chip address is programmable by Pin CA.

The PLL addresses C0, C2, C4, C6 are officially allocated to PLL-IC's.

The addresses C8, CA, CC, CE are not officially allocated. Care has to be taken in the application that no conflict occurs with other devices on the same I²C Bus when using the addresses C8 to CE.

CA Pin (13)	A ₃	A ₂	A ₁	A ₀	Address	Function
-0.04 V _{CC1} to 0.1 V _{CC1}	0	0	0	0	C0	1st PLL
	0	0	1	0	C2	1st DAC
Open or 0.2 V _{CC1} to 0.3 V _{CC1}	0	1	0	0	C4	2nd PLL
	0	1	1	0	C6	2nd DAC
0.42 V _{CC1} to 0.75 V _{CC1}	1	0	0	0	C8	3rd PLL
	1	0	1	0	CA	3rd DAC
0.9 V _{CC1} to 1.2 V _{CC1}	1	1	0	0	CC	4th PLL
	1	1	1	0	CE	4th DAC

PLL SECTION

Data Format and Bus Receiver

The circuit receives the information for tuning and control via I²C Bus. The incoming information is treated in the bus receiver. The definition of the permissible bus protocol is shown in the four examples below:

Ex. 1 STA CA1 CO BA STO
 Ex. 2 STA CA1 FM FL STO
 Ex. 3 STA CA1 CO BA FM FL STO
 Ex. 4 STA CA1 FM FL CO BA STO

STA = Start Condition

STO = Stop Condition

CA1 = Chip Address Byte of the PLL Section

CO = Data Byte for Control Information

BA = Band Information

FM = Data Byte for Frequency Information (MSB's)

FL = Data Byte for Frequency Information (LSB's)

Figure 6 shows the five bytes of information that are needed for circuit operation: there is a chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received, the third data byte is ignored. If five or more data bytes are received, the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit F. If the function bit $F = 0$, frequency information is acknowledged and if $F = 1$, control/band information is acknowledged.

If the address is correct (signal AD1) the information is loaded into latches.

A function bit in the first and third data byte is used to pass this data either into the latches of the programmable divider (signal DTF) or into the latches for band and control information (signal DTB). The data transfer to the latches (signals DTF and DTB) is initiated after the 2nd and 4th data bytes.

A second string of latches is used for the data transfer into the programmable divider to inhibit the transfer during the preset operation (signal TDI, signal AVA is an internal "address valid" command).

The switching levels of clock and data (Pins 18 and 19) are $0.5 \times V_{CC1}$.

The control and band information bits have the following functions.

Bits R₀, R₁: Controls Reference Divider Division Ratio

R ₀	R ₁	Division Ratio
0	0	2048
1	0	1024
0	1	512
1	1	256

Bits R₂, R₃: Switches Internal Signals to the Buffer Outputs

R ₂	R ₃	Pin 16	Pin 17
0	0	—	—
0	1	62.5 kHz	—
1	0	F _{ref}	F _{BY2}
1	1	—	—

Bit B₅ has to be "one" when Pin 16 is used to output 62.5 kHz. Bits B₅ and B₇ have to be "one" to output F_{ref} and F_{BY2}. F_{BY2} is the programmable divider output frequency divided by two.

Bits R₂, R₆, T: Controls the Phase Comparator Output Stage

R ₂	R ₆	T	Output State
0	0	0	Normal Operation
0	0	1	"Off" (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	"Off"
1	1	0	Normal Operation
1	1	1	"Off"

The Band Buffers

The band buffers are open collector transistors and are active "low" when $B_n = 1$. They are designed for 15 mA with typical on-voltage of 1.8 V. These buffers are designed to withstand relative high output voltage in the off-state (15 V).

B₅ and B₇ buffers (Pins 16 and 17) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

Buffer B₅ may also be used to output a 62.5 kHz frequency from an intermediate stage of the reference divider. The bits B₅ and B₇ have to be "one" if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$$N = 16384 \times N_{14} + 8192 \times N_{13} + \dots + 4 \times N_2 + 2 \times N_1 + N_0$$

Maximum Ratio 32767

Minimum Ratio 256

where $N_0 \dots N_{14}$ are the different bits for frequency information.

The counter reloads correctly as long as its output frequency does not exceed 1.0 MHz.

Division ratios of < 256 are not allowed. At power-up the counter bit N₈ is preset to "1". All other bits are undetermined. In this way, the counter always starts with a division ratio of 256 or higher.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of $N = 256$ or higher.

The Prescaler

The prescaler has a preamplifier and may be bypassed (Bit P). The signal then passes through preamplifier 2.

The table on the following page shows the frequency ranges which may be synthesized with and without prescaler.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Operational Amplifier

The operational amplifier for the tuning voltage is designed for low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 30 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28.5 V.

Figure 4 shows the usual filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

As a starting point for optimization, the component values in Figure 4 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

The Oscillator

The oscillator uses a 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.

The crystal is driven through a 1.6 k Ω resistor on chip.

The voltage at Pin 16 "crystal", has low amplitude and low harmonic distortion.

The negative resistance of the oscillator at Pin 1 (XTAL) is about 3.0 k Ω .

MC44864

Input Data		Ref. Divider Div. Ratio	Ref. Freq. Hz ⁽¹⁾	With Int. Prescaler P = 0		Without Prescaler P = 1	
				Frequency Steps kHz	Max. Input Freq. MHz	Frequency Steps kHz	Max. Input Freq. MHz
R ₀	R ₁						
0	0	2048	1953.125	15.625	512	1.953125	64
1	0	1024	3906.25	31.25	1024	3.90625	128
0	1	512	7812.5	62.5	1300 ⁽²⁾	7.8125	165 ⁽³⁾
1	1	256	15625.0	125.0	1300 ⁽²⁾	15.625	165 ⁽³⁾

NOTES: 1. With 4.0 MHz Crystal
2. Limit of Prescaler
3. Limit of Programmable Divider

For satellite tuner applications the circuit may be used with an external /4 prescaler and a reference divider ration of 1024 (R₀ = 1, R₁ = 0). In this way, frequencies up to 4.0 GHz can be synthesized with 125 kHz resolution (4.0 MHz crystal).

The same result can be achieved with an external /32 prescaler when the internal prescaler is bypassed (P = 1).

The Reference Divider

The reference divider of the MC44864 is programmable (Bits R₀ and R₁) for ratios of 2048, 1024, 512 and 256. This feature makes the circuit versatile.

Bit P: Controls the Prescaler

P	Prescaler Function
0	Prescaler Active
1	Prescaler Bypassed Prescaler Power Supply "Off"

Bits B₁, B₃, B₅, B₇: Controls the Band Buffers

B ₁ , B ₃ , B ₅ , B ₇ = 0	Buffer "Off"
= 1	Buffer "On"

D/A SECTION

Basic Function

The D/A section has four separate chip addresses from the PLL section. Three D-to-A converters that have a resolution of 6 bits (5 bits plus sign) are on chip. The analog output voltages are dc. The converters are buffered to the analog outputs DA1, DA2 and DA3 by operational amplifiers with an output voltage range that is equal to the tuning voltage range (about 0 to 30 V). The operational amplifiers are arranged such that a positive or negative offset can be generated from the tuning voltage.

Data Format and Bus Protocols

The D-to-A information consists of the D/A chip address (CA2) and four data bytes. The first two bits of the data bytes are used as the function address. Thus the bytes C₁, C₂ and

C₃ contain the address for the individual converter and the 6 bits to be converted. Bit D₅ is the sign (log "1" for positive offset, log "0" for negative offset) and the bits D₀ to D₄ determine the number of steps to be made as an offset from the tuning voltage. The bits S₀ and S₁ in the data byte RA define the step size (V_{step}) and the range of the converters (see Figures 8 and 9). The range is the same for all converters.

After the chip address (CA2) is acknowledged, up to four data bytes may be received by the IC. If more than four bytes are received, the fifth and following bytes are ignored and the last acknowledge pulse is sent after the fourth data byte. The data transfer to the converters (signal DTC) is initiated each time a complete data byte is received.

The following shows some examples of the permissible bus protocols of the D-to-A section. The data bytes may be sent to the IC in random order with up to four in one sequence. The same converter may be loaded up to four times as shown in example 6. Below are 6 examples of permissible bus protocols.

Ex. 1 STA CA2 C1 STO
Ex. 2 STA CA2 C1 C2 STO
Ex. 3 STA CA2 C1 C2 C3 STO
Ex. 4 STA CA2 C1 C2 C3 RA STO
Ex. 5 STA CA2 RA C1 C2 C3 STO
Ex. 6 STA CA2 C1 C1 C1 C1 STO

STA = Start Condition

STO = Stop Condition

CA2 = Chip Address Byte for D/A Section

C₁, C₂, C₃ = Data Bytes for D/A Converters

RA = Data Byte for Range

Figure 7. Definition of Bytes

CA2_D/A Chip Address	1	1	0	0	A ₂	A ₁	A ₀ = 0	ACK	
C1_Converter 1	0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	ACK
C2_Converter 2	0	1	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	ACK
C3_Converter 3	1	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	ACK
RA_Range Selection	1	1	X	X	X	X	S ₁	S ₀	ACK

Figure 8. Output Voltage (D/A Converters)

$V_{DA} = V_{TUN} \pm V_{step} (D_0 + 2 D_1 + 4 D_2 + 8 D_3 + 16 D_4)$	
$D_5 = 1$ positive sign; $D_5 = 0$ negative sign	
V_{TUN} : Tuning Voltage set by PLL	
V_{step} : Voltage Step (LSB) of the D/A Converters	

Figure 9. Range Selection of the D/A Converters

Input Data		Typ. Step Size V_{step}	Guaranteed Range 31 Steps
S_0	S_1		
0	0	225 mV	6.25 V
1	0	125 mV	3.40 V
0	1	70 mV	1.90 V
1	1	40 mV	1.05 V

The D/A Converters

The D/A converters convert 5 bit into analog current of which the polarity is switched by the sixth bit. The reference voltage of the converters is programmed by two bits (S_0 , S_1 of the RA-byte) to determine the scaling factor. The analog

currents are then converted into voltages and added to their respective operational amplifier nominal bias. The resulting voltages at Pins 6, 7 and 8 are the tuning voltages (V_{TUN} , see Figure 4) at Pin 5 plus any offset provided by information in the D/A converters.

If the data bits D_0 to D_4 are all "0", the three D/A output voltages on Pins 6, 7 and 8 are equal to the tuning voltage (Pin 5) within the DAC offset voltages.

The four amplifiers have the same output characteristics with the maximum output voltage being 1.5 V lower than V_{CC2} in the worst case. The four analog outputs are short-circuit protected. At power-up, the D/A outputs are undetermined.

The D/A converters are guaranteed to be monotonic with a voltage step variation of ± 0.5 LSB.

The D/A converters work correctly as long as the PLL loop is active. V_{TUN} is then between 0.3 V and $V_{CC2} - 1.5$ V. If the loop saturates, the DACs do not work.

The DAC-OFFSET is defined as the difference between the DAC output voltage (with bits D_0 to $D_4 = 0$) and the tuning voltage (PLL active). The DAC operation is guaranteed from 0.3 V to $V_{CC2} - 1.5$ V. On typical samples, the DACs will operate down to 0.2 V.

