

High-side driver with CurrentSense analog feedback for automotive seat heating systems



Octapak

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	4 mΩ
Current limitation (typ.)	I_{LIMH}	135 A
Stand-by current (max.)	I_{STBY}	0.5 μA

- AEC-Q100 qualified 
- General
 - Single channel smart high-side driver with CurrentSense analog feedback
 - Very low standby current
 - Compatible with 3.0 V and 5 V CMOS outputs
- Diagnostic functions
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection
 - Output short to V_{CC} detection
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Loss of ground and loss of V_{CC}
 - Configurable latch-off on overtemperature or power limitation
 - Reverse battery
 - Electrostatic discharge protection

Product status link

[VN7004SLH](#)

Product summary

Order code	VN7004SLHTR
Package	Octapak
Packing	Tape and reel

Application

Specially intended for Automotive seat heating systems.

Description

The device is a single channel high-side driver manufactured using ST proprietary VIPower technology and housed in the Octapak package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.

A combination of INPUT and FR_DIAG pins latches the output in case of fault, disables the latch-off functionality and enables OFF-state diagnostic.

1 Block diagram and pin description

Figure 1. Block diagram

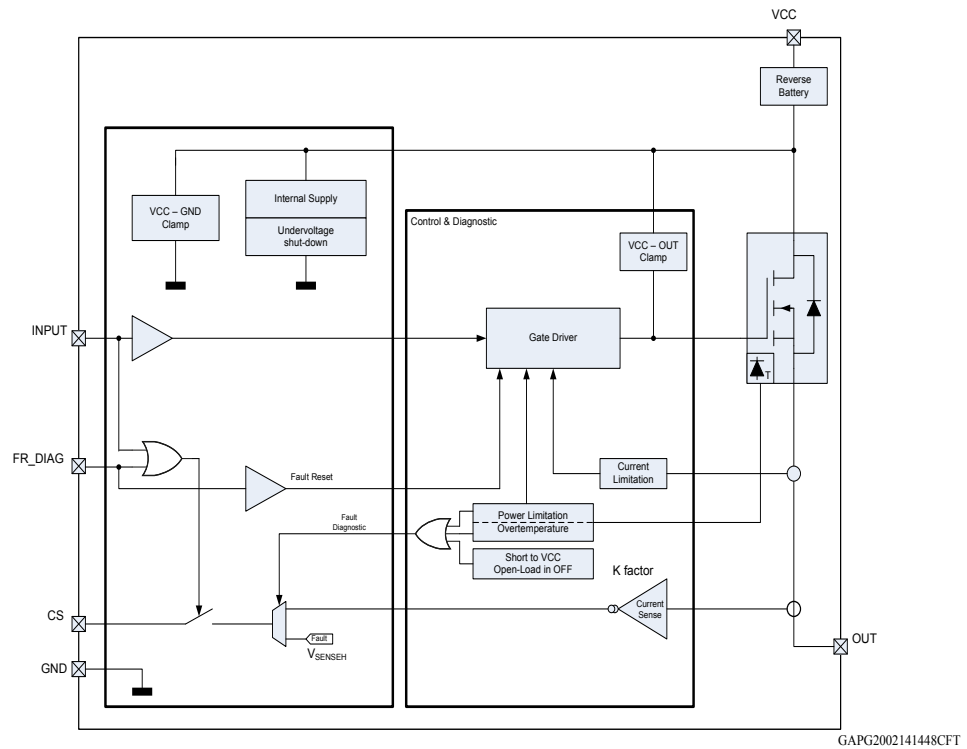
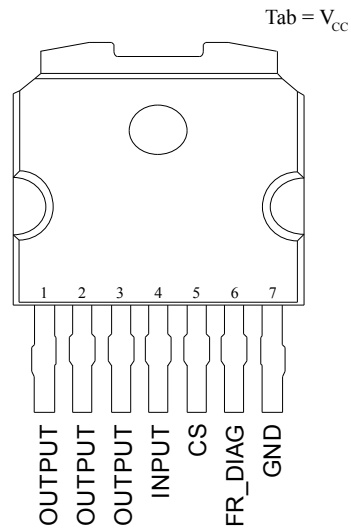


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT	Power outputs. All the pins must be connected together.
GND	Ground connection.
INPUT	Voltage controlled input pin with hysteresis. Compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
CS	Analog current sense output pin delivers a current proportional to the load current.
FR_DIAG	It sets auto-restart and latch-off protection. Moreover, it enables OFF-state diagnostic.

Figure 2. Configuration diagram (top view)



GAPG2804161118CFT

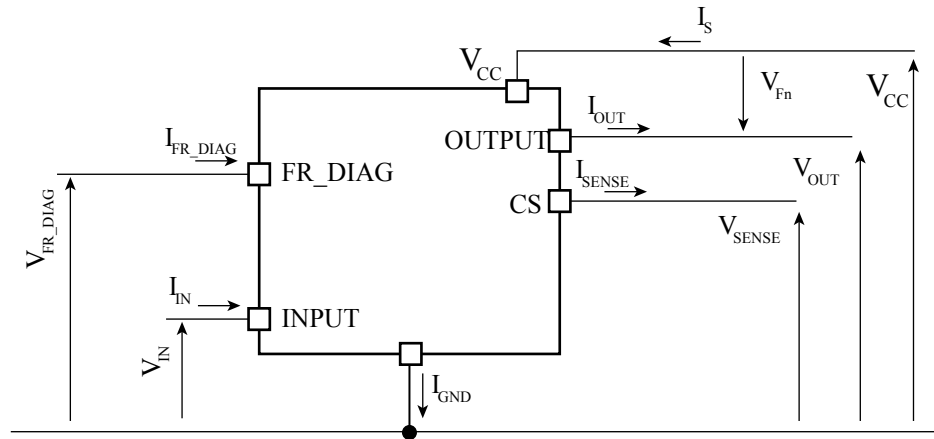
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CS	N.C.	Output	Input	FR_DIAG
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



GAPG0310141204CFT

Note: $V_F = V_{OUT} - V_{CC}$ when $V_{OUT} > V_{CC}$ and $INPUT = LOW$

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. **Absolute maximum ratings** may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; $R_L = 4 \Omega$)	40	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	38	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{FR_DIAG}	FR_DIAG DC input current		
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0 V$)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0 V$)	-20	
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.13 ms$; $T_{jstart} = 150 ^\circ C$)	105	mJ

Symbol	Parameter	Value	Unit
V _{ESD}	Electrostatic discharge (JEDEC 22A-114F)	4000	V
	• INPUT	2000	V
	• CurrentSense	4000	V
	• FR_DIAG	4000	V
	• OUTPUT	4000	V
	• V _{CC}	4000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
R _{thj-case}	Thermal resistance junction-case ⁽¹⁾	1.45	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽²⁾	58.1	
R _{thj-amb}	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾	15.6	

1. Device mounted on four-layers 2s2p PCB

2. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		4	13	28	V
V _{USD}	Undervoltage shutdown				4	
V _{USDReset}	Undervoltage shutdown reset				5	
V _{USDhyst}	Undervoltage shutdown hysteresis			0.3		
R _{ON}	On-state resistance	I _{OUT} = 15 A; T _j = 25°C		4		mΩ
		I _{OUT} = 15 A; T _j = 150°C			8	
		I _{OUT} = 15 A; V _{CC} = 4 V; T _j = 25°C			6	
R _{ON_Rev}	R _{DS(on)} in reverse battery condition	V _{CC} = -13 V; I _{OUT} = -15 A; T _j = 25°C		4		mΩ
V _{clamp}	Clamp voltage	I _S = 20 mA; T _j = -40°C	38			V
		I _S = 20 mA; 25°C < T _j < 150°C	41	46	52	V
I _{STBY}	Supply current in standby at V _{CC} = 13 V ⁽¹⁾	V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR_DIAG} = 0 V; T _j = 25°C			0.5	μA
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR_DIAG} = 0 V; T _j = 85°C ⁽²⁾			1.4	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{STBY}	Supply current in standby at $V_{CC} = 13\text{ V}$ ⁽¹⁾	$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{FR_DIAG} = 0\text{ V}$; $T_j = 125^\circ\text{C}$			11	μA
t_{D_STBY}	Standby mode blanking time	$V_{CC} = 13\text{ V}$; $V_{IN} = 5\text{ V}$; $V_{FR_DIAG} = 0\text{ V}$; $I_{OUT} = 0\text{ A}$	200	1150	2000	μs
$I_{S(ON)}$	Supply current	$V_{CC} = 13\text{ V}$; $V_{FR_DIAG} = 0\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		4	6.5	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	$V_{CC} = 13\text{ V}$; $V_{FR_DIAG} = 5\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 15\text{ A}$			9	mA
$I_{L(off)}$	Off-state output current at $V_{CC} = 13\text{ V}$	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25^\circ\text{C}$	0	0.01	0.5	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125^\circ\text{C}$	0		11	
V_F	Output - V_{CC} diode voltage	$I_{OUT} = -15\text{ A}$; $T_j = 150^\circ\text{C}$			0.7	V

1. PowerMOS leakage included.
2. Parameter specified by design; not subject to production test.

Table 6. Switching

$V_{CC} = 13\text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ ⁽¹⁾	Turn-on delay time	$R_L = 1.8\ \Omega$	290	640	1100	μs
$t_{d(off)}$ ⁽¹⁾	Turn-off delay time		160	330	510	
$(dV_{OUT}/dt)_{on}$ ⁽¹⁾	Turn-on voltage slope	$R_L = 1.8\ \Omega$	0.015	0.023	0.041	V/ μs
$(dV_{OUT}/dt)_{off}$ ⁽¹⁾	Turn-off voltage slope		0.018	0.031	0.056	
W_{ON}	Switching energy losses at turn-on (t_{won})	$R_L = 1.8\ \Omega$	—	11.5	18 ⁽²⁾	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	$R_L = 1.8\ \Omega$	—	8	12 ⁽²⁾	mJ
t_{SKEW} ⁽¹⁾	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 1.8\ \Omega$	-780	-410	-40	μs

1. See Figure 6. Switching times and Pulse skew.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 7. Logic inputs

7 V < V _{CC} < 28 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		
FR_DIAG characteristics (7 V < V _{CC} < 18 V)						
V _{FR_DIAGL}	Input low level voltage				0.9	V

7 V < V _{CC} < 28 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{FR_DIAGL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{FR_DIAGH}	Input high level voltage		2.1			V
I _{FR_DIAGH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{FR_DIAG(hyst)}	Input hysteresis voltage		0.2			V
V _{FR_DIAGCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		

Table 8. Protections

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH} ⁽¹⁾	DC short circuit current	V _{CC} = 13 V	80	135	175	A
		4 V < V _{CC} < 18 V ⁽²⁾			175	
I _{LIML}	Short circuit current during thermal cycling	V _{CC} = 13 V; T _R < T _j < T _{TSD}		38		A
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽²⁾		T _{RS} + 1	T _{RS} + 7		°C
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR_DIAG} = 5 V;	135			°C
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R) ⁽²⁾			7		°C
ΔT _{J_SD}	Dynamic temperature	V _{CC} = 13 V		60		K
t _{LATCH_RST}	Fault reset time for output unlatch ⁽²⁾	V _{FR_DIAG} = 5 V to 0 V; V _{IN} = 5 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2 A; L = 6 mH; T _j = -40°C	V _{CC} - 38			V
		I _{OUT} = 2 A; L = 6 mH; T _j = 25°C to 150°C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. CurrentSense

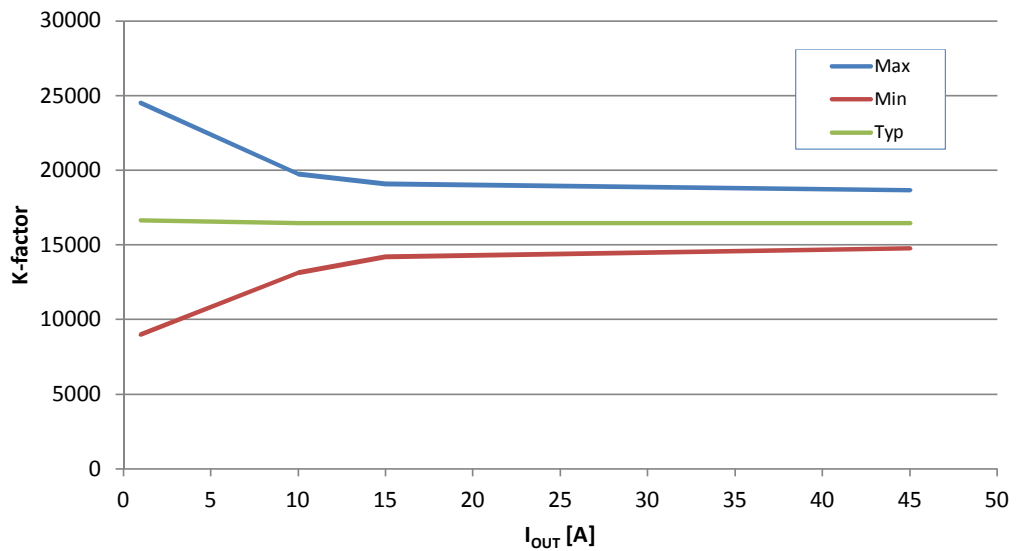
7 V < V _{CC} < 18 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	CurrentSense clamp voltage	V _{FR_DIAG} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{FR_DIAG} = 0 V; I _{SENSE} = -1 mA		7		V
CurrentSense characteristics						
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 1 A; V _{SENSE} = 0.5 V	9000	16650	24500	
dK ₀ /K ₀ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 1 A; V _{SENSE} = 0.5 V	-30		30	%

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 7 A; V _{SENSE} = 4 V	13150	16450	19750	
dK ₁ /K ₁ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 7 A; V _{SENSE} = 4 V	-10		10	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 12 A; V _{SENSE} = 4 V	14200	16450	19100	
dK ₂ /K ₂ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 12 A; V _{SENSE} = 4 V	-7		7	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 45 A; V _{SENSE} = 4 V	14760	16450	18670	
dK ₃ /K ₃ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 45 A; V _{SENSE} = 4 V	-5		5	%
I _{SENSE 0}	CurrentSense leakage current	CurrentSense disabled: V _{FR_DIAG} = 0 V	0		0.5	μA
		CurrentSense disabled: -1 V < V _{SENSE} < 5 ⁽¹⁾	-0.5		0.5	μA
		CurrentSense enabled: V _{IN} = 5 V; I _{OUT} = 0 A	0		25	μA
V _{OUT_CSD} ⁽¹⁾	Output Voltage for CurrentSense shutdown	V _{FR_DIAG} = 5 V; R _{SENSE} = 2.7 kΩ; V _{IN} = 5 V; I _{OUT} = 15 A		5		V
V _{SENSE_SAT}	Multisense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 10 kΩ; V _{FR_DIAG} = 5 V; V _{IN} = 5 V; I _{OUT} = 15 A; T _j = -40°C	5			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{FR_DIAG} = 5 V; T _j = 150°C	4			mA
I _{OUT_SAT} ⁽¹⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN} = 5 V; V _{FR_DIAG} = 5 V; T _j = -150°C	75			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{IN} = 0 V; V _{FR_DIAG} = 5 V	2	3	4	V
I _{L(off2)}	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40°C to 125°C	-100		-15	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 7. T _{DSTKON})	V _{IN} = 5 V to 0 V; V _{FR_DIAG} = 5 V; I _{OUT} = 0 A; V _{OUT} = 4 V	400	1480	2500	μs
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of FR_DIAG	V _{IN} = 0 V; V _{FR} = 0 V; V _{OUT} = 4 V; V _{FR_DIAG} = 0 V to 5 V			60	μs
t _{D_VOL}	OFF-state diagnostic delay time from rising edge of V _{OUT}	V _{IN} = 0 V; V _{FR_DIAG} = 5 V; V _{OUT} = 0 V to 4 V		5	30	μs
Fault diagnostic feedback (see Table 10. Truth table)						
V _{SENSEH}	CurrentSense output voltage in fault condition	V _{CC} = 13 V; V _{IN} = 0 V; V _{FR_DIAG} = 5 V; I _{OUT} = 0 A; V _{OUT} = 4 V; R _{SENSE} = 1 kΩ	5		6.6	V
I _{SENSEH}	CurrentSense output current in fault condition	V _{CC} = 13 V; V _{SENSE} = 5 V	7	20	30	mA
CurrentSense timings (current sense mode) ⁽³⁾						
t _{DSSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{FR_DIAG} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 Ω		1200	3750	μs

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta t_{\text{DSENSE2H}}$	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{FR_DIAG} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 0.87 Ω			690	μs
t_{DSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{FR_DIAG} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 Ω		510	880	μs

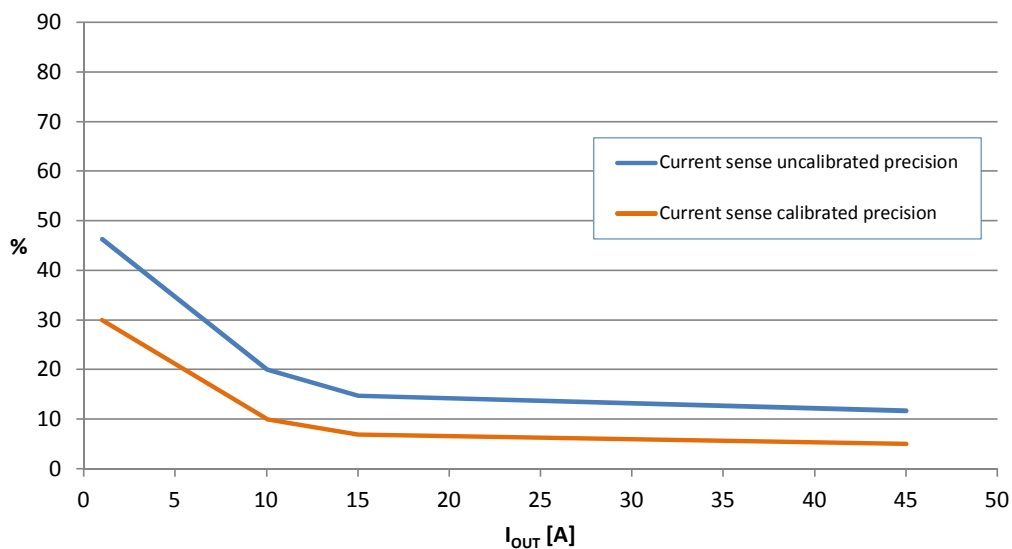
1. Parameter guaranteed by design and characterization; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
3. Transition delay is measured up to ±10% of final conditions.

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}



GADG1207161458SMD

Figure 5. Current sense precision vs. I_{OUT}



GADG1207161502SMD

Figure 6. Switching times and Pulse skew

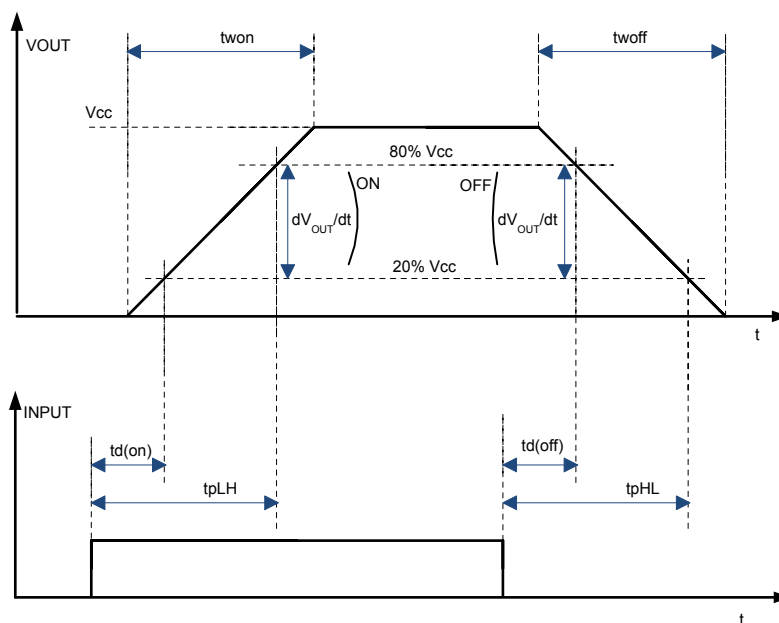
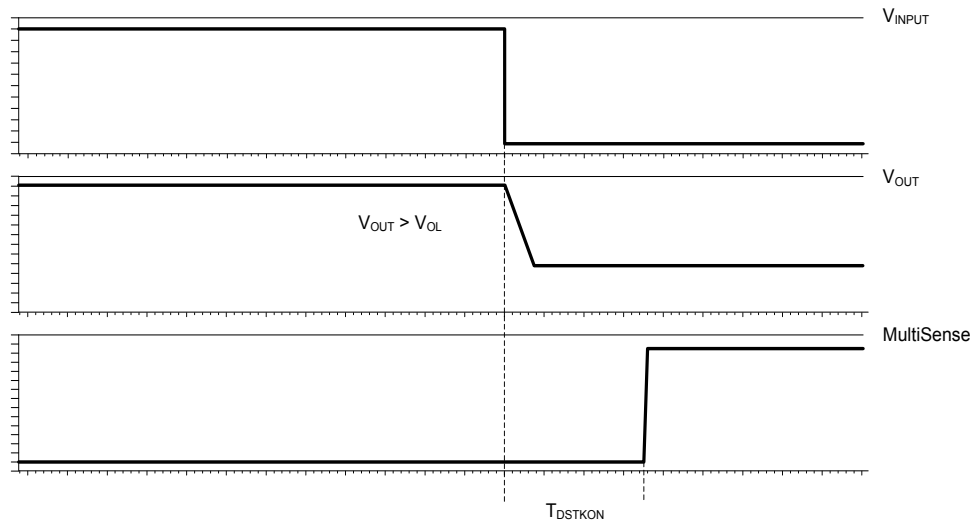


Figure 7. T_{DSTKON}


GAPG2609141140CFT

Table 10. Truth table

Mode	Conditions	IN	FR_DIAG	OUT	Current Sense	Comments
Stand by	All logic inputs low	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150^\circ\text{C}$	L	H	L	0	OFF-state diagnostic enabled
		H	L	H	$I_{\text{SENSE}} = 1/K * I_{\text{OUT}}$	Autorestart mode
		H	H	H	$I_{\text{SENSE}} = 1/K * I_{\text{OUT}}$	Latch-off mode
Overload	Overload or short to GND causing: $T_j > T_{\text{TSD}}$ or $\Delta T_j > \Delta T_{j_SD}$	H	L	H	V_{SENSEH}	Autorestart mode
		H	H	H	V_{SENSEH}	Latch-off mode
Under-voltage	$V_{\text{CC}} < V_{\text{USD}}$ (falling)	X	X	L	Hi-Z	Re-start when $V_{\text{CC}} > V_{\text{USD}} + V_{\text{USDhyst}}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	H	H	V_{SENSEH}	
	Open-load	L	H	H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	$< 0\text{ V}$	0	

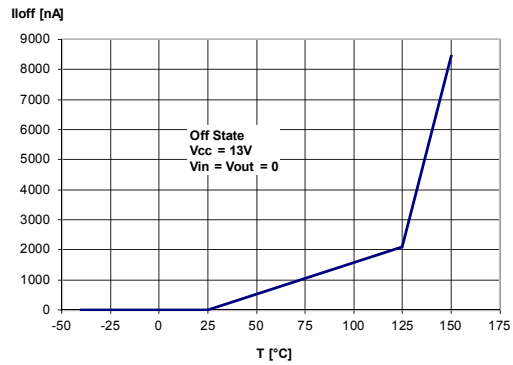
Table 11. FR_DIAG functionality

FR_DIAG	Input	Diagnostic	Overload protection
0	0	Disabled	X ⁽¹⁾
0	1	Enabled	Auto-restart
1	0	Enabled (OFF-state diagnostic)	X ⁽¹⁾
1	1	Enabled	Latch-off

1. X: do not care.

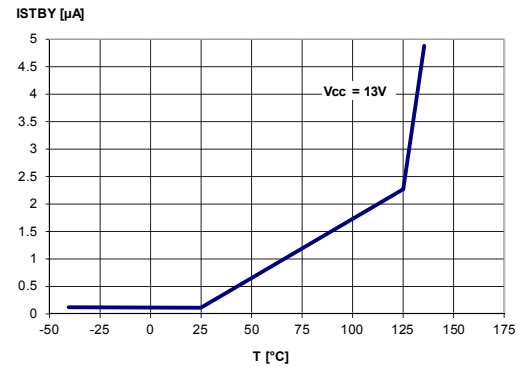
2.4 Electrical characteristics curves

Figure 8. OFF-state output current



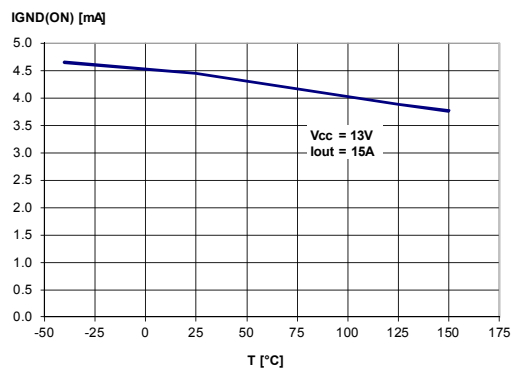
GADG1207161530SMD

Figure 9. Standby current



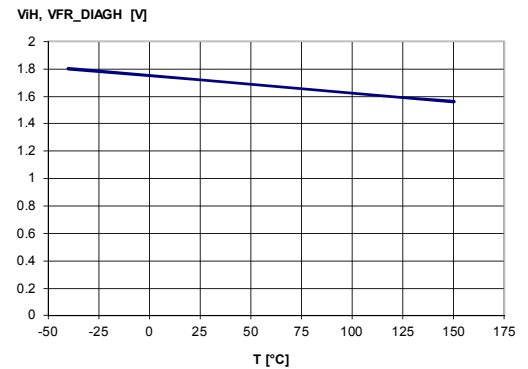
GADG1207161531SMD

Figure 10. $I_{GND(ON)}$ vs. I_{out}



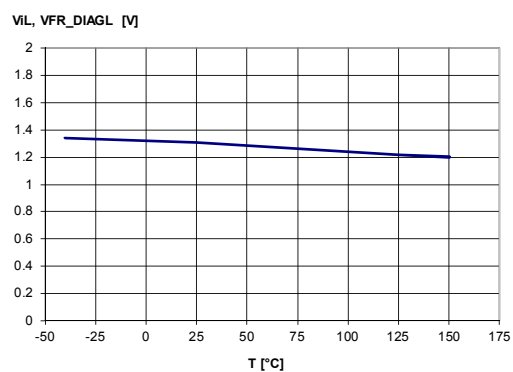
GADG1207161532SMD

Figure 11. Logic input high level voltage



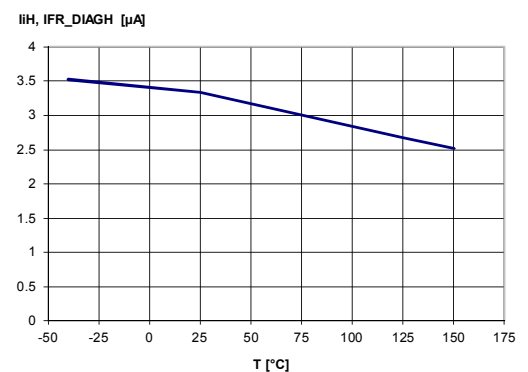
GADG1207161533SMD

Figure 12. Logic input low level voltage



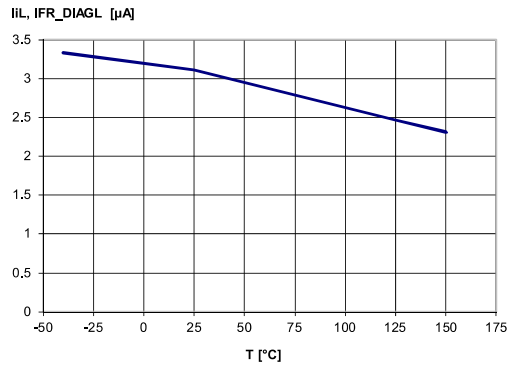
GADG1207161534SMD

Figure 13. High level logic input current



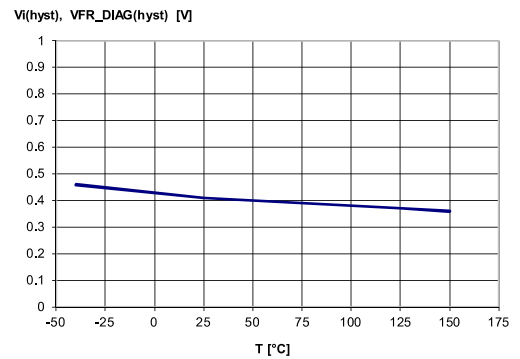
GADG1207161535SMD

Figure 14. Low level logic input current



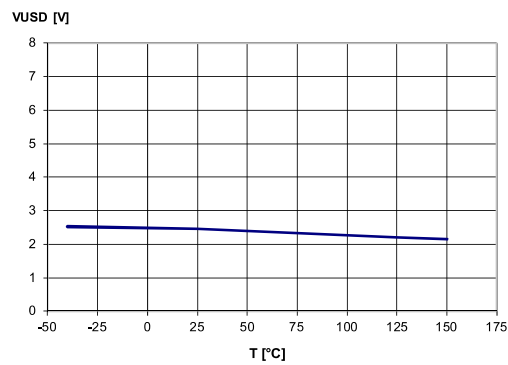
GADG1207161538SMD

Figure 15. Logic input hysteresis voltage



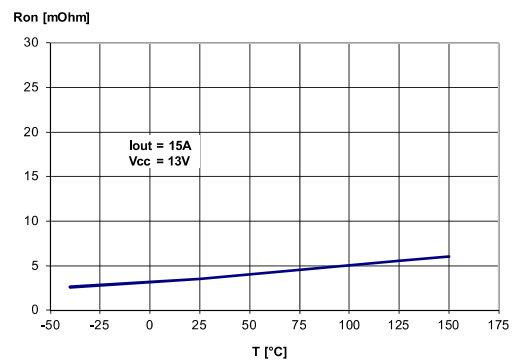
GADG1207161537SMD

Figure 16. Undervoltage shutdown



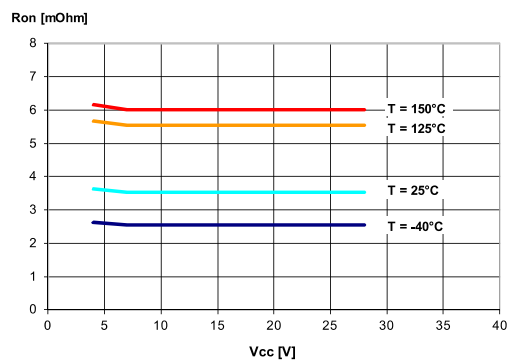
GADG1207161538SMD

Figure 17. On-state resistance vs. T_{case}



GADG1207161539SMD

Figure 18. On-state resistance vs. V_{CC}



GADG1207161540SMD

Figure 19. Turn-on voltage slope

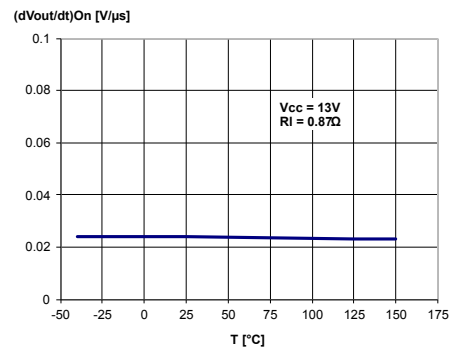


Figure 20. Turn-off voltage slope

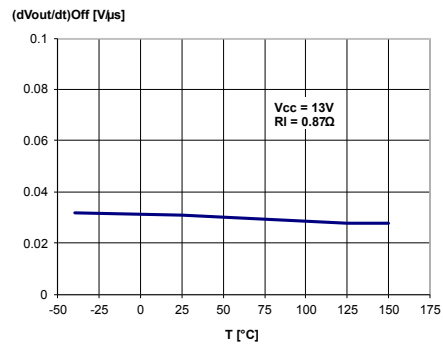


Figure 21. Won vs. T_{case}

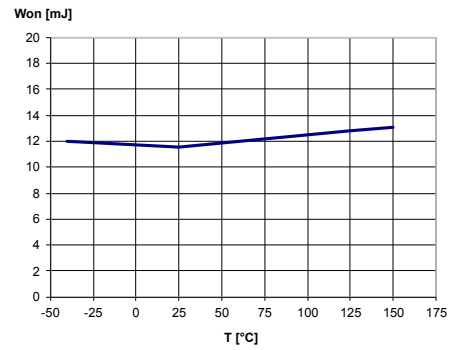


Figure 22. Woff vs. T_{case}

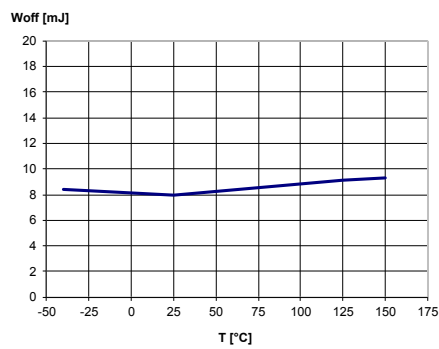
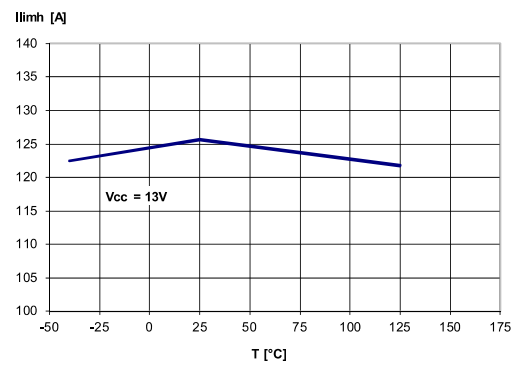
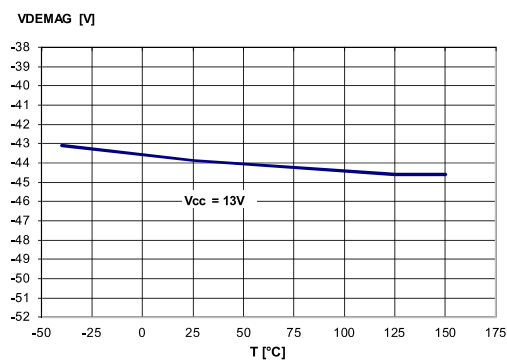


Figure 23. I_{LIMH} vs. T_{case}



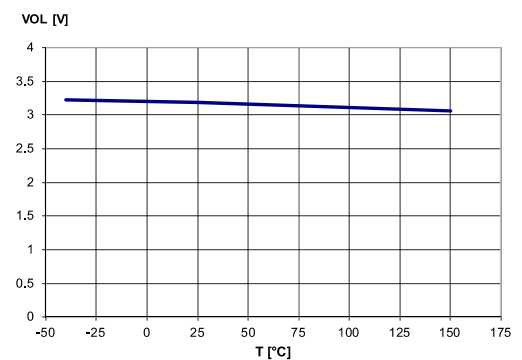
GADG1207161545SMD

Figure 24. Turn-off output voltage clamp



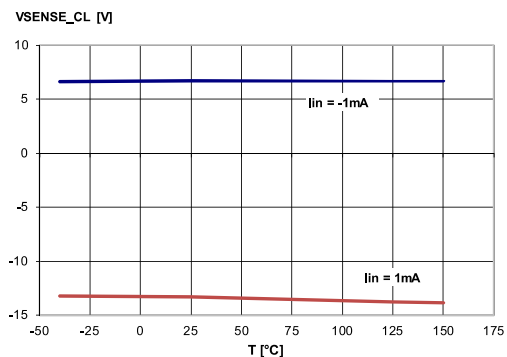
GADG1207161546SMD

Figure 25. OFF-state open-load voltage detection threshold



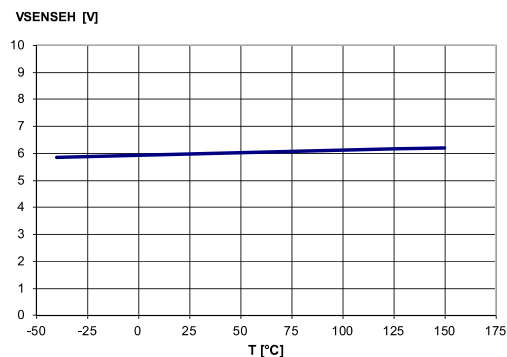
GADG1207161547SMD

Figure 26. V_s clamp vs. T_{case}



GADG1207161548SMD

Figure 27. V_{senseh} vs. T_{case}



GADG1207161549SMD

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . According to the voltage level on the FR_DIAG pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FR_DIAG = Low) or remains off (FR_DIAG = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FR_DIAG pin, the device switches on again as soon as its junction temperature drops to T_R (FR_DIAG = Low) or remains off (FR_DIAG = High).

3.3 Current limitation

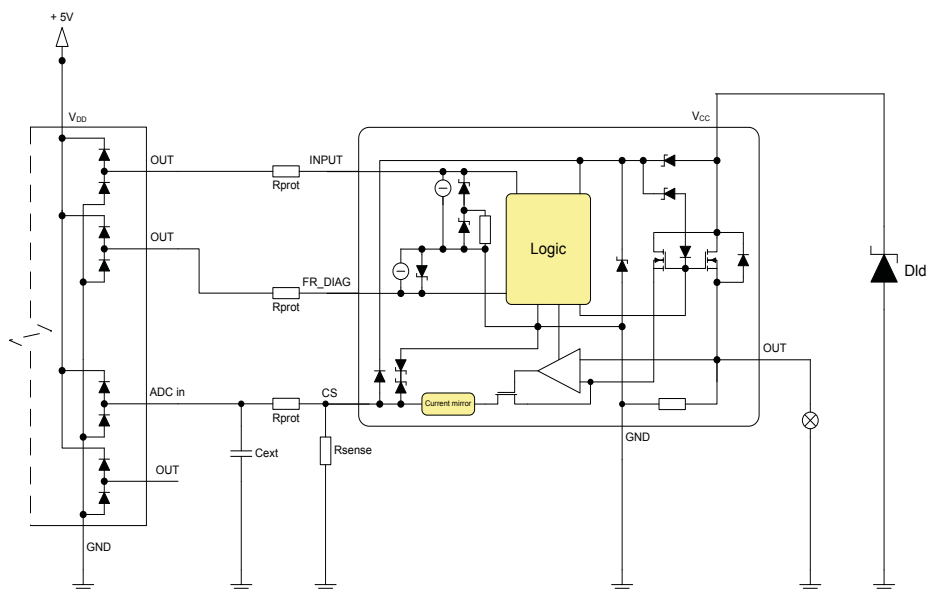
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative values during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMG} , allowing the inductor energy to be dissipated without damaging the device.

4 Application information

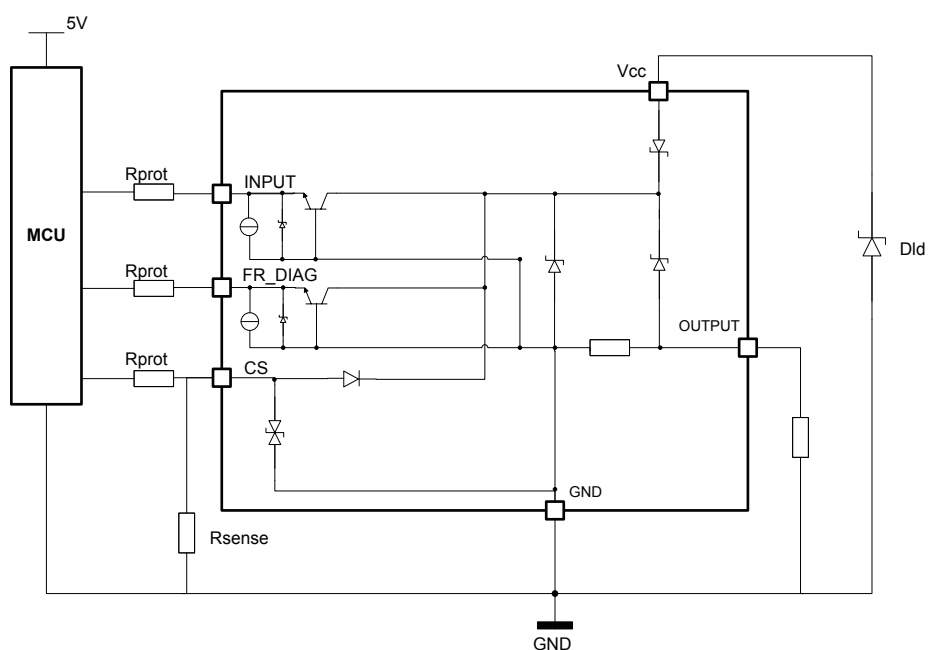
Figure 28. Application diagram



GAPG1607150817CFT

4.1 GND protection network against reverse battery

Figure 29. Simplified internal structure



GAPG1606150821CFT

The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 12. ISO 7637-2 - electrical transient conduction along supply line](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S ⁽¹⁾		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50μs, 2Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1μs, 50Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1μs, 50Ω
4 ⁽²⁾	IV	-7V	1 pulse			100ms, 0.01Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		40V	5 pulse	1 min		400ms, 2Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 40 V external suppressor referred to ground ($-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation:

$$V_{CC\text{peak}}/I_{\text{latchup}} \leq R_{\text{prot}} \leq (V_{OH} \mu C - V_{IH} - V_{GND}) / I_{IH\text{max}}$$

Calculation example:

For $V_{CC\text{peak}} = -150\text{ V}$; $I_{\text{latchup}} \geq 20\text{mA}$; $V_{OH} \mu C \geq 4.5\text{V}$

$$7.5\text{ k}\Omega \leq R_{\text{prot}} \leq 140\text{ k}\Omega.$$

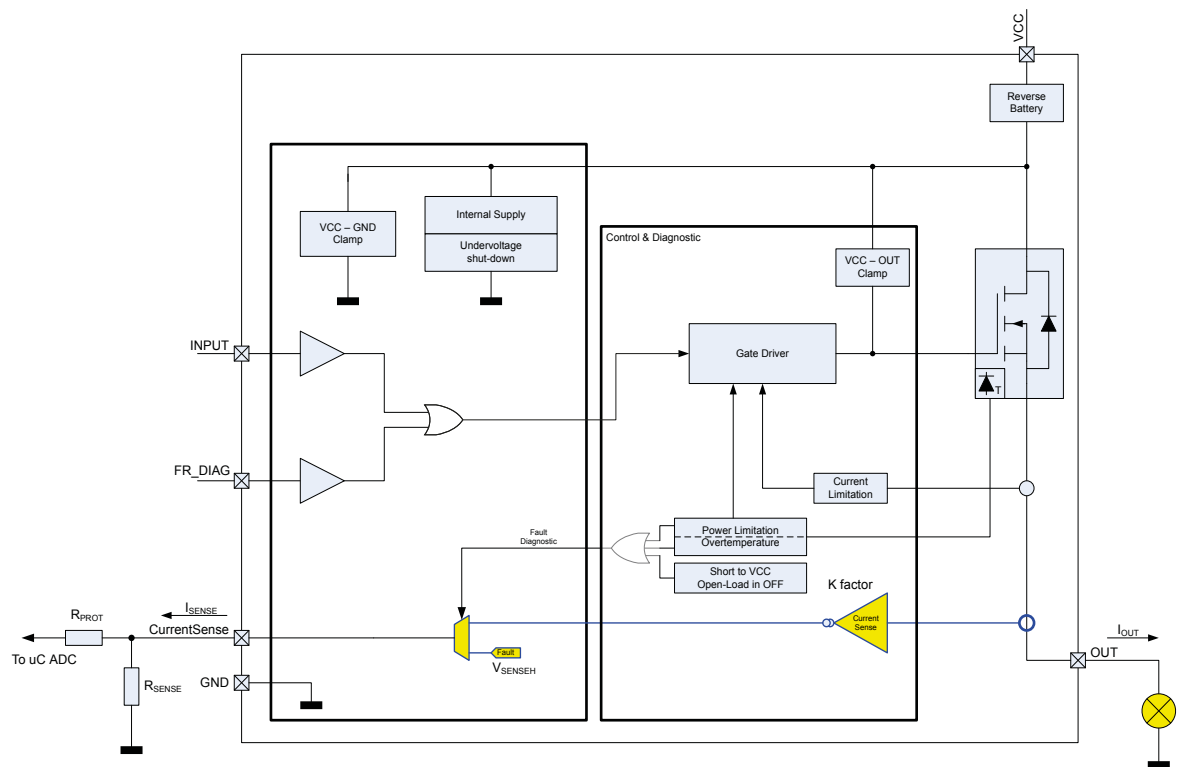
Recommended values: $R_{\text{prot}} = 15\text{ k}\Omega$

4.4 CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signal:

- Current monitor: current monitor of channel output current

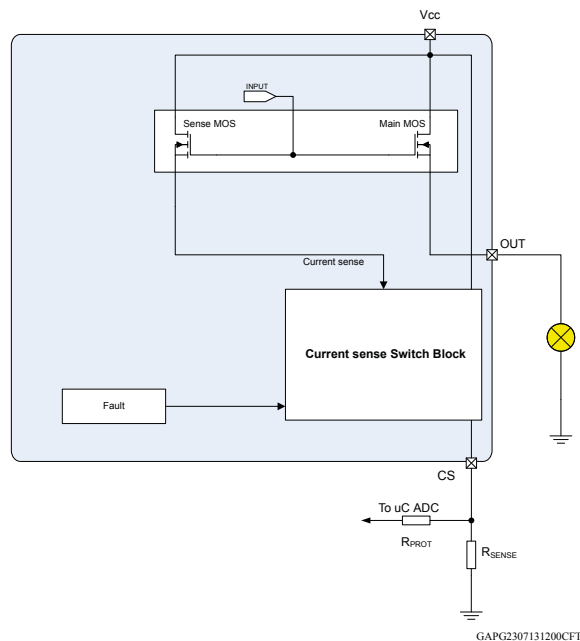
Figure 30. CurrentSense and diagnostic - block diagram



GAPG2704161550CFT

4.4.1 Principle of CurrentSense signal generation

Figure 31. CurrentSense block diagram



Current sense

This output is capable of providing:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to a known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CurrentSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

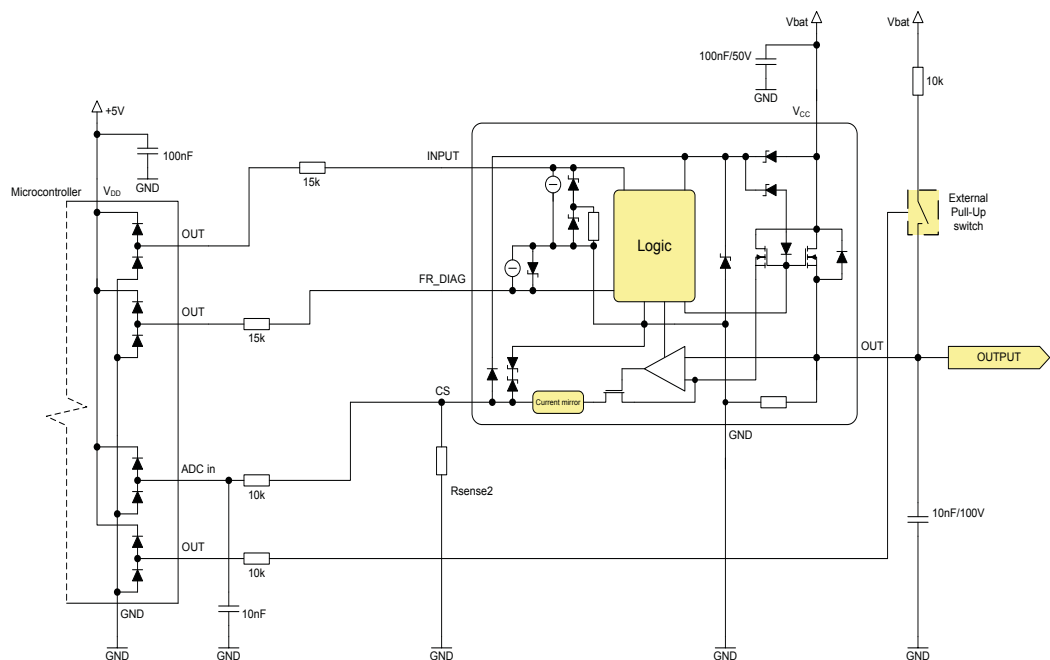
- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from the CS pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of the overall circuitry specifying the ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a "current limited" voltage source, V_{SENSEH} .

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH} .

Figure 32. Analogue HSD – open-load detection in off-state



GAPG1606150857CFT

Figure 33. Open-load / short to V_{CC} condition

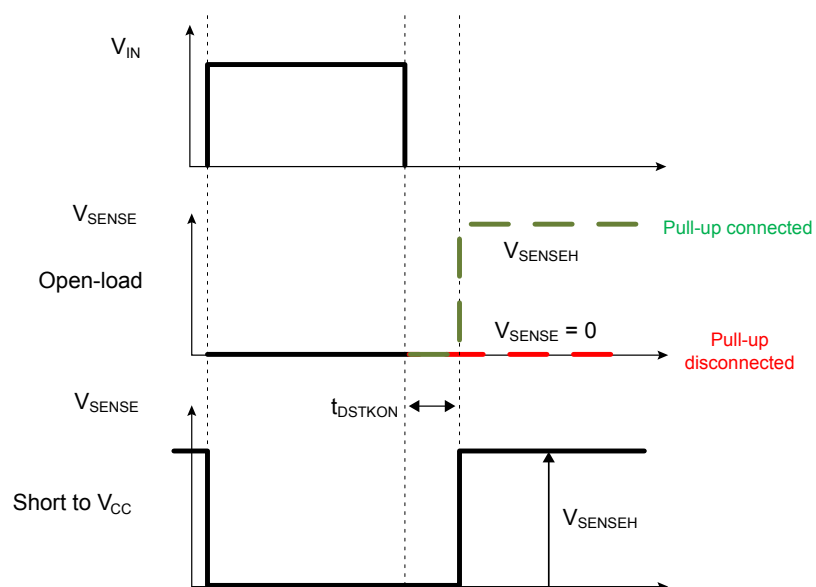


Table 13. CurrentSense pin levels in off-state

Condition	Output	CurrentSense	FR_DIAG
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

5 Package and PCB thermal data

5.1 Octapak thermal data

Figure 34. Octapak on two-layer PCB (2s0p to JEDEC JESD 51-5)

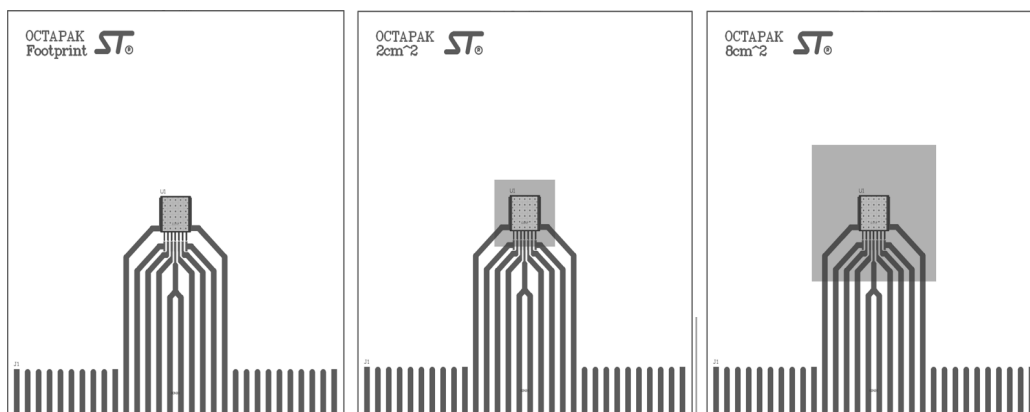


Figure 35. Octapak on four-layer PCB (2s2p to JEDEC JESD 51-7)

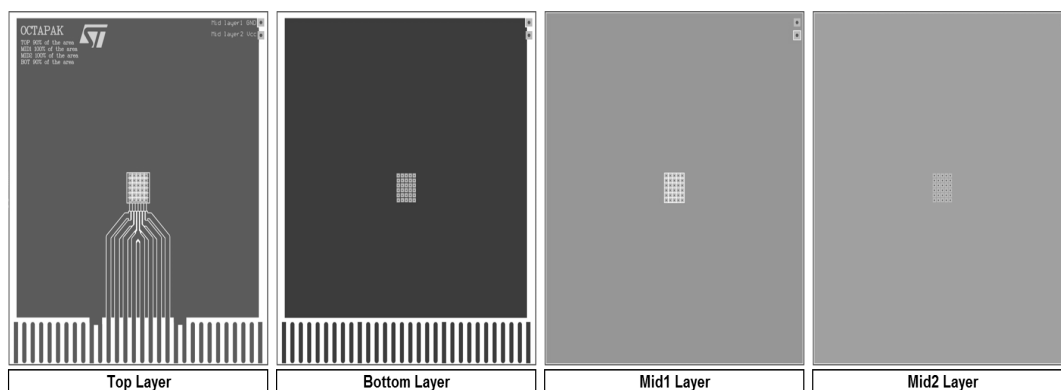
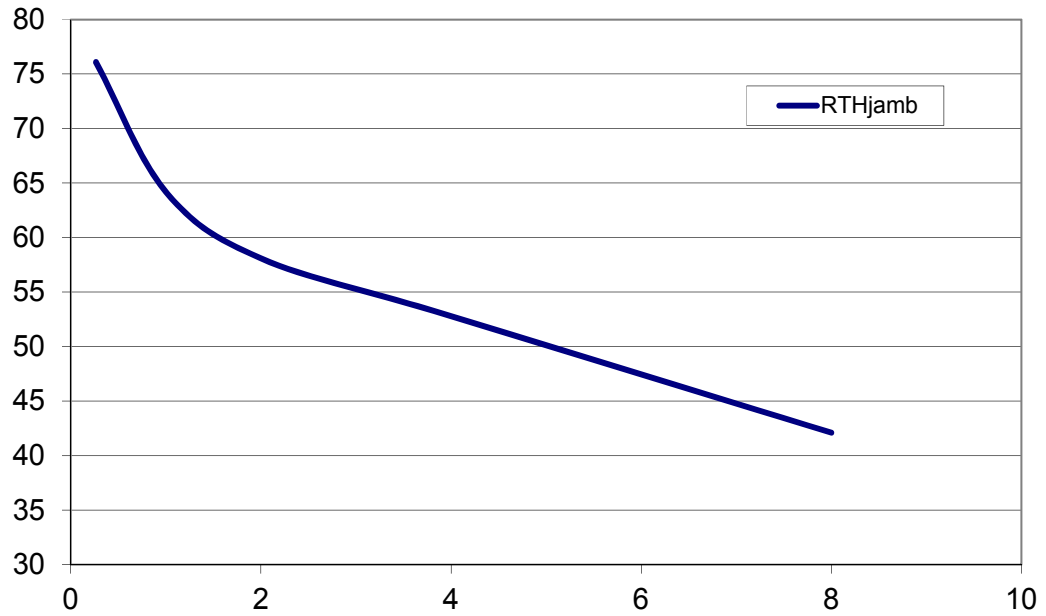


Table 14. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	6.4 mm x 7 mm

Dimension	Value
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

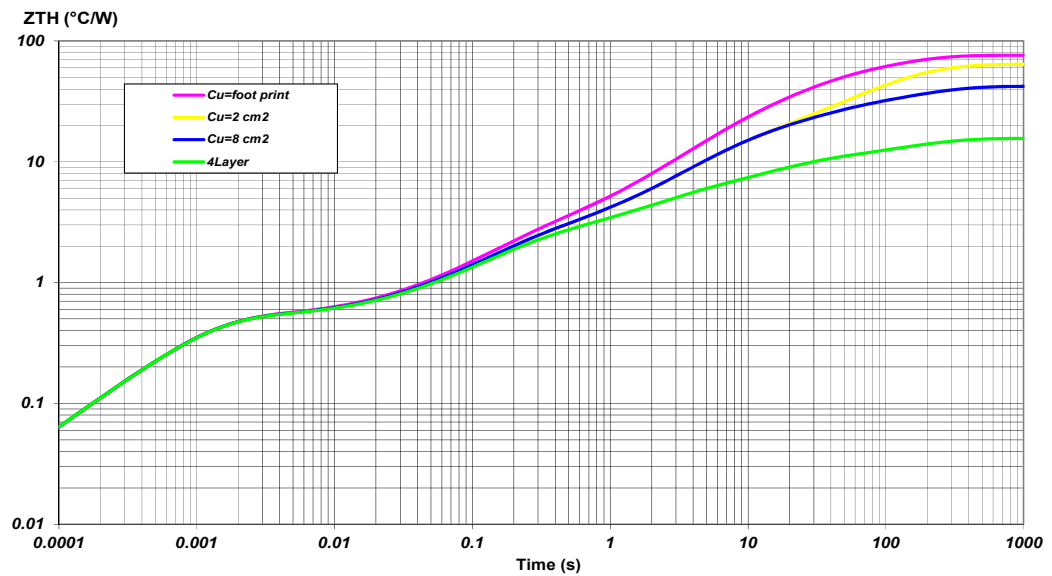
Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air conditions



$R_{thj-amb}$ on 4Layer PCB: 15.6°C/W

GADG1107161840SMD

Figure 37. Octapak thermal impedance junction ambient single pulse



GADG1107161845SMD

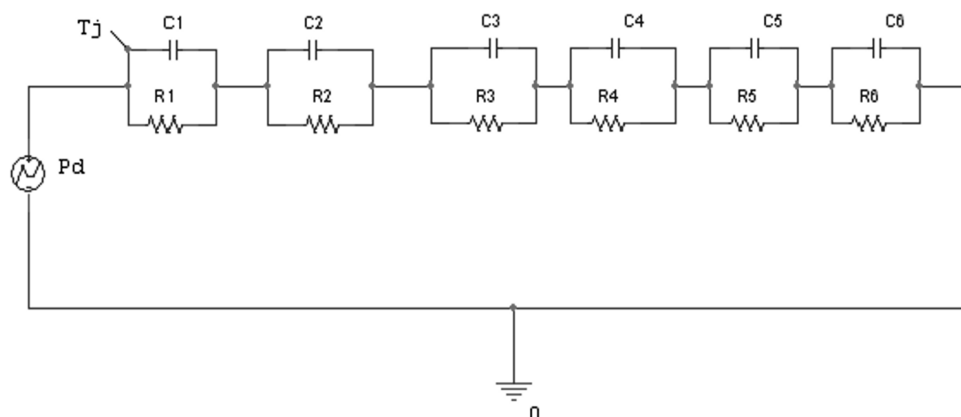
Pulse calculation formula

Equation:

$$Z_{TH\delta} = R_{TH} \cdot + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 38. Thermal fitting model for Octapak



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

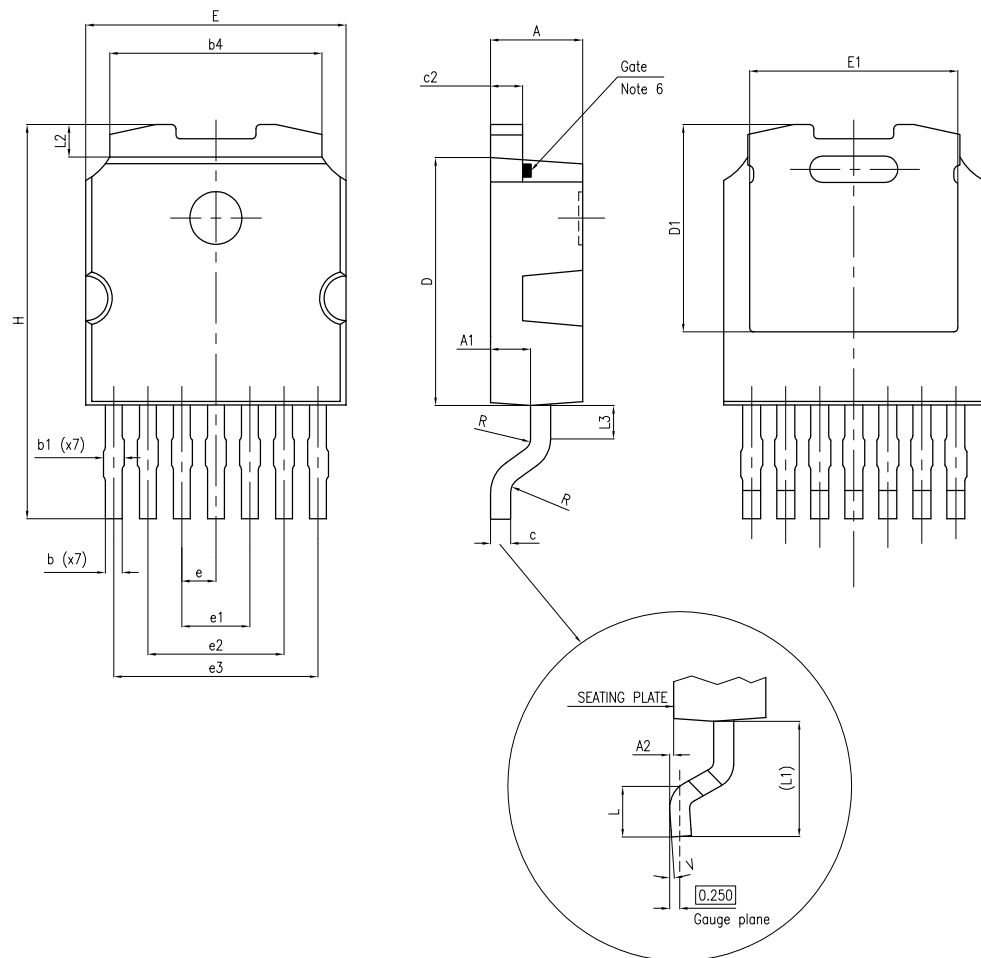
Area/island (cm ²)	Footprint	2	8	4L
R1 (°C/W)	0.01	0.01	0.01	0.01
R2 (°C/W)	0.5	0.5	0.5	0.5
R3 (°C/W)	1.6	1.6	1.6	1.6
R4 (°C/W)	10	10	10	2.5
R5 (°C/W)	28	20	12	5
R6 (°C/W)	36	26	18	6
C1 (W.s/°C)	0.001	0.001	0.001	0.001
C2 (W.s/°C)	0.0018	0.0018	0.0018	0.0018
C3 (W.s/°C)	0.11	0.11	0.11	0.11
C4 (W.s/°C)	0.6	0.6	0.6	0.8
C5 (W.s/°C)	0.8	1.4	2.2	3
C6 (W.s/°C)	3	6	9	25

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Octapak package information

Figure 39. Octapak package dimensions



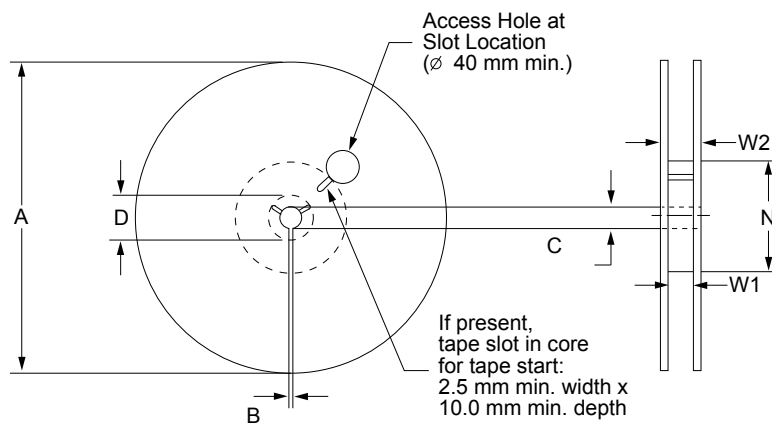
GAPGCFT00665

Table 16. Octapak mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.90	1.00	1.10
A2	0.03		0.15
b	0.38	0.45	0.52
b1			0.70
b4	5.20	5.30	5.40
c	0.45	0.50	0.60
c2	0.75	0.80	0.90
D	6.00	6.10	6.20
D1		5.15	
E	6.40	6.50	6.60
E1		5.30	
e	0.85 BSC		
e1	1.60	1.70	1.80
e2	3.30	3.40	3.50
e3	5.00	5.10	5.20
H	9.35	9.70	10.10
L	1.00		—
(L1)		2.80	
L2		0.80	
L3		0.85	
R	0.40 BSC		
V2	0°		8°

6.2 Octapak packing information

Figure 40. Octapak reel 13"



TAPG2004151655CFT

Table 17. Reel dimensions

Description	Value ⁽¹⁾
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D	20.2
N	100
W1 (+2 /-0)	16.4
W2 (max)	22.4

1. All dimensions are in mm.

Figure 41. Octapak carrier tape

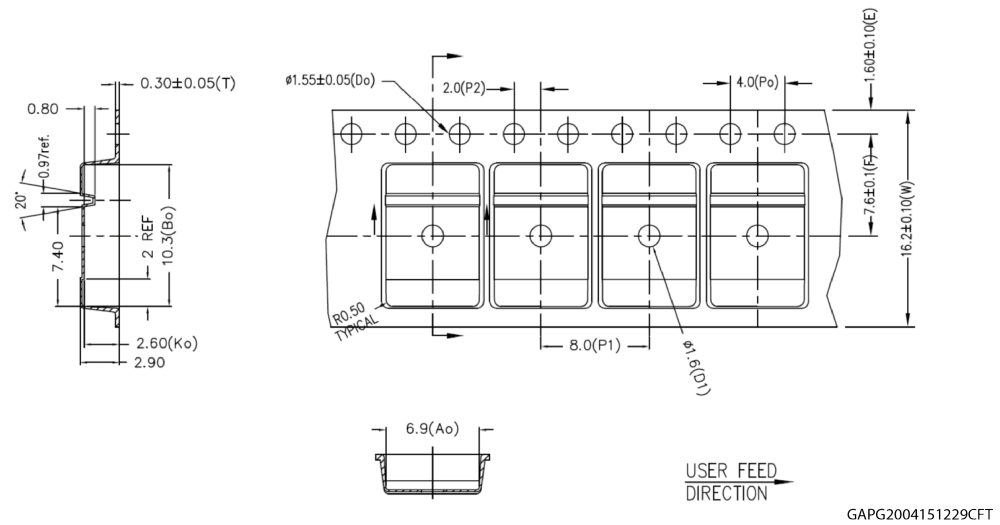
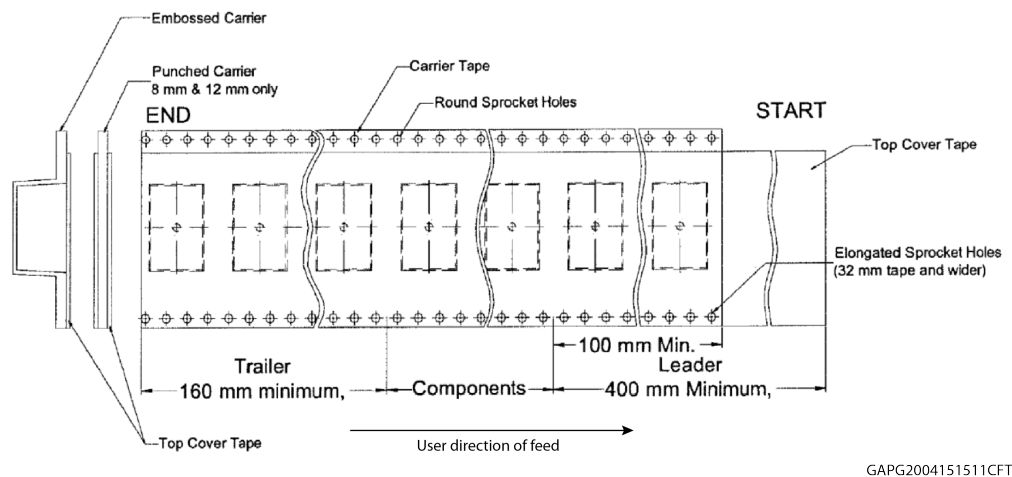
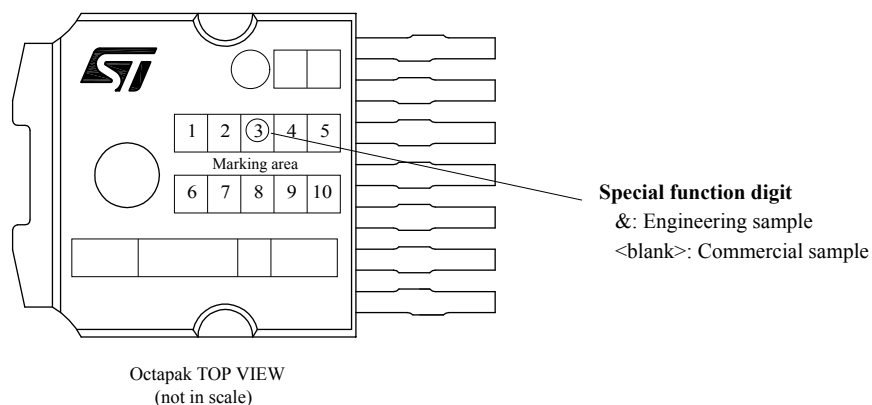


Figure 42. Octapak schematic drawing of leader and trailer tape



6.3 Octapak marking information

Figure 43. Octapak marking information



GAPG1604151015CFT

Parts marked as "&" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 18. Document revision history

Date	Version	Changes
15-Mar-2021	1	Initial release.
28-Oct-2021	2	Updated features in cover page. Updated Table 5. Power section and Table 9. CurrentSense . Added Section 2.4 Electrical characteristics curves .

Contents

1	Block diagram and pin description	2
2	Electrical specification	4
2.1	Absolute maximum ratings	4
2.2	Thermal data	5
2.3	Main electrical characteristics	5
2.4	Electrical characteristics curves	12
3	Protections	16
3.1	Power limitation	16
3.2	Thermal shutdown	16
3.3	Current limitation	16
3.4	Negative voltage clamp	16
4	Application information	17
4.1	GND protection network against reverse battery	17
4.2	Immunity against transient electrical disturbances	18
4.3	MCU I/Os protection	18
4.4	CS - analog current sense	19
4.4.1	Principle of CurrentSense signal generation	20
4.4.2	Short to VCC and OFF-state open-load detection	22
5	Package and PCB thermal data	23
5.1	Octapak thermal data	23
6	Package information	26
6.1	Octapak package information	26
6.2	Octapak packing information	28
6.3	Octapak marking information	30
	Revision history	31

List of tables

Table 1.	Pin functions	2
Table 2.	Suggested connections for unused and not connected pins	3
Table 3.	Absolute maximum ratings	4
Table 4.	Thermal data	5
Table 5.	Power section	5
Table 6.	Switching	6
Table 7.	Logic inputs	6
Table 8.	Protections	7
Table 9.	CurrentSense	7
Table 10.	Truth table	11
Table 11.	FR_DIAG functionality	11
Table 12.	ISO 7637-2 - electrical transient conduction along supply line	18
Table 13.	CurrentSense pin levels in off-state	22
Table 14.	PCB properties	23
Table 15.	Thermal parameters	25
Table 16.	Octapak mechanical data	27
Table 17.	Reel dimensions	28
Table 18.	Document revision history	31

List of figures

Figure 1.	Block diagram	2
Figure 2.	Configuration diagram (top view).	3
Figure 3.	Current and voltage conventions.	4
Figure 4.	I_{OUT}/I_{SENSE} versus I_{OUT}	9
Figure 5.	Current sense precision vs. I_{OUT}	10
Figure 6.	Switching times and Pulse skew	10
Figure 7.	T_{DSTKON}	11
Figure 8.	OFF-state output current	12
Figure 9.	Standby current	12
Figure 10.	$I_{GND(ON)}$ vs. I_{out}	12
Figure 11.	Logic input high level voltage	12
Figure 12.	Logic input low level voltage	12
Figure 13.	High level logic input current.	12
Figure 14.	Low level logic input current	13
Figure 15.	Logic input hysteresis voltage.	13
Figure 16.	Undervoltage shutdown	13
Figure 17.	On-state resistance vs. T_{case}	13
Figure 18.	On-state resistance vs. V_{CC}	13
Figure 19.	Turn-on voltage slope	13
Figure 20.	Turn-off voltage slope	14
Figure 21.	W_{on} vs. T_{case}	14
Figure 22.	W_{off} vs. T_{case}	14
Figure 23.	I_{LIMH} vs. T_{case}	14
Figure 24.	Turn-off output voltage clamp	14
Figure 25.	OFF-state open-load voltage detection threshold	14
Figure 26.	V_s clamp vs. T_{case}	15
Figure 27.	V_{senseh} vs. T_{case}	15
Figure 28.	Application diagram.	17
Figure 29.	Simplified internal structure	17
Figure 30.	CurrentSense and diagnostic - block diagram.	19
Figure 31.	CurrentSense block diagram	20
Figure 32.	Analogue HSD – open-load detection in off-state	21
Figure 33.	Open-load / short to V_{CC} condition	21
Figure 34.	Octapak on two-layer PCB (2s0p to JEDEC JESD 51-5)	23
Figure 35.	Octapak on four-layer PCB (2s2p to JEDEC JESD 51-7)	23
Figure 36.	$R_{thj-amb}$ vs PCB copper area in open box free air conditions	24
Figure 37.	Octapak thermal impedance junction ambient single pulse	24
Figure 38.	Thermal fitting model for Octapak	25
Figure 39.	Octapak package dimensions.	26
Figure 40.	Octapack reel 13"	28
Figure 41.	Octapak carrier tape	29
Figure 42.	Octapak schematic drawing of leader and trailer tape	29
Figure 43.	Octapak marking information	30

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2021 STMicroelectronics – All rights reserved