- **Member of the Texas Instruments Widebus+™ Family**

- **Supports SSTL_2 Data Inputs**

- **Outputs Meet SSTL_2 Class II Specifications**

- **Differential Clock Inputs (CLK and $\overline{CLK}$)**

- **Supports LVCMOS Switching Levels on the $\overline{RESET}$ Input**

- **$\overline{RESET}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**

- **Flow-through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

description

This 26-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{RESET}$) input. All outputs are SSTL_2, Class II compatible.

The SN74SSTV32877 operates from a differential clock (CLK and $\overline{CLK}$). Data are registered at the crossing of CLK going high and $\overline{CLK}$ going low.

The device supports low-power standby operation. When $\overline{RESET}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{RESET}$ input always must be held at a valid logic high or low level. When $\overline{OE}$ and $\overline{RESET}$ are high, the outputs are in the high-impedance state.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

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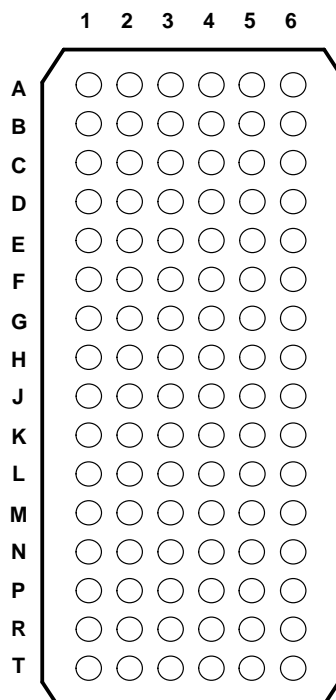Copyright © 2002, Texas Instruments Incorporated

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SN74SSTV32877
26-BIT REGISTERED BUFFER
WITH SSTL_2 INPUTS AND OUTPUTS

SCES378B – OCTOBER 2001 – REVISED MAY 2002

GKE PACKAGE
(TOP VIEW)

terminal assignments

	1	2	3	4	5	6
A	D1	V_{CC}	GND	V_{DDQ}	Q1	Q2
B	D3	D2	V_{REF}	GND	Q3	Q4
C	D5	D4	NC	GND	Q5	Q6
D	D7	D6	GND	V_{DDQ}	Q7	Q8
E	D9	D8	V_{CC}	GND	Q9	V_{DDQ}
F	D11	D10	GND	V_{DDQ}	Q10	GND
G	D13	D12	V_{CC}	V_{DDQ}	Q12	Q11
H	D15	D14	GND	GND	GND	Q13
J	CLK	NC	GND	GND	GND	Q14
K	$\overline{CLK}$	$\overline{RESET}$	V_{CC}	V_{DDQ}	Q15	Q16
L	D16	D17	GND	V_{DDQ}	Q17	GND
M	D18	D19	V_{CC}	GND	Q18	V_{DDQ}
N	D20	D21	GND	V_{DDQ}	Q20	Q19
P	D22	D23	NC	GND	Q22	Q21
R	D24	D25	$\overline{OE}$	GND	Q24	Q23
T	D26	V_{CC}	GND	V_{DDQ}	Q26	Q25

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTV32877GKER	SV877

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design
guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{RESET}$	$\overline{OE}$	CLK	$\overline{CLK}$	D	Q
H	L	↑	↓	H	H
H	L	↑	↓	L	L
H	L	L or H	L or H	X	Q_0
H	H	X	X	X	Z
L	X or floating	X or floating	X or floating	X or floating	L

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logic diagram (positive logic)

To 25 Other Channels
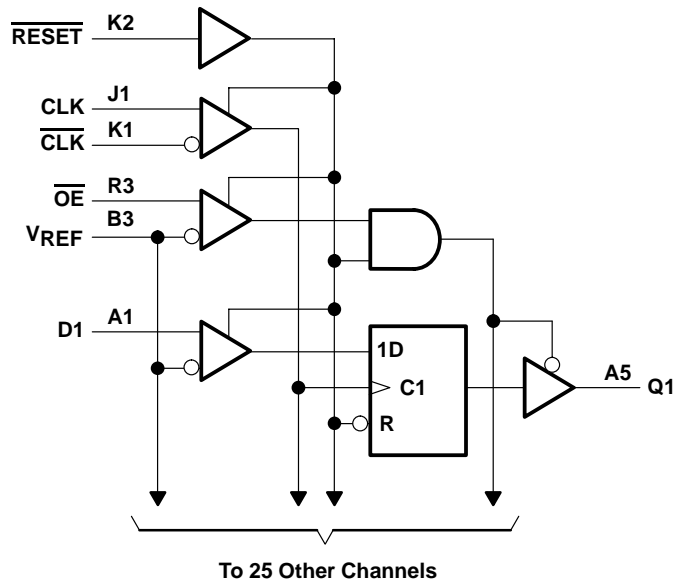
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} or V_{DDQ} .... −0.5 V to 3.6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ}) .... ±50 mA
Continuous current through each V_{CC}, V_{DDQ}, or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) .... 40°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage		2.3		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)		1.15	1.25	1.35	V
V_{TT}	Termination voltage		$V_{REF}-40mV$	V_{REF}	$V_{REF}+40mV$	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	$\overline{OE}$, data inputs	$V_{REF}+310mV$			V
V_{IL}	AC low-level input voltage	$\overline{OE}$, data inputs			$V_{REF}-310mV$	V
V_{IH}	DC high-level input voltage	$\overline{OE}$, data inputs	$V_{REF}+150mV$			V
V_{IL}	DC low-level input voltage	$\overline{OE}$, data inputs			$V_{REF}-150mV$	V
V_{IH}	High-level input voltage	$\overline{RESET}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{RESET}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	360			mV
I_{OH}	High-level output current				-20	mA
I_{OL}	Low-level output current				20	
T_A	Operating free-air temperature		0		70	°C

NOTE 4: The $\overline{RESET}$ input of the device must be held at V_{CC} or GND to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{IK}		$I_I = -18$ mA		2.3 V			−1.2	V
V_{OH}		$I_{OH} = -100$ µA		2.3 V to 2.7 V	V_{CC}−0.2			V
		$I_{OH} = -16$ mA		2.3 V	1.95			
V_{OL}		$I_{OL} = 100$ µA		2.3 V to 2.7 V			0.2	V
		$I_{OL} = 16$ mA		2.3 V			0.35	
I_I	All inputs	$V_I = V_{CC}$ or GND		2.7 V			±5	µA
I_{CC}	Static standby	$\overline{RESET} = $ GND	$I_O = 0$	2.7 V			40	µA
	Static operating	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					95	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	$I_O = 0$	2.5 V		44		µA/ MHz
	Dynamic operating – per each data input	$\overline{RESET} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				5		µA/ clock MHz/ D input
I_{OZ}	Outputs	$V_O = V_{CC}$ or GND,	$V_I (\overline{OE}) = V_{CC}$	2.7 V			±10	µA
r_{OH}	Output high	$I_{OH} = -20$ mA		2.3 V to 2.7 V	7		20	Ω
r_{OL}	Output low	$I_{OL} = 20$ mA		2.3 V to 2.7 V	7		20	Ω
$r_{O(\Delta)}$	$\lvert r_{OH} - r_{OL} \rvert$	$I_O = 20$ mA, $T_A = 25°C$		2.5 V			6	Ω
C_i‡	Data inputs and $\overline{OE}$	$V_I = V_{REF} \pm 310$ mV		2.5 V	2.5	3.3	4	pF
	CLK, $\overline{CLK}$	$V_{ICR} = 1.25$ V,	$V_{I(PP)} = 360$ mV		3	3.5	4	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND			3	4	4.5	
C_o‡	Outputs	$V_O = 1.7$ V or 0.8 V		2.5 V	6.5	7.6	9	pF

† All typical values are at $V_{CC} = 2.5$ V, $T_A = 25°C$.
‡ Measured with 50-MHz input frequency

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

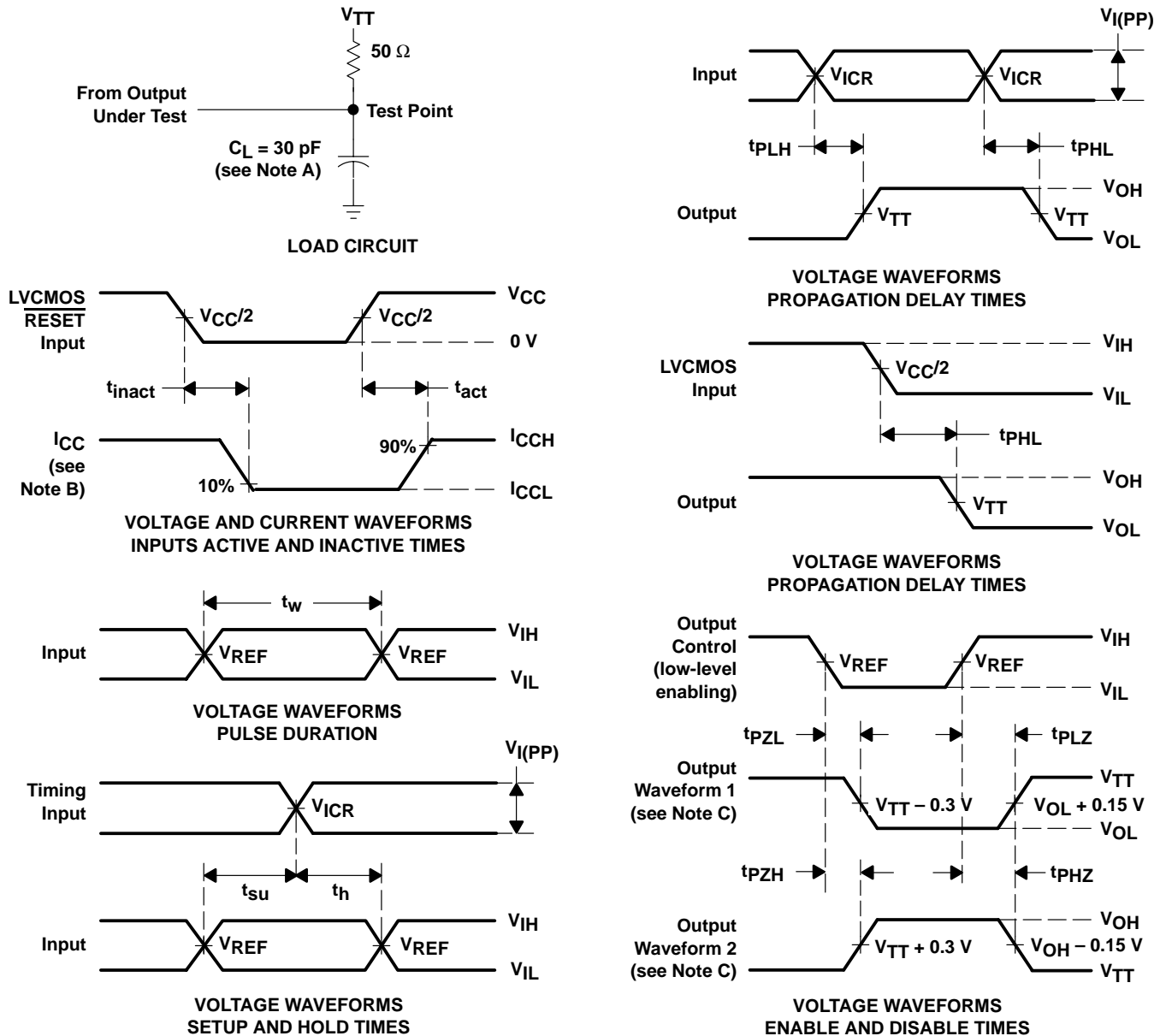|			V_{CC} = 2.5 V $\pm$ 0.2 V		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low		2.5		ns
t_{act}	Differential inputs active time (see Note 5)			22	ns
t_{inact}	Differential inputs inactive time (see Note 6)			22	ns
t_{su}	Setup time	Fast slew rate (see Notes 7 and 9)	Data before CLK↑, $\overline{CLK}$↓	0.75		ns
		Slow slew rate (see Notes 8 and 9)		0.9		
t_h	Hold time	Fast slew rate (see Notes 7 and 9)	Data after CLK↑, $\overline{CLK}$↓	0.75		ns
		Slow slew rate (see Notes 8 and 9)		0.9		

NOTES: 5. Data inputs must be low a minimum time of t_{act} min, after $\overline{RESET}$ is taken high.
6. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} min, after $\overline{RESET}$ is taken low.
7. Data signal input slew rate ≥1 V/ns
8. Data signal input slew rate ≥0.5 V/ns and <1 V/ns
9. CLK, $\overline{CLK}$ input slew rates are ≥1 V/ns.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V $\pm$ 0.2 V		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CLK and $\overline{CLK}$	Q	1.1	2.8	ns
t_{PHL}	$\overline{RESET}$	Q		5	ns
t_{en}	$\overline{OE}$	Q		5	ns
t_{dis}	$\overline{OE}$	Q		6.3	ns

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

V_{TT}

50 Ω

From Output Under Test — Test Point

C_L = 30 pF (see Note A)

**VOLTAGE AND CURRENT WAVEFORMS
INPUTS ACTIVE AND INACTIVE TIMES**

LVCMOS $\overline{RESET}$ Input

$V_{CC}/2$ $V_{CC}/2$

V_{CC}

0 V

t_{inact} t_{act}

I_{CC} (see Note B)

90%

10%

I_{CCH}

I_{CCL}

**VOLTAGE WAVEFORMS
PULSE DURATION**

t_w

Input

V_{REF} V_{REF}

V_{IH}

V_{IL}

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

Timing Input

V_{ICR}

$V_{I(PP)}$

t_{su} t_h

Input

V_{REF} V_{REF}

V_{IH}

V_{IL}

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

Input

V_{ICR} V_{ICR}

$V_{I(PP)}$

t_{PLH} t_{PHL}

Output

V_{TT} V_{TT}

V_{OH}

V_{OL}

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

LVCMOS Input

$V_{CC}/2$

V_{IH}

V_{IL}

t_{PHL}

Output

V_{TT}

V_{OH}

V_{OL}

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

Output Control (low-level enabling)

V_{REF} V_{REF}

V_{IH}

V_{IL}

t_{PZL} t_{PLZ}

Output Waveform 1 (see Note C)

$V_{TT} - 0.3$ V $V_{OL} + 0.15$ V

V_{TT}

V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 (see Note C)

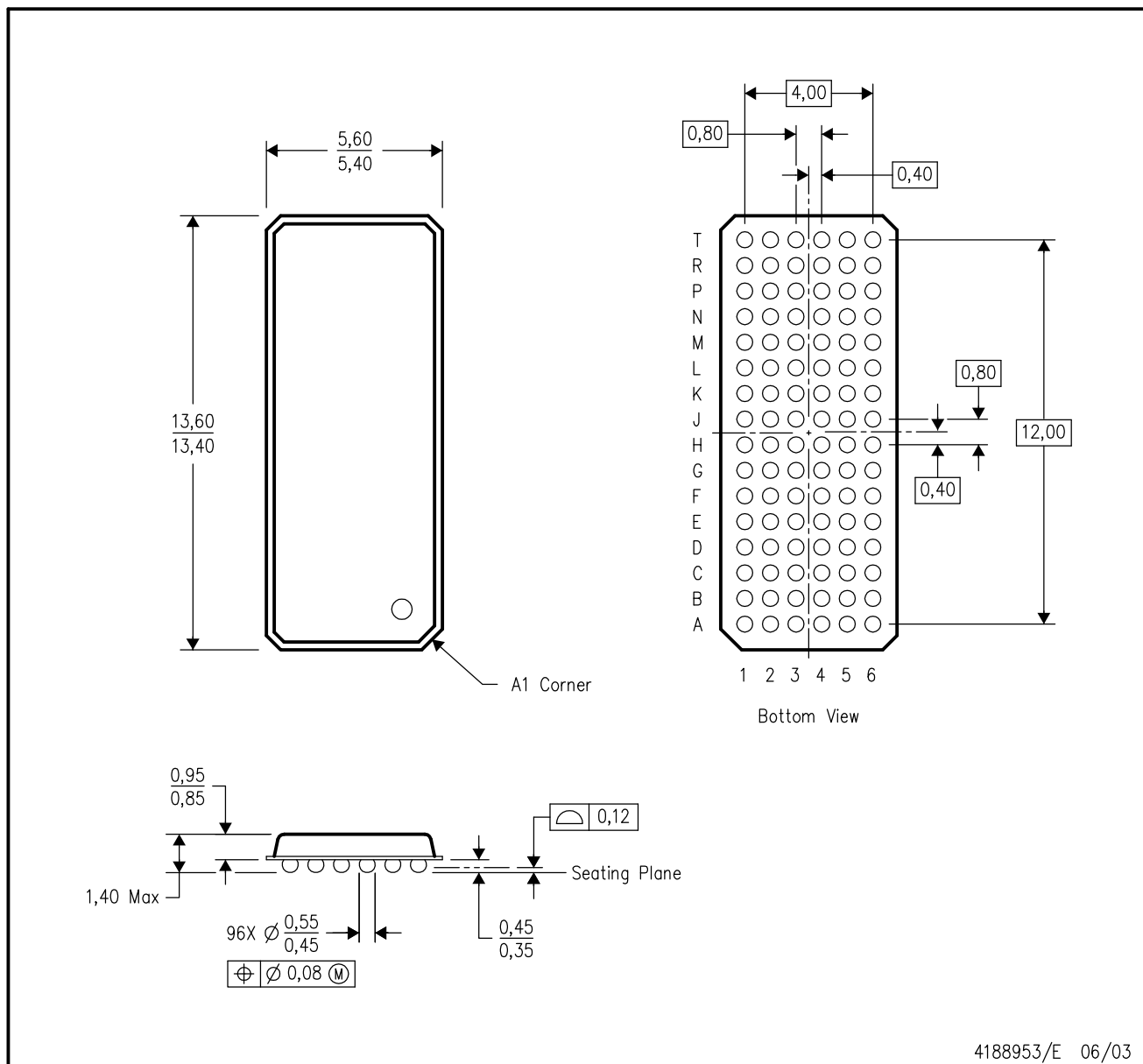$V_{TT} + 0.3$ V $V_{OH} - 0.15$ V

V_{OH}

V_{TT}

NOTES: A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
E. The outputs are measured one at a time with one transition per measurement.
F. $V_{TT} = V_{REF} = V_{DDQ}/2$
G. $V_{IH} = V_{REF} + 310$ mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
H. $V_{IL} = V_{REF} - 310$ mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
I. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
J. t_{PZL} and t_{PZH} are the same as t_{en}.
K. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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GKE (R−PBGA−N96)   PLASTIC BALL GRID ARRAY

5,60
5,40

13,60
13,40

A1 Corner

4,00

0,80

0,40

T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

0,80

12,00

0,40

1 2 3 4 5 6

Bottom View

0,95
0,85

1,40 Max

Seating Plane

0,12

96X Ø 0,55
0,45

0,45
0,35

⊕ Ø 0,08 Ⓜ

4188953/E 06/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   MicroStar BGA™ configuration
         D.   Falls within JEDEC MO−205 variation CC.
         E.   This package is tin−lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead−free.

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