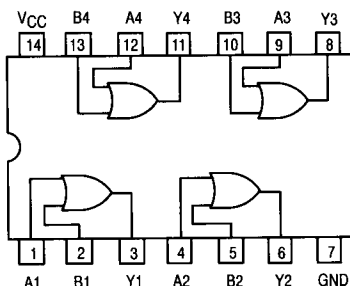




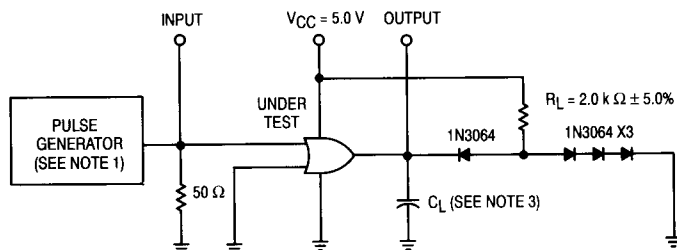
Quad 2-Input OR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30501

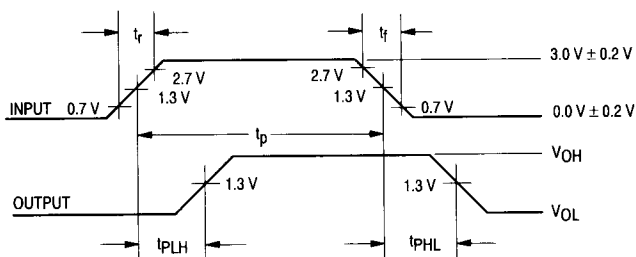
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. Pulse generator has the following characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_p = 0.5 \mu\text{s}$, $PRR = 1.0 \text{ MHz}$, and $Z_{OUT} \approx 50 \Omega$.
2. Terminal conditions (pins not designated may be high $\geq 2.0 \text{ V}$, low $\leq 0.7 \text{ V}$, or open).
3. $C_L = 50 \text{ pF} \pm 10\%$, including scope probe, wiring and stray capacitance.
4. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.
6. All diodes are 1N3064 or equivalent.
7. Each gate tested separately.

Military 54LS32



AVAILABLE AS:

- 1) JAN: JM38510/30501BXA
- 2) SMD: N/A
- 3) 883: 54LS32/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCTION	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	VCC
Y1	3	3	4	VCC
A2	4	4	6	VCC
B2	5	5	8	VCC
Y2	6	6	9	VCC
GND	7	7	10	GND
Y3	8	8	12	VCC
A3	9	9	13	VCC
B3	10	10	14	VCC
Y4	11	11	16	VCC
A4	12	12	18	VCC
B4	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
 $V_{CC} = 5.0 \text{ V MIN}/6.0 \text{ V MAX}$

TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

54LS32

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 400 μA, V _{IH} = 2.0 V, other input = 0.7 V.
V _{OL}	Logical “0” Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V on both inputs.
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, other inputs are open.
I _{IH1}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V, other input = 0 V.
I _{IH2}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other input = 0 V.
I _{IL}	Logical “0” Input Current	– 150	– 380	– 150	– 380	– 150	– 380	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other input = 5.5 V.
I _{OS}	Output Short Circuit Supply	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (both inputs), V _{OUT} = 0 V.
I _{CCH}	Power Supply Current		6.2		6.2		6.2	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (both inputs).
I _{CCL}	Power Supply Current		9.8		9.8		9.8	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (both inputs).
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	÷ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL} t _{PHL}	Propagation Delay /Data-Output Output <u>High-Low</u>	2.0 —	20 22	2.0 —	35 30	2.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH} t _{PLH}	Propagation Delay /Data-Output Output <u>Low-High</u>	2.0 —	20 22	2.0 —	35 30	2.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTE:

1. The limits specified for C_L = 15 pF are guaranteed but not tested.