

Rail-to-Rail Input Rail-to-Rail Output Zero-Drift Op Amp

FEATURES

- Input Common-Mode Range Includes Both Rails
- Output Swings Rail to Rail
- Output Will Drive 1k Ω Load
- No External Components Required
- Input Offset Voltage: 10 μ V Max
- Input Offset Drift: 100nV/ $^{\circ}$ C Max
- Minimum CMRR: 115dB
- Supply Current: 3.0mA Max
- Shutdown Pin Drops Supply Current to 5 μ A Max
- Output Configurable to Drive Any Capacitive Load
- Operates from 2.7V to 14V Total Supply Voltage

APPLICATIONS

- Rail-to-Rail Amplifiers and Buffers
- High Resolution Data Acquisition Systems
- Supply Current Sensing in Either Rail
- Low Supply Voltage Transducer Amplifiers
- High Accuracy Instrumentation
- Single Negative Supply Operation

DESCRIPTION

The LTC[®]1152 is a high performance, low power zero-drift op amp featuring an input stage that common modes to both power supply rails and an output stage that provides rail-to-rail swing, even into heavy loads. The wide input common-mode range is achieved with a high frequency on-board charge pump. This technique eliminates the crossover distortion and limited CMRR imposed by competing technologies. The LTC1152 is a C-Load[™] of amp, enabling it to drive any capacitive load.

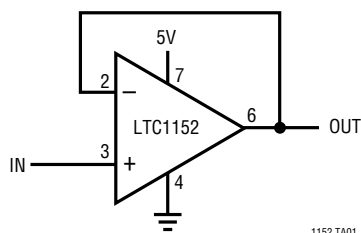
The LTC1152 shares the excellent DC performance specs of LTC's other zero-drift amplifiers. Typical offset voltage is 1 μ V and typical offset drift is 10nV/ $^{\circ}$ C. CMRR and PSRR are 130dB and 120dB and open-loop gain is 130dB. Input noise voltage is 2 μ V_{P-P} from 0.1Hz to 10Hz. Gain-bandwidth product is 0.7MHz and slew rate is 0.5V/ μ s, all with supply current of 3.0mA max over temperature. The LTC1152 also includes a shutdown feature which drops supply current to 1 μ A and puts the output stage in a high impedance state.

The LTC1152 is available in 8-pin PDIP and 8-pin SO packages and uses the standard op amp pinout, allowing it to be a plug-in replacement for many standard op amps.

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C-Load is trademark of Linear Technology Corporation.

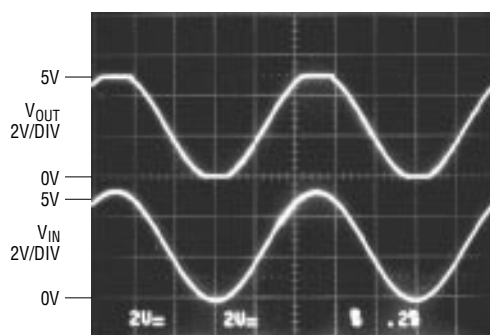
TYPICAL APPLICATION

Rail-to-Rail Buffer



1152 TA01

Input and Output Waveforms

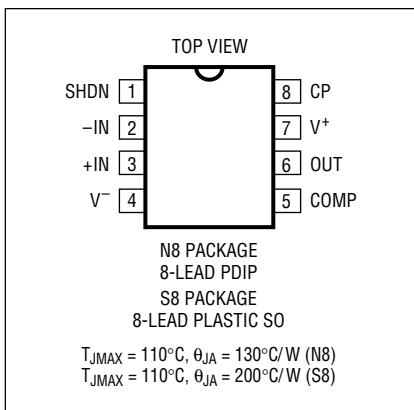


1152 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	14V
Input Voltage	$V^+ + 0.3V$ to $V^- - 0.3V$
Output Short-Circuit Duration (Pin 6)	Indefinite
Operating Temperature Range	
LTC1152C	0°C to 70°C
LTC1152I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LTC1152CN8 LTC1152CS8 LTC1152IN8 LTC1152IS8
	S8 PART MARKING
	1152 1152I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS $V_S = 5V$, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 1)		± 1	± 10	μV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●	± 10	± 100	$\text{nV}/^\circ\text{C}$
	Long-Term Offset Drift			± 50		$\text{nV}/\sqrt{\text{Mo}}$
I_B	Input Bias Current	$T_A = 25^\circ\text{C}$ (Note 2)	●	± 10	± 100 ± 1000	pA pA
I_{OS}	Input Offset Current	$T_A = 25^\circ\text{C}$ (Note 2)	●	± 20	± 200 ± 500	pA pA
e_n	Input Noise Voltage (Note 3)	$R_S = 100\Omega$, 0.1Hz to 10Hz $R_S = 100\Omega$, 0.1Hz to 1Hz		2 0.5	3 1	$\mu\text{V}_{\text{P-P}}$ $\mu\text{V}_{\text{P-P}}$
i_n	Input Noise Current	$f = 10\text{Hz}$		0.6		$\text{fA}/\sqrt{\text{Hz}}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 5V	●	115	130	dB
PSRR	Power Supply Rejection Ratio	$V_S = 3V$ to 12V	●	110 105	120	dB dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = 0.5V$ to 4.5V	●	110	130	dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 1k$, $V_S = \text{Single } 5V$ $R_L = 1k$, $V_S = \pm 2.5V$ $R_L = 100k$, $V_S = \pm 2.5V$	● ●	4.0 ± 2.0	4.4 2.2 ± 2.49	V V V
SR	Slew Rate	$R_L = 10k$, $C_L = 50\text{pF}$, $V_S = \pm 2.5V$		0.5		$\text{V}/\mu\text{s}$
GBW	Gain-Bandwidth Product	$R_L = 10k$, $C_L = 50\text{pF}$, $V_S = \pm 2.5V$		0.7		MHz
I_S	Supply Current	No Load Shutdown = 0V	● ●	2.2 1	3.0 5	mA μA
I_{OSD}	Output Leakage Current	Shutdown = 0V	●	± 10	± 100	nA
V_{CP}	Charge Pump Output Voltage	$I_{CP} = 0$		7.3		V
V_{IL}	Shutdown Pin Input Low Voltage			2.5		V
V_{IH}	Shutdown Pin Input High Voltage			4		V
I_{IN}	Shutdown Pin Input Current	$V_{SHDN} = 0V$	●	-1	-5	μA
f_{CP}	Internal Charge Pump Frequency	$T_A = 25^\circ\text{C}$		4.7		MHz
f_{SMPL}	Internal Sampling Frequency	$T_A = 25^\circ\text{C}$		2.3		kHz

ELECTRICAL CHARACTERISTICS $V_S = 3V$, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 1)		± 1	± 10	μV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●	± 10	± 100	$\text{nV}/^\circ\text{C}$
I_B	Input Bias Current	$T_A = 25^\circ\text{C}$ (Note 2)	●	± 5	± 100 ± 1000	pA pA
I_{OS}	Input Offset Current	$T_A = 25^\circ\text{C}$ (Note 2)	●	± 10	± 200 ± 500	pA pA
e_n	Input Noise Voltage (Note 3)	$R_S = 100\Omega$, 0.1Hz to 10Hz $R_S = 100\Omega$, 0.1Hz to 1Hz		2 0.75		μV_{P-P} μV_{P-P}
i_n	Input Noise Current	$f = 10\text{Hz}$		0.6		$\text{fA}/\sqrt{\text{Hz}}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0\text{V}$ to 3V	●	130		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}$, $V_{OUT} = 0.5\text{V}$ to 2.5V	●	106	130	dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 1\text{k}$, $V_S = \text{Single } 3\text{V}$ $R_L = 100\text{k}$, $V_S = \pm 1.5\text{V}$	●	2.0	2.5 ± 1.48	V V
SR	Slew Rate	$R_L = 10\text{k}$, $C_L = 50\text{pF}$, $V_S = \pm 1.5\text{V}$		0.4		$\text{V}/\mu\text{s}$
GBW	Gain-Bandwidth Product	$R_L = 10\text{k}$, $C_L = 50\text{pF}$, $V_S = \pm 1.5\text{V}$		0.5		MHz
I_S	Supply Current	No Load Shutdown = 0V	● ●	1.8 1	2.5 5	mA μA
I_{OSD}	Output Leakage Current	Shutdown = 0V	●	± 10		nA
V_{CP}	Charge Pump Output Voltage	$I_{CP} = 0$		4.5		V
V_{IL}	Shutdown Pin Input Low Voltage			1.2		V
V_{IH}	Shutdown Pin Input High Voltage			2.3		V
I_{IN}	Shutdown Pin Input Current	$V_{SHDN} = 0\text{V}$		-1		μA
f_{CP}	Internal Charge Pump Frequency	$T_A = 25^\circ\text{C}$		4.2		MHz
f_{SMPL}	Internal Sampling Frequency	$T_A = 25^\circ\text{C}$		2.1		kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

Note 2: At $T \leq 0^\circ\text{C}$ these parameters are guaranteed by design and not tested.

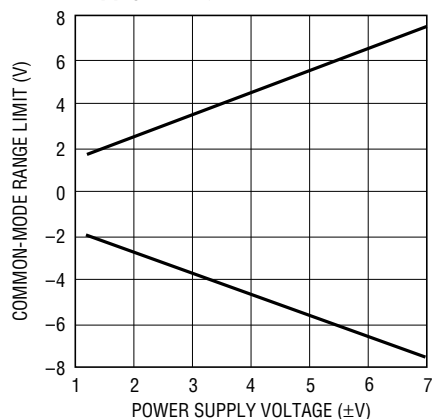
Note 3: 0.1Hz to 10Hz noise is specified DC coupled in a 10-sec window; 0.1Hz to 1Hz noise is specified in a 100-sec window with an RC highpass

filter at 0.1Hz. Contact LTC factory for sample tested or 100% tested noise parts.

Note 4: All output swing measurements are taken with the load resistor connected from output to ground. For single supply tests, only the positive swing is specified (negative swing will be 0V due to the pull-down effect of the load resistor). For dual supply operation, both positive and negative swing are specified.

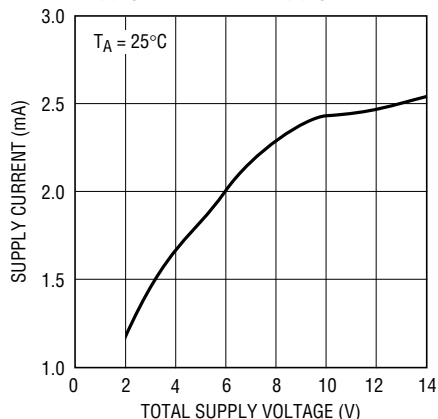
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Range vs Supply Voltage



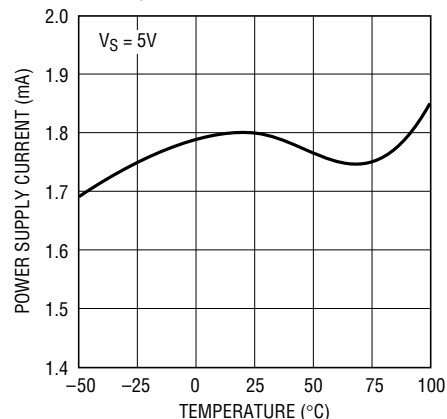
1152 G01

Supply Current vs Supply Voltage



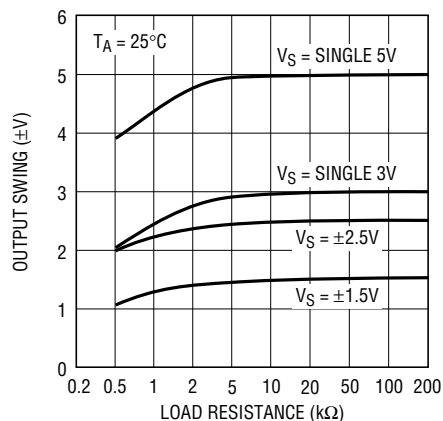
1152 G02

Supply Current vs Temperature



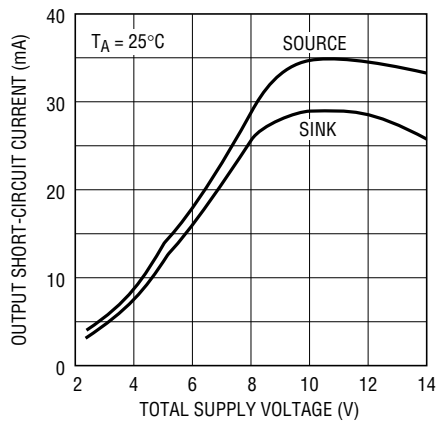
1152 G03

Output Swing vs Load Resistance



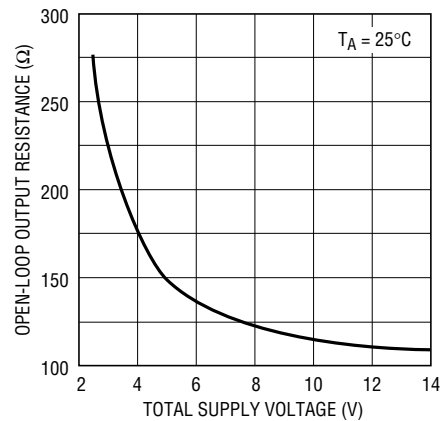
1152 G04

Output Short-Circuit Current vs Supply Voltage



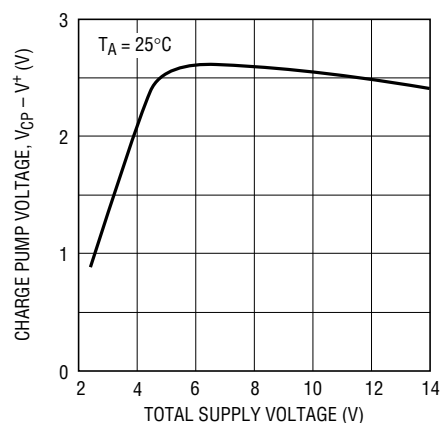
1152 G05

Open-Loop Output Resistance vs Supply Voltage



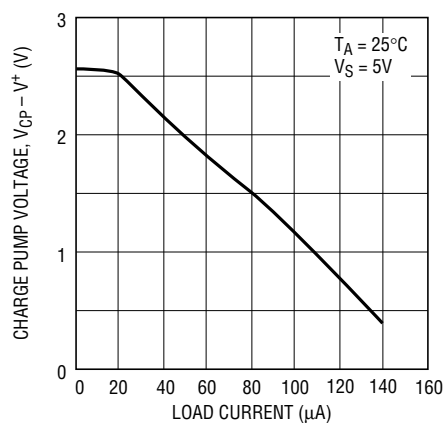
1152 G06

Charge Pump Voltage vs Supply Voltage



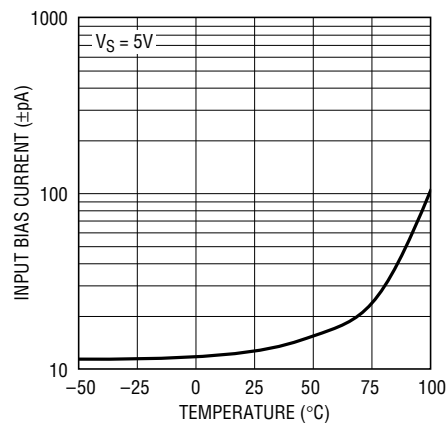
1152 G07

Charge Pump Voltage vs Load Current



1152 G08

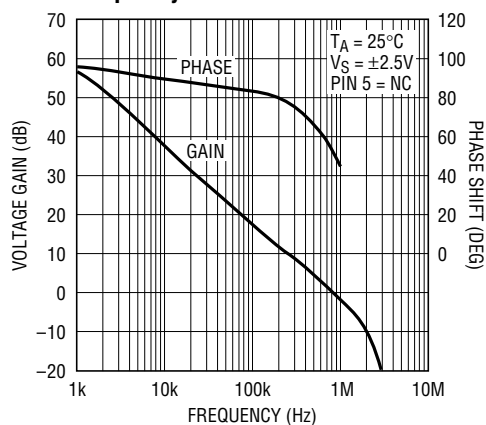
Input Bias Current vs Temperature



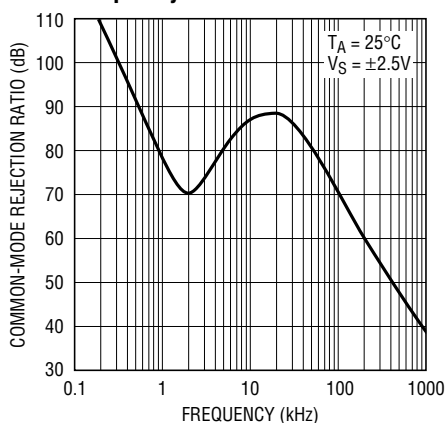
1152 G09

TYPICAL PERFORMANCE CHARACTERISTICS

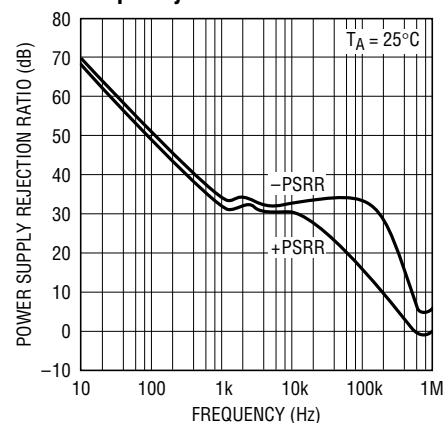
Gain and Phase Shift vs Frequency



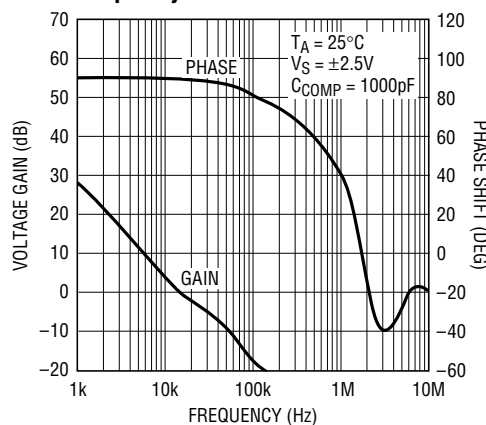
Common-Mode Rejection Ratio vs Frequency



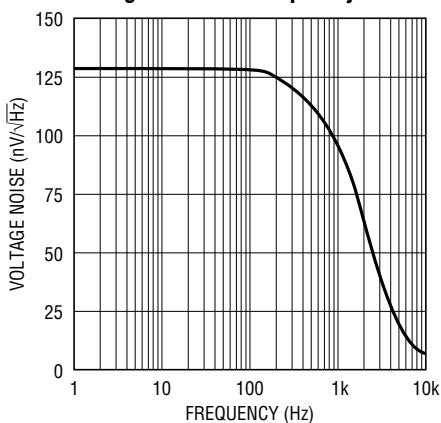
Power Supply Rejection Ratio vs Frequency



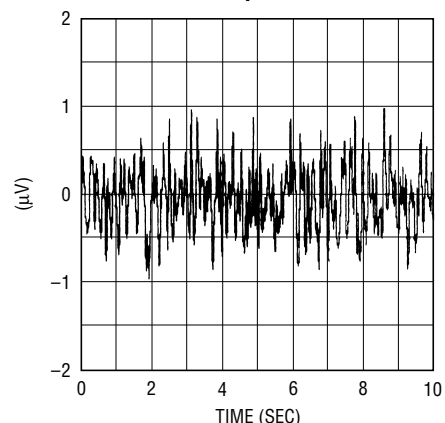
Gain and Phase Shift vs Frequency



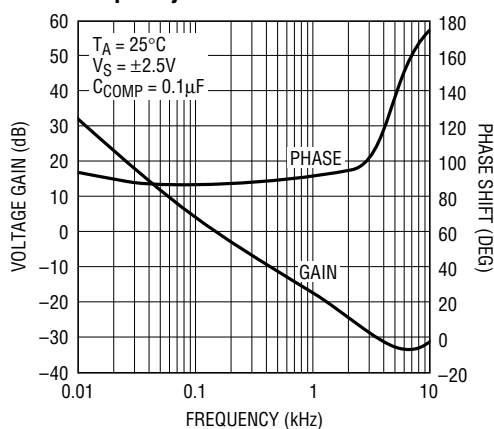
Voltage Noise vs Frequency



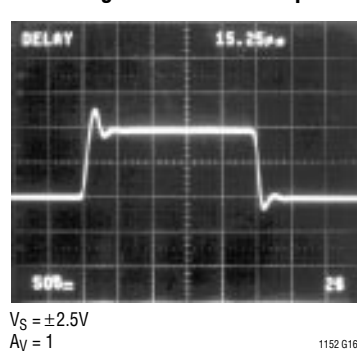
0.1Hz to 10Hz Input Noise



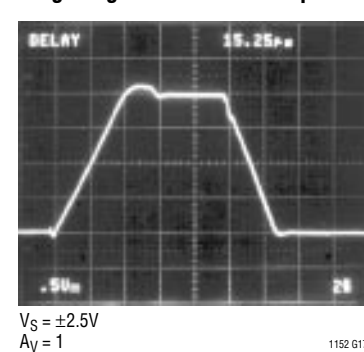
Gain and Phase Shift vs Frequency



Small-Signal Transient Response



Large-Signal Transient Response



APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LTC1152 is a rail-to-rail input common-mode range, rail-to-rail output swing op amp. Most CMOS op amps, including the entire LTC zero-drift amplifier line, and even a few bipolar op amps, can and do, claim rail-to-rail output swing. One obvious use for such a device is to provide a unity-gain buffer for 0V to 5V signals running from a single 5V power supply. This is not possible with the vast majority of so-called “rail-to-rail” op amps; although the output can swing to both rails, the negative input (which is connected to the output) will exceed the common-mode input range of the device at some point (generally about 1.5V below the positive supply), opening the feedback loop and causing unpredictable and sometimes bizarre behavior.

The LTC1152 is an exception to this rule. It features both rail-to-rail output swing and rail-to-rail input common-mode range (CMR); the input CMR actually extends beyond either rail by about 0.3V. This allows unity-gain buffer circuits to operate with any input signal within the power supply rails; input signal swing is limited only by the output stage swing into the load. Additionally, signals occurring at either rail (power supply current sensing, for example) can be amplified without any special circuitry.

Internal Charge Pump

The LTC1152 achieves its rail-to-rail input CMR by using a charge pump to generate an internal voltage approximately 2V higher than V^+ . The input stages of the op amp are run from this higher voltage, making signals at V^+ appear to be 2V below the front end’s power supply (Figure 1). The charge pump is contained entirely within the LTC1152; no external components are required.

About $100\mu V_{P-P}$ of residual charge pump switching noise will be present on the output of the LTC1152. This feedthrough is at 4.7MHz, higher than the gain-bandwidth of the LTC1152, and will generally not cause any problems. Very sensitive applications can reduce this feedthrough by connecting a capacitor from the CP pin (pin 8) to V^+ (pin 7); a $0.1\mu F$ capacitor will reduce charge pump feedthrough to negligible levels. The LTC1152 includes an internal diode from pin 8 to pin 7 to prevent external parasitic capacitance from lengthening start-up

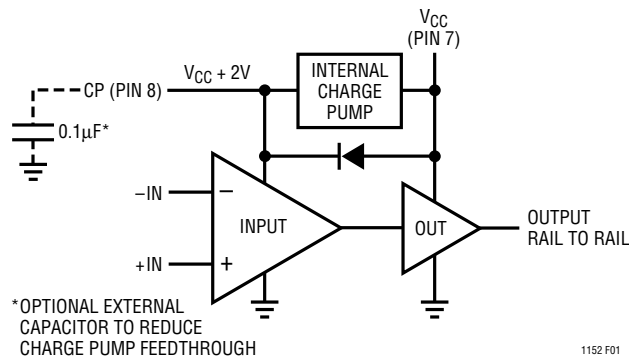


Figure 1. LTC1152 Internal Block Diagram

time. This diode can stand short-term peak currents of about 50mA, allowing it to quickly charge external capacitance to ground or V^- . Large capacitors ($>1\mu F$) should not be connected between pin 8 and ground or V^- to prevent excessive diode current from flowing at start-up. The LTC1152 can withstand continuous short circuits between pin 8 and V^+ ; however, short circuiting pin 8 to ground or V^- will cause large amounts of current to flow through the diode, destroying the LTC1152. Don’t do it.

Output Drive

The LTC1152 features an enhanced output stage that can sink and source 10mA with a single 5V supply while maintaining rail-to-rail output swing under most loading conditions. The output stage can be modeled as a perfect rail-to-rail voltage source with a resistor in series with it; this open-loop output resistance limits the output swing by creating a resistor divider with the output load.

The output resistance drops as total power supply voltage increases, as shown in the typical performance curves. It is typically 140Ω with a single 5V supply, allowing a 4.4V output swing into a 1k resistor with a single 5V supply.

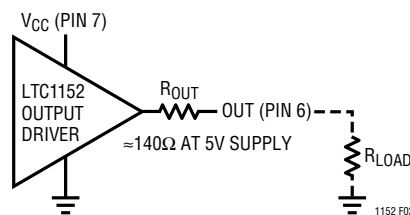


Figure 2. LTC1152 Output Resistance Model

APPLICATIONS INFORMATION

Compensation/Bandwidth Limiting

The LTC1152 is unity-gain stable with capacitive loads up to 1000pF. Larger capacitive loads can be driven by externally compensating the LTC1152. Adding 1000pF between COMP (pin 5) and OUT (pin 6) allows capacitive loading of up to 1 μ F; 0.1 μ F between pins 5 and 6 allows the LTC1152 to drive infinite capacitive load (Figure 3).

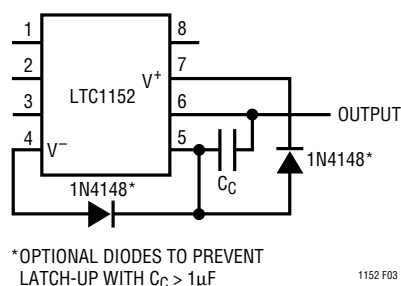


Figure 3. Output Compensation Connection

Large compensation capacitors can also be used to limit the bandwidth of the LTC1152. With 0.1 μ F from pin 5 to pin 6, the LTC1152's gain-bandwidth product is reduced from 700kHz to around 200Hz. Note that compensation capacitors greater than 1 μ F can cause latch-up under severe output fault conditions; this can be prevented by clamping pin 5 to each supply with standard signal diodes, as shown in Figure 3.

Shutdown

The LTC1152 includes a shutdown pin (pin 1). When this pin is at V^+ , the LTC1152 operates normally. An internal 1 μ A pull-up keeps the pin high if it is left floating. When pin 1 is pulled low, the part enters shutdown mode; supply current drops to 1 μ A, all internal clocking stops and the output enters a high impedance state. During shutdown the voltage at the CP pin (pin 8) will drop to 0.5V below V^+ . When pin 1 is brought high again, about 10 μ s will elapse before the charge pump regains full voltage. During this time the LTC1152 will operate normally, but the input CMR may not include V^+ . Pin 1 is compatible with CMOS logic running from the same supply as the LTC1152. Additionally, the input trip levels allow ground referenced CMOS logic signals to interface directly to pin 1 when the LTC1152

is running from $\pm 5\text{V}$ or $\pm 3\text{V}$ supplies. The internal 1 μ A pull-up also allows pin 1 to interface with open-collector/open-drain devices or discrete transistors.

The high impedance output in shutdown allows several LTC1152s to be connected together as a MUX, with their outputs tied in parallel and the active channel selected by using the shutdown pins. Deselected (shutdown) channels will go to high impedance at the outputs, preventing them from fighting with the active channel. This works best when the individual LTC1152s are connected in noninverting feedback configurations to prevent the feedback resistors from passing signals through deselected channels. See the Typical Applications section for a circuit example.

Zero-Drift Operation

The LTC1152 is a zero-drift op amp. Like other LTC zero-drift op amps, it features virtually error-free DC performance, very little drift over time and temperature, and very low noise at low frequencies. The internal nulling clock runs at about 2.3kHz (the charge pump frequency of 4.7MHz divided by 2048) and is synchronized to the internal charge pump to prevent beat frequencies from appearing at the output. The self-nulling circuit constantly corrects the input offset voltage, keeping it typically below $\pm 1\mu\text{V}$ over the entire input common-mode range. This has the added benefit of providing exceptional CMRR and PSRR at low frequencies—far better than competing rail-to-rail op amps.

Because it uses a sampling front end, the LTC1152 will exhibit aliasing behavior and clock noise at frequencies near the internal 2.3kHz sampling frequency. The LTC1152 includes an internal anti-aliasing circuit to keep these error terms to a minimum. As a rule, alias frequencies will be down by $(80\text{dB} - A_{CLG})$ in most standard amplifier configurations, where A_{CLG} is the closed-loop gain of the LTC1152 circuit. Clock noise is also dependent on closed-loop gain; it will generally consist of spikes of about 100 μV in amplitude, input referred. In general, these error terms are too small to affect most applications. For a more detailed explanation of zero-drift amplifier behavior, see the LTC1051/LTC1053 data sheet.

The circuit diagram shows a precision current source. The input voltage is 5V, and the output is labeled "OUT 1V/100mA LOAD CURRENT IN MEASURED CIRCUIT". The circuit includes an LTC1152 precision centaur current source and an LT1097 precision current source. The LTC1152 is configured with a 0.01Ω sense resistor and a 0.1μF capacitor. The LT1097 is configured with a 10kΩ resistor and a 0.1μF capacitor. The output current is 1V/100mA.

[illegible]

Dimensions in inches (millimeters) unless otherwise noted.

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

Top View Dimensions:

- Overall Width: 0.400^* (10.160) MAX
- Overall Height: $0.255 \pm 0.015^*$ (6.477 $\pm$ 0.381)
- Pin Numbers: 1, 2, 3, 4 (bottom); 5, 6, 7, 8 (top)

Side View Dimensions:

- Top Flange Width: $0.300 - 0.325$ (7.620 - 8.255)
- Top Flange Thickness: $0.009 - 0.015$ (0.229 - 0.381)
- Pin Diameter: 0.065 (1.651) TYP
- Pin Spacing (Center-to-Center): 0.045 ± 0.015 (1.143 $\pm$ 0.381)
- Pin Length: 0.100 ± 0.010 (2.540 $\pm$ 0.254)
- Pin Tip Radius: 0.018 ± 0.003 (0.457 $\pm$ 0.076)
- Pin Tip Width: 0.125 (3.175) MIN
- Pin Tip Height: 0.01 (0.38) MIN

Detail View Dimensions:

- Pin Spacing (Center-to-Center): $0.045 - 0.065$ (1.143 - 1.651)
- Pin Diameter: 0.130 ± 0.005 (3.302 $\pm$ 0.127)

The drawing shows the mechanical specifications for the BSC package. The top view indicates a square footprint with a width of 0.189 - 0.197" (4.801 - 5.004) and a height of 0.228 - 0.244" (5.791 - 6.197). It features four pins on each side, numbered 1 through 8. The side view shows a package height of 0.150 - 0.157" (3.810 - 3.988) and a thickness of 0.053 - 0.069" (1.346 - 1.752). The bottom view shows a pin pitch of 0.014 - 0.019" (0.355 - 0.483) and a pin width of 0.050" (1.270). A lead angle of -8° TYP is specified. The package is identified as BSC.