



MOTOROLA

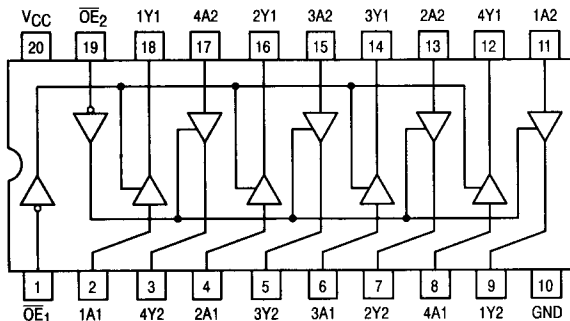
Octal Buffer With Active Low Enable 3-State Non-Inverted Outputs

**ELECTRICALLY TESTED PER:
MIL-M-38510/33203**

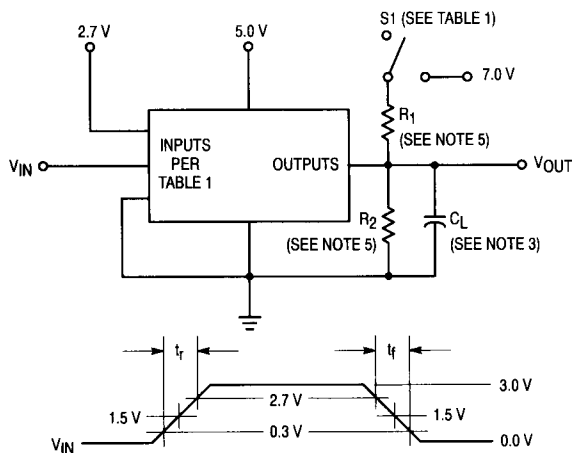
The F244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Register
- Outputs Sink 64 mA
- 15 mA Source Current
- Input Clamp Diodes Limit High Speed Termination Effects

LOGIC DIAGRAM



AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-118

Military 54F244



AVAILABLE AS:

- 1) JAN: JM38510/33203BXA
- 2) SMD: N/A
- 3) 883: 54F244/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2 /**

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
OE ₁	1	1	1	VCC
1A ₁	2	2	2	VCC
4Y ₂	3	3	3	OPEN
2A ₁	4	4	4	VCC
3Y ₂	5	5	5	OPEN
3A ₁	6	6	6	VCC
2Y ₂	7	7	7	OPEN
4A ₁	8	8	8	VCC
1Y ₂	9	9	9	OPEN
GND	10	10	10	GND
1A ₂	11	11	11	VCC
4Y ₁	12	12	12	OPEN
2A ₂	13	13	13	VCC
3Y ₁	14	14	14	OPEN
3A ₂	15	15	15	VCC
2Y ₁	16	16	16	OPEN
4A ₂	17	17	17	VCC
1Y ₁	18	18	18	OPEN
OE ₂	19	19	19	VCC
VCC	20	20	20	VCC

**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

TRUTH TABLE

Inputs		Output
OE ₁ , OE ₂	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = HIGH Impedance

WAVEFORMS

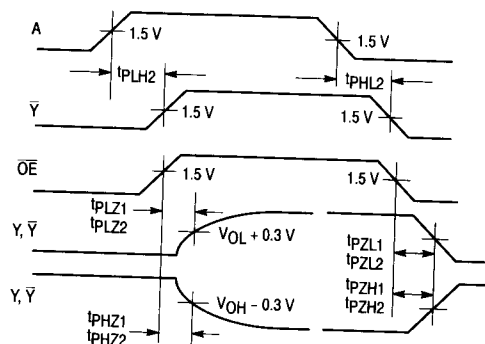


Table 1

Test Type	S1
tPLH	open
tPHL	open
tPHZ	open
tPZH	open
tPLZ	closed
tPZL	closed

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = –3.0 mA, V _{IN} = 2.0 V, other input = 0.8 V.
V _{OL}	Logical “0” Output Voltage		0.55		0.55		0.55	V	V _{CC} = 4.5 V, I _{OL} = 48 mA, V _{IN} = 0.8 V (both inputs).
V _{IC}	Input Clamping Voltage		–1.2					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open.
I _{OD}	Diode Current	65		65		65		mA	V _{CC} = 4.5 V, V _{IN} = GND, other input = GND, V _{OUT} = 2.5 V.
I _{IL1}	Logical “0” Input Current (OE)	–0.3	–1.6	–0.3	–1.6	–0.3	–1.6	mA	V _{CC} = 5.5 V, V _{IL} = 0.5 V, other inputs are open.
I _{IL2}	Logical “0” Input Current (A)	–0.3	–1.0	–0.3	–1.0	–0.3	–1.0	mA	V _{CC} = 5.5 V, V _{IL} = 0.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	–100	–325	–100	–325	–100	–325	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other input = 0 V, V _{OUT} = 0 V.
I _{IOZH}	Output Off Current High		50		50		50	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other input = 0 V, V _{OUT} = 2.4 V.
I _{IOZL}	Output Off Current Low		–50		–50		–50	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other input = 4.5 V, V _{OUT} = 0.5 V.
I _{CCH}	Power Supply Current		60		60		60	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other input = 0 V.
I _{CCL}	Power Supply Current		90		90		90	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
I _{CCZ}	Power Supply Current Off		90		90		90	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other inputs are open.
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.

54F244

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
	Functional Tests	+ 25°C	+ 125°C	– 55°C		per Truth Table with $V_{CC} = 4.5\text{ V}$, (Repeat at), $V_{CC} = 5.5\text{ V}$, $V_{INL} = 0.5\text{ V}$, $V_{INH} = 2.5\text{ V}$.
		Subgroup 7	Subgroup 8A	Subgroup 8B		

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL2}	Propagation Delay /Data-Output Output <u>High-Low</u>	1.0	6.0	1.0	7.0	1.0	7.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 500 Ω.
t _{PLH2}	Propagation Delay /Data-Output Output <u>Low-High</u>	1.0	5.2	1.0	6.5	1.0	6.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 500 Ω.
t _{PLZ2}	Propagation Delay /Data-Output Output <u>Low-High</u>	2.0	6.0	2.0	7.5	2.0	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 500 Ω.
t _{PHZ2}	Propagation Delay /Data-Output Output <u>High-Low</u>	2.0	6.0	2.0	7.0	2.0	7.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 500 Ω.
t _{PZL2}	Propagation Delay /Data-Output Output <u>Low-High</u>	2.0	7.0	2.0	8.5	2.0	8.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 500 Ω.
t _{PZH2}	Propagation Delay /Data-Output Output <u>High-Low</u>	2.0	5.7	2.0	7.0	2.0	7.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 500 Ω.

NOTES:

1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5\text{ ns}$, $\text{PRR} \leq 1.0\text{ MHz}$ and $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pin not designated may be high $\geq 2.0\text{ V}$, low $\leq 0.8\text{ V}$, or open).
3. $C_L = 50\text{ pF} \pm 10\%$ including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2 = 500\ \Omega \pm 5.0\%$.