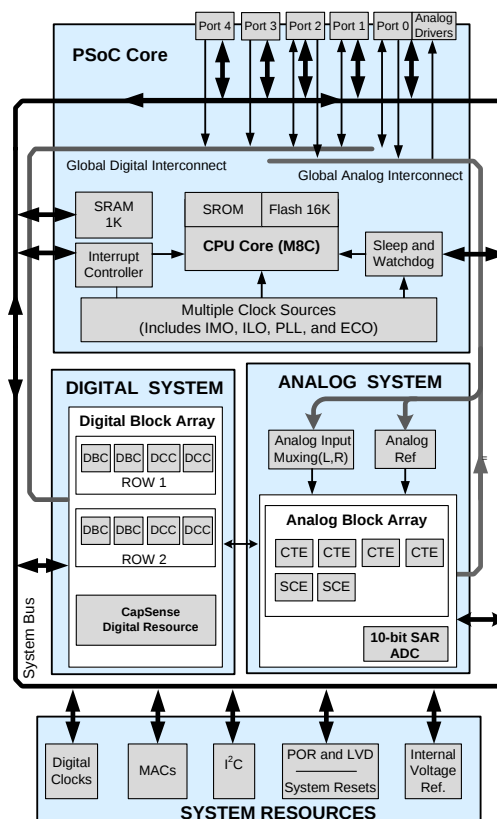


## Features

- Powerful Harvard-architecture processor:
  - M8C processor speeds up to 24 MHz
  - 8 × 8 multiply, 32-bit accumulate
  - Low power at high speed
  - 3.0 V to 5.25 V operating voltage
  - Industrial temperature range: –40 °C to +85 °C
- Advanced peripherals (PSoC® Blocks)
  - Six analog type “E” PSoC blocks provide:
    - Single or dual 8-Bit ADC
    - Comparators (up to four)
  - Up to eight digital PSoC blocks provide:
    - 8- to 32-bit timers and counters, 8- and 16-bit pulse-width modulators (PWMs)
    - One shot, multi-shot mode support in timers and PWMs
    - PWM with deadband support in one digital block
    - Shift register, CRC, and PRS modules
    - Full duplex UART
    - Multiple SPI masters or slaves, variable data length Support: 8- to 16-Bit
    - Can be connected to all GPIO pins
  - Complex peripherals by combining blocks
  - Shift function support for FSK detection
  - Powerful synchronize feature support. Analog module operations can be synchronized by digital blocks or external signals.
- High speed 10-bit SAR ADC with sample and hold optimized for embedded control
- Precision, programmable clocking:
  - Internal ± 5% <sup>[1]</sup> 24/48 MHz oscillator across the industrial temperature range
  - High accuracy 24 MHz with optional 32 kHz crystal and PLL
  - Optional external oscillator, up to 24 MHz
  - Internal/external oscillator for watchdog and sleep
- Flexible on-chip memory:
  - Up to 16 KB flash program storage 50,000 erase/write cycles
  - Up to 1-KB SRAM data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Optimized CapSense® resource:
  - Two IDAC support up to 640 µA source current to replace external resistor
  - Two dedicated clock resources for CapSense:
- CSD\_CLK: 1/2/4/8/16/32/128/256 derive from SYSCLK
- CNT\_CLK: 1/2/4/8 Derive from CSD\_CLK
- Dedicated 16-bit timers/counters for CapSense scanning
- Support dual CSD channels simultaneous scanning
- Programmable pin configurations:
  - 25 mA sink, 10 mA source on all GPIOs
  - Pull-up, pull-down, high Z, Strong, or open-drain drive modes on all GPIOs
  - Up to 38 analog inputs on GPIOs
  - Configurable interrupt on all GPIOs
- Additional system resources:
  - I<sup>2</sup>C™ slave, master, and multimaster to 400 kHz
  - Supports hardware addressing feature
  - Watchdog and sleep timers
  - User configurable low voltage detection
  - Integrated supervisory circuit
  - On-Chip precision voltage reference
  - Supports RTC block into digital peripheral logic

## Top Level Block Diagram



**Errata:** For information on silicon errata, see “Errata” on page 35. Details include trigger conditions, devices affected, and proposed workaround.

### Note

1. **Errata:** When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see “Errata” on page 35.

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## PSoC Functional Overview

The PSoC family consists of many On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, shown in [Figure 1](#), consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows the combining of all the device resources into a complete custom system. The PSoC family can have up to five I/O ports connecting to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general-purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 21 vectors, to simplify the programming of real time embedded events.

Program execution is timed and protected using the included Sleep and watchdog timers (WDT).

Memory encompasses 16 KB of Flash for program storage, 1 K bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

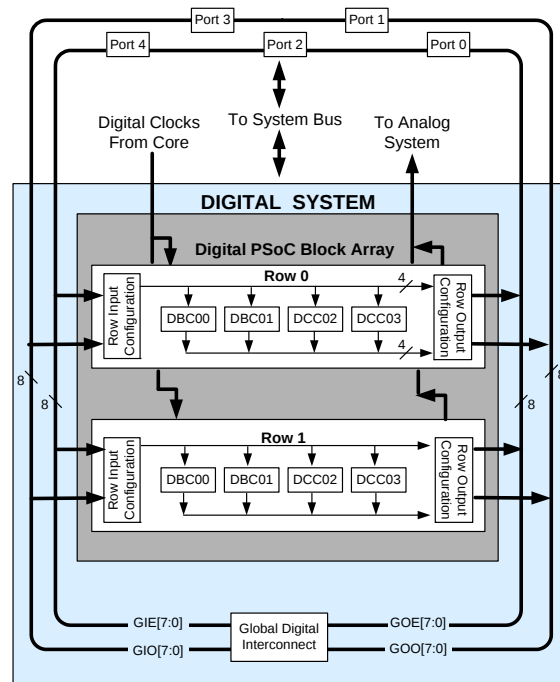
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator). The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the Sleep timer and WDT. If crystal accuracy is required, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC), and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin can also generate a system interrupt on high level, low level, and change from last read.

### Digital System

The Digital System is composed of eight digital PSoC blocks. Each block is an 8-bit resource that may be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

**Figure 1. Digital System Block Diagram**



Digital peripheral configurations are:

- PWMs (8- and 16-Bit)
- PWMs with Dead band (8- and 16-Bit)
- Counters (8 to 32-Bit)
- Timers (8 to 32-Bit)
- UART 8 Bit with Selectable Parity (Up to Two)
- SPI Master and Slave (Up to Two)
- Shift Register (1 to 32-Bit)
- I2C Slave and Master (One Available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32-Bit)
- IrDA (Up to Two)
- Pseudo Random Sequence Generators (8 to 32-Bit)

The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides a choice of system resources for your application. Family resources are shown in [Table 1 on page 5](#).

## Analog System

The Analog System consists of a 10-bit SAR ADC and six configurable blocks.

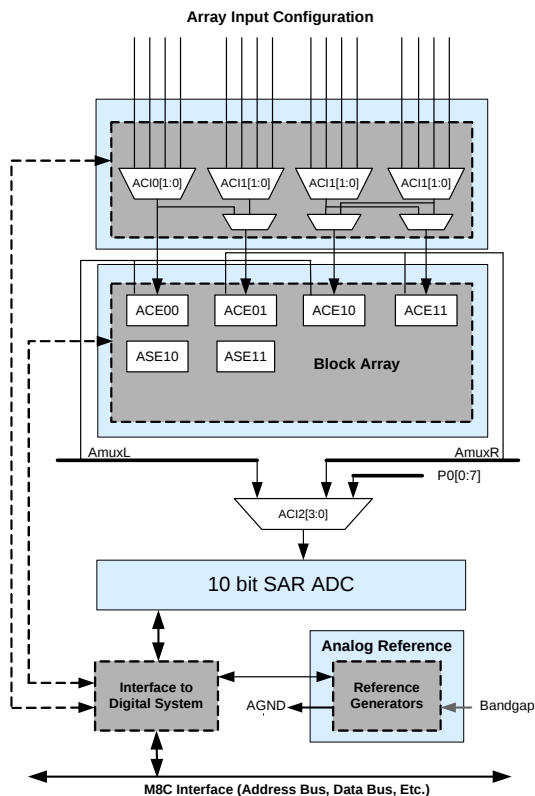
The programmable 10-bit SAR ADC is an optimized ADC that can be run up to 200 ksp/s with  $\pm 1.5$  LSB DNL and  $\pm 2.5$  LSB INL (true for  $V_{DD} \geq 3.0$  V and  $V_{ref} \geq 3.0$  V). External filters are required on ADC input channels for antialiasing. This ensures that any out-of-band content is not folded into the input signal band.

Reconfigurable analog resources allow creating complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-Digital converters (Single or Dual, with 8-bit resolution)
- Pin-to-pin Comparator
- Single ended comparators with absolute (1.3 V) reference or 5-bit DAC reference
- 1.3 V reference (as a System Resource)

Analog blocks are provided in columns of four, which include CT-E (Continuous Time) and SC-E (Switched Capacitor) blocks. These devices provide limited functionality Type “E” analog blocks.

**Figure 2. Analog System Block Diagram**



## Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a MAC, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Additional Digital resources and clocks optimized for CSD.
- Support “RTC” block into digital peripheral logic.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number          | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks               | SRAM Size | Flash Size |
|---------------------------|-------------|--------------|----------------|---------------|----------------|----------------|-----------------------------|-----------|------------|
| CY8C29x66 <sup>[2]</sup>  | up to 64    | 4            | 16             | up to 12      | 4              | 4              | 12                          | 2 K       | 32 K       |
| CY8C28xxx                 | up to 44    | up to 3      | up to 12       | up to 44      | up to 4        | up to 6        | up to 12 + 4 <sup>[3]</sup> | 1 K       | 16 K       |
| CY8C27x43                 | up to 44    | 2            | 8              | up to 12      | 4              | 4              | 12                          | 256       | 16 K       |
| CY8C24x94 <sup>[2]</sup>  | up to 56    | 1            | 4              | up to 48      | 2              | 2              | 6                           | 1 K       | 16 K       |
| CY8C24x23A <sup>[2]</sup> | up to 24    | 1            | 4              | up to 12      | 2              | 2              | 6                           | 256       | 4 K        |
| CY8C23x33                 | up to 26    | 1            | 4              | up to 12      | 2              | 2              | 4                           | 256       | 8 K        |
| CY8C22x45 <sup>[2]</sup>  | up to 38    | 2            | 8              | up to 38      | 0              | 4              | 6 <sup>[3]</sup>            | 1 K       | 16 K       |
| CY8C21x45 <sup>[2]</sup>  | up to 24    | 1            | 4              | up to 24      | 0              | 4              | 6 <sup>[3]</sup>            | 512       | 8 K        |
| CY8C21x34 <sup>[2]</sup>  | up to 28    | 1            | 4              | up to 28      | 0              | 2              | 4 <sup>[3]</sup>            | 512       | 8 K        |
| CY8C21x23                 | up to 16    | 1            | 4              | up to 8       | 0              | 2              | 4 <sup>[3]</sup>            | 256       | 4 K        |
| CY8C20x34 <sup>[2]</sup>  | up to 28    | 0            | 0              | up to 28      | 0              | 0              | 3 <sup>[3,4]</sup>          | 512       | 8 K        |
| CY8C20xx6                 | up to 36    | 0            | 0              | up to 36      | 0              | 0              | 3 <sup>[3,4]</sup>          | up to 2 K | up to 32 K |

## Getting Started

For in-depth information, along with detailed programming details, see the [CY8C22x45](#), [CY8C21345: PSoC® Programmable System-on-Chip™ Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

## Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs. Use [PSoC 1 Application note finder](#) to search application notes or example projects for a specific application and/or family.

## Development Kits

[PSoC 1 kits](#) are available online from Cypress and also available through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. The [kit selector guide](#) available in cypress website offers the list of all available development kits, programming and debugging kits for each PSoC 1 family.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com), covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

## Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

### Notes

2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense® block.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

### PSoC Designer Software Subsystems

#### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run

time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

#### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

#### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

#### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

#### *In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#).
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance

specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

## Pinouts

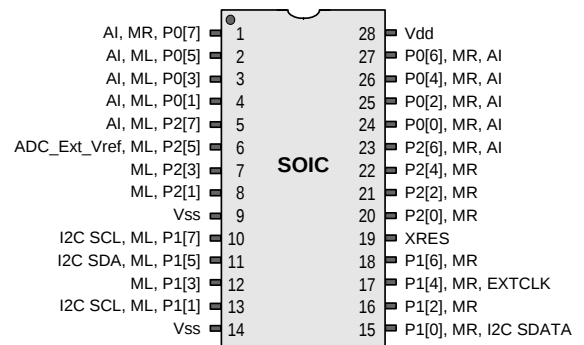
This PSoC device family is available in a variety of packages that are listed in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

### CY8C22345, CY8C21345 28-pin SOIC

**Table 2. Pin Definitions**

| Pin No. | Type    |        | Pin Name | Description                                       |
|---------|---------|--------|----------|---------------------------------------------------|
|         | Digital | Analog |          |                                                   |
| 1       | I/O     | I, MR  | P0[7]    | Integration Capacitor for MR                      |
| 2       | I/O     | I, ML  | P0[5]    | Integration Capacitor for ML                      |
| 3       | I/O     | I, ML  | P0[3]    |                                                   |
| 4       | I/O     | I, ML  | P0[1]    |                                                   |
| 5       | I/O     | I, ML  | P2[7]    | To Compare Column 0                               |
| 6       | I/O     | ML     | P2[5]    | Optional ADC External Vref                        |
| 7       | I/O     | ML     | P2[3]    |                                                   |
| 8       | I/O     | ML     | P2[1]    |                                                   |
| 9       | Power   |        | Vss      | Ground Connection <sup>[5]</sup>                  |
| 10      | I/O     | ML     | P1[7]    | I2C serial clock (SCL)                            |
| 11      | I/O     | ML     | P1[5]    | I2C serial data (SDA)                             |
| 12      | I/O     | ML     | P1[3]    |                                                   |
| 13      | I/O     | ML     | P1[1]    | I2C serial clock (SCL), ISSP-SCLK <sup>[6]</sup>  |
| 14      | Power   |        | Vss      | Ground Connection <sup>[5]</sup>                  |
| 15      | I/O     | MR     | P1[0]    | I2C serial Clock (SCL), ISSP-SDATA <sup>[6]</sup> |
| 16      | I/O     | MR     | P1[2]    |                                                   |
| 17      | I/O     | MR     | P1[4]    | Optional external clock input (EXT-CLK)           |
| 18      | I/O     | MR     | P1[6]    |                                                   |
| 19      | Input   |        | XRES     | Active High Pin Reset with Internal Pull Down     |
| 20      | I/O     | MR     | P2[0]    |                                                   |
| 21      | I/O     | MR     | P2[2]    |                                                   |
| 22      | I/O     | MR     | P2[4]    |                                                   |
| 23      | I/O     | I, MR  | P2[6]    | To Compare Column 1                               |
| 24      | I/O     | I, MR  | P0[0]    |                                                   |
| 25      | I/O     | I, MR  | P0[2]    |                                                   |
| 26      | I/O     | I, MR  | P0[4]    |                                                   |
| 27      | I/O     | I, MR  | P0[6]    |                                                   |
| 28      | Power   |        | Vdd      | Supply Voltage                                    |

**Figure 3. Pin Diagram**



**LEGEND:** A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input.

#### Notes

- All V<sub>SS</sub> pins should be brought out to one common GND plane.
- If ISSP is not used, pins P1[0] and P1[1] will respond differently to a POR or XRES event. After a POR or XRES event, both pins are pulled down to ground by going into the resistive zero Drive mode, before reaching the High Z Drive mode.

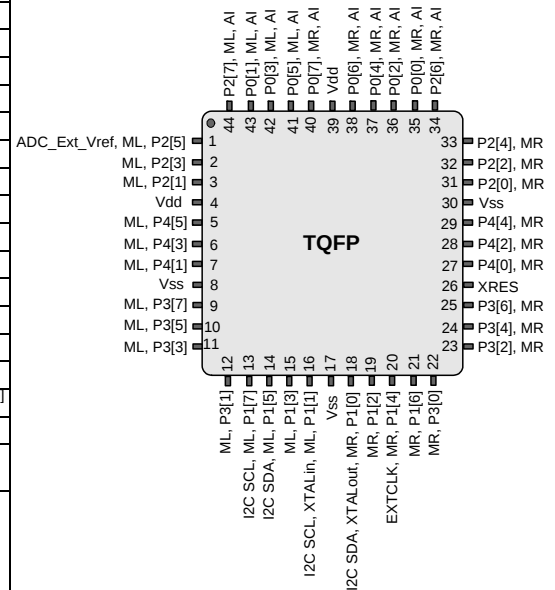
**CY8C22545 44-pin TQFP**
**Table 3. Pin Definitions** <sup>[7]</sup>

| Pin No. | Type    |        | Pin Name | Description                                         |
|---------|---------|--------|----------|-----------------------------------------------------|
|         | Digital | Analog |          |                                                     |
| 1       | I/O     | ML     | P2[5]    | Optional ADC External Vref                          |
| 2       | I/O     | ML     | P2[3]    |                                                     |
| 3       | I/O     | ML     | P2[1]    |                                                     |
| 4       | Power   |        | Vdd      | Supply Voltage                                      |
| 5       | I/O     | ML     | P4[5]    |                                                     |
| 6       | I/O     | ML     | P4[3]    |                                                     |
| 7       | I/O     | ML     | P4[1]    |                                                     |
| 8       | Power   |        | Vss      | Ground Connection                                   |
| 9       | I/O     | ML     | P3[7]    |                                                     |
| 10      | I/O     | ML     | P3[5]    |                                                     |
| 11      | I/O     | ML     | P3[3]    |                                                     |
| 12      | I/O     | ML     | P3[1]    |                                                     |
| 13      | I/O     | ML     | P1[7]    | I2C serial clock (SCL)                              |
| 14      | I/O     | ML     | P1[5]    | I2C serial data (SDA)                               |
| 15      | I/O     | ML     | P1[3]    |                                                     |
| 16      | I/O     | ML     | P1[1]    | Crystal (XTALin), I2C SCL, ISSP SCLK <sup>[6]</sup> |
| 17      | Power   |        | Vss      | Ground Connection                                   |
| 18      | I/O     | MR     | P1[0]    | Crystal (XTALout), I2C SDA, ISSP SDA <sup>[6]</sup> |
| 19      | I/O     | MR     | P1[2]    |                                                     |
| 20      | I/O     | MR     | P1[4]    | Optional external clock input (EXTCLK)              |
| 21      | I/O     | MR     | P1[6]    |                                                     |
| 22      | I/O     | MR     | P3[0]    |                                                     |
| 23      | I/O     | MR     | P3[2]    |                                                     |
| 24      | I/O     | MR     | P3[4]    |                                                     |
| 25      | I/O     | MR     | P3[6]    |                                                     |
| 26      | Input   |        | XRES     | Active High Pin Reset with Internal Pull Down       |
| 27      | I/O     | MR     | P4[0]    |                                                     |
| 28      | I/O     | MR     | P4[2]    |                                                     |
| 29      | I/O     | MR     | P4[4]    |                                                     |
| 30      | Power   |        | Vss      | Ground Connection                                   |
| 31      | I/O     | MR     | P2[0]    |                                                     |
| 32      | I/O     | MR     | P2[2]    |                                                     |
| 33      | I/O     | MR     | P2[4]    |                                                     |
| 34      | I/O     | I, MR  | P2[6]    | To Compare Column 1                                 |
| 35      | I/O     | I, MR  | P0[0]    |                                                     |
| 36      | I/O     | I, MR  | P0[2]    |                                                     |
| 37      | I/O     | I, MR  | P0[4]    |                                                     |
| 38      | I/O     | I, MR  | P0[6]    |                                                     |
| 39      | Power   |        | Vdd      | Supply Voltage                                      |
| 40      | I/O     | I, MR  | P0[7]    | Integration Capacitor for MR                        |
| 41      | I/O     | I, ML  | P0[5]    | Integration Capacitor for ML                        |
| 42      | I/O     | I, ML  | P0[3]    |                                                     |
| 43      | I/O     | I, ML  | P0[1]    |                                                     |
| 44      | I/O     | I, ML  | P2[7]    | To Compare Column 0                                 |

**LEGEND:** A = Analog, I = Input, O = Output, M=Analog Mux input, MR= Analog Mux right input, ML= Analog Mux left input.

**Note**

7. All V<sub>SS</sub> pins should be brought out to one common GND plane.

**Figure 4. Pin Diagram**


## Registers

This section lists the registers of this PSoC device family by mapping tables. For detailed register information, refer the *PSoC Programmable System-on Chip Technical Reference Manual*.

### Register Conventions

**Table 4. Abbreviations**

| Convention | Description                       |
|------------|-----------------------------------|
| RW         | Read and write register or bit(s) |
| R          | Read register or bit(s)           |
| W          | Write register or bit(s)          |
| L          | Logical register or bit(s)        |
| C          | Clearable register or bit(s)      |
| #          | Access is bit specific            |

### Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts. The XIO bit in the Flag register determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.



Table 5. Register Map Bank 0 Table: User Space

| Name     | Addr (0,Hex) | Access | Name       | Addr (0,Hex) | Access | Name      | Addr (0,Hex) | Access | Name      | Addr (0,Hex) | Access |
|----------|--------------|--------|------------|--------------|--------|-----------|--------------|--------|-----------|--------------|--------|
| PRT0DR   | 00           | RW     |            | 40           | #      | ASC10CR0* | 80*          | RW     |           | C0           | RW     |
| PRT0IE   | 01           | RW     |            | 41           | W      |           | 81           | RW     |           | C1           | RW     |
| PRT0GS   | 02           | RW     |            | 42           | RW     |           | 82           | RW     |           | C2           | RW     |
| PRT0DM2  | 03           | RW     |            | 43           | #      |           | 83           | RW     |           | C3           | RW     |
| PRT1DR   | 04           | RW     |            | 44           | #      | ASD11CR0* | 84*          | RW     |           | C4           | RW     |
| PRT1IE   | 05           | RW     |            | 45           | W      |           | 85           | RW     |           | C5           | RW     |
| PRT1GS   | 06           | RW     |            | 46           | RW     |           | 86           | RW     |           | C6           | RW     |
| PRT1DM2  | 07           | RW     |            | 47           | #      |           | 87           | RW     |           | C7           | RW     |
| PRT2DR   | 08           | RW     |            | 48           | #      |           | 88           | RW     | PWMVREF0  | C8           | #      |
| PRT2IE   | 09           | RW     |            | 49           | W      |           | 89           | RW     | PWMVREF1  | C9           | #      |
| PRT2GS   | 0A           | RW     |            | 4A           | RW     |           | 8A           | RW     | IDAC_MODE | CA           | RW     |
| PRT2DM2  | 0B           | RW     |            | 4B           | #      |           | 8B           | RW     | PWM_SRC   | CB           | #      |
| PRT3DR   | 0C           | RW     |            | 4C           | #      |           | 8C           | RW     | TS_CR0    | CC           | RW     |
| PRT3IE   | 0D           | RW     |            | 4D           | W      |           | 8D           | RW     | TS_CMPH   | CD           | RW     |
| PRT3GS   | 0E           | RW     |            | 4E           | RW     |           | 8E           | RW     | TS_Cmpl   | CE           | RW     |
| PRT3DM2  | 0F           | RW     |            | 4F           | #      |           | 8F           | RW     | TS_CR1    | CF           | RW     |
| PRT4DR   | 10           | RW     | CSD0_DR0_L | 50           | R      |           | 90           | RW     | CUR_PP    | D0           | RW     |
| PRT4IE   | 11           | RW     | CSD0_DR1_L | 51           | W      |           | 91           | RW     | STK_PP    | D1           | RW     |
| PRT4GS   | 12           | RW     | CSD0_CNT_L | 52           | R      |           | 92           | RW     | PRV_PP    | D2           | RW     |
| PRT4DM2  | 13           | RW     | CSD0_CR0   | 53           | #      |           | 93           | RW     | IDX_PP    | D3           | RW     |
|          | 14           | RW     | CSD0_DR0_H | 54           | R      |           | 94           | RW     | MVR_PP    | D4           | RW     |
|          | 15           | RW     | CSD0_DR1_H | 55           | W      |           | 95           | RW     | MVW_PP    | D5           | RW     |
|          | 16           | RW     | CSD0_CNT_H | 56           | R      |           | 96           | RW     | I2C0_CFG  | D6           | RW     |
|          | 17           | RW     | CSD0_CR1   | 57           | RW     |           | 97           | RW     | I2C0_SCR  | D7           | #      |
|          | 18           | RW     | CSD1_DR0_L | 58           | R      |           | 98           | RW     | I2C0_DR   | D8           | RW     |
|          | 19           | RW     | CSD1_DR1_L | 59           | W      |           | 99           | RW     | I2C0_MSCR | D9           | #      |
|          | 1A           | RW     | CSD1_CNT_L | 5A           | R      |           | 9A           | RW     | INT_CLR0  | DA           | RW     |
|          | 1B           | RW     | CSD1_CR0   | 5B           | #      |           | 9B           | RW     | INT_CLR1  | DB           | RW     |
|          | 1C           | RW     | CSD1_DR0_H | 5C           | R      |           | 9C           | RW     | INT_CLR2  | DC           | RW     |
|          | 1D           | RW     | CSD1_DR1_H | 5D           | W      |           | 9D           | RW     | INT_CLR3  | DD           | RW     |
|          | 1E           | RW     | CSD1_CNT_H | 5E           | R      |           | 9E           | RW     | INT_MSK3  | DE           | RW     |
|          | 1F           | RW     | CSD_CR1    | 5F           | RW     |           | 9F           | RW     | INT_MSK2  | DF           | RW     |
| DBC00DR0 | 20           | #      | AMX_IN     | 60           | RW     |           | A0           |        | INT_MSK0  | E0           | RW     |
| DBC00DR1 | 21           | W      | AMUX_CFG   | 61           | RW     |           | A1           |        | INT_MSK1  | E1           | RW     |
| DBC00DR2 | 22           | RW     | PWM_CR     | 62           | RW     |           | A2           |        | INT_VC    | E2           | RC     |
| DBC00CR0 | 23           | #      | ARF_CR     | 63           | RW     |           | A3           |        | RES_WDT   | E3           | W      |
| DBC01DR0 | 24           | #      | CMP_CR0    | 64           | #      |           | A4           |        | DEC_DH    | E4           | RW     |
| DBC01DR1 | 25           | W      | ASY_CR     | 65           | #      |           | A5           |        | DEC_DL    | E5           | RW     |
| DBC01DR2 | 26           | RW     | CMP_CR1    | 66           | RW     |           | A6           |        | DEC_CR0*  | E6           | RW     |
| DBC01CR0 | 27           | #      |            | 67           | RW     |           | A7           |        | DEC_CR1*  | E7           | RW     |
| DCC02DR0 | 28           | #      | ADC0_CR    | 68           | #      |           | A8           | W      | MUL0_X    | E8           | W      |
| DCC02DR1 | 29           | W      | ADC1_CR    | 69           | #      |           | A9           | W      | MUL0_Y    | E9           | W      |
| DCC02DR2 | 2A           | RW     | SADC_DH    | 6A           | RW     |           | AA           | R      | MUL0_DH   | EA           | R      |
| DCC02CR0 | 2B           | #      | SADC_DL    | 6B           | RW     |           | AB           | R      | MUL0_DL   | EB           | R      |
| DCC03DR0 | 2C           | #      | TMP_DR0    | 6C           | RW     |           | AC           | RW     | ACC0_DR1  | EC           | RW     |
| DCC03DR1 | 2D           | W      | TMP_DR1    | 6D           | RW     |           | AD           | RW     | ACC0_DR0  | ED           | RW     |
| DCC03DR2 | 2E           | RW     | TMP_DR2    | 6E           | RW     |           | AE           | RW     | ACC0_DR3  | EE           | RW     |
| DCC03CR0 | 2F           | #      | TMP_DR3    | 6F           | RW     |           | AF           | RW     | ACC0_DR2  | EF           | RW     |
| DBC10DR0 | 30           | #      |            | 70           | RW     | RDI0RI    | B0           | RW     | CPU_A     | F0           | #      |
| DBC10DR1 | 31           | W      |            | 71           | RW     | RDI0SYN   | B1           | RW     | CPU_T1    | F1           | #      |
| DBC10DR2 | 32           | RW     | ACB00CR1*  | 72*          | RW     | RDI0IS    | B2           | RW     | CPU_T2    | F2           | #      |
| DBC10CR0 | 33           | #      | ACB00CR2*  | 73*          | RW     | RDI0LT0   | B3           | RW     | CPU_X     | F3           | #      |
| DBC11DR0 | 34           | #      |            | 74           | RW     | RDI0LT1   | B4           | RW     | CPU_PCL   | F4           | #      |
| DBC11DR1 | 35           | W      |            | 75           | RW     | RDI0RO0   | B5           | RW     | CPU_PCH   | F5           | #      |
| DBC11DR2 | 36           | RW     | ACB01CR1*  | 76*          | RW     | RDI0RO1   | B6           | RW     | CPU_SP    | F6           | #      |
| DBC11CR0 | 37           | #      | ACB01CR2*  | 77*          | RW     | RDI0DSM   | B7           | RW     | CPU_F     | F7           | I      |
| DCC12DR0 | 38           | #      |            | 78           | RW     | RDI1RI    | B8           | RW     | CPU_TST0  | F8           | RW     |
| DCC12DR1 | 39           | W      |            | 79           | RW     | RDI1SYN   | B9           | RW     | CPU_TST1  | F9           | RW     |
| DCC12DR2 | 3A           | RW     |            | 7A           | RW     | RDI1IS    | BA           | RW     | CPU_TST2  | FA           | RW     |
| DCC12CR0 | 3B           | #      |            | 7B           | RW     | RDI1LT0   | BB           | RW     | CPU_TST3  | FB           | #      |
| DCC13DR0 | 3C           | #      |            | 7C           | RW     | RDI1LT1   | BC           | RW     | DAC1_D    | FC           | RW     |
| DCC13DR1 | 3D           | W      |            | 7D           | RW     | RDI1RO0   | BD           | RW     | DAC0_D    | FD           | RW     |
| DCC13DR2 | 3E           | RW     |            | 7E           | RW     | RDI1RO1   | BE           | RW     | CPU_SCR1  | FE           | #      |
| DCC13CR0 | 3F           | #      |            | 7F           | RW     | RDI1DSM   | BF           | RW     | CPU_SCR0  | FF           | #      |

Shaded fields are Reserved and must not be accessed.

# Access is bit specific. \* has a different meaning.



Table 6. Register Map Bank 1 Table: Configuration Space

| Name     | Addr (1,Hex) | Access | Name       | Addr (1,Hex) | Access | Name         | Addr (1,Hex) | Access | Name      | Addr (1,Hex) | Access |
|----------|--------------|--------|------------|--------------|--------|--------------|--------------|--------|-----------|--------------|--------|
| PRT0DM0  | 0            | RW     |            | 40           | RW     | ASCI0CR0*    | 80*          | RW     |           | C0           | RW     |
| PRT0DM1  | 1            | RW     |            | 41           | RW     |              | 81           | RW     |           | C1           | RW     |
| PRT0IC0  | 2            | RW     |            | 42           | RW     |              | 82           | RW     |           | C2           | RW     |
| PRT0IC1  | 3            | RW     |            | 43           | RW     |              | 83           | RW     |           | C3           | RW     |
| PRT1DM0  | 4            | RW     |            | 44           | RW     | ASD1ICR0*    | 84*          | RW     |           | C4           | RW     |
| PRT1DM1  | 5            | RW     |            | 45           | RW     |              | 85           | RW     |           | C5           | RW     |
| PRT1IC0  | 6            | RW     |            | 46           | RW     |              | 86           | RW     |           | C6           | RW     |
| PRT1IC1  | 7            | RW     |            | 47           | RW     |              | 87           | RW     |           | C7           | RW     |
| PRT2DM0  | 8            | RW     |            | 48           | RW     |              | 88           | RW     |           | C8           | #      |
| PRT2DM1  | 9            | RW     |            | 49           | RW     |              | 89           | RW     |           | C9           | RW     |
| PRT2IC0  | 0A           | RW     |            | 4A           | RW     |              | 8A           | RW     |           | CA           | RW     |
| PRT2IC1  | 0B           | RW     |            | 4B           | RW     |              | 8B           | RW     |           | CB           | RW     |
| PRT3DM0  | 0C           | RW     |            | 4C           | RW     |              | 8C           | RW     |           | CC           | #      |
| PRT3DM1  | 0D           | RW     |            | 4D           | RW     |              | 8D           | RW     |           | CD           | RW     |
| PRT3IC0  | 0E           | RW     |            | 4E           | RW     |              | 8E           | RW     |           | CE           | RW     |
| PRT3IC1  | 0F           | RW     |            | 4F           | RW     |              | 8F           | RW     |           | CF           | RW     |
| PRT4DM0  | 10           | RW     | CMP0CR1    | 50           | RW     |              | 90           | RW     | GDI_O_IN  | D0           | RW     |
| PRT4DM1  | 11           | RW     | CMP0CR2    | 51           | RW     |              | 91           | RW     | GDI_E_IN  | D1           | RW     |
| PRT4IC0  | 12           | RW     |            | 52           | RW     |              | 92           | RW     | GDI_O_OU  | D2           | RW     |
| PRT4IC1  | 13           | RW     | VDAC50CR0  | 53           | RW     |              | 93           | RW     | GDI_E_OU  | D3           | RW     |
|          | 14           | RW     | CMP1CR1    | 54           | RW     |              | 94           | RW     |           | D4           | RW     |
|          | 15           | RW     | CMP1CR2    | 55           | RW     |              | 95           | RW     |           | D5           | RW     |
|          | 16           | RW     |            | 56           | RW     |              | 96           | RW     |           | D6           | RW     |
|          | 17           | RW     | VDAC51CR0  | 57           | RW     |              | 97           | RW     |           | D7           | RW     |
|          | 18           | RW     | CSCMPCR0   | 58           | #      |              | 98           | RW     | MUX_CR0   | D8           | RW     |
|          | 19           | RW     | CSCMPGOEN  | 59           | RW     |              | 99           | RW     | MUX_CR1   | D9           | RW     |
|          | 1A           | RW     | CSLUTCR0   | 5A           | RW     |              | 9A           | RW     | MUX_CR2   | DA           | RW     |
|          | 1B           | RW     | CMPCOLMUX  | 5B           | RW     |              | 9B           | RW     | MUX_CR3   | DB           | RW     |
|          | 1C           | RW     | CMPPWMCR   | 5C           | RW     |              | 9C           | RW     | DAC_CR1#  | DC           | RW     |
|          | 1D           | RW     | CMPFLTCR   | 5D           | RW     |              | 9D           | RW     | OSC_GO_EN | DD           | RW     |
|          | 1E           | RW     | CMPCLK1    | 5E           | RW     |              | 9E           | RW     | OSC_CR4   | DE           | RW     |
|          | 1F           | RW     | CMPCLK0    | 5F           | RW     |              | 9F           | RW     | OSC_CR3   | DF           | RW     |
| DBC00FN  | 20           | RW     | CLK_CR0    | 60           | RW     | GDI_O_IN_CR  | A0           | RW     | OSC_CR0   | E0           | RW     |
| DBC00IN  | 21           | RW     | CLK_CR1    | 61           | RW     | GDI_E_IN_CR  | A1           | RW     | OSC_CR1   | E1           | RW     |
| DBC00OU  | 22           | RW     | ABF_CR0    | 62           | RW     | GDI_O_OU_CR  | A2           | RW     | OSC_CR2   | E2           | RW     |
| DBC00CR1 | 23           | RW     | AMD_CR0    | 63           | RW     | GDI_E_OU_CR  | A3           | RW     | VLT_CR    | E3           | RW     |
| DBC01FN  | 24           | RW     | CMP_GO_EN  | 64           | RW     | RTC_H        | A4           | RW     | VLT_CMP   | E4           | R      |
| DBC01IN  | 25           | RW     | CMP_GO_EN1 | 65           | RW     | RTC_M        | A5           | RW     | ADC0_TR*  | E5           | RW     |
| DBC01OU  | 26           | RW     | AMD_CR1    | 66           | RW     | RTC_S        | A6           | RW     | ADC1_TR*  | E6           | RW     |
| DBC01CR1 | 27           | RW     | ALT_CR0    | 67           | RW     | RTC_CR       | A7           | RW     | V2BG_TR   | E7           | RW     |
| DCC02FN  | 28           | RW     | ALT_CR1    | 68           | RW     | SADC_CR0     | A8           | RW     | IMO_TR    | E8           | W      |
| DCC02IN  | 29           | RW     | CLK_CR2    | 69           | RW     | SADC_CR1     | A9           | RW     | ILO_TR    | E9           | W      |
| DCC02OU  | 2A           | RW     |            | 6A           | RW     | SADC_CR2     | AA           | RW     | BDG_TR    | EA           | RW     |
| DBC02CR1 | 2B           | RW     | CLK_CR3    | 6B           | RW     | SADC_CR3TRIM | AB           | RW     | ECO_TR    | EB           | W      |
| DCC03FN  | 2C           | RW     | TMP_DR0    | 6C           | RW     | SADC_CR4     | AC           | RW     | MUX_CR4   | EC           | RW     |
| DCC03IN  | 2D           | RW     | TMP_DR1    | 6D           | RW     | I2C0_AD      | AD           | RW     | MUX_CR5   | ED           | RW     |
| DCC03OU  | 2E           | RW     | TMP_DR2    | 6E           | RW     |              | AE           | RW     | MUX_CR6   | EE           | RW     |
| DBC03CR1 | 2F           | RW     | TMP_DR3    | 6F           | RW     |              | AF           | RW     | MUX_CR7   | EF           | RW     |
| DBC10FN  | 30           | RW     |            | 70           | RW     | RD10RI       | B0           | RW     | CPU_A     | F0           | #      |
| DBC10IN  | 31           | RW     |            | 71           | RW     | RD10SYN      | B1           | RW     | CPU_T1    | F1           | #      |
| DBC10OU  | 32           | RW     | ACB00CR1*  | 72           | RW     | RD10IS       | B2           | RW     | CPU_T2    | F2           | #      |
| DBC10CR1 | 33           | RW     | ACB00CR2*  | 73           | RW     | RD10LT0      | B3           | RW     | CPU_X     | F3           | #      |
| DBC11FN  | 34           | RW     |            | 74           | RW     | RD10LT1      | B4           | RW     | CPU_PCL   | F4           | #      |
| DBC11IN  | 35           | RW     |            | 75           | RW     | RD10RO0      | B5           | RW     | CPU_PCH   | F5           | #      |
| DBC11OU  | 36           | RW     | ACB01CR1*  | 76*          | RW     | RD10RO1      | B6           | RW     | CPU_SP    | F6           | #      |
| DBC11CR1 | 37           | RW     | ACB01CR2*  | 77*          | RW     | RD10DSM      | B7           | RW     | CPU_F     | F7           | I      |
| DCC12FN  | 38           | RW     |            | 78           | RW     | RD11RI       | B8           | RW     | FLS_PRO   | F8           | RW     |
| DCC12IN  | 39           | RW     |            | 79           | RW     | RD11SYN      | B9           | RW     | FLS_TR    | F9           | W      |
| DCC12OU  | 3A           | RW     |            | 7A           | RW     | RD11IS       | BA           | RW     | FLS_PR1   | FA           | RW     |
| DBC12CR1 | 3B           | RW     |            | 7B           | RW     | RD11LT0      | BB           | RW     |           | FB           |        |
| DCC13FN  | 3C           | RW     |            | 7C           | RW     | RD11LT1      | BC           | RW     | FAC_CR0   | FC           | SW     |
| DCC13IN  | 3D           | RW     |            | 7D           | RW     | RD11RO0      | BD           | RW     | DAC_CR0#  | FD           | RW     |
| DCC13OU  | 3E           | RW     |            | 7E           | RW     | RD11RO1      | BE           | RW     | CPU_SCR1  | FE           | #      |
| DBC13CR1 | 3F           | RW     |            | 7F           | RW     | RD11DSM      | BF           | RW     | CPU_SCR0  | FF           | #      |

Shaded fields are Reserved and must not be accessed.

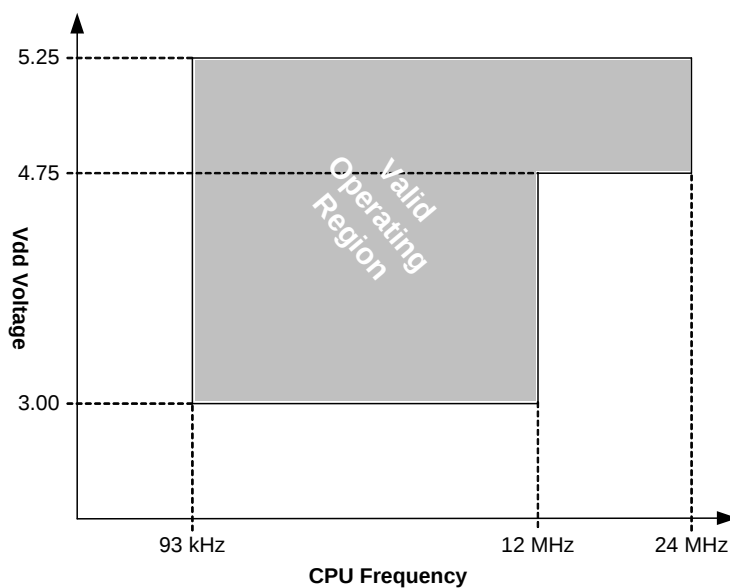
# Access is bit specific. \* has a different meaning.

## Electrical Specifications

This section presents the DC and AC electrical specifications of this PSoC device family. For the latest electrical specifications, check the most recent data sheet by visiting <http://www.cypress.com>.

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$ , except where noted. Specifications for devices running at greater than 12 MHz are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$  and  $T_J \leq 82\text{ }^{\circ}\text{C}$ .

**Figure 5. Voltage versus Operating Frequency**



## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 7. Absolute Maximum Ratings**

| Symbol                | Description                                                   | Min                   | Typ | Max                   | Units | Notes                                                  |
|-----------------------|---------------------------------------------------------------|-----------------------|-----|-----------------------|-------|--------------------------------------------------------|
| T <sub>STG</sub>      | Storage temperature                                           | –55                   | –   | +100                  | °C    | Higher storage temperatures reduce data retention time |
| T <sub>BAKETEMP</sub> | Bake temperature                                              | –                     | 125 | See Package label     | °C    |                                                        |
| T <sub>BAKETIME</sub> | Bake time                                                     | See package label     | –   | 72                    | Hours |                                                        |
| T <sub>A</sub>        | Ambient temperature with power applied                        | –40                   | –   | +85                   | °C    |                                                        |
| V <sub>DD</sub>       | Supply voltage on V <sub>DD</sub> relative to V <sub>SS</sub> | –0.5                  | –   | +6.0                  | V     |                                                        |
| V <sub>IO</sub>       | DC input voltage                                              | V <sub>SS</sub> - 0.5 | –   | V <sub>DD</sub> + 0.5 | V     |                                                        |
| V <sub>IOZ</sub>      | DC voltage applied to tristate                                | V <sub>SS</sub> - 0.5 | –   | V <sub>DD</sub> + 0.5 | V     |                                                        |
| I <sub>MIO</sub>      | Maximum current into any port pin                             | –25                   | –   | +50                   | mA    |                                                        |
| ESD                   | Electr static discharge voltage                               | 2000                  | –   | –                     | V     | Human Body Model ESD                                   |
| LU                    | Latch up current                                              | –                     | –   | 200                   | mA    |                                                        |

## Operating Temperature

**Table 8. Operating Temperature**

| Symbol         | Description          | Min | Typ | Max  | Units | Notes                                                                                                                                                                                   |
|----------------|----------------------|-----|-----|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T <sub>A</sub> | Ambient temperature  | –40 | –   | +85  | °C    |                                                                                                                                                                                         |
| T <sub>J</sub> | Junction temperature | –40 | –   | +100 | °C    | The temperature rise from ambient to junction is package specific. See <a href="#">Table 30 on page 28</a> . The user must limit the power consumption to comply with this requirement. |

## DC Electrical Characteristics

### DC Chip Level Specifications

Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at  $25^{\circ}\text{C}$ , and are for design guidance only, unless specified otherwise.

**Table 9. DC Chip Level Specifications**

| Symbol              | Description                                                                                                   | Min   | Typ | Max   | Units | Notes                                                                                                                                              |
|---------------------|---------------------------------------------------------------------------------------------------------------|-------|-----|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>DD</sub>     | Supply voltage                                                                                                | 3.0   | –   | 5.25  | V     | See Table 17 on page 19                                                                                                                            |
| I <sub>DD</sub>     | Supply current                                                                                                | –     | 7   | 12    | mA    | Conditions are V <sub>DD</sub> = 5.0 V, 25°C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz VC2 = 93.75 kHz VC3 = 93.75 kHz                          |
| I <sub>DD3</sub>    | Supply current                                                                                                | –     | 4   | 7     | mA    | Conditions are V <sub>DD</sub> = 3.3 V T <sub>A</sub> = 25 °C, CPU = 3 MHz 48 MHz = Disabled VC1 = 1.5 MHz, VC2 = 93.75 kHz VC3 = 93.75 kHz        |
| I <sub>SB</sub>     | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT <sup>[8]</sup>                                       | –     | 3   | 6.5   | μA    | Conditions are with internal slow speed oscillator, V <sub>DD</sub> = 3.3 V $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$                 |
| I <sub>SBH</sub>    | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature <sup>[8]</sup>                   | –     | 4   | 25    | μA    | Conditions are with internal slow speed oscillator, V <sub>DD</sub> = 3.3 V $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$                     |
| I <sub>SBXTL</sub>  | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal <sup>[8]</sup>                     | –     | 4   | 7.5   | μA    | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V <sub>DD</sub> = 3.3 V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$ |
| I <sub>SBXTLH</sub> | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature <sup>[8]</sup> | –     | 5   | 26    | μA    | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V <sub>DD</sub> = 3.3 V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$     |
| V <sub>REF</sub>    | Reference Voltage (Bandgap)                                                                                   | 1.275 | 1.3 | 1.325 | V     | Trimmed for appropriate V <sub>DD</sub>                                                                                                            |

#### Note

8. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

## DC GPIO Specifications

Table 10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only, unless otherwise specified.

**Table 10. DC GPIO Specifications**

| Symbol         | Description                       | Min            | Typ | Max  | Units     | Notes                                                                                                                                                                                                                        |
|----------------|-----------------------------------|----------------|-----|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $R_{PU}$       | Pull-up resistor                  | 4              | 5.6 | 8    | $k\Omega$ |                                                                                                                                                                                                                              |
| $R_{PD}^{[9]}$ | Pull-down resistor                | 4              | 5.6 | 8    | $k\Omega$ |                                                                                                                                                                                                                              |
| $V_{OH}$       | High output level                 | $V_{DD} - 1.0$ | –   | –    | V         | $I_{OH} = 10\text{ mA}$ , $V_{DD} = 4.75\text{ to }5.25\text{ V}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined $I_{OH}$ budget.  |
| $V_{OL}$       | Low output level                  | –              | –   | 0.75 | V         | $I_{OL} = 25\text{ mA}$ , $V_{DD} = 4.75\text{ to }5.25\text{ V}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined $I_{OL}$ budget. |
| $I_{OH}$       | High level source current         | 10             | –   | –    | mA        | $V_{OH} = V_{DD} - 1.0\text{ V}$ , see the limitations of the total current in the note for $V_{OH}$ .                                                                                                                       |
| $I_{OL}$       | Low level sink current            | 25             | –   | –    | mA        | $V_{OL} = 0.75\text{ V}$ , see the limitations of the total current in the note for $V_{OL}$ .                                                                                                                               |
| $V_{IL}^{[9]}$ | Input Low level                   | –              | –   | 0.8  | V         | $V_{DD} = 3.0\text{ to }5.25$                                                                                                                                                                                                |
| $V_{IH}^{[9]}$ | Input High level                  | 2.1            | –   | –    | V         | $V_{DD} = 3.0\text{ to }5.25$                                                                                                                                                                                                |
| $V_H^{[9]}$    | Input hysteresis                  | –              | 60  | –    | mV        |                                                                                                                                                                                                                              |
| $I_{IL}^{[9]}$ | Input leakage (absolute value)    | –              | 1   | –    | nA        | Gross tested to 1 $\mu\text{A}$                                                                                                                                                                                              |
| $C_{IN}^{[9]}$ | Capacitive load on pins as input  | –              | 3.5 | 10   | pF        | Package and pin dependent. Temp = 25 °C                                                                                                                                                                                      |
| $C_{OUT}$      | Capacitive load on pins as output | –              | 3.5 | 10   | pF        | Package and pin dependent. Temp = 25 °C                                                                                                                                                                                      |

### Note

9. The DC GPIO specifications apply to the XRES pin as well.

### DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 11. 5 V DC Operational Amplifier Specifications**

| Symbol                     | Description                                | Min | Typ | Max                 | Units                          | Notes                                                     |
|----------------------------|--------------------------------------------|-----|-----|---------------------|--------------------------------|-----------------------------------------------------------|
| $V_{\text{OSOA}}$          | Input offset voltage (absolute value)      | –   | 2.5 | 15                  | mV                             |                                                           |
| $\text{TCV}_{\text{OSOA}}$ | Average input offset voltage drift         | –   | 10  | –                   | $\mu\text{V}/^{\circ}\text{C}$ |                                                           |
| $I_{\text{EBOA}}^{[10]}$   | Input leakage current (Port 0 Analog Pins) | –   | 200 | –                   | pA                             | Gross tested to 1 $\mu\text{A}$                           |
| $C_{\text{INOA}}$          | Input capacitance (Port 0 Analog Pins)     | –   | 4.5 | 9.5                 | pF                             | Package and pin dependent.<br>Temp = $25^{\circ}\text{C}$ |
| $V_{\text{CMOA}}$          | Common mode Voltage Range                  | 0.0 | –   | $V_{\text{DD}} - 1$ | V                              |                                                           |

**Table 12. 3.3 V DC Operational Amplifier Specifications**

| Symbol                     | Description                                | Min | Typ | Max                 | Units                          | Notes                                                     |
|----------------------------|--------------------------------------------|-----|-----|---------------------|--------------------------------|-----------------------------------------------------------|
| $V_{\text{OSOA}}$          | Input offset voltage (absolute value)      | –   | 2.5 | 15                  | mV                             |                                                           |
| $\text{TCV}_{\text{OSOA}}$ | Average input offset voltage drift         | –   | 10  | –                   | $\mu\text{V}/^{\circ}\text{C}$ |                                                           |
| $I_{\text{EBOA}}^{[10]}$   | Input leakage current (Port 0 Analog Pins) | –   | 200 | –                   | pA                             | Gross tested to 1 $\mu\text{A}$                           |
| $C_{\text{INOA}}$          | Input capacitance (Port 0 Analog Pins)     | –   | 4.5 | 9.5                 | pF                             | Package and pin dependent.<br>Temp = $25^{\circ}\text{C}$ |
| $V_{\text{CMOA}}$          | Common mode voltage range                  | 0   | –   | $V_{\text{DD}} - 1$ | V                              |                                                           |

### DC IDAC Specifications

The following table lists the guaranteed maximum and minimum specifications for automotive A-grade and E-grade devices. Unless otherwise noted, all specifications in the table apply to A-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Unless otherwise noted, all specifications in the table also apply to E-grade devices for the voltage and temperature ranges of: 4.75 V to 5.25 V and  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Typical parameters apply to 5 V and 3.3 V at  $25^{\circ}\text{C}$ , unless specified otherwise, and are for design guidance only.

**Table 13. DC IDAC Specifications**

| Symbol                           | Description                                                                        | Min | Typ  | Max  | Units         | Notes                                                   |
|----------------------------------|------------------------------------------------------------------------------------|-----|------|------|---------------|---------------------------------------------------------|
| $\text{IDAC}_{\text{GAIN}}$      | IDAC gain                                                                          | –   | 75.4 | 218  | nA/bit        | IDAC gain at 1x current gain                            |
|                                  |                                                                                    | –   | 335  | 693  | nA/bit        | IDAC gain at 4x current gain                            |
|                                  |                                                                                    | –   | 1160 | 2410 | nA/bit        | IDAC gain at 16x current gain                           |
|                                  |                                                                                    | –   | 2340 | 5700 | nA/bit        | IDAC gain at 32x current gain                           |
|                                  | Monotonicity                                                                       | No  | –    | –    | –             | IDAC gain is non-monotonous at step intervals of (0x10) |
| $\text{IDAC}_{\text{GAIN\_VAR}}$ | IDAC gain variation over temperature $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ | –   | 3.22 | –    | nA            | at 1x current gain                                      |
|                                  |                                                                                    | –   | 18.1 | –    | nA            | at 4x current gain                                      |
|                                  |                                                                                    | –   | 59.9 | –    | nA            | at 16x current gain                                     |
|                                  |                                                                                    | –   | 120  | –    | nA            | at 32x current gain                                     |
| $I_{\text{IDAC}}$                | IDAC current at maximum code (0xFF)                                                | –   | 19.2 | –    | $\mu\text{A}$ | at 1x current gain                                      |
|                                  |                                                                                    | –   | 85.4 | –    | $\mu\text{A}$ | at 4x current gain                                      |
|                                  |                                                                                    | –   | 295  | –    | $\mu\text{A}$ | at 16x current gain                                     |
|                                  |                                                                                    | –   | 596  | –    | $\mu\text{A}$ | at 32x current gain                                     |

#### Note

10. Atypical behavior:  $I_{\text{EBOA}}$  of Port 0 Pin 0 is below 1 nA at  $25^{\circ}\text{C}$ ; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

### DC Low Power Comparator Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  respectively. Typical parameters apply to 5 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 14. DC Low Power Comparator Specifications**

| Symbol              | Description                                        | Min | Typ | Max                 | Units | Notes |
|---------------------|----------------------------------------------------|-----|-----|---------------------|-------|-------|
| $V_{\text{REFLPC}}$ | Low power comparator (LPC) reference voltage range | 0.2 | –   | $V_{\text{DD}} - 1$ | V     |       |
| $V_{\text{OSLPC}}$  | LPC voltage offset                                 | –   | 2.5 | 30                  | mV    |       |

### SAR10 ADC DC Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 15. SAR10 ADC DC Specifications**

| Symbol               | Description                                                             | Min  | Typ | Max  | Units | Notes                                                                                                                                                                                                                                                            |
|----------------------|-------------------------------------------------------------------------|------|-----|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{\text{adcvref}}$ | Reference voltage at pin P2[5] when configured as ADC reference voltage | 3.0  | –   | 5.25 | V     | When $V_{\text{REF}}$ is buffered inside ADC, the voltage level at P2[5] (when configured as ADC reference voltage) must be always maintained to be at least 300 mV less than the chip supply voltage level on Vdd pin. ( $V_{\text{adcvref}} < V_{\text{DD}}$ ) |
| $I_{\text{adcvref}}$ | Current when P2[5] is configured as ADC $V_{\text{REF}}$                | –    | –   | 0.5  | mA    | Disables the internal voltage reference buffer                                                                                                                                                                                                                   |
| INL at 10 bits       | Integral Nonlinearity                                                   | –2.5 | –   | 2.5  | LSB   | For $V_{\text{DD}} \geq 3.0\text{ V}$ and $V_{\text{ref}} \geq 3.0\text{ V}$                                                                                                                                                                                     |
|                      |                                                                         | –5.0 | –   | 5.0  | LSB   | For $V_{\text{DD}} < 3.0\text{ V}$ or $V_{\text{ref}} < 3.0\text{ V}$                                                                                                                                                                                            |
| DNL at 10 bits       | Differential Nonlinearity                                               | –1.5 | –   | 1.5  | LSB   | For $V_{\text{DD}} \geq 3.0\text{ V}$ and $V_{\text{ref}} \geq 3.0\text{ V}$                                                                                                                                                                                     |
|                      |                                                                         | –4.0 | –   | 4.0  | LSB   | For $V_{\text{DD}} < 3.0\text{ V}$ or $V_{\text{ref}} < 3.0\text{ V}$                                                                                                                                                                                            |
| SPS <sup>[11]</sup>  | Sample per second                                                       | –    | –   | 150  | ksps  | Resolution 10 bits                                                                                                                                                                                                                                               |

#### Note

11. **Errata:** When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data. For more information, see “Errata” on page 35.

### DC Analog Mux Bus Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 16. DC Analog Mux Bus Specifications**

| Symbol    | Description                                | Min | Typ | Max | Units    | Notes              |
|-----------|--------------------------------------------|-----|-----|-----|----------|--------------------|
| $R_{SW}$  | Switch Resistance to Common Analog Bus     | —   | —   | 400 | $\Omega$ | $V_{DD} \geq 3.00$ |
| $R_{gnd}$ | Resistance of Initialization Switch to gnd | —   | —   | 800 | $\Omega$ |                    |

### DC POR and LVD Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 17. DC POR and LVD Specifications**

| Symbol      | Description                            | Min  | Typ  | Max  | Units | Notes                                                                                                       |
|-------------|----------------------------------------|------|------|------|-------|-------------------------------------------------------------------------------------------------------------|
| $V_{PPOR1}$ | Vdd Value for PPOR Trip                | —    | 2.82 | 2.95 | V     | Vdd must be greater than or equal to 3.0 V during startup, reset from the XRES pin, or reset from Watchdog. |
| $V_{PPOR2}$ | PORLEV[1:0] = 01b<br>PORLEV[1:0] = 10b |      | 4.55 | 4.70 | V     |                                                                                                             |
| $V_{LVD2}$  | Vdd Value for LVD Trip                 | 2.95 | 3.02 | 3.09 | V     |                                                                                                             |
| $V_{LVD3}$  | VM[2:0] = 010b                         | 3.06 | 3.13 | 3.20 | V     |                                                                                                             |
| $V_{LVD4}$  | VM[2:0] = 011b                         | 4.37 | 4.48 | 4.55 | V     |                                                                                                             |
| $V_{LVD5}$  | VM[2:0] = 100b                         | 4.50 | 4.64 | 4.75 | V     |                                                                                                             |
| $V_{LVD6}$  | VM[2:0] = 101b                         | 4.62 | 4.73 | 4.83 | V     |                                                                                                             |
| $V_{LVD7}$  | VM[2:0] = 110b                         | 4.71 | 4.81 | 4.95 | V     |                                                                                                             |

### DC Programming Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 18. DC Programming Specifications**

| Symbol                | Description                                                                          | Min            | Typ | Max             | Units | Notes                                                                                  |
|-----------------------|--------------------------------------------------------------------------------------|----------------|-----|-----------------|-------|----------------------------------------------------------------------------------------|
| $V_{DDP}$             | $V_{DD}$ for programming and erase                                                   | 4.5            | 5.0 | 5.5             | V     | This specification applies to the functional requirements of external programmer tools |
| $V_{DDL V}$           | Low $V_{DD}$ for verify                                                              | 3.0            | 3.1 | 3.2             | V     | This specification applies to the functional requirements of external programmer tools |
| $V_{DDH V}$           | High $V_{DD}$ for verify                                                             | 5.1            | 5.2 | 5.3             | V     | This specification applies to the functional requirements of external programmer tools |
| $V_{DDIWRITE}$        | Supply voltage for flash write operation                                             | 3.0            | –   | 5.25            | V     | This specification applies to this device when it is executing internal flash writes   |
| $I_{DDP}$             | Supply Current during Programming or Verify                                          | –              | 5   | 25              | mA    |                                                                                        |
| $V_{ILP}$             | Input Low Voltage during Programming or Verify                                       | –              | –   | 0.8             | V     |                                                                                        |
| $V_{IHP}$             | Input High Voltage during Programming or Verify                                      | 2.2            | –   | –               | V     |                                                                                        |
| $I_{ILP}$             | Input Current when Applying $V_{ILP}$ to P1[0] or P1[1] during Programming or Verify | –              | –   | 0.2             | mA    | Driving internal pull down resistor                                                    |
| $I_{IHP}$             | Input Current when Applying $V_{IHP}$ to P1[0] or P1[1] during Programming or Verify | –              | –   | 1.5             | mA    | Driving internal pull down resistor                                                    |
| $V_{OLV}$             | Output Low Voltage during Programming or Verify                                      | –              | –   | $V_{SS} + 0.75$ | V     |                                                                                        |
| $V_{OHV}$             | Output High Voltage during Programming or Verify                                     | $V_{DD} - 1.0$ | –   | $V_{DD}$        | V     |                                                                                        |
| Flash <sub>ENPB</sub> | Flash Endurance (per block) <sup>[13]</sup>                                          | 50,000         | –   | –               | –     | Erase/write cycles per block                                                           |
| Flash <sub>ENT</sub>  | Flash Endurance (total) <sup>[12]</sup>                                              | 1,800,000      | –   | –               | –     | Erase/write cycles                                                                     |
| Flash <sub>DR</sub>   | Flash Data Retention                                                                 | 10             | –   | –               | Years |                                                                                        |

### DC I<sup>2</sup>C Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 19. DC I<sup>2</sup>C Specifications**

| Parameter           | Description      | Min                 | Typ | Max                  | Units | Notes                                          |
|---------------------|------------------|---------------------|-----|----------------------|-------|------------------------------------------------|
| $V_{IL I2C}^{[14]}$ | Input low level  | –                   | –   | $0.3 \times V_{DD}$  | V     | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$   |
|                     |                  | –                   | –   | $0.25 \times V_{DD}$ | V     | $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ |
| $V_{IH I2C}^{[14]}$ | Input high level | $0.7 \times V_{DD}$ | –   | –                    | V     | $3.0\text{ V} \leq V_{DD} \leq 5.25\text{ V}$  |

#### Note

12. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).  
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.
13. The 50,000 cycle Flash endurance per block is guaranteed only if the Flash operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V
14. All GPIOs meet the DC GPIO  $V_{IL}$  and  $V_{IH}$  specifications found in the DC GPIO specifications sections. The I<sup>2</sup>C GPIO pins also meet the above specs.

## AC Electrical Characteristics

### AC Chip Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 20. 5 V and 3.3 V AC Chip-Level Specifications**

| Symbol                                   | Description                                            | Min   | Min(%) | Typ | Max                          | Max(%) | Units | Notes                                                                                                                                                       |
|------------------------------------------|--------------------------------------------------------|-------|--------|-----|------------------------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F <sub>IMO24</sub> <sup>[15]</sup>       | Internal Main Oscillator Frequency for 24 MHz          | 22.8  | —      | 24  | 25.2 <sup>[16, 17, 18]</sup> | —      | MHz   | Trimmed for 5 V or 3.3 V operation using factory trim values. See <a href="#">Figure 5 on page 13</a> . SLIMO mode = 0 < 85.                                |
| F <sub>IMO6</sub>                        | Internal Main Oscillator Frequency for 6 MHz           | 5.5   | 8      | 6   | 6.5 <sup>[16, 17, 18]</sup>  | 8      | MHz   | Trimmed for 5 V or 3.3 V operation using factory trim values. See <a href="#">Figure 5 on page 13</a> . SLIMO mode = 0 < 85.                                |
| F <sub>CPU1</sub>                        | CPU Frequency (5 V Nominal)                            | 0.089 | —      | 24  | 24.6 <sup>[16, 17]</sup>     | —      | MHz   | 24 MHz only for SLIMO mode = 0.                                                                                                                             |
| F <sub>CPU2</sub>                        | CPU Frequency (3.3 V Nominal)                          | 0.089 | —      | 12  | 12.3 <sup>[17, 18]</sup>     | —      | MHz   | SLIMO mode = 0.                                                                                                                                             |
| F <sub>BLK5</sub>                        | Digital PSoC Block Frequency (5 V Nominal)             | 0     | —      | 48  | 49.2 <sup>[16, 17, 19]</sup> | —      | MHz   | Refer to <a href="#">Table 24 on page 23</a> .                                                                                                              |
| F <sub>BLK33</sub>                       | Digital PSoC Block Frequency (3.3 V Nominal)           | 0     | —      | 24  | 24.6 <sup>[17, 19]</sup>     | —      | MHz   |                                                                                                                                                             |
| F <sub>32K1</sub>                        | Internal Low Speed Oscillator Frequency                | 15    | —      | 32  | 85                           | —      | kHz   |                                                                                                                                                             |
| F <sub>32KU</sub>                        | Untrimmed Internal Low Speed Oscillator Frequency      | 5     | —      | —   | 100                          | —      | kHz   | The ILO is not adjusted with the factory trim values until after the CPU starts running. See the "System Resets" section in the Technical Reference Manual. |
| T <sub>XRES</sub>                        | External Reset Pulse Width                             | 10    | —      | —   | —                            | —      | μs    | This specification refers to the minimum pulse width required to achieve complete device Reset. Shorter pulse widths may cause undefined chip behavior.     |
| DC <sub>24M</sub>                        | 24 MHz Duty Cycle                                      | 40    | —      | 50  | 60                           | —      | %     |                                                                                                                                                             |
| DC <sub>ILO</sub>                        | Internal Low Speed Oscillator Duty Cycle               | 20    | —      | 50  | 80                           | —      | %     |                                                                                                                                                             |
| F <sub>MAX</sub>                         | Maximum frequency of signal on row input or row output | —     | —      | —   | 12.3                         | —      | MHz   |                                                                                                                                                             |
| SR <sub>POWERUP</sub>                    | Power supply slew rate                                 | —     | —      | —   | 250                          | —      | V/ms  | Vdd slew rate during power up.                                                                                                                              |
| T <sub>POWERUP</sub>                     | Time from end of POR to CPU executing code             | —     | —      | —   | 100                          | —      | ms    |                                                                                                                                                             |
| t <sub>jitter</sub> _IMO <sup>[20]</sup> | 24 MHz IMO cycle-to-cycle jitter (RMS)                 | —     | —      | 200 | 700                          | —      | ps    |                                                                                                                                                             |
|                                          | 24 MHz IMO long term N cycle-to-cycle jitter (RMS)     | —     | —      | 300 | 900                          | —      | ps    | N = 32                                                                                                                                                      |
|                                          | 24 MHz IMO period jitter (RMS)                         | —     | —      | 100 | 400                          | —      | ps    |                                                                                                                                                             |
| t <sub>jitter</sub> _PLL <sup>[20]</sup> | 24 MHz IMO cycle-to-cycle jitter (RMS)                 | —     | —      | 200 | 800                          | —      | ps    |                                                                                                                                                             |
|                                          | 24 MHz IMO long term N cycle-to-cycle jitter (RMS)     | —     | —      | 300 | 1200                         | —      | ps    | N = 32                                                                                                                                                      |
|                                          | 24 MHz IMO period jitter (RMS)                         | —     | —      | 100 | 700                          | —      | ps    |                                                                                                                                                             |

#### Notes

15. **Errata:** When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see ["Errata"](#) on page 35.

16. Valid only for 4.75 V < Vdd < 5.25 V.

17. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.

18. 3.0 V < Vdd < 3.6 V.

19. Refer to the individual user module data sheets for information on maximum frequencies for user modules.

20. Refer to Cypress Jitter Specifications, [Understanding Datasheet Jitter Specifications for Cypress Timing Products](#) for more information.

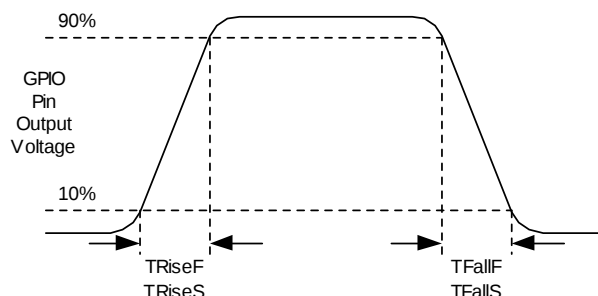
### AC GPIO Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 21. 5 V and 3.3 V AC GPIO Specifications**

| Symbol             | Description                                                      | Min | Typ | Max | Units | Notes                                                         |
|--------------------|------------------------------------------------------------------|-----|-----|-----|-------|---------------------------------------------------------------|
| $F_{\text{GPIO}}$  | GPIO operating frequency                                         | 0   | –   | 12  | MHz   | Normal Strong Mode                                            |
| $T_{\text{RiseF}}$ | Rise time, normal strong mode, $C_{\text{load}} = 50 \text{ pF}$ | 3   | –   | 18  | ns    | $V_{\text{dd}} = 4.5 \text{ to } 5.25 \text{ V}$ , 10% to 90% |
| $T_{\text{FallF}}$ | Fall time, normal strong mode, $C_{\text{load}} = 50 \text{ pF}$ | 2   | –   | 18  | ns    | $V_{\text{dd}} = 4.5 \text{ to } 5.25 \text{ V}$ , 10% to 90% |
| $T_{\text{RiseS}}$ | Rise time, slow strong mode, $C_{\text{load}} = 50 \text{ pF}$   | 7   | 27  | –   | ns    | $V_{\text{dd}} = 3 \text{ to } 5.25 \text{ V}$ , 10% to 90%   |
| $T_{\text{FallS}}$ | Fall time, slow strong mode, $C_{\text{load}} = 50 \text{ pF}$   | 7   | 22  | –   | ns    | $V_{\text{dd}} = 3 \text{ to } 5.25 \text{ V}$ , 10% to 90%   |

**Figure 6. GPIO Timing Diagram**



### AC Operational Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 22. AC Operational Amplifier Specifications**

| Symbol            | Description                          | Min | Typ | Max | Units | Notes                              |
|-------------------|--------------------------------------|-----|-----|-----|-------|------------------------------------|
| $T_{\text{COMP}}$ | Comparator Mode Response Time, 50 mV |     |     | 100 | ns    | $V_{\text{dd}} \geq 3.0 \text{ V}$ |

### AC Low Power Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 23. AC Low Power Comparator Specifications**

| Symbol            | Description       | Min | Typ | Max | Units         | Notes                                                                              |
|-------------------|-------------------|-----|-----|-----|---------------|------------------------------------------------------------------------------------|
| $T_{\text{RLPC}}$ | LPC response time | –   | –   | 50  | $\mu\text{s}$ | $\geq 50 \text{ mV}$ overdrive comparator reference set within $V_{\text{REFLPC}}$ |

### AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V, at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 24. AC Digital Block Specifications**

| Function          | Description                               | Min                | Typ | Max                  | Units | Notes                                                                                     |
|-------------------|-------------------------------------------|--------------------|-----|----------------------|-------|-------------------------------------------------------------------------------------------|
| All functions     | Block Input Clock Frequency               |                    |     |                      |       |                                                                                           |
|                   | Vdd $\geq$ 4.75 V                         | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd < 4.75 V                              | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
| Timer             | Input Clock Frequency                     |                    |     |                      |       |                                                                                           |
|                   | No Capture, Vdd $\geq$ 4.75 V             | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | No Capture, Vdd < 4.75 V                  | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | With Capture                              | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Capture Pulse Width                       | 50 <sup>[22]</sup> | –   | –                    | ns    |                                                                                           |
| Counter           | Input Clock Frequency                     |                    |     |                      |       |                                                                                           |
|                   | No Enable Input, Vdd $\geq$ 4.75 V        | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | No Enable Input, Vdd < 4.75 V             | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | With Enable Input                         | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Enable Input Pulse Width                  | 50 <sup>[22]</sup> | –   | –                    | ns    |                                                                                           |
| Dead Band         | Kill Pulse Width                          |                    |     |                      |       |                                                                                           |
|                   | Asynchronous Restart Mode                 | 20                 | –   | –                    | ns    |                                                                                           |
|                   | Synchronous Restart Mode                  | 50 <sup>[22]</sup> | –   | –                    | ns    |                                                                                           |
|                   | Disable Mode                              | 50 <sup>[22]</sup> | –   | –                    | ns    |                                                                                           |
|                   | Input Clock Frequency                     |                    |     |                      |       |                                                                                           |
|                   | Vdd $\geq$ 4.75 V                         | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd < 4.75 V                              | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
| CRCPRS (PRS Mode) | Input Clock Frequency                     |                    |     |                      |       |                                                                                           |
|                   | Vdd $\geq$ 4.75 V                         | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd < 4.75 V                              | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
| CRCPRS (CRC Mode) | Input Clock Frequency                     | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
| SPIM              | Input Clock Frequency                     | –                  | –   | 8.4 <sup>[21]</sup>  | MHz   | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS              | Input Clock (SCLK) Frequency              | –                  | –   | 4.2 <sup>[21]</sup>  | MHz   | The input clock is the SPI SCLK in SPIS mode.                                             |
|                   | Width of SS_Negated Between Transmissions | 50 <sup>[22]</sup> | –   | –                    | ns    |                                                                                           |
| Transmitter       | Input Clock Frequency                     |                    |     |                      |       | The baud rate is equal to the input clock frequency divided by 8.                         |
|                   | Vdd $\geq$ 4.75 V, 2 Stop Bits            | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd $\geq$ 4.75 V, 1 Stop Bit             | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd < 4.75 V                              | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
| Receiver          | Input Clock Frequency                     |                    |     |                      |       | The baud rate is equal to the input clock frequency divided by 8.                         |
|                   | Vdd $\geq$ 4.75 V, 2 Stop Bits            | –                  | –   | 50.4 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd $\geq$ 4.75 V, 1 Stop Bit             | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |
|                   | Vdd < 4.75 V                              | –                  | –   | 25.2 <sup>[21]</sup> | MHz   |                                                                                           |

#### Notes

21. Accuracy derived from IMO with appropriate trim for V<sub>DD</sub> range.

22. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

### AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 25. 5 V AC External Clock Specifications**

| Symbol              | Description            | Min   | Typ | Max  | Units | Notes |
|---------------------|------------------------|-------|-----|------|-------|-------|
| F <sub>OSCEXT</sub> | Frequency              | 0.093 | –   | 24.6 | MHz   |       |
| –                   | High Period            | 20.6  | –   | 5300 | ns    |       |
| –                   | Low Period             | 20.6  | –   | –    | ns    |       |
| –                   | Power Up IMO to Switch | 150   | –   | –    | μs    |       |

**Table 26. 3.3 V AC External Clock Specifications**

| Symbol              | Description                                     | Min   | Typ | Max  | Units | Notes                                                                                                                                                                                                               |
|---------------------|-------------------------------------------------|-------|-----|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F <sub>OSCEXT</sub> | Frequency with CPU Clock divide by 1            | 0.093 | –   | 12.3 | MHz   | Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.                                                 |
| F <sub>OSCEXT</sub> | Frequency with CPU Clock divide by 2 or greater | 0.186 | –   | 24.6 | MHz   | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| –                   | High Period with CPU Clock divide by 1          | 41.7  | –   | 5300 | ns    |                                                                                                                                                                                                                     |
| –                   | Low Period with CPU Clock divide by 1           | 41.7  | –   | –    | ns    |                                                                                                                                                                                                                     |
| –                   | Power Up IMO to Switch                          | 150   | –   | –    | μs    |                                                                                                                                                                                                                     |

### SAR10 ADC AC Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 27. SAR10 ADC AC Specifications**

| Symbol            | Description               | Min | Typ | Max | Units | Notes |
|-------------------|---------------------------|-----|-----|-----|-------|-------|
| Freq <sub>3</sub> | Input clock frequency 3 V | –   | –   | 2.7 | MHz   |       |
| Freq <sub>5</sub> | Input clock frequency 5 V | –   | –   | 2.7 | MHz   |       |

### AC Programming Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V, or 3.3 V at 25 °C and are for design guidance only.

**Table 28. AC Programming Specifications**

| Symbol                     | Description                                | Min | Typ | Max | Units | Notes                                             |
|----------------------------|--------------------------------------------|-----|-----|-----|-------|---------------------------------------------------|
| $T_{\text{RSCLK}}$         | Rise Time of SCLK                          | 1   | –   | 20  | ns    |                                                   |
| $T_{\text{FSCLK}}$         | Fall Time of SCLK                          | 1   | –   | 20  | ns    |                                                   |
| $T_{\text{SSCLK}}$         | Data Set up Time to Falling Edge of SCLK   | 40  | –   | –   | ns    |                                                   |
| $T_{\text{HSCLK}}$         | Data Hold Time from Falling Edge of SCLK   | 40  | –   | –   | ns    |                                                   |
| $F_{\text{SCLK}}$          | Frequency of SCLK                          | 0   | –   | 8   | MHz   |                                                   |
| $F_{\text{SCLK3}}$         | Frequency of SCLK3                         | 0   | –   | 6   | MHz   | $V_{\text{DD}} < 3.6 \text{ V}$                   |
| $T_{\text{ERASEB}}$        | Flash Erase Time (Block)                   | –   | 10  | –   | ms    |                                                   |
| $T_{\text{WRITE}}$         | Flash Block Write Time                     | –   | 40  | –   | ms    |                                                   |
| $T_{\text{DSCLK}}$         | Data Out Delay from Falling Edge of SCLK   | –   | –   | 55  | ns    | $3.6 < V_{\text{DD}}$ ; at 30 pF Load             |
| $T_{\text{DSCLK3}}$        | Data Out Delay from Falling Edge of SCLK   | –   | –   | 65  | ns    | $3.0 \leq V_{\text{DD}} \leq 3.6$ ; at 30 pF Load |
| $T_{\text{ERASEALL}}$      | Flash Erase Time (Bulk)                    | –   | 40  | –   | ms    |                                                   |
| $T_{\text{PROGRAM\_HOT}}$  | Flash Block Erase + Flash Block Write Time | –   | –   | 100 | ms    |                                                   |
| $T_{\text{PROGRAM\_COLD}}$ | Flash Block Erase + Flash Block Write Time | –   | –   | 200 | ms    |                                                   |

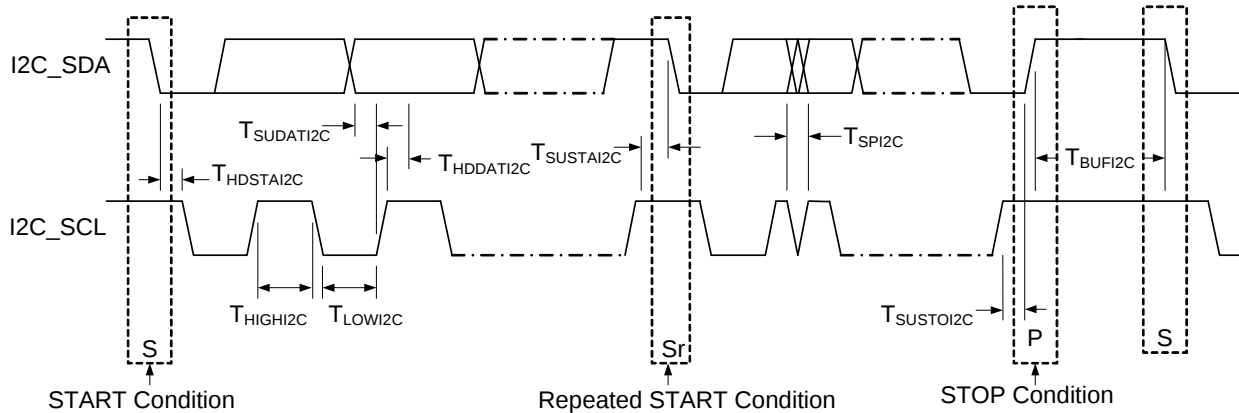
## AC I<sup>2</sup>C Specifications

Table 29 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , and 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 29. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins for  $V_{DD} \geq 3.0\text{ V}$**

| Symbol          | Description                                                                                  | Standard Mode |     | Fast Mode           |     | Units         | Notes |
|-----------------|----------------------------------------------------------------------------------------------|---------------|-----|---------------------|-----|---------------|-------|
|                 |                                                                                              | Min           | Max | Min                 | Max |               |       |
| $F_{SCL I2C}$   | SCL Clock Frequency                                                                          | 0             | 100 | 0                   | 400 | kHz           |       |
| $T_{HDSTA I2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0           | –   | 0.6                 | –   | $\mu\text{s}$ |       |
| $T_{LOW I2C}$   | LOW Period of the SCL Clock                                                                  | 4.7           | –   | 1.3                 | –   | $\mu\text{s}$ |       |
| $T_{HIGH I2C}$  | HIGH Period of the SCL Clock                                                                 | 4.0           | –   | 0.6                 | –   | $\mu\text{s}$ |       |
| $T_{SUSTA I2C}$ | Setup Time for a Repeated START Condition                                                    | 4.7           | –   | 0.6                 | –   | $\mu\text{s}$ |       |
| $T_{HDDAT I2C}$ | Data Hold Time                                                                               | 0             | –   | 0                   | –   | $\mu\text{s}$ |       |
| $T_{SUDAT I2C}$ | Data Setup Time                                                                              | 250           | –   | 100 <sup>[23]</sup> | –   | ns            |       |
| $T_{SUSTOI2C}$  | Setup Time for STOP Condition                                                                | 4.0           | –   | 0.6                 | –   | $\mu\text{s}$ |       |
| $T_{BUFI2C}$    | Bus Free Time Between a STOP and START Condition                                             | 4.7           | –   | 1.3                 | –   | $\mu\text{s}$ |       |
| $T_{SPI2C}$     | Pulse Width of spikes are suppressed by the Input Filter                                     | –             | –   | 0                   | 50  | ns            |       |

**Figure 7. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**

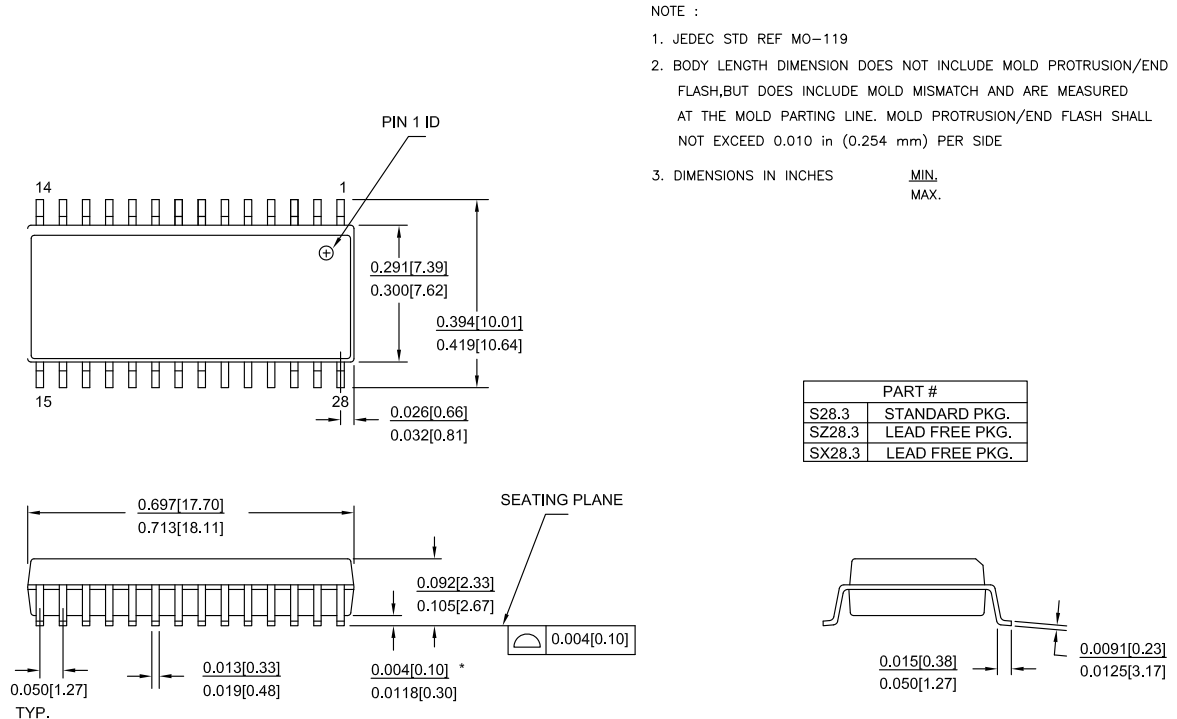


### Note

23. A Fast-Mode I<sup>2</sup>C-bus device may be used in a Standard-Mode I<sup>2</sup>C-bus system, but the requirement  $T_{SUDAT I2C} \geq 250\text{ ns}$  must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{\text{max}} + T_{SUDAT I2C} = 1000 + 250 = 1250\text{ ns}$  (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

## Packaging Information

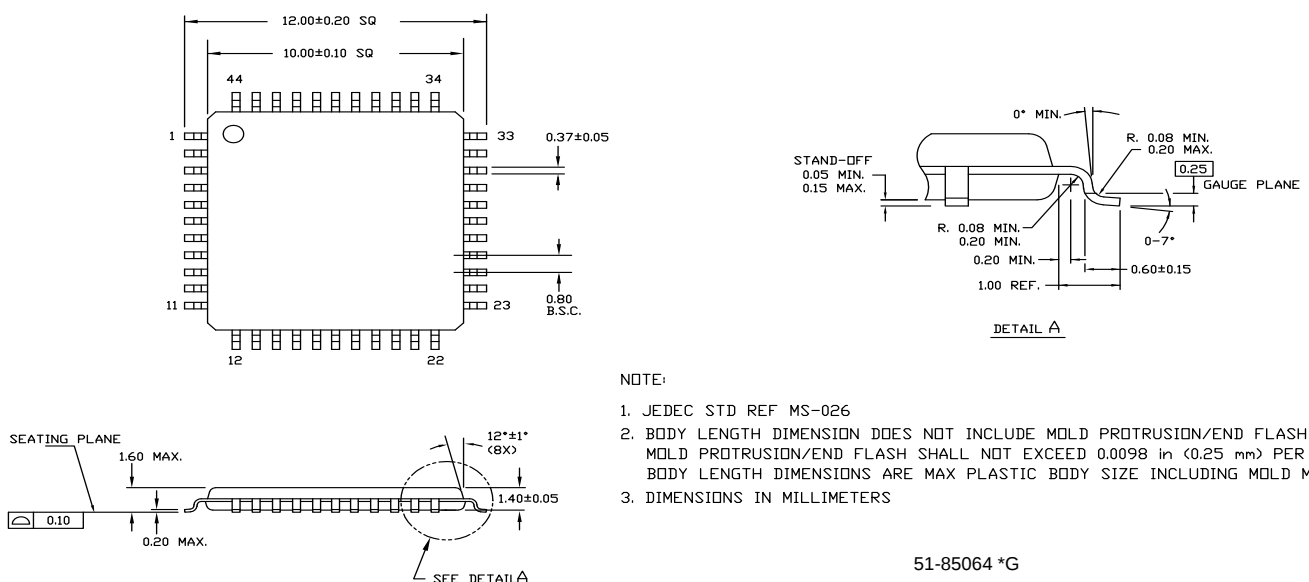
**Figure 8. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026**



51-85026 \*H

**Figure 9. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064**

**44 Lead Thin Plastic Quad Flatpack 10 X 10 X 1.4mm**



51-85064 \*G

## Thermal Impedances

**Table 30. Thermal Impedances per Package**

| Package     | Typical $\theta_{JA}$ <sup>[25]</sup> |
|-------------|---------------------------------------|
| 28-pin SOIC | 68 °C/W                               |
| 44-pin TQFP | 61 °C/W                               |

## Solder Reflow Specifications

Table 31 shows the solder reflow temperature limits that must not be exceeded.

**Table 31. Solder Reflow Specifications**

| Package     | Maximum Peak Temperature ( $T_C$ ) | Maximum Time above $T_C - 5\text{ °C}$ |
|-------------|------------------------------------|----------------------------------------|
| 28-pin SOIC | 260 °C                             | 30 seconds                             |
| 44-pin TQFP | 260 °C                             | 30 seconds                             |

## Ordering Information

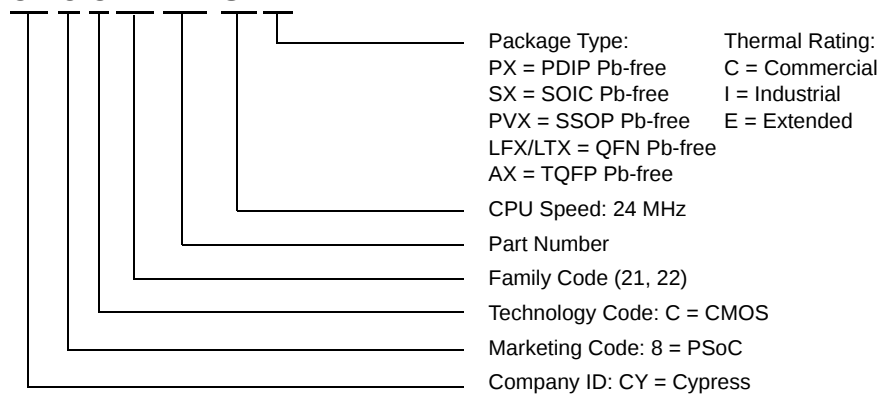
The following table lists the key package features and ordering codes of this PSoC device family.

**Table 32. PSoC Device Family Key Features and Ordering Information**

| Package                     | Ordering Code    | Flash (Kbytes) | RAM (Bytes) | Temperature Range | Digital Blocks (Rows of 4) | Analog Blocks (Columns of 3) | Digital I/O Pins | Analog Inputs      | Analog Outputs | XRES Pin |
|-----------------------------|------------------|----------------|-------------|-------------------|----------------------------|------------------------------|------------------|--------------------|----------------|----------|
| 28-pin SOIC                 | CY8C21345-24SXI  | 8              | 512B        | -40 °C to +85 °C  | 4                          | 6                            | 24               | 24 <sup>[24]</sup> | 0              | Y        |
| 28-pin SOIC (Tape and Reel) | CY8C21345-24SXIT | 8              | 512B        | -40 °C to +85 °C  | 4                          | 6                            | 24               | 24 <sup>[24]</sup> | 0              | Y        |
| 28-pin SOIC                 | CY8C22345-24SXI  | 16             | 1K          | -40 °C to +85 °C  | 8                          | 6                            | 24               | 24 <sup>[24]</sup> | 0              | Y        |
| 28-pin SOIC (Tape and Reel) | CY8C22345-24SXIT | 16             | 1K          | -40 °C to +85 °C  | 8                          | 6                            | 24               | 24 <sup>[24]</sup> | 0              | Y        |
| 44-pin TQFP                 | CY8C22545-24AXI  | 16             | 1K          | -40 °C to +85 °C  | 8                          | 6                            | 38               | 38 <sup>[24]</sup> | 0              | Y        |
| 44-pin TQFP (Tape and Reel) | CY8C22545-24AXIT | 16             | 1K          | -40 °C to +85 °C  | 8                          | 6                            | 38               | 38 <sup>[24]</sup> | 0              | Y        |

## Ordering Code Definitions

CY 8 C 2x xxx-SPxx



### Note

24. Ten direct inputs.

25.  $T_J = T_A + \text{POWER} \times \theta_{JA}$

## Acronyms

Table 33 lists the acronyms that are used in this document.

**Table 33. Acronyms Used in this Datasheet**

| Acronym | Description                                         | Acronym | Description                                   |
|---------|-----------------------------------------------------|---------|-----------------------------------------------|
| AC      | alternating current                                 | MAC     | multiply-accumulate                           |
| ADC     | analog-to-digital converter                         | MCU     | microcontroller unit                          |
| API     | application programming interface                   | MIPS    | million instructions per second               |
| CMOS    | complementary metal oxide semiconductor             | PCB     | printed circuit board                         |
| CPU     | central processing unit                             | PGA     | programmable gain amplifier                   |
| CRC     | cyclic redundancy check                             | PLL     | phase-locked loop                             |
| CSD     | CapSense sigma delta                                | POR     | power on reset                                |
| CT      | continuous time                                     | PPOR    | precision power on reset                      |
| DAC     | digital-to-analog converter                         | PRS     | pseudo-random sequence                        |
| DC      | direct current                                      | PSoC®   | Programmable System-on-Chip                   |
| DNL     | differential nonlinearity                           | PWM     | pulse width modulator                         |
| ECO     | external crystal oscillator                         | QFN     | quad flat no leads                            |
| EEPROM  | electrically erasable programmable read-only memory | RTC     | real time clock                               |
| FSK     | frequency-shift keying                              | SAR     | successive approximation                      |
| GPIO    | general-purpose I/O                                 | SC      | switched capacitor                            |
| I/O     | input/output                                        | SLIMO   | slow IMO                                      |
| ICE     | in-circuit emulator                                 | SOIC    | small-outline integrated circuit              |
| IDE     | integrated development environment                  | SPI™    | serial peripheral interface                   |
| IDAC    | current DAC                                         | SRAM    | static random access memory                   |
| ILO     | internal low speed oscillator                       | SROM    | supervisory read only memory                  |
| IMO     | internal main oscillator                            | SSOP    | shrink small-outline package                  |
| INL     | integral nonlinearity                               | TQFP    | thin quad flat pack                           |
| IrDA    | infrared data association                           | UART    | universal asynchronous receiver / transmitter |
| ISSP    | in-system serial programming                        | USB     | universal serial bus                          |
| LPC     | low power comparator                                | WDT     | watchdog timer                                |
| LSB     | least-significant bit                               | XRES    | external reset                                |
| LVD     | low voltage detect                                  |         |                                               |

## Reference Documents

CY8C22x45 and CY8C21345 PSoC® Programmable System-on-Chip™ [Technical Reference Manual \(TRM\)](#) (001-48461)

[Design Aids – Reading and Writing PSoC® Flash – AN2015](#) (001-40459)

[Understanding Datasheet Jitter Specifications for Cypress Timing Products](#)

## Document Conventions

### Units of Measure

Table 34 lists the units of measures.

**Table 34. Units of Measure**

| Symbol     | Unit of Measure       | Symbol  | Unit of Measure    |
|------------|-----------------------|---------|--------------------|
| kB         | 1024 bytes            | mV      | millivolts         |
| °C         | degree Celsius        | nA      | nanoampere         |
| kHz        | kilohertz             | ns      | nanosecond         |
| k $\Omega$ | kilohm                | W       | ohm                |
| LSB        | least significant bit | %       | percent            |
| MHz        | megahertz             | pF      | picofarad          |
| $\mu$ A    | microampere           | ps      | picosecond         |
| $\mu$ s    | microsecond           | sps     | samples per second |
| $\mu$ V    | microvolt             | pA      | pikoampere         |
| mA         | milliampere           | V       | volts              |
| mm         | millimeter            | $\mu$ W | microwatts         |
| ms         | millisecond           | W       | watt               |

### Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

### Glossary

|                                         |                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| active high                             | <ol style="list-style-type: none"> <li>1. A logic signal having its asserted state as the logic 1 state.</li> <li>2. A logic signal having the logic 1 state as the higher voltage of the two states.</li> </ol>                                                                                                                                        |
| analog blocks                           | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.                                                                                                                                     |
| analog-to-digital (ADC)                 | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.                                                                                                                                  |
| API (Application Programming Interface) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.                                                                                              |
| asynchronous                            | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.                                                                                                                                                                                                                                                        |
| bandgap reference                       | A stable voltage reference design that matches the positive temperature coefficient of $V_T$ with the negative temperature coefficient of $V_{BE}$ , to produce a zero temperature coefficient (ideally) reference.                                                                                                                                     |
| bandwidth                               | <ol style="list-style-type: none"> <li>1. The frequency range of a message or information processing system measured in hertz.</li> <li>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.</li> </ol> |

## Glossary (continued)

|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bias                          | <ol style="list-style-type: none"> <li>1. A systematic deviation of a value from a reference value.</li> <li>2. The amount by which the average of a set of values departs from a reference value.</li> <li>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.</li> </ol>                                                                                                                                                               |
| block                         | <ol style="list-style-type: none"> <li>1. A functional unit that performs a single function, such as an oscillator.</li> <li>2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.</li> </ol>                                                                                                                                                                                                                                                 |
| buffer                        | <ol style="list-style-type: none"> <li>1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.</li> <li>2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.</li> <li>3. An amplifier used to lower the output impedance of a system.</li> </ol> |
| bus                           | <ol style="list-style-type: none"> <li>1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.</li> <li>2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].</li> <li>3. One or more conductors that serve as a common connection for a group of related devices.</li> </ol>                                                                                |
| clock                         | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.                                                                                                                                                                                                                                                                                                                                                                            |
| comparator                    | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.                                                                                                                                                                                                                                                                                                                                                                        |
| compiler                      | A program that translates a high level language, such as C, into machine language.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| configuration space           | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| crystal oscillator            | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.                                                                                                                                                                                                                                                                                                                                       |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.                                                                                                                                                                                                                                                                                                             |
| data bus                      | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.                                                                                                                                                                                                                                                                                                 |
| debugger                      | A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.                                                                                                                                                                                                                                                                                   |
| dead band                     | A period of time when neither of two or more signals are in their active state or in transition.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| digital blocks                | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.                                                                                                                                                                                                                                                                                                                                                                           |
| digital-to-analog (DAC)       | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.                                                                                                                                                                                                                                                                                                                                                                   |

## Glossary (continued)

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| duty cycle                      | The relationship of a clock period high time to its low time, expressed as a percent.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| emulator                        | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| external reset (XRES)           | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| flash                           | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.                                                                                                                                                                                                                                                                                                                                                             |
| Flash block                     | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| frequency                       | The number of cycles or events per unit of time, for a periodic function.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| gain                            | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| I <sup>2</sup> C                | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I <sup>2</sup> C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I <sup>2</sup> C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE                             | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).                                                                                                                                                                                                                                                                                                                                                                                                                     |
| input/output (I/O)              | A device that introduces data into or extracts data from a system.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| interrupt                       | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.                                                                                                                                                                                                                                                                                                                                                                                                                   |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.                                                                                                                                                                                                                                                       |
| jitter                          | <ol style="list-style-type: none"> <li>1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.</li> <li>2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.</li> </ol>                                                                                                                                                                               |
| low-voltage detect (LVD)        | A circuit that senses V <sub>dd</sub> and provides an interrupt to the system when V <sub>dd</sub> falls below a selected threshold.                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| M8C                             | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| master device                   | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the <b>slave device</b> .                                                                                                                                                                                                                                                                                         |

## Glossary (continued)

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| microcontroller             | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal                | The reference to a circuit containing both analog and digital techniques and components.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| modulator                   | A device that imposes a signal on a carrier.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| noise                       | <ol style="list-style-type: none"> <li>1. A disturbance that affects a signal and that may distort the information carried by the signal.</li> <li>2. The random variations of one or more characteristics of any entity such as voltage, current, or data.</li> </ol>                                                                                                                                                                                                                                              |
| oscillator                  | A circuit that may be crystal controlled and is used to generate a clock frequency.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| parity                      | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).                                                                                                                                                                                                                                                                                                         |
| phase-locked loop (PLL)     | An electronic circuit that controls an <b>oscillator</b> so that it maintains a constant phase angle relative to a reference signal.                                                                                                                                                                                                                                                                                                                                                                                |
| pinouts                     | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.                                                                                                                                                                                          |
| port                        | A group of pins, usually eight.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| power on reset (POR)        | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.                                                                                                                                                                                                                                                                                                                                                                                       |
| PSoC®                       | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.                                                                                                                                                                                                                                                                                                                                                                                                 |
| PSoC Designer™              | The software for Cypress' Programmable System-on-Chip technology.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RAM                         | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.                                                                                                                                                                                                                                                                                                                                                                                          |
| register                    | A storage device with a specific capacity, such as a bit or byte.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| reset                       | A means of bringing a system back to a know state. See hardware reset and software reset.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ROM                         | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.                                                                                                                                                                                                                                                                                                                                                                                          |
| serial                      | <ol style="list-style-type: none"> <li>1. Pertaining to a process in which all events occur one after the other.</li> <li>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.</li> </ol>                                                                                                                                                                                                                                                     |
| settling time               | The time it takes for an output signal or value to stabilize after the input has changed from one value to another.                                                                                                                                                                                                                                                                                                                                                                                                 |

## Glossary (continued)

|                 |                                                                                                                                                                                                                                                                                                                                                     |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| shift register  | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.                                                                                                                                                                                                                                     |
| slave device    | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM            | An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.                                     |
| SROM            | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.                                                                                                           |
| stop bit        | A signal following a character or block that prepares the receiving device to receive the next character or block.                                                                                                                                                                                                                                  |
| synchronous     | <ol style="list-style-type: none"> <li>1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.</li> <li>2. A system whose operation is synchronized by a clock signal.</li> </ol>                                                                                                                    |
| tri-state       | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.                                                                         |
| UART            | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.                                                                                                                                                                                                                                     |
| user modules    | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level <b>API (Application Programming Interface)</b> for the peripheral function.                                                                            |
| user space      | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.                                                                         |
| V <sub>DD</sub> | A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.                                                                                                                                                                                                                                        |
| V <sub>SS</sub> | A name for a power net meaning “voltage source.” The most negative power supply signal.                                                                                                                                                                                                                                                             |
| watchdog timer  | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.                                                                                                                                                                                                                                 |

## Errata

This section describes the errata for the CY8C21x45, CY8C22x45 family of PSoC devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

| Part Number | Device Characteristics |
|-------------|------------------------|
| CY8C21345   | All Variants           |
| CY8C22345   | All Variants           |
| CY8C22545   | All Variants           |

### CY8C21x45, CY8C22x45 Qualification Status

Product Status: In Production

### Errata Summary

The following table defines the errata applicable for this PSoC family device.

| Items                                                                         | Part Number                               | Silicon Revision | Fix Status                               |
|-------------------------------------------------------------------------------|-------------------------------------------|------------------|------------------------------------------|
| 1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC | All CY8C21x45, CY8C22x45 devices affected | All              | Silicon fix not planned. Use workaround. |
| 2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes | All CY8C21x45, CY8C22x45 devices affected | All              | Silicon fix not planned. Use workaround. |

#### 1. Free Running Nonstop Reading cause 7 LSB Pseudo Code Variation in SAR10ADC

##### ■ Problem Definition

In free running mode, there can be a variation of up to 7 LSB in the digital output of SAR10 ADC.

##### ■ Parameters Affected

Code Variation. This is not a specified parameter.

It is defined as the number of unique output codes generated by the ADC for a given constant input voltage, in addition to the correct code. For example, for an input voltage of 2.000 V, the expected code is 190hex and the ADC generates three codes: 191hex, 190hex, and 192hex. The code variation is 2 LSB.

##### ■ Trigger Condition(S)

SAR10 ADC is configured in the free running mode. When ADC is operated in free running mode, for a constant input voltage output of ADC can have a variation of up to 7LSB. This can be resolved by using the averaging technique or by disabling the free running mode before reading the data and enabling again after reading the data.

##### ■ Scope of Impact

Inaccurate output is possible.

##### ■ Workaround

This issue can be averted by using one or both of the following workarounds. Consult a Cypress representative for additional assistance.

- Use the averaging technique. That is, take multiple samples of the input, and use a digital averaging filter.
- Disable the free running mode before reading data out, and enable the free running mode after completing the read operation.

##### ■ Fix Status

No silicon fix is planned.

## 2. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

### ■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

### ■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is  $\pm 5\%$ .

### ■ Trigger Condition(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of  $\pm 2.5\%$  when operated beyond the temperature range of 0 to +70 °C.

### ■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

### ■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

### ■ Fix Status

The cause of this problem and its solution has been identified. No silicon fix is planned to correct the deficiency in silicon.

## Document History Page

| Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip<br>Document Number: 001-43084 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                       | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| **                                                                                                             | 2251907 | PMP / AESA      | See ECN         | New data sheet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *A                                                                                                             | 2506377 | EIJ / AESA      | See ECN         | Changed data sheet status to "Preliminary". Changed part numbers to CY8C22x45. Updated data sheet template.<br>Added 56-Pin OCD information. Added: "You must put filters on intended ADC input channels for anti-aliasing. This ensures that any out-of-band content is not folded into the Input Signal Band." To Section <a href="#">Analog System on page 4</a> .<br>Corrected Minimum Electro Static Discharge Voltage in <a href="#">Table 7 on page 14</a> .                                                                                                                                     |
| *B                                                                                                             | 2558750 | PMP / AESA      | 08/28/2008      | Updated <a href="#">Features on page 1</a> , <a href="#">PSoC Core on page 3</a> , <a href="#">Analog System on page 4</a> .<br>Changed DBB to DBC, and DCB to DCC in Register Tables <a href="#">Table 5 on page 11</a> and <a href="#">Table 6 on page 12</a> .<br>Removed INL at 8 bit reference in <a href="#">Table 15 on page 18</a> .<br>Changed IDD3 value <a href="#">Table 17 on page 19</a> Typ:3.3 mA, Max 6 mA<br>Added "3.0 V < Vdd < 3.6 V and -40C < T <sub>A</sub> < 85C, IMO can guarantee 5% accuracy only" to <a href="#">Table 20 on page 21</a> .<br>Updated data sheet template. |
| *C                                                                                                             | 2606793 | NUQ / AESA      | 11/19/2008      | Updated data sheet status to "Final". Updated block diagram on page 1.<br>Removed CY8C22045 56-Pin OCD information. Added part numbers CY8C21345, CY8C22345, and CY8C22545. For more details, see CDT 31271.                                                                                                                                                                                                                                                                                                                                                                                            |
| *D                                                                                                             | 2615697 | PMP / AESA      | 12/03/2008      | Confirmed CY8C22345 and CY8C21345 have same pinout on page 8.<br>Confirmed that IMO has 5% accuracy in <a href="#">Table 20 on page 21</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| *E                                                                                                             | 2631733 | PMP / PYRS      | 01/07/2009      | Updated Table 16. SAR10 ADC DC Specifications and Table 29 AC Programming Specifications. Title changed to "CY8C21345, CY8C22345, CY8C22545 PSoC® Programmable System-on-Chip™"                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *F                                                                                                             | 2648800 | JHU / AESA      | 01/28/2009      | Updated INL, DNL information in <a href="#">Table 15 on page 18</a> , <a href="#">Development Tools on page 6</a> , and T <sub>DSCLK</sub> parameter in <a href="#">Table 28 on page 25</a> .                                                                                                                                                                                                                                                                                                                                                                                                           |
| *G                                                                                                             | 2658078 | HMI / AESA      | 02/11/2009      | Updated section <a href="#">Features on page 1</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| *H                                                                                                             | 2667311 | JHU / AESA      | 03/16/2009      | Added parameter "F <sub>32KU</sub> " and added Min% and Max % to parameter "F <sub>IMO6</sub> " in <a href="#">Table 20 on page 21</a> , according to updated SLIMO spec.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| *I                                                                                                             | 2748976 | JZHU / PYRS     | 08/06/2009      | Updated F <sub>32K1</sub> max rating in <a href="#">Table 20 on page 21</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| *J                                                                                                             | 2786560 | JZHU            | 10/23/2009      | Added DC <sub>ILO</sub> , T <sub>ERASEALL</sub> , T <sub>PROGRAM_HOT</sub> , T <sub>PROGRAM_COLD</sub> , SR <sub>POWERUP</sub> , I <sub>OH</sub> , and I <sub>OL</sub> parameters.<br>Added Tape and Reel parts in Ordering Information table                                                                                                                                                                                                                                                                                                                                                           |
| *K                                                                                                             | 2901653 | NJF             | 03/30/2010      | Updated <a href="#">PSoC Designer Software Subsystems</a> .<br>Added T <sub>BAKETEMP</sub> and T <sub>BAKETIME</sub> parameters in <a href="#">Absolute Maximum Ratings Modified Note 6 on page 17</a> .<br>Added F <sub>OUT48M</sub> parameter in <a href="#">5 V and 3.3 V AC Chip-Level Specifications</a> .<br>Removed AC Analog Mux Bus Specifications.<br>Updated <a href="#">Ordering Code Definitions</a> .<br>Updated links in <a href="#">Sales, Solutions, and Legal Information</a> .                                                                                                       |
| *L                                                                                                             | 3114978 | NJF             | 12/19/10        | Added DC I <sup>2</sup> C Specifications.<br>Added T <sub>jitter</sub> IMO specification, removed existing jitter specifications.<br>Updated DC Programming Specifications.<br>Updated AC Digital Block Specifications.<br>Updated I <sup>2</sup> C Timing Diagram.<br>Added Solder Reflow Peak Temperature table.<br>Updated Units of Measure, Acronyms, Glossary, and References sections.                                                                                                                                                                                                            |

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| Document Title: CY8C21345/CY8C22345/CY8C22545, PSoC® Programmable System-on-Chip<br>Document Number: 001-43084 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                       | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| *M                                                                                                             | 3231771 | BOBH / ECU      | 04/18/11        | Updated analog inputs column in <a href="#">Table 32 on page 28</a> and included reference to Note 24.<br>Updated the following sections: <a href="#">Getting Started</a> , <a href="#">Development Tools</a> , and <a href="#">Designing with PSoC Designer</a> as all the System level designs have been de-emphasized.<br>Updated <a href="#">Table 31, "Solder Reflow Specifications,"</a> on page 28.<br>Updated package diagrams:<br>51-85026 to *F<br>51-85064 to *E                                                                                                                                                                                                                                                                                                                                           |
| *N                                                                                                             | 3578757 | PMAD            | 04/11/2012      | Removed reference to AN2012 as the document is in obsolete status.<br>Updated template.<br>No technical updates. Completing sunset review.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| *O                                                                                                             | 3598230 | LURE / XZNG     | 04/24/2012      | Changed the PWM description string from "8- to 32-bit" to "8- and 16-bit".                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| *P                                                                                                             | 3915358 | SAMP            | 02/27/2013      | Updated <a href="#">Electrical Specifications</a> (Updated <a href="#">DC Electrical Characteristics</a> (Updated <a href="#">DC GPIO Specifications</a> (Updated <a href="#">Table 10</a> (Updated Notes for V <sub>OH</sub> and V <sub>OL</sub> parameters))))).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| *Q                                                                                                             | 3959550 | SAMP            | 04/09/2013      | Added <a href="#">Errata</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| *R                                                                                                             | 4081559 | PMAD            | 07/30/2013      | Added Errata footnotes (Note 1, 11, 15).<br><br>Updated <a href="#">Features</a> :<br>Added Note 1 and referred the same note in $\pm 5\%$ under "Precision, programmable clocking".<br><br>Updated <a href="#">Electrical Specifications</a> :<br>Updated <a href="#">DC Electrical Characteristics</a> :<br>Updated <a href="#">SAR10 ADC DC Specifications</a> :<br>Added Note 11 and referred the same note in SPS parameter.<br>Updated <a href="#">AC Electrical Characteristics</a> :<br>Updated <a href="#">AC Chip Level Specifications</a> :<br>Added Note 15 and referred the same note in F <sub>IMO24</sub> parameter.<br><br>Updated <a href="#">Packaging Information</a> :<br>spec 51-85026 – Changed revision from *F to *G.<br><br>Updated <a href="#">Errata</a> .<br><br>Updated in new template. |
| *S                                                                                                             | 4416752 | RAHU            | 06/26/2014      | Updated <a href="#">Pinouts</a> :<br>Updated <a href="#">CY8C22345, CY8C21345 28-pin SOIC</a> :<br>Updated Note 6.<br>Updated <a href="#">CY8C22545 44-pin TQFP</a> :<br>Updated <a href="#">Table 3</a> :<br>Replaced "TC" with "ISSP" in description of pin 16 and pin 18.<br><br>Updated <a href="#">Packaging Information</a> :<br>spec 51-85026 – Changed revision from *G to *H.<br>spec 51-85064 – Changed revision from *E to *F.                                                                                                                                                                                                                                                                                                                                                                             |

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|----------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                       | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *T                                                                                                             | 4473295 | MSUR            | 08/13/2014      | Updated <a href="#">Getting Started</a> :<br>Updated description.<br>Updated <a href="#">Application Notes</a> :<br>Updated description.<br>Updated <a href="#">Development Kits</a> :<br>Updated description.<br><br>Updated <a href="#">Electrical Specifications</a> :<br>Updated <a href="#">DC Electrical Characteristics</a> :<br>Updated <a href="#">DC GPIO Specifications</a> :<br>Updated <a href="#">Table 10</a> :<br>Added Note 9 and referred the same note in <a href="#">Table 10</a> .<br>Updated <a href="#">AC Electrical Characteristics</a> :<br>Updated <a href="#">AC Chip Level Specifications</a> :<br>Updated <a href="#">Table 20</a> :<br>Renamed T <sub>XRST</sub> as T <sub>XRES</sub> and added details in “Notes” column for the same parameter.<br>Removed F <sub>OUT48M</sub> parameter and its details. |
| *U                                                                                                             | 4515350 | MSUR            | 09/26/2014      | Updated <a href="#">Electrical Specifications</a> :<br>Updated <a href="#">DC Electrical Characteristics</a> :<br>Added <a href="#">DC IDAC Specifications</a> .<br>Updated <a href="#">DC GPIO Specifications</a> :<br>Updated <a href="#">Table 10</a> :<br>Removed reference of Note 9 from table caption.<br>Referred Note 9 in R <sub>PD</sub> , V <sub>IL</sub> , V <sub>IH</sub> , V <sub>H</sub> , I <sub>IL</sub> , C <sub>IN</sub> parameters.                                                                                                                                                                                                                                                                                                                                                                                   |
| *V                                                                                                             | 4599794 | DIMA            | 12/17/2014      | Updated <a href="#">Pinouts</a> :<br>Updated <a href="#">CY8C22345, CY8C21345 28-pin SOIC</a> :<br>Updated <a href="#">Table 2</a> :<br>Added Note 5 and referred the same note in description of pin 9 and pin 14.<br>Updated <a href="#">CY8C22545 44-pin TQFP</a> :<br>Updated <a href="#">Table 3</a> :<br>Added Note 7 and referred the same note in caption of <a href="#">Table 3</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| *W                                                                                                             | 5733894 | DIMA            | 05/12/2017      | Updated <a href="#">Packaging Information</a><br>Changed Spec 51-85064 from *F to *G.<br><br>Updated Cypress Logo and Copyright.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

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