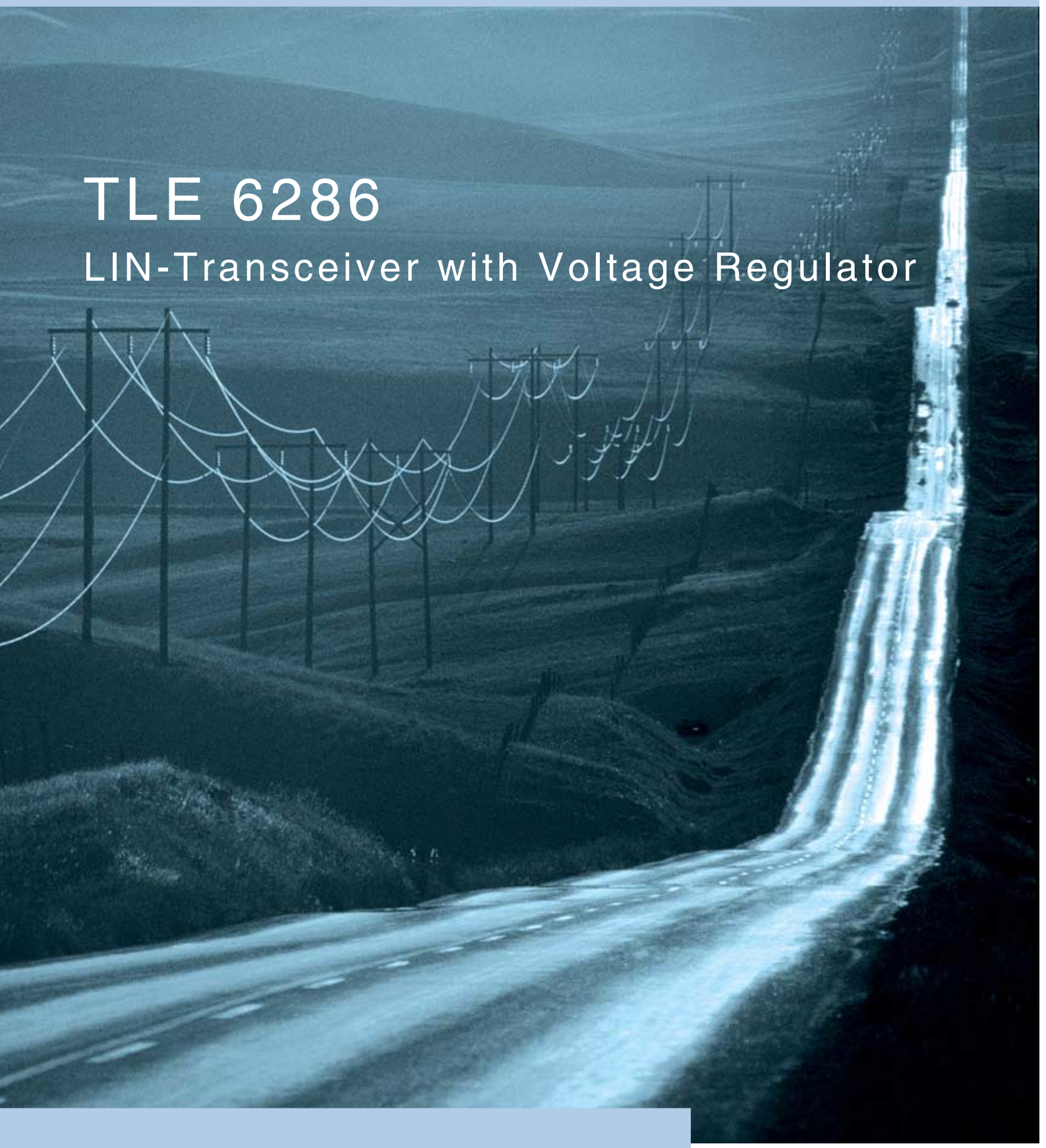
Preliminary Data Sheet, Rev. 1.20, April 2004



TLE 6286

LIN-Transceiver with Voltage Regulator

Automotive Power

Infineon technologies

Never stop thinking.

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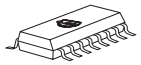
Features



P-DSO-16-9, -11

- Single-wire transceiver, suitable for **LIN** protocol
- Transmission rate up to 20 kBaud
- Compatible to LIN specification 1.3, 2.0
- Compatible to ISO 9141 functions
- Low current consumption in sleep mode
- Control output for voltage regulator
- LIN bus, short circuit proof to ground and battery
- Integrated 5V Low drop voltage regulator
- Output voltage tolerance ≤ ±2%
- 200 mA output current capability
- Watchdog
- Wide temperature range
- Overtemperature protection
- Suitable for use in automotive electronics

Description

The TLE 6286 is a single-wire transceiver with a 5V voltage regulator. It is a chip-by-chip integrated circuit in a P-DSO-16-11 package. It works as an interface between the protocol controller and the physical bus. The TLE 6286 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

To reduce the current consumption the TLE 6286 offers a sleep operation mode. In this setup a voltage regulator can be controlled by the LIN Transceiver to minimize the current consumption of the whole application. The on-chip voltage regulator is designed for this application but it is also possible to use an external voltage regulator. A wake-up caused by a message on the bus enables the voltage regulator and sets the RxD output low until the device is switched to normal operation mode.

The TLE 6286 is designed to withstand the severe conditions of automotive applications.

Type	Ordering Code	Package
TLE 6286 G	on request	P-DSO-16-11

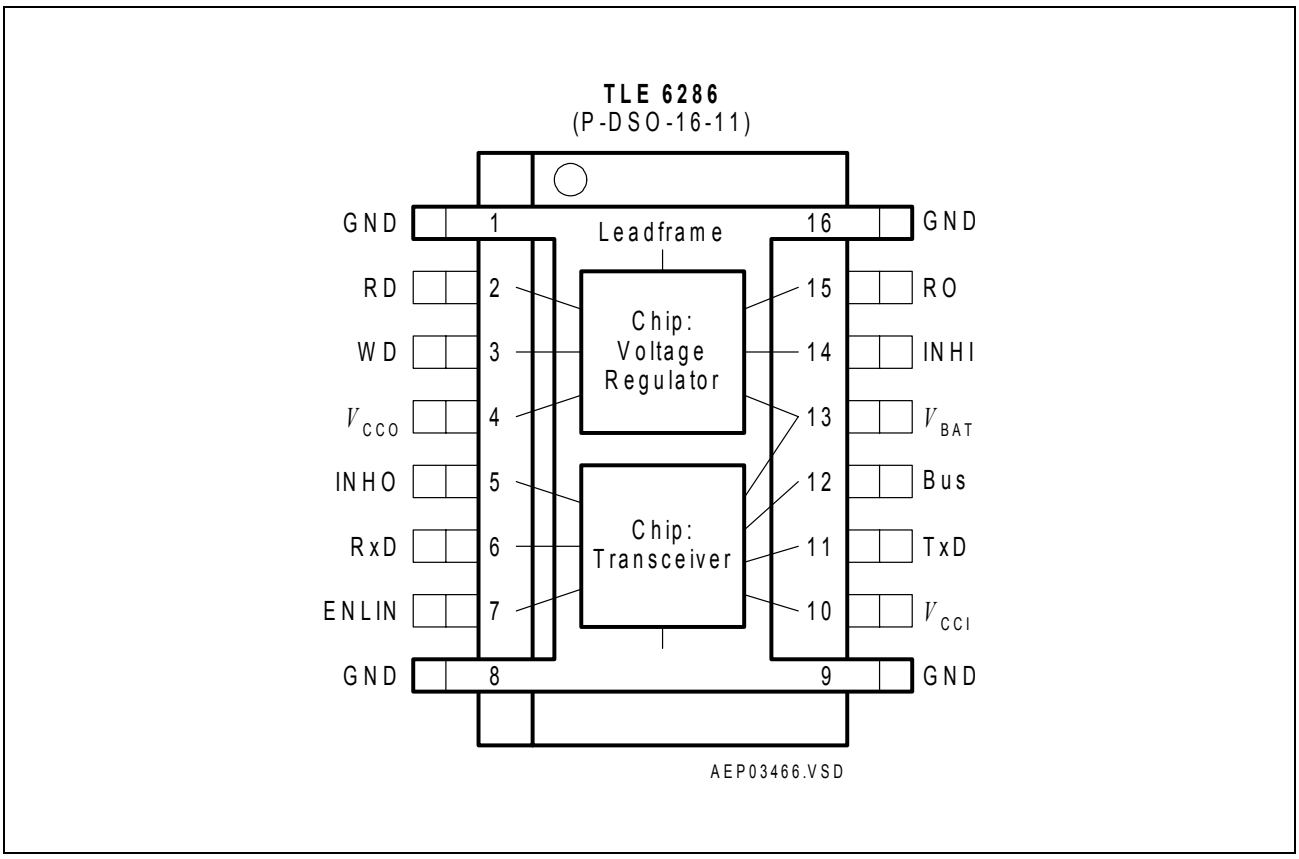


Figure 1 **Pin Configuration** (top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1, 8, 9, 16	GND	**Ground;** place to cooling tabs to improve thermal behavior
2	RD	**Reset delay;** connected to ground with external delay capacitor
3	WD	**Watchdog;** rising-edge triggered, for monitoring a microcontroller
4	V_{CCO}	**5-V Output;** connected to GND with 22 µF capacitor, ESR < 3 Ω at 10kHz
5	INHO	**Inhibit LIN Output;** to control a voltage regulator
6	RxD	**Receive Data Output;** internal pull-up, LOW in dominate state
7	ENLIN	**Enable LIN Input;** integrated 30 kΩ pull-down, transceiver in normal operation mode when HIGH
10	V_{CCI}	**5-V Supply Input;** V_{CC} input to supply the LIN transceiver
11	TxD	**Transmit Data Input;** internal pull-up, LOW in dominant state
12	BUS	**LIN BUS Output/Input;** internal 30 kΩ pull-up to V_S, LOW in dominant state
13	V_{BAT}	**Battery Supply Input;** a reverse current protection diode is required, block GND with 100 nF ceramic capacitor and 22 µF capacitor
14	INHI	**Inhibit Voltage Regulator Input;** TTL compatible, HIGH active input (HIGH switches the VR on); connect to V_{BAT} if not needed
15	RO	**Reset Output;** open collector output connected to the output via a resistor of 30 kΩ

Functional Block Diagram

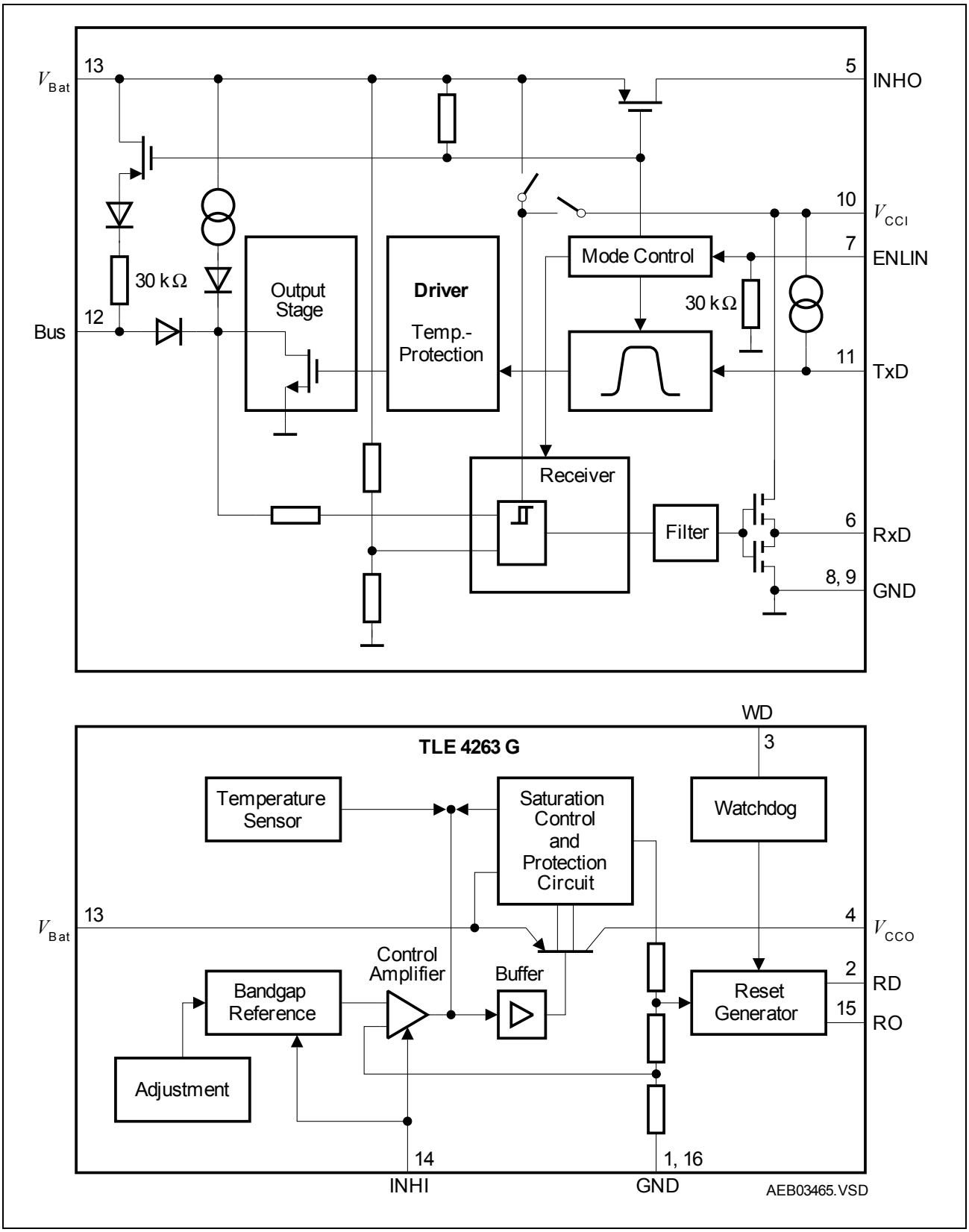


Figure 2 Block Diagram

Circuit Description

The TLE 6286 is a single-wire transceiver combined with a LDO. It is a chip-by-chip integrated circuit in a P-DSO-16-11 package. It works as an interface between the protocol controller and the physical bus. The TLE 6286 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems. The on-chip voltage regulator with watchdog is designed for sleep mode applications but it is also possible to use an external voltage regulator.

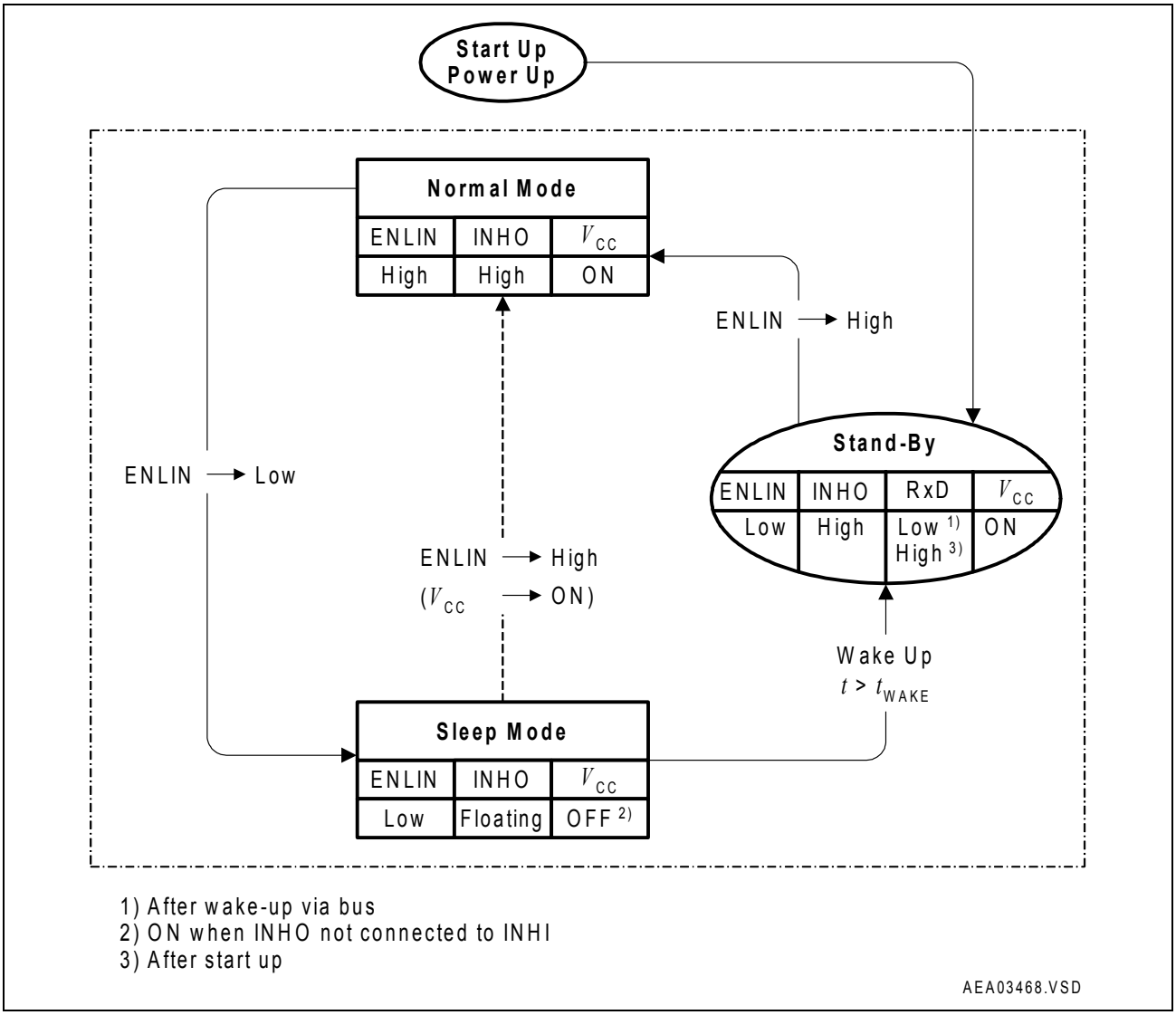


Figure 3 Operation Mode State Diagram

Operation Modes

In order to reduce the current consumption the TLE 6286 offers a sleep operation mode. This mode is selected by switching the enable input ENLIN low (see **Figure 3**, **Operation Mode State Diagram**). In the sleep mode a voltage regulator can be controlled via the INHO output in order to minimize the current consumption of the whole

application. A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INHO output high. In parallel the wake-up is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

In case the voltage regulator control input INHI is not connected to INHO output or the microcontroller is active respectively, the TLE 6286 can be set in normal operation mode without a wake-up via the communication bus.

LIN Transceiver

The LIN Transceiver has already a pull-up resistor of 30 kΩ as termination implemented. There is also a diode in this path, to protect the circuit from feedback of voltages from the bus line to the power supply. To configure the TLE 6286 as a master node, an additional external termination resistor of about 1 kΩ is required. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is also recommended to place a diode in series to the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF in the master node (see **Figure 8**, **Application Example without Bus Short to GND Protection**).

An capacitor of 10 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

Bus Short to GND Feature

The TLE 6286 also has a BUS short to GND feature implemented, in order to protect the battery from running out of charge. A normal master termination connection like described above, 1 kΩ resistor and diode between bus and V_S, would cause a constantly drawn current via this path. The resulting resistance of this short to GND is lower than 1 kΩ. To avoid this current during a generator off state, like a parked car, the sleep mode has a bus short to GND feature implemented in the TLE 6286. This feature is only applicable, if the master termination is connected with the INHO pin, instead of the V_S. For a more detailed information see the application circuit in **Figure 8** and **Figure 9**.

Voltage Regulator

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold V_{DRL}, a reset signal occurs at the reset output and is held

until the upper threshold V_{DU} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typ. 4.65 V. A connected microcontroller will be monitored through the watchdog logic. In case of missing pulses at pin W, the reset output is set to low. The pulse sequence time can be set in a wide range with the reset delay capacitor. The IC can be switched at the TTL-compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against overload, overtemperature, reverse polarity.

Input Capacitor

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR < 3 Ω at 10kHz within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (t_{rd} \times I_{D,ch}) / \Delta V \quad (1)$$

Definitions:

- C_D = delay capacitor
- t_{rd} = reset delay time
- $I_{D,ch}$ = charge current, typical 60 µA
- $\Delta V = V_{DU}$, typical 1.70 V
- V_{DU} = upper delay switching threshold at C_D for reset delay time

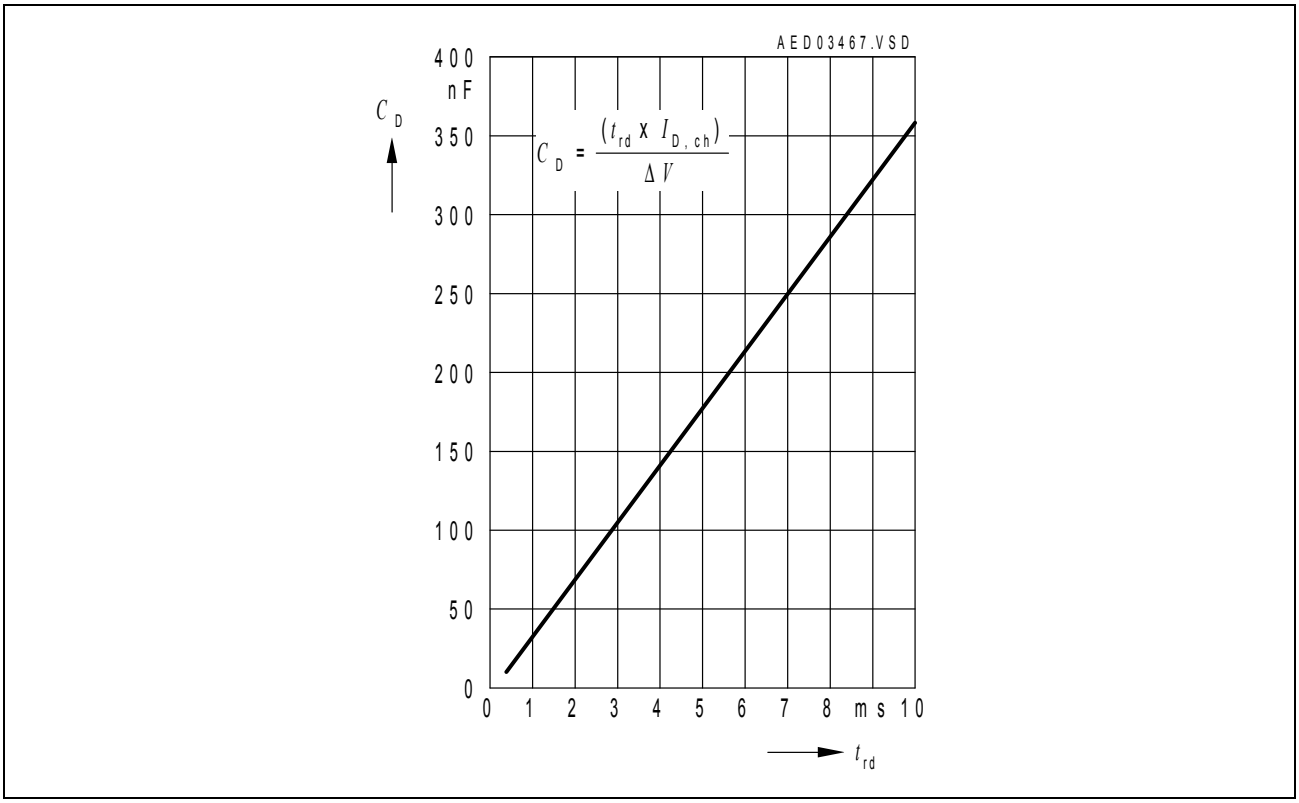


Figure 4 Typical Reset Delay Timing vs. Delay Capacitance

The reset reaction time t_{rr} is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 47 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{rr} \approx 20\ \text{s/F} \times C_D \quad (2)$$

For the reset timing diagram please refer to **Figure 6**.

Watchdog Timing

The frequency of the watchdog pulses has to be higher than the minimum pulse sequence which is set by the external reset delay capacitor C_D. Calculation can be done according to the formulas given in **Figure 5**. For the watchdog timing diagram please refer to **Figure 7**.

$$T_{WI,tr} = [(V_{DU} \times V_{DWL}) / I_{D,wd}] / C_D \quad (3)$$

Definitions:

- $T_{WI,tr}$ = watchdog trigger time
- $I_{D,wd}$ = discharge current, typical 6.25 µA
- V_{DWL} = lower timing threshold

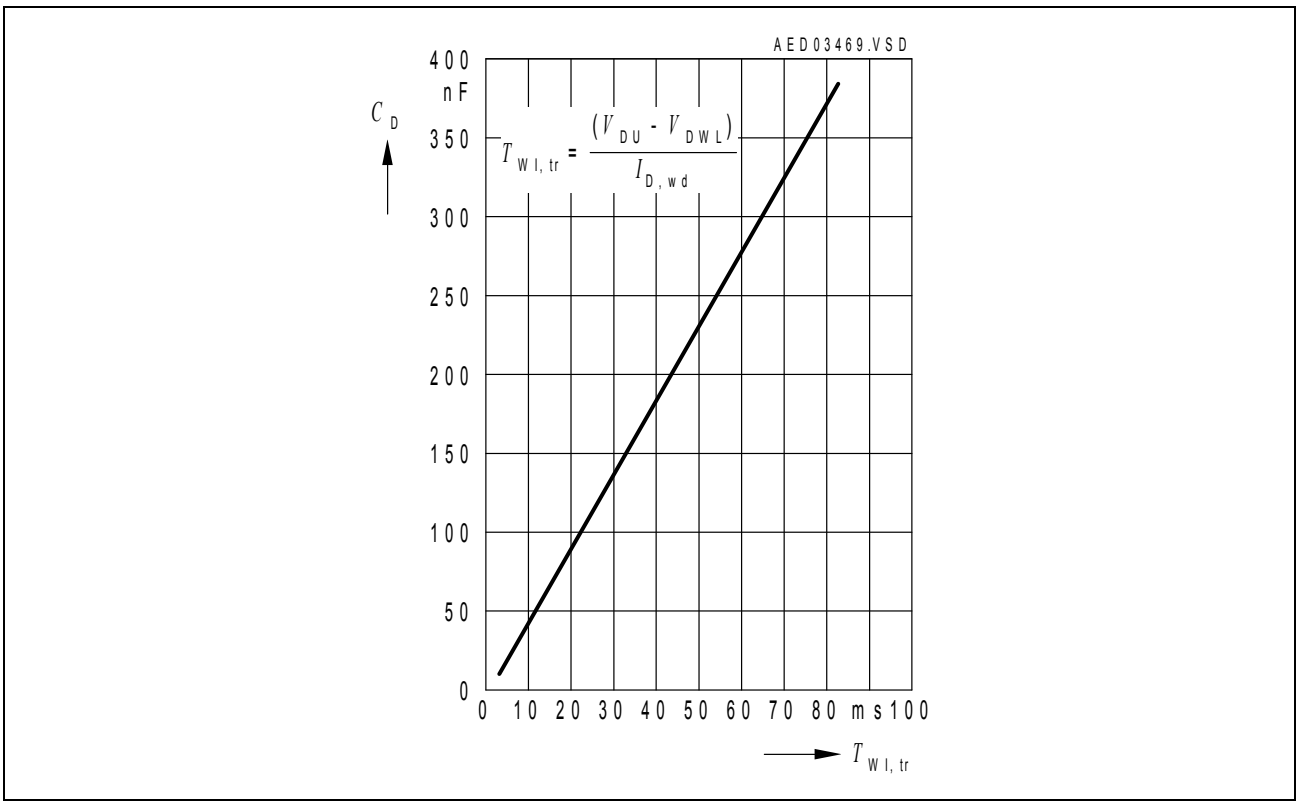


Figure 5 Typical Watchdog Trigger Time vs. Delay Capacitance

Please note that in all calculations with capacitances, the leakage current of the capacitor is neglected!

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Supply voltage	V_{CCI}	-0.3	6	V	–
Battery supply voltage	V_{BAT}	-0.3	40	V	–
Bus input voltage	V_{bus}	-20	32	V	–
Bus input voltage	V_{bus}	-20	40	V	t < 1 s
Logic voltages at ENLIN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Input voltages at INHO	V_{INHO}	-0.3	V_S + 0.3	V	–
Output current at INHO	I_{INHO}	–	20	mA	–
Reset output voltage	V_{RO}	-0.3	40	V	–
Reset delay voltage	V_{RD}	-0.3	40	V	–
Output voltage V_{CCO}	V_{CCO}	-0.3	7	V	–
INHI voltage	V_{INHI}	-40	40	V	–
Watchdog voltage	V_{WD}	-0.3	6	V	–
Electrostatic discharge voltage at V_S, Bus vs. GND	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 3 Operating Range

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Supply voltage	V_{CCI}	4.5	–	5.5	V	–
Battery Supply voltage	V_{BAT}	6	–	35	V	–
Junction temperature	T_j	-40	–	150	°C	–
Thermal Shutdown (junction temperature)						
Thermal shutdown temp.	T_{jSD}	150	170	190	°C	–
Thermal shutdown hyst.	ΔT	–	10	–	K	–
Thermal Resistances						
Junction ambient	R_{thj-a}	–	80	–	K/W	PCB heat sink area 300mm^2

Table 4 Electrical Characteristics

V_{CC} = 5.0 V;V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Sym-bol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Current Consumption						
Current consumption at V_{BAT} (LIN + voltage regulator)	I_{BAT}	–	1.5	2.3	mA	recessive state; INHI = INHO = HIGH; $V_{TxD} = V_{CC}$; without R_L
	I_{BAT}	–	2.1	3.3	mA	dominant state; INHI = INHO = HIGH; V_{TxD} = 0 V; without R_L
Current consumption V_{CCI} (LIN only)	I_{CCI}	–	0.4	0.7	mA	recessive state; LDO sleep; $V_{TxD} = V_{CC}$
	I_{CCI}	–	0.4	0.8	mA	dominant state; LDO sleep; V_{TxD} = 0 V
Current consumption sleep mode (LIN + voltage regulator)	I_{BAT}	–	20	40	µA	sleep mode; INHI = INHO = LOW; T_j < 85 °C
(LIN only)	I_{CCI}	–	3	10	µA	sleep mode; INHI = INHO = LOW
Current consumption LDO (voltage regulator only, LIN in sleep mode)	I_{BAT}	–	900	1300	µA	I_{CCO} = 0 mA
	I_{BAT}	–	10	18	mA	I_{CCO} = 150 mA
	I_{BAT}	–	15	23	mA	I_{CCO} = 150 mA; V_{BAT} = 4.5V
Enable Input (pin ENLIN)						
HIGH level input voltage threshold	$V_{EN,on}$	–	2.8	0.7 × V_{CC}	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.3 × V_{CC}	2.2	–	V	low power mode
ENLIN input hysteresis	$V_{EN,hys}$	300	600	900	mV	–
ENLIN pull-down resistance	R_{EN}	15	30	60	kΩ	–

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5.0 V;V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Sym-bol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Inhibit Output (pin INHO)						
Inhibit R_{ON} resistance	R_{onINHO}	–	65	120	Ω	I_{INHO} = -15 mA
Leakage current	$I_{INHO,lk}$	-5.0	–	5.0	µA	sleep mode; V_{INHO} = 0 V
V_{CC} Output (pin V_{CCO})						
Output voltage	V_{CCO}	4.90	5.00	5.10	V	5 mA ≤ I_{CCO} ≤ 150 mA; 6 V ≤ V_{BAT} ≤ 28 V
Output voltage	V_{CCO}	4.90	5.00	5.10	V	6 V ≤ V_{BAT} ≤ 32 V; I_{CCO} = 100 mA; T_j = 100 °C
Output current	I_{CCO}	200	250	400	mA	1)
Drop voltage	V_{dr}	–	0.35	0.50	V	I_{CCO} = 150 mA 1)
Load regulation	$\Delta V_{CCO,lo}$	–	–	25	mV	I_{CCO} = 5 mA to 150 mA
Line regulation	$\Delta V_{CCO,li}$	–	3	25	mV	V_{BAT} = 6 V to 28 V; I_{CCO} = 150 mA
Power Supply Ripple Rejection	$PSRR$	–	54	–	dB	2) f_r = 100 Hz; V_r = 0.5 Vpp
Reset Generator (pin RD)						
Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	-
Reset low voltage	$V_{RO,l}$	–	0.10	0.40	V	I_{RO} = 1 mA
Saturation voltage	$V_{D,sat}$	–	50	100	mV	$V_Q < V_{R,th}$
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower reset timing threshold	V_{DRL}	0.20	0.35	0.55	V	–
Charge current	$I_{D,ch}$	40	60	85	µA	–
Reset delay time	t_{rd}	1.3	2.8	4.1	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	1.2	4	µs	C_D = 100 nF

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5.0 V;V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Sym-bol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Watchdog (pin WD)						
Discharge current	$I_{D,wd}$	4.40	6.25	9.10	µA	V_D = 1.0 V
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower timing threshold	V_{DWL}	0.20	0.35	0.55	V	–
Watchdog trigger time	$T_{WI,tr}$	16	22.5	27	ms	C_D = 100 nF
Inhibit Input (INHI)						
Switching voltage	$V_{INHI,ON}$	3.6	–	–	V	IC turned on
Turn-OFF voltage	$V_{INHI,OFF}$	–	–	0.8	V	IC turned off
Input current	I_{INHI}	5	10	25	µA	V_{INHI} = 5 V
Receiver Output RxD						
HIGH level output current	$I_{RxD,H}$	-1.2	-0.8	-0.5	mA	$V_{RxD} = 0.8 \times V_{CC}$
LOW level output current	$I_{RxD,L}$	0.5	0.8	1.2	mA	$V_{RxD} = 0.2 \times V_{CC}$
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TxD,H}$	–	2.9	0.7 $\times V_{CC}$	V	recessive state
TxD input hysteresis	$V_{TxD,hys}$	300	700	900	mV	–
LOW level input voltage threshold	$V_{TxD,L}$	0.3 $\times V_{CC}$	2.1	–	V	dominant state
TxD pull-up current	I_{TxD}	-150	-110	-70	µA	$V_{TxD} < 0.3\ V_{CC}$

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5.0 V;V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Sym-bol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Bus Receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 × V_S	0.48 × V_S	–	V	-8 V < V_{bus} < $V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$	–	0.56 × V_S	0.60 × V_S	V	$V_{bus,rec}$ < V_{bus} < 20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 × V_S	0.04 × V_S	0.10 × V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
Receiver threshold center voltage	$V_{bus,cnt}$	0.475 × V_S	0.5 × V_S	0.525 × V_S		LIN2.0 table 3.1
Input leakage current	$I_{bus,lek}$	-1			mA	V_{bus} = 0V, V_{bat} = 12V, pull-up resistor as specified in LIN2.0
Wake-up threshold voltage	V_{wake}	0.40 × V_S	0.50 × V_S	0.60 × V_S	V	–
Bus Transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 × V_S	–	V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$	0	–	2	V	V_{TxD} = 0 V 7.3V<V_S<27V
		0	–	1.2	V	V_{TxD} = 0 V 6V<V_S<7.3V
Bus short circuit current	$I_{bus,sc}$	40	100	150	mA	$V_{bus,short}$ = 13.5 V
Leakage current	$I_{bus,lk}$	-1	-	–	mA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V,
		–	10	20	µA	V_{CC} = 0 V, V_S = 13.5V, V_{bus} = 20 V,
Bus pull-up resistance	R_{bus}	20	30	47	kΩ	Normal mode

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5.0 V;V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Sym-bol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Dynamic Transceiver Characteristics						
Falling edge slew rate	$S_{bus(L)}$	-3	-2.0	-1	V/µs	60% > V_{bus} > 40% 1 µs < (τ = $R_{BUS} \times C_{BUS}$) < 5 µs[3]; V_{CC} = 5 V; V_S = 13.5 V
Rising edge slew rate	$S_{bus(H)}$	1	1.5	3	V/µs	40% < V_{bus} < 60% 1 µs < (τ = $R_{BUS} \times C_{BUS}$) < 5 µs[3]; V_{CC} = 5 V; V_S = 13.5 V
Slope symmetry	$t_{slopesym}$	-5	–	5	µs	t_{fslope} - t_{rslope}
Propagation delay TxD LOW to bus	$t_{d(L),T}$	–	1	4	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$	–	1	4	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T}$ = $t_{d(L),T}$ - $t_{d(H),T}$
Duty cycle D1	t_{duty1}	0.396	–	–		duty cycle 1[3] TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit};
Duty cycle D2	t_{duty2}	–	–	0.581		duty cycle 2[3] TH_{Rec}(max) = 0.422× V_S; TH_{Dom}(max) = 0.264 × V_S V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit};

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5.0 V;V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Sym-bol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Wake-up delay time	t_{wake}	30	100	150	µs	$T_j \leq$ 125 °C
		–	–	170	µs	$T_j \leq$ 150 °C[2)]
Delay time for change sleep/stand by mode - normal mode	t_{snorm}	–	–	50	µs	–
Delay time for change normal mode - sleep mode	t_{nsleep}	–	–	50	µs	–

1) Drop voltage = V_i - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6V input).

2) Not subject to production test, specified by design

3) Bus load conditions concerning LIN spec 2.0 C_{bus}, R_{bus} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω

Note: The reset output is low within the range V_Q = 1 V to $V_{Q,rt}$.

Diagrams

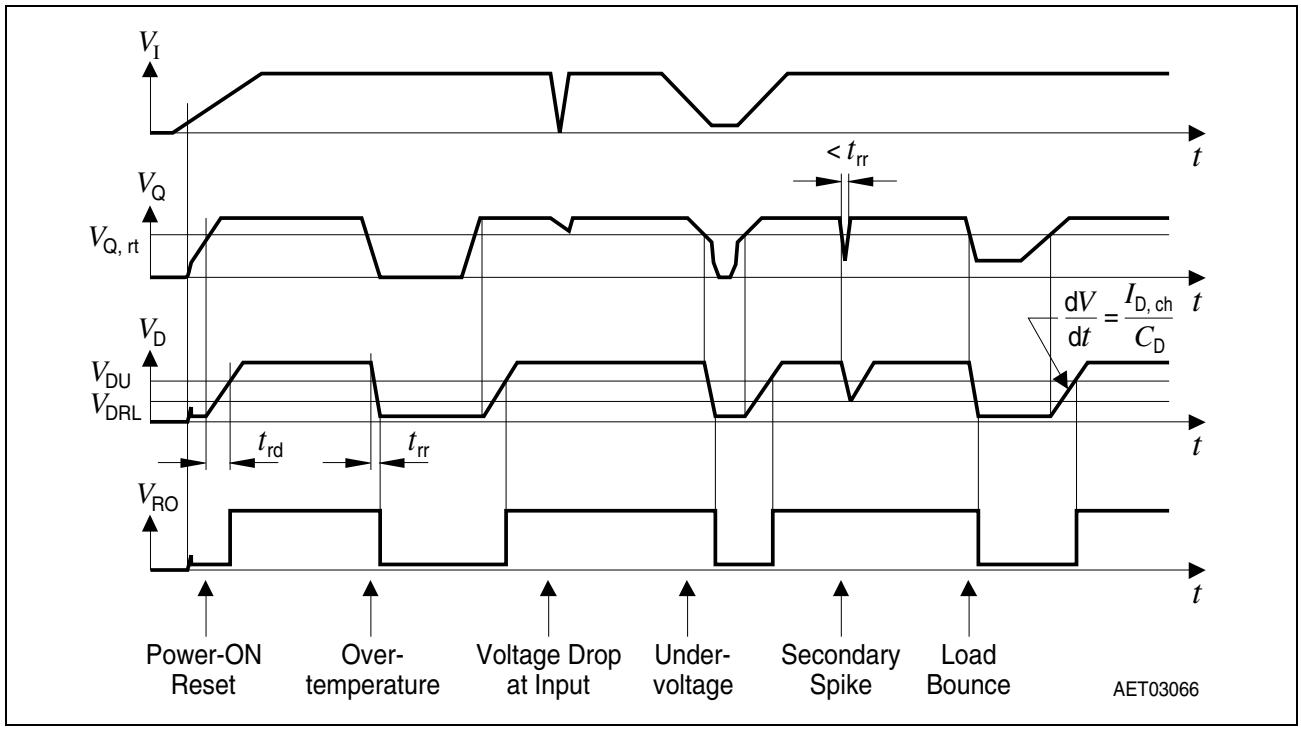


Figure 6 Time Response, Watchdog with High-Frequency Clock

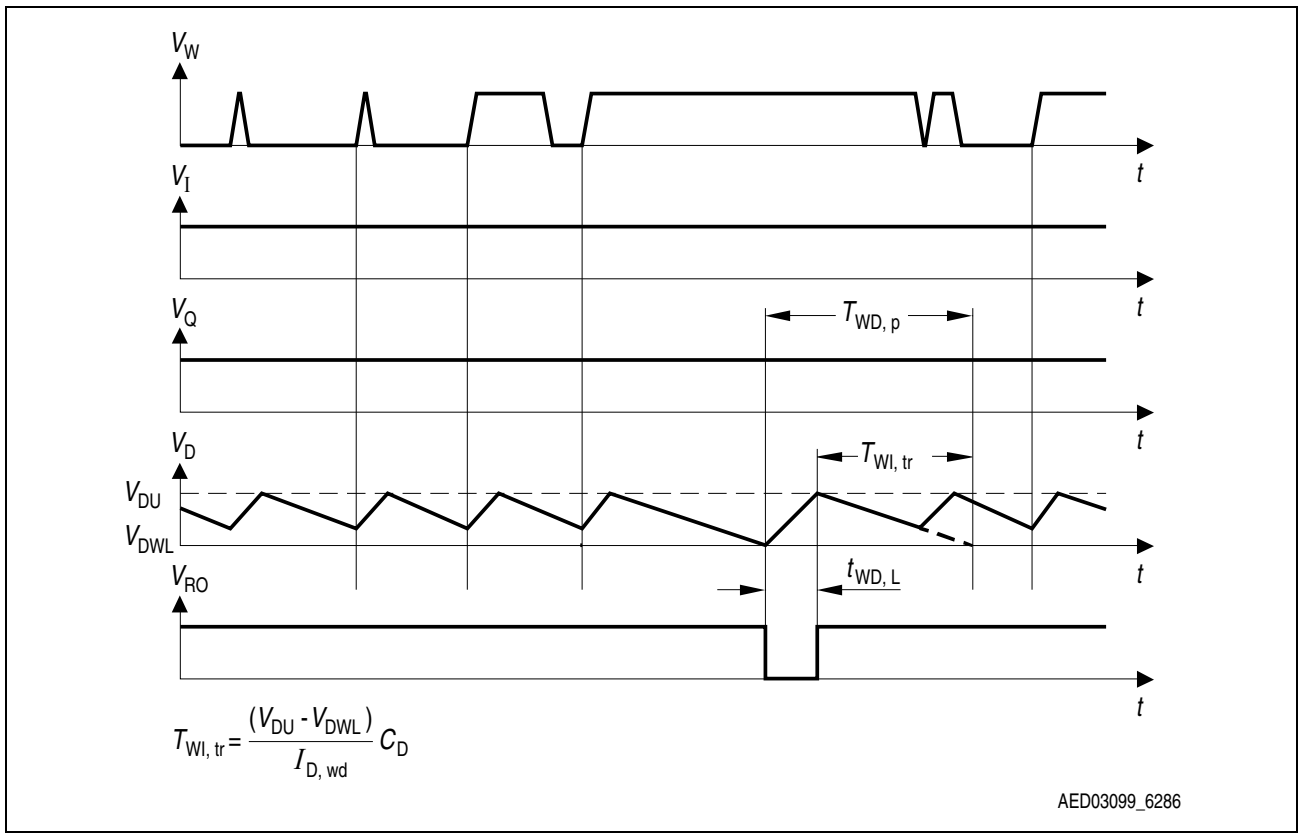


Figure 7 Timing of the Watchdog Function Reset

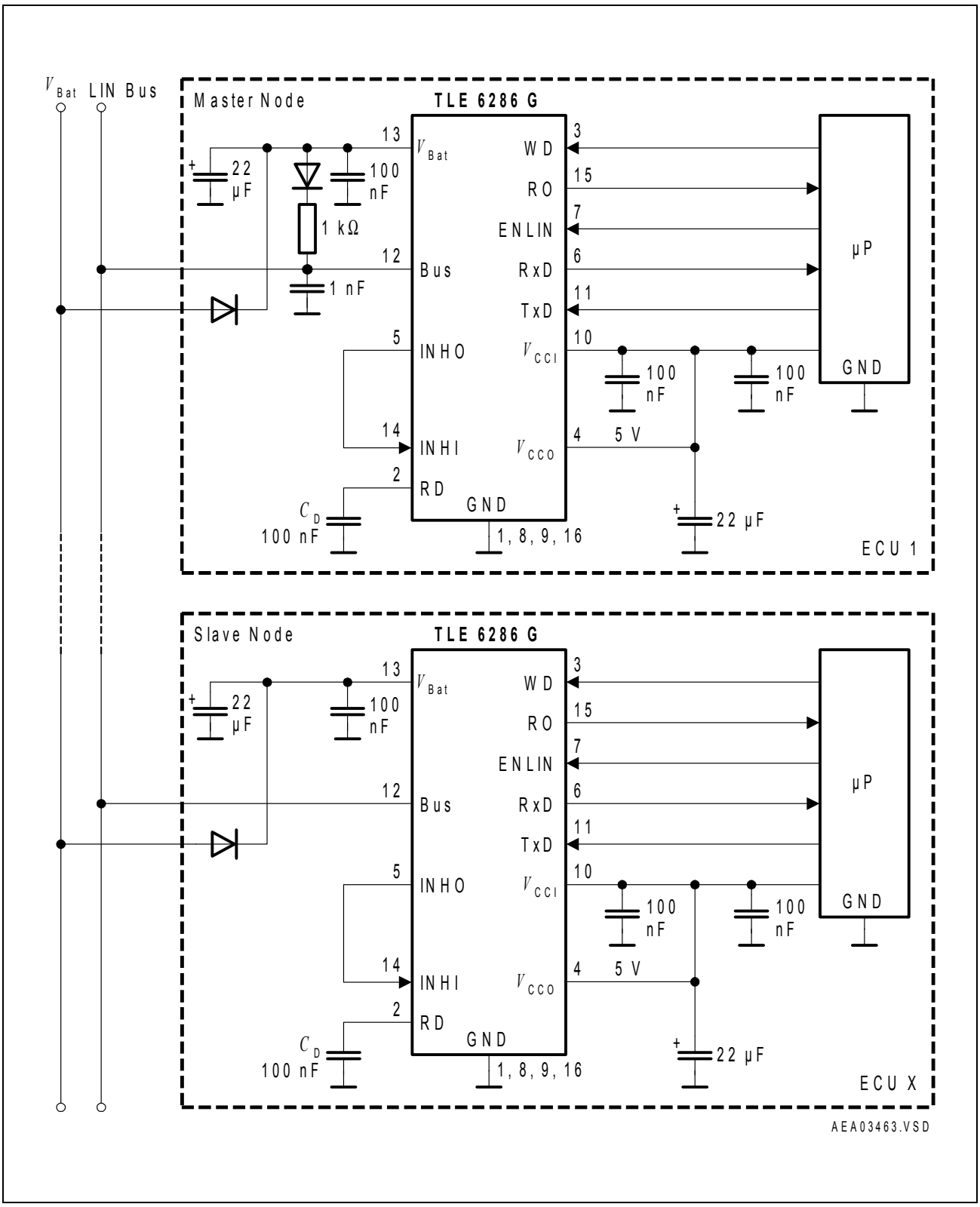


Figure 8 Application Example without Bus Short to GND Protection

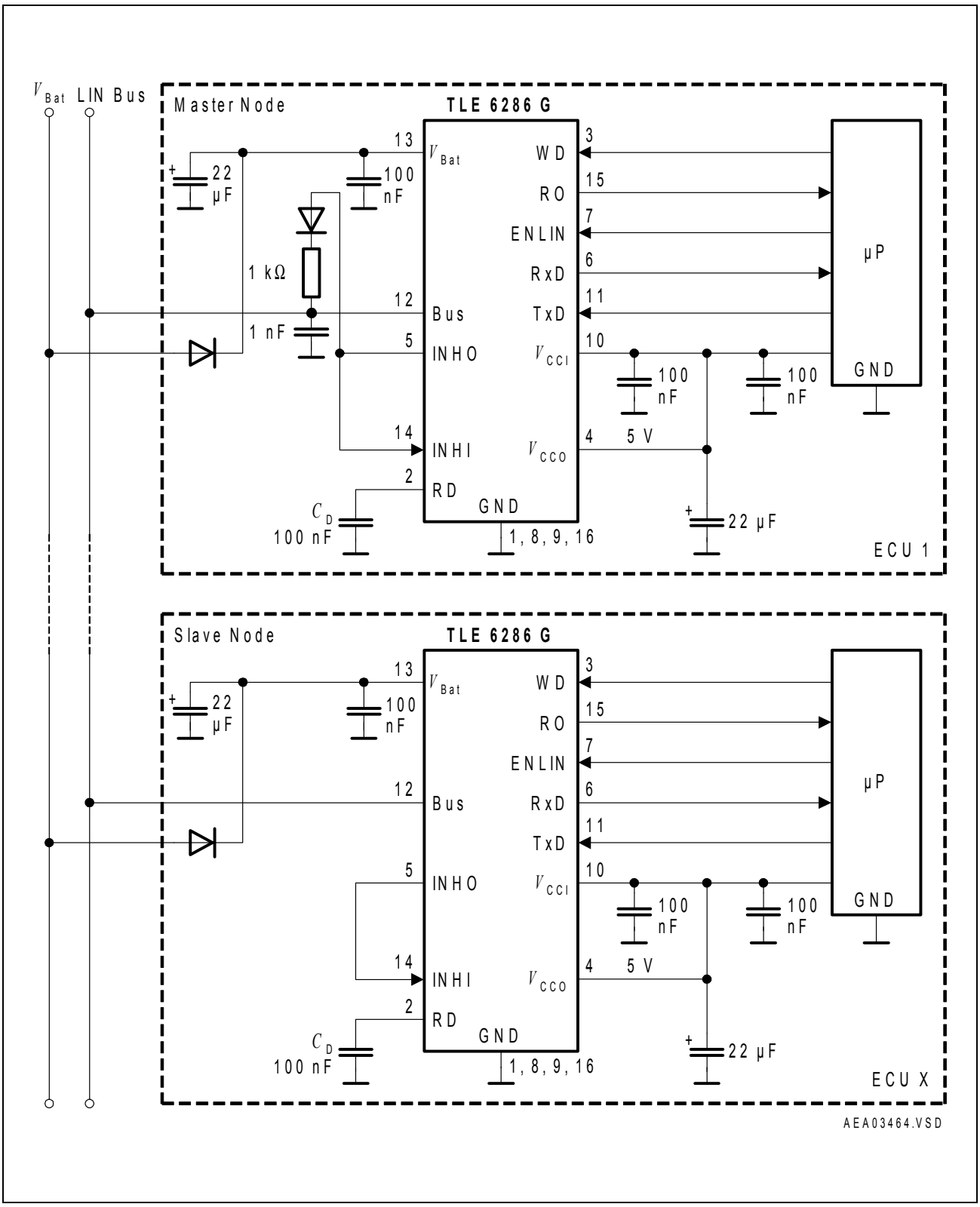
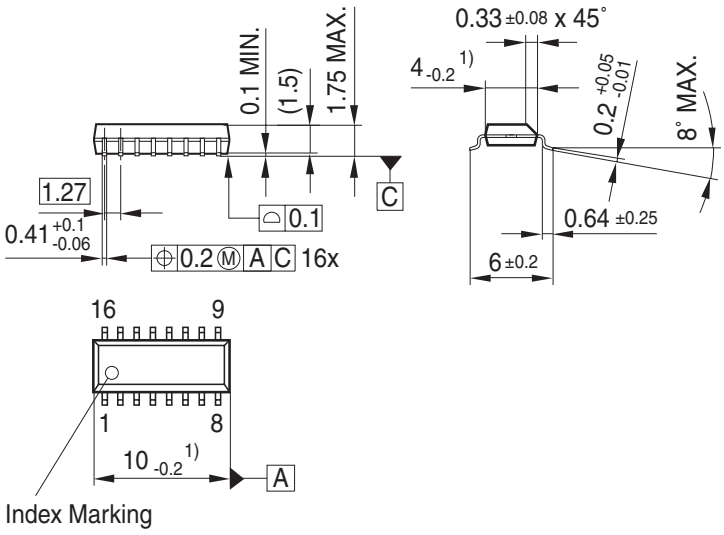


Figure 9 Application Example with Bus Short to GND Protection

Package Outlines



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPS09453

Figure 10 **P-DSO-16-11** (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm