L99PD08

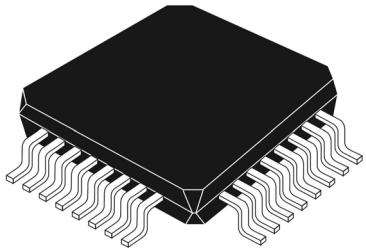
SPI control diagnosis interface device for VIPower™ M0-5 and M0-5E high side drivers

Features

- 8 channel VIPower driver and diagnostics device
- Supports analog and digital VIPower status readback
- 8 independent PWM channels
- Selectable PWM base clock (2 external, one internal)
- Programmable PWM turn on phase shift
- Programmable diagnostic thresholds (analog VIPower)
- Programmable over temperature latch off for enhanced HSD short circuit reliability
- Limp home safety mode
- ST-SPI interface protocol for data communication
- External enable pin for low power mode
- Detailed and filtered diagnostic for each channel
- Direct multiplexed VIPower status / current sense feedback
- Supply voltage 3.3 or 5.0 V (two pins)

Applications

- Exterior and interior automotive light system



LQFP32

Description

The device has integrated several functions which save job load of the microcontroller and save necessary connections to the microcontroller. It's possible to connect analog and digital high side drivers (HSD) to the device and control them via SPI interface. A synchronous detailed diagnostics feature is integrated.

The device has 8 outputs to the HSD with the possibility to be driven either by steady state ON/OFF mode or by PWM. Two clock inputs used as base frequency to generate the PWM signal internally are provided. The outputs are fully independent and can also be driven with phase shift to improve characteristics of power net during the inrush phase. The device has 8 current sense (CS)/status (ST) pins connected to the HSD to run diagnostics. The index of ST/CS pin corresponds to the input connected to the same HSD channel (ST0/CS0 with OUT0, ST1/CS1 with OUT1 …).

Table 1. Summary device

Package	Order codes	
	Tube	Tape and reel
LQFP32	L99PD08	L99PD08TR

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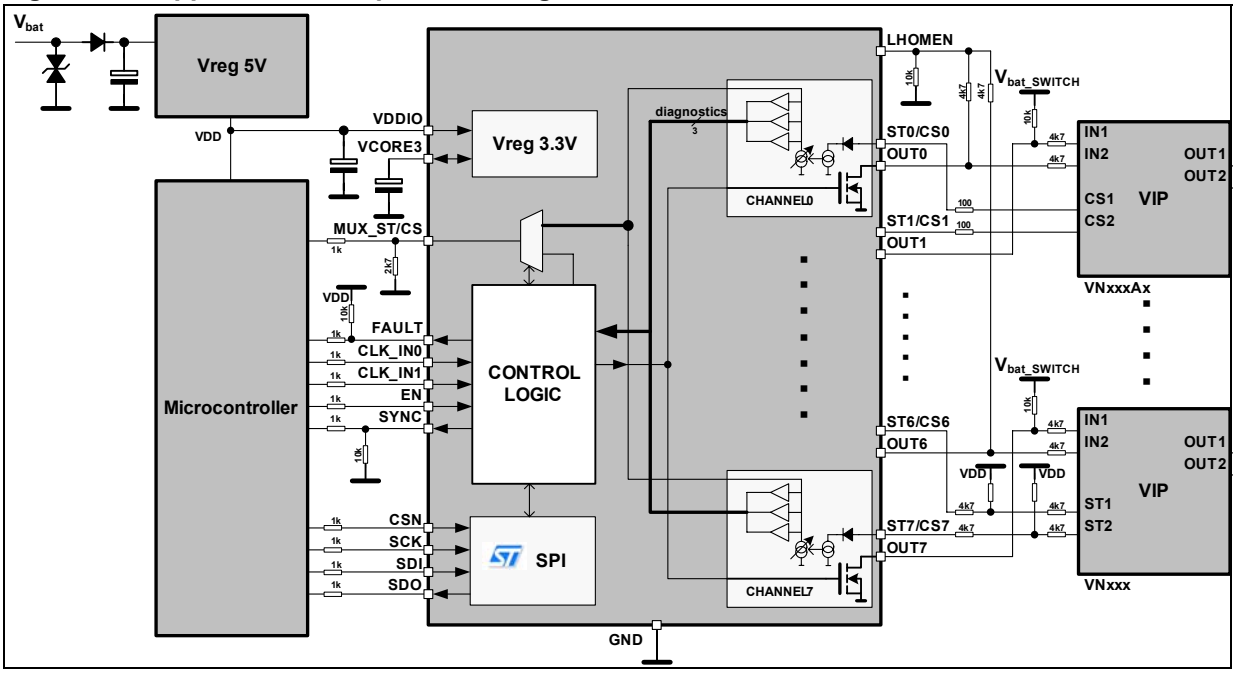
1 Block diagram

Figure 1. Application example block diagram

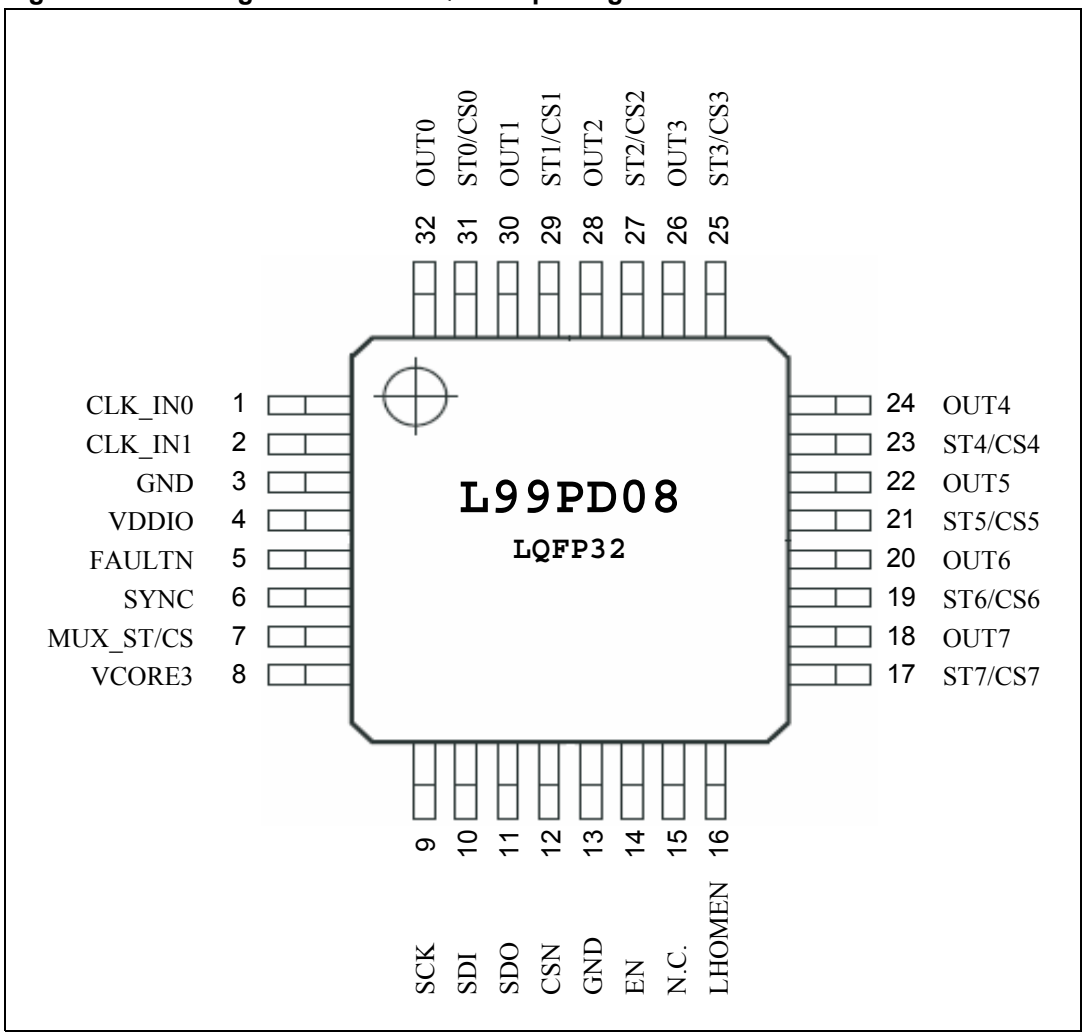


2 Pin definitions and functions

Table 2. Pin definition and function

Pin	Symbol	Function
1	CLK_IN0	PWM clock input 0
2	CLK_IN1	PWM clock input 1
3, 13	GND	Common ground
4	VDDIO	I/O and 3.3 V voltage regulator supply (3.3 V or 5 V)
5	FAULTN	Failure on HSD or communication error
6	SYNC	Output of OUT0-OUT7 signals, selected by control register
7	MUX_ST/CS	Output from ST/CS multiplexer
8	VCORE3	Core supply voltage (3.3 V only)
9	SCK	ST-SPI – serial clock input
10	SDI	ST-SPI – serial data input
11	SDO	ST-SPI – serial data output
12	CSN	ST-SPI – chip select input
14	EN	Enable pin
15	N.C.	Not connected
16	LHOMEN	Active mode pull-up supply – limp home
17	ST7/CS7	Input from HSD status / current sense pin
18	OUT7	Output to High side driver – channel 7
19	ST6/CS6	Input from HSD status / current Sense pin
20	OUT6	Output to high side driver – channel 6
21	ST5/CS5	Input from HSD status / current sense pin
22	OUT5	Output to high side driver – channel 5
23	ST4/CS4	Input from HSD status / current sense pin
24	OUT4	Output to high side driver – channel 4
25	ST3/CS3	Input from HSD status / current sense pin
26	OUT3	Output to high side driver – channel 3
27	ST2/CS2	Input from HSD status / current sense pin
28	OUT2	Output to high side driver – channel 2
29	ST1/CS1	Input from HSD status / current sense pin
30	OUT1	Output to high side driver – channel 1
31	ST0/CS0	Input from HSD status / current sense pin
32	OUT0	Output to high side driver – channel 0

Figure 2. Pinning of device in LQFP-32 package



2.1 ST-SPI: SCK, SDI, SDO, CSN

A 16-bit SPI interface is used to control the device. The communication interface is activated by pulling CSN to low. The SDI is captured with the positive edge of SCK and the data is shifted out at SDO at the negative edge of SCK. A CSN timeout is implemented.

2.2 CLK_IN0, CLK_IN1

These pins are used to run the two internal PWM base frequency counters to generate the output PWM.

Each channel can be programmed as steady state ON/OFF output or a PWM output through the PWM_EN (Addr: hex03) SPI register. During PWM mode, the PWM signal can be generated either from CLK_IN0 or CLK_IN1 as base counter, selected through the SPI register CLK_SEL (Addr: hex04). Phase shift and duty cycle are set through the dedicated registers DUTY_CHx (Addr: hex10 – hex17) and PHASE_CHx (Addr: hex18 – hex1F).

The output PWM period is a factor of 256 of the frequency applied on CLK_INx signal.

If the external clock signal is not available or is below $f_{PWM(min)}$, the device will fallback to an internal PWM frequency generator f_{PWM} of approximately 122Hz periode.

2.3 LHOMEN

This pin allows connecting the output pull-down resistor for LIMP HOME mode. This pin is pulled to VDDIO in normal mode and is pulled low in case of failure (RESET and FAIL SAVE mode).

If power supply VDDIO is not connected, LHOMEN becomes weak low (LIMP HOME mode).

2.4 Output 0 to 7 (OUT0 … OUT7)

True open drain outputs are used to drive the High Side Driver inputs. These lines must have a pull-up resistor connected either to a separate supply or LHOMEN signal if LIMP HOME is supported.

These outputs are high impedance during RESET, Fail Safe modes and during SW Reset.

2.5 Status/current sense inputs (ST0/CS0 … ST7/CS7)

Those inputs are used to take the status or current sense information from DIGITAL or ANALOG HSD and provide information to the internal diagnosis. Every output has to correspond to the same HSD channel like the ST/CS input (OUT0 with ST0/CS0, OUT1 with ST1/CS1, …). Status of digital channels have to have an external pull-up resistor (4.7 kOhm) and a series protection resistor of 4.7 kOhm to STx/CSx, current sense signals of analog channels have to be connected to STx/CSx pins through a 100 Ohm reverse battery protection resistor.

The HSD type which is connected to the device (digital or analog) must be selected through the register DEV_TYPE (Addr: hex02).

2.6 Multiplexed status/current sense output (MUX_ST/CS)

The MUX_ST/CS Pin reflects the status or current sense information corresponding to the channel selected in the control register bits MUX_EN, MUX_A, B, C (Addr: hex00; Bit 7-4).

This pin delivers up to 3 mA at 2.7 V. It is recommended to use a 1.6k to 2.7kOhm external resistor to ground for the maximum dynamic range. The best choice for the external resistor depends on the Rdson class of the analog current sense HSD and of the loads.

If the multiplexer is disabled the MUX_ST/CS pin is in tristate condition.

2.7 VDDIO, VCORE3

The digital voltage supply of the device is internally limited to 3.3 V. In order to support also the 5 V supply voltages a linear internal voltage regulator can be used.

2.7.1 5.0 volt operation

The voltage regulator input is available at the terminal VDDIO, the output is available at VCORE3.

In the 5V operation mode it is recommended to attach a decoupling capacitor on VCORE3 to stabilize the regulator. Due to the limited current capability of this regulator no external loads should be attached on VCORE3.

2.7.2 3.3 volt operation

In applications with 3.3 V supply only, both, VDDIO and VCORE3 have to be attached (shorted) to the local supply.

If the internal supply (VCORE3) is below the threshold of the internal power-and-reset circuit, the device is in standby mode. The device is in low power consumption and no SPI communications are possible.

2.8 GND (2 pins)

These two pins are the GND voltage supply of the device and have to be connected externally.

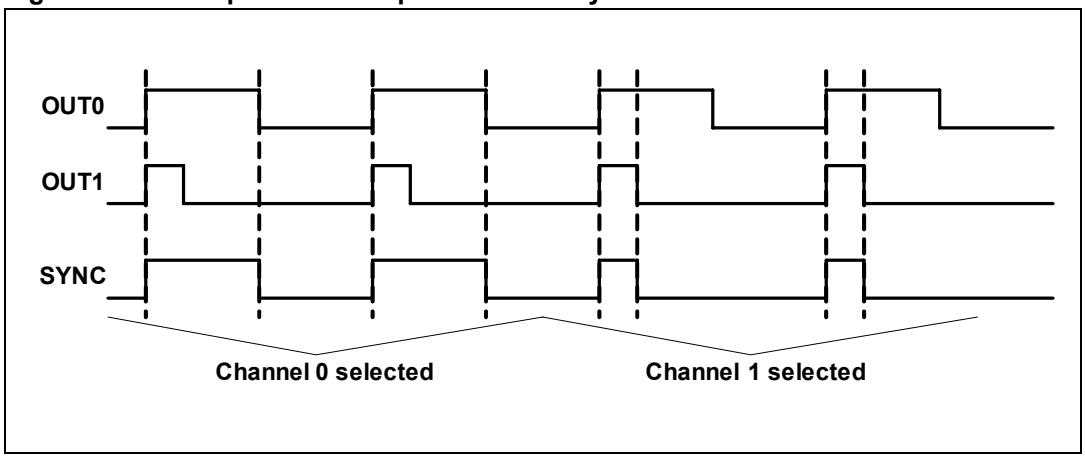
2.9 Faultn

This active low pin indicates any internal error reported by the device. This can be a High Side Driver failure or a communication error. In fault condition this open drain output is set to low, while during reset it is left open. This pin has to be connected to a pull up resistor.

2.10 SYNC

The SYNC pin reflects the OUTx corresponding to the channel selected in the control register bits MUX_EN, MUX_A, B, C (Addr: hex00; Bit 7-4). If the multiplexer is disabled the SYNC pin is actively pulled low.

Figure 3. Example for SYNC pin functionality



2.11 EN

With this pin pulled high, the device leaves low power mode. An internal pull down resistor guarantees the OFF condition when not connected.

3 Device mode

Table 3. Device modes

Mode	Source	Actions	CS-timer	SPI state	Outputs state	ChipReset-bit	LHOMEN
Power down	Low VCORE3	All registers are cleared	Not active	No comm.	High-Z fail safe	1	LOW(1)
Standby	EN = '0'	All registers are cleared	Not active	No comm.	High-Z fail safe	1	LOW(1)
Fail save	CSNTO(2) / LHOMEN bit ='0'	-	Active	Active	High-Z fail safe	0	LOW(1)
	SW reset	All registers are cleared				1	
Normal	LHOMEN-bit = '1'	-	Active	Active	Normal	0	VDDIO

1. Max. sink current can only be guaranteed for VCORE3 VCORE3$_{min}$. Therefore an external pull down is recommended.
2. ChipSelectNot-TimeOut

Note: To leave FAIL SAVE the LHOMEN-bit in ControlRegister (Addr.: hex00, Bit 0) has to be set to '1'. FAIL SAVE is reentered by either ChipSelectNot-TimeOut (CSNTO) or SW-Reset (in both cases LHOME-bit is automatically reset) or setting this bit to '0' via SPI access.

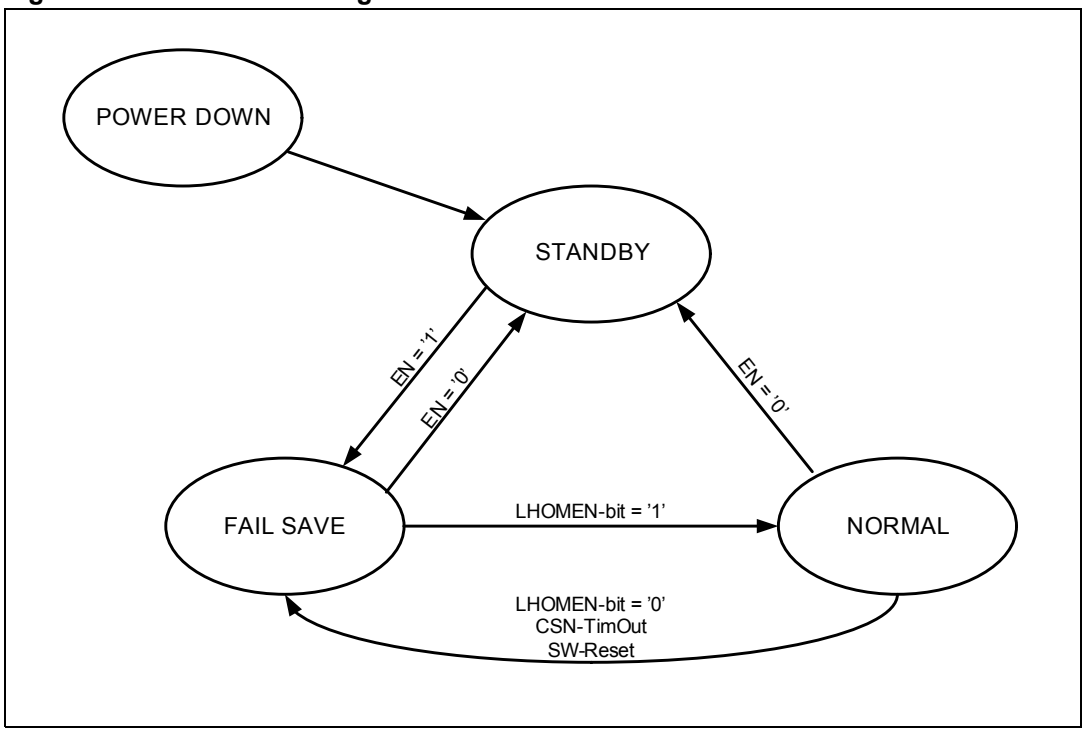
To stay in normal mode a rising edge has to be generated at CSN within every timeframe programmed in the control register (Addr.: hex00, Bit 3,2). Else a CSNTO is detected and FAIL SAVE entered.

When SDI is stuck to GND the device enters automatically FAIL SAVE.

When SDI is stuck to logical high level then the device receives a SW-Reset and enters FAIL SAVE. A read of ROM address Addr.: hex3F is detected as stuck to logical high level.

In FAIL SAVE the SYNC pin is logical high.

Figure 4. Device state diagram



4 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCORE3	Stabilized supply voltage	-0.3 to 3.6	V
VDDIO	Stabilized supply voltage	-0.3 to 5.5	V
EN, SCK, DI, CSN, CLK_INx / DO, SYNC, LHOMEN	Digital input / output voltage	-0.3 to VDDIO + 0.3	V
OUT 1-8, FAULTN	Output current (open drain)	10	mA
MUX ST/CS	Output current	1	mA
ST/CS 1-8	Input current	10	mA
ST/CS 1-8	Input Voltage	-14 to 6.5	V

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit.

4.1 ESD protection

Table 5. ESD protection

Parameter	Value	Unit
All pins	±2	kV

Note: HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A HBM with all unzapped pins grounded

4.2 Operating junction temperature

Table 6. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	operating junction temperature	-40 to 150	°C
R_{thmax}		90	K/W

5 Electrical characteristics

VDDIO = 3.15 V to 5.25 V, VCORE3 = 3.15 V to 3.4 V, T_j = -40 to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDDIO	Operating supply voltage range 5V		4.75	5.0	5.25	V
	Operating supply voltage range 3.3V		3.15	3.3	3.35	V
VCORE3	Regulated output voltage range	I_{out} = 2 mA, VDDIO=5.0 V	3.15	3.3	3.35	V
I_{CORE}	VDDIO DC supply current	VDDIO = 5.0 V, EN=5.0 V, All IOs open/floating		1	5	mA
	VDDIO quiescent supply current	VDDIO = 5.0 V = CSN, EN = 0 (standby mode), All IOs open/floating		0	1	µA
	VDDIO quiescent supply current	VDDIO = 3.3 V = CSN, EN = 0 (standby mode), all IOs open/floating		0	6	µA

Table 8. Undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{POR\ OFF}$	Power-on reset threshold	VCORE3 increasing			3.0	V
$V_{POR\ ON}$	Power-on reset threshold	VCORE3 decreasing	2.3			V
$V_{POR\ hyst}$	Power-on reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.3		V

Table 9. EN pin

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{EN}	High voltage	EN = VCORE3 rising/falling	1.0	-	2.0	V
$V_{CLAMP}P$	Positive clamping voltage		7	-	10	V
$V_{CLAMP}N$	Negative clamping voltage		-20	-	-16	V

Table 10. Output switches/fault pin

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OUT}sat	Output saturation voltage	I_{OUT1-8} = 1 mA		0.1	0.3	V
I_{leak}	Output leakage current	OUTx off, V_{OUT} = 5.0 V		50	70	µA
V_{IL}(1)	Input low voltage	VCORE3 = 3.3 V, increasing			2.0	V
V_{IH}(1)	Input high voltage	VCORE3 = 3.3 V, decreasing	1.2			V
V_{CLAMP}P	Positive clamping voltage		7		10	V
V_{CLAMP}N	Negative clamping voltage		-20		-16	V

1. Output switches read back only

Table 11. Current sense/status inputs

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SAT}	Input saturation voltage	I_{IN} = 6 mA	2.4	3.0	3.5	V
		I_{IN} = 50 µA	0.8	1.0	1.4	V
I_{INH}ST	ST input current threshold to detect high level	Increasing	80	110	140	µA
I_{INL}ST	ST input current threshold to detect low level	Decreasing	50	85	110	µA
V_{CLAMP}P	Positive clamping voltage		8		11	V
V_{CLAMP}N	Negative clamping voltage		-20		-16	V
t_{TD_SENSE} low	Filter time for TD_SENSE = '0' blanking (t_{CS_filter} included)		300		600	µs
t_{TD_SENSE} high	Filter time for TD_SENSE = '1' blanking (t_{CS_filter} included)		600		1000	µs
t_{CS_OFF}	CS filter OFF time		1.0		1.55	ms
t_{CS_filter}	CS diagnosis filter time		54		111	µs
$t_{ON\text{-}state}$	ST diagnosis ON-State blanking time		200		350	µs
$t_{ON\text{-}OFF\_trans}$	ST diagnosis ON-OFF transition blanking time		20		33	µs
t_{trans_valid}	ST diagnosis transition valid time		20		190	µs
$t_{OFF\text{-}state}$	ST diagnosis OFF-State blanking time		1.0		1.55	ms
t_{ST_filter}	ST diagnosis filter time		54		111	µs
t_{blank}	Blanking time for inrush current CHx1,0 = [0,1], 15ms		15		21	ms
	Blanking time for inrush current CHx1,0 = [1,0], 70ms		70		100	ms
	Blanking time for inrush current CHx1,0 = [1,1], 200ms		200		280	ms

Figure 5. CS pin timing

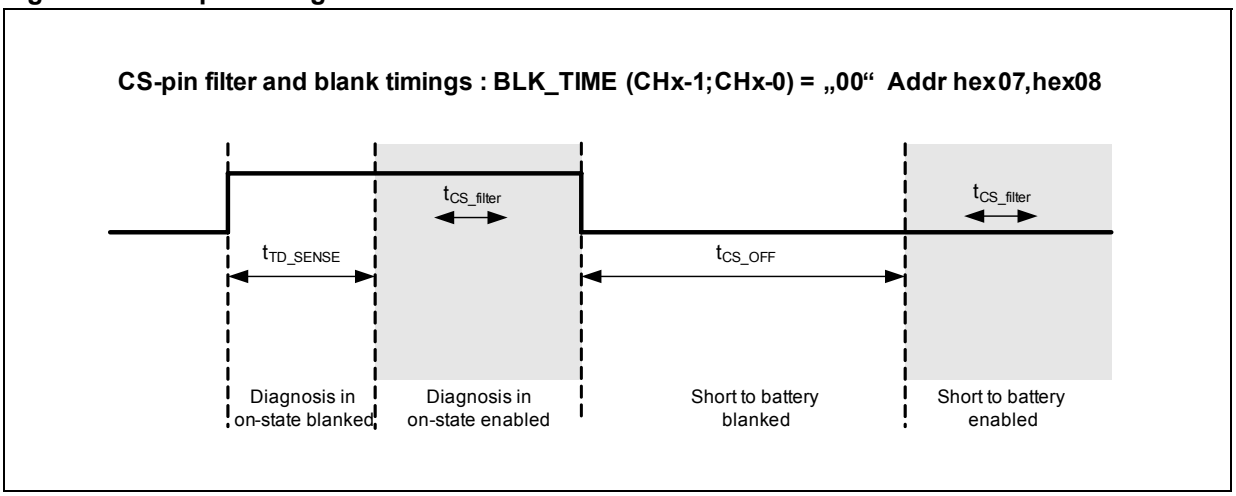


Figure 6. ST pin timing

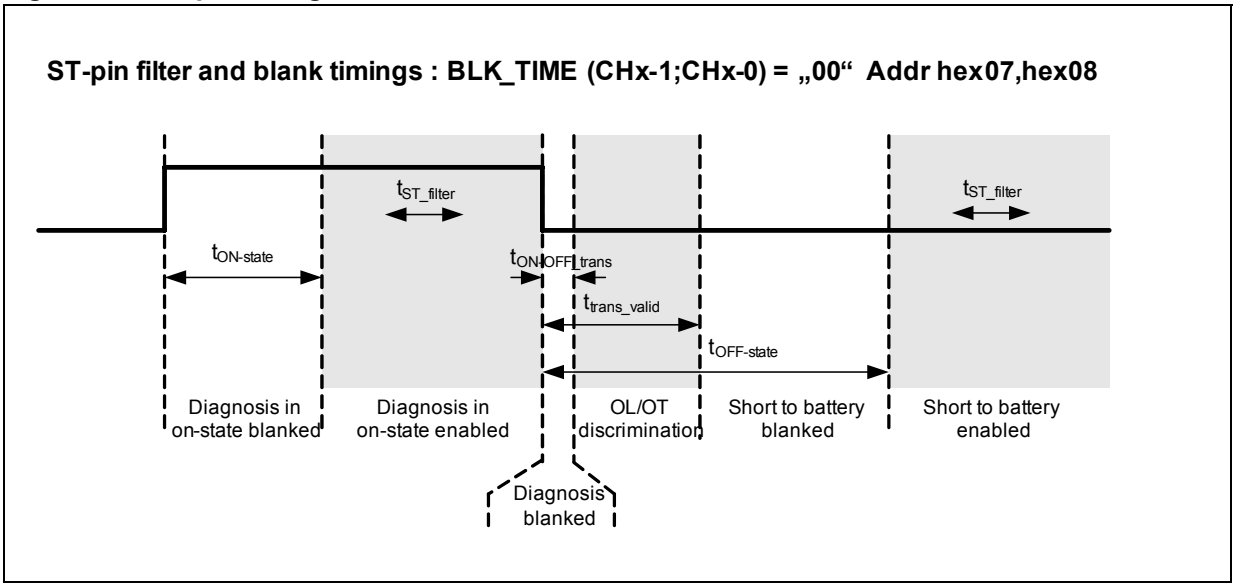


Table 12. MUX_ST/CS output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OUT1mA}	Current mode output saturation voltage	I_{OUT} = 1 mA, VCORE3 = 3.3 V	3.0	-	-	V
V_{OUT3mA}	Current mode output saturation voltage	I_{OUT} = 3 mA, VCORE3 = 3.3 V	2.7	-	-	V
V_{OUT5mA}	Current mode output saturation voltage	I_{OUT} = 5 mA, VCORE3 = 3.3 V	2.6	-	-	V
V_{OUT1mA}	Voltage mode output saturation voltage	I_{OUT} = 1 mA, VCORE3 = 3.3 V	3.1	-	-	V

Table 13. Current MUX_ST/CS ratio

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
k_{0_00}	current MUX_ST/CS ratio @ I_{CS} = 2.04 mA	CFL = 0, OLOVL[1,0] = 0,0	0.790	0.833	0.910	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 2.04 mA		0.780	0.833	0.910	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 2.04 mA		0.760	0.833	0.930	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 2.04 mA		0.700	0.833	0.980	-
k_{0_01}	current MUX_ST/CS ratio @ I_{CS} = 3.4 mA	CFL = 0, OLOVL[1,0] = 0,1	0.470	0.500	0.520	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 3.4 mA		0.470	0.500	0.520	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 3.4 mA		0.470	0.500	0.530	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 3.4 mA		0.450	0.500	0.550	-
k_{0_10}	current MUX_ST/CS ratio @ I_{CS} = 5.1 mA	CFL = 0, OLOVL[1,0] = 1,0	0.310	0.333	0.350	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 5.1 mA		0.310	0.333	0.350	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 5.1 mA		0.300	0.333	0.360	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 5.1 mA		0.300	0.333	0.370	-
k_{0_11}	current MUX_ST/CS ratio @ I_{CS} = 10.2 mA	CFL = 0, OLOVL[1,0] = 1,1	0.150	0.167	0.180	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 10.2 mA		0.150	0.167	0.180	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 10.2 mA		0.150	0.167	0.180	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 10.2 mA		0.150	0.167	0.180	-

Table 13. Current MUX_ST/CS ratio (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
k_{1_00}	current MUX_ST/CS ratio @ I_{CS} = 204 µA	CFL = 1, OLOVL[1,0] = 0,0	8.20	8.33	8.90	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 204 µA		8.15	8.33	8.90	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 204 µA		8.10	8.33	8.90	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 204 µA		7.60	8.33	8.90	-
	current MUX_ST/CS ratio @ I_{CS} = 5 µA		7.30	8.33	8.90	-
k_{1_01}	current MUX_ST/CS ratio @ I_{CS} = 340 µA	CFL = 1, OLOVL[1,0] = 0,1	4.70	5.00	5.30	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 340 µA		4.70	5.00	5.35	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 340 µA		4.70	5.00	5.35	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 340 µA		4.45	5.00	5.45	-
	current MUX_ST/CS ratio @ I_{CS} = 5 µA		4.20	5.00	5.45	-
k_{1_10}	current MUX_ST/CS ratio @ I_{CS} = 510 µA	CFL = 1, OLOVL[1,0] = 1,0	3.10	3.33	3.50	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 510 µA		3.10	3.33	3.50	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 510 µA		3.10	3.33	3.50	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 510 µA		3.10	3.33	3.50	-
	current MUX_ST/CS ratio @ I_{CS} = 5 µA		2.80	3.33	3.70	-

Table 13. Current MUX_ST/CS ratio (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
k_{1_11}	current MUX_ST/CS ratio @ I_{CS} = 1.02 mA	CFL = 1, OLOVL[1,0] = 1,1	1.50	1.67	1.80	-
	current MUX_ST/CS ratio @ I_{CS} = 70% * 1.02 mA		1.50	1.67	1.80	-
	current MUX_ST/CS ratio @ I_{CS} = 35% * 1.02 mA		1.50	1.67	1.80	-
	current MUX_ST/CS ratio @ I_{CS} = 5% * 1.02 mA		1.50	1.67	1.80	-
	current MUX_ST/CS ratio @ I_{CS} = 5 µA		1.25	1.67	1.90	-

Figure 7. MUX_ST/CS ratio

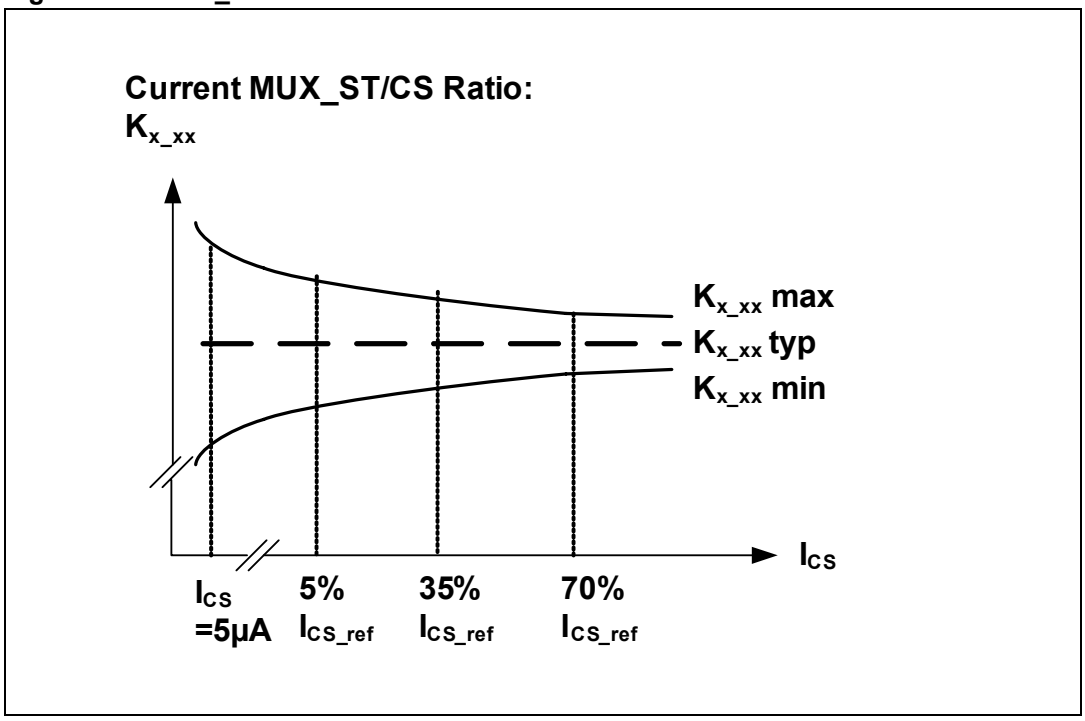


Table 14. Current sense diagnostic thresholds

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{OPLD}	Open-load detection current threshold (1:1)	CFL = 1, OLOVL[1,0] = 0,0	3.5	5	6.5	µA
		CFL = 1, OLOVL[1,0] = 0,1	3.5	5	6.5	
		CFL = 1, OLOVL[1,0] = 1,0	6	10	13	
		CFL = 1, OLOVL[1,0] = 1,1	31	40	47	
	Open-load detection current threshold (1:10)	CFL = 0, OLOVL[1,0] = 0,0	35	50	65	µA
		CFL = 0, OLOVL[1,0] = 0,1	35	50	65	
		CFL = 0, OLOVL[1,0] = 1,0	60	100	130	
		CFL = 0, OLOVL[1,0] = 1,1	310	400	470	
I_{OVLD}	Overload detection current threshold (1:1)	CFL = 1, OLOVL[1,0] = 0,0	90	120	150	µA
		CFL = 1, OLOVL[1,0] = 0,1	190	240	290	
		CFL = 1, OLOVL[1,0] = 1,0	300	360	420	
		CFL = 1, OLOVL[1,0] = 1,1	490	600	720	
	Overload detection current threshold (1:10)	CFL = 0, OLOVL[1,0] = 0,0	0.9	1.2	1.5	mA
		CFL = 0, OLOVL[1,0] = 0,1	1.9	2.4	2.9	
		CFL = 0, OLOVL[1,0] = 1,0	3.0	3.6	4.2	
		CFL = 0, OLOVL[1,0] = 1,1	4.9	6.0	7.2	
I_{OVTEMP}	Over temperature		4.9	6.0	7.2	mA

Table 15. LHOMEN and SYNC pin

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	I_{out} = 5 mA		-	0.4	V
V_{OH}	Output high voltage	I_{out} = 5 mA	VDDIO – 1.0	-		V
$V_{CLAMP}P$	Positive clamping voltage		7	-	10	V
$V_{CLAMP}N$	Negative clamping voltage		-20	-	-16	V

An external pull down of 10 kOhm is recommended to guarantee sufficient low level in case of VDDIO is not connected.

6 SPI

VDDIO = 3.15 V to 5.25 V, VCORE3 = 3.15 V to 3.4 V, T_j = -40 to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin

Table 16. DC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
SDI, SCK, CSN, CLK_INx						
V_{IL}	Input low voltage	VDDIO = 3.3 V, increasing			2.0	V
V_{IH}	Input high voltage	VDDIO = 3.3 V, decreasing	1.2			V
$R_{CSN\ in}$	CSN pull up resistor		110	150	210	kΩ
$R_{SCK\ in}$	SCK pull down resistor		50	100	150	kΩ
$R_{SDI\ in}$	SDI pull down resistor		50	100	150	kΩ
R_{CLK_INx}	CLK_INx pull down resistor		50	100	150	kΩ
$V_{CLAMP}P$	Positive clamping voltage		7		10	V
$V_{CLAMP}N$	Negative clamping voltage		-20		-16	V
SDO						
V_{OL}	Output low voltage	I_{out} = 5 mA			0.4	V
V_{OH}	Output high voltage	I_{out} = 5 mA	VDDIO – 1.0			V
$V_{CLAMP}P$	Positive clamping voltage		7		10	V
$V_{CLAMP}N$	Negative clamping voltage		-20		-16	V

Table 17. Dynamic characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
f_{SCK}	Serial clock frequency			1	4	MHz
t_{CSNQV}	CSN falling until SDO valid	C_{out} = 50 pF			50	ns
t_{CSNQT}	CSN rising until SDO tristate	C_{out} = 50 pF			150	ns
t_{SCKQV}	SCK rising until SDO valid	C_{out} = 50 pF			100	ns
t_{SCSN}	CSN setup time before SCK rising		125			ns
t_{SSDI}	SDI setup time before SCK rising		20			ns
t_{HSCK}	Minimum SCK high time		100			ns
t_{LSCK}	Minimum SCK low time		100			ns

Table 17. Dynamic characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{HCSN}	Minimum CSN high time		5			µs
t_{SSCK}	SCK setup time before NCS rising		50			ns

6.1 SPI timing parameter definition

Figure 8. SPI timing diagram

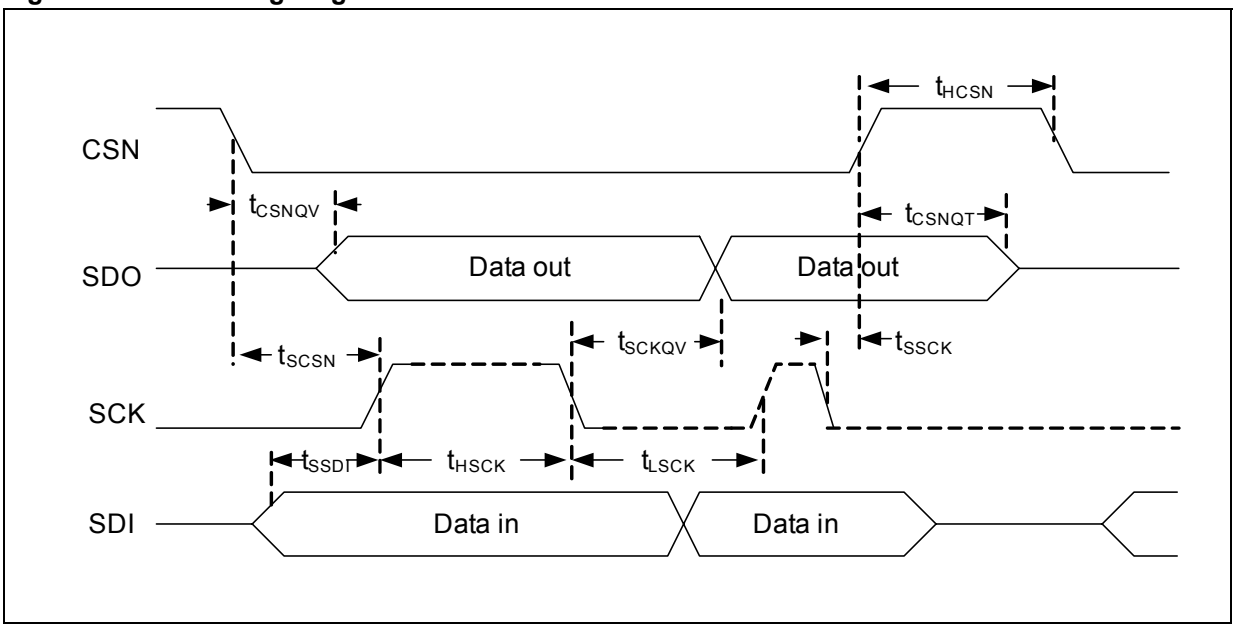


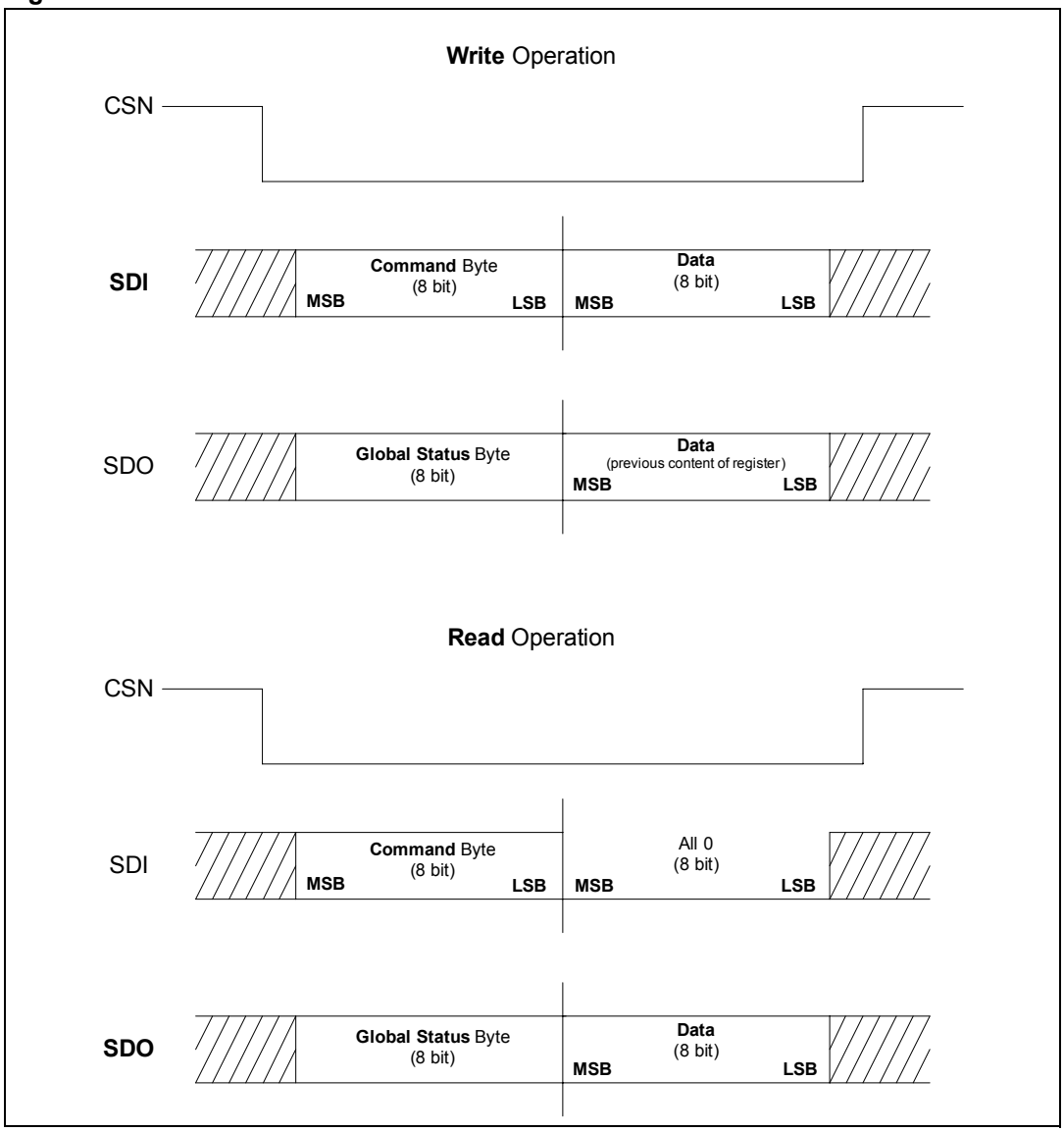
Table 18. CSN timeout/CLK_INx timings

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{CSN\_TIMEOUT}$	CSN timeout 50ms		50		72	ms
	CSN timeout 100ms		100		145	ms
	CSN timeout 200ms		200		285	ms
	CSN timeout 400ms		400		570	ms
f_{FAIL}	CLK_INx fail detected		4.8	5.0	6.2	kHz
$f_{OK\_}$	CLK_INx ok detected		5.2	7.0	9.2	kHz
f_{CLK_INx}	CLK_INx frequency range				102.4	kHz

6.2 Functional description of the SPI

This device uses a 16 bit SPI slave protocol structured according to the ST SPI Standard to communicate with a microcontroller.

Figure 9. SPI frame structure



6.2.1 Serial clock (SCK)

This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK). Data on Serial Data Out (SDO) is shifted out at the falling edge of Serial Clock (SCK).

The writing to the selected data input register is only enabled if exactly one frame length is transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored and a SPI frame error is signaled in the Global Status register. This safety function is implemented to avoid an unwanted activation of output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

6.2.2 Serial data input (SDI)

This input is used to transfer data serially into the device. It receives the data to be written. Values are latched on the rising edge of Serial Clock (SCK).

6.2.3 Serial data output (SDO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

SDO also reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status Register>) while CSN is low and no clock signal is present

6.2.4 Chip select not (CSN)

When this input signal is High, the communication interface of the device is deselected and Serial Data Output (SDO) is high impedance. Driving this input Low enables the communication. The communication must start and stop on a Low level of Serial Clock (SCK). A CSN timeout is implemented.

6.3 SPI communication flow

6.3.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines. Each communication frame consists of an instruction byte which is followed by 1 data byte.

The data returned on DO within the same frame always starts with the <Global Status> Byte. It provides general status information about the device. It is followed by 1 data byte containing the current of the addressed register (i. e. ‘In-frame-response’).

6.3.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Fault Reset>, <Read Device Information>) and a 6 bit address.

Table 19. Command byte

Command byte							
MSB							**LSB**
Op code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

Note: OCx: Operating Code

Ax: Address

6.3.3 Operating code definition

Table 20. Operating code definition

OC1	OC0	Description
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Clear Status>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device, e.g. write to control registers or read status information.

A <Clear Status> Operation addressed to a device specific status register will read back and subsequently clear this status register. A <Clear Status> Operation with address 3FH clears all status registers at a time and reads back the <Configuration> byte.

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version and register width.

6.3.4 Global status byte

Table 21. Global status byte

Bit	7	6	5	4	3	2	1	0
Name	Global error flag	Communication error	No (chip reset or communication error)	Over temp/ over load	n/a	Open-load	STK_ON	Fail save

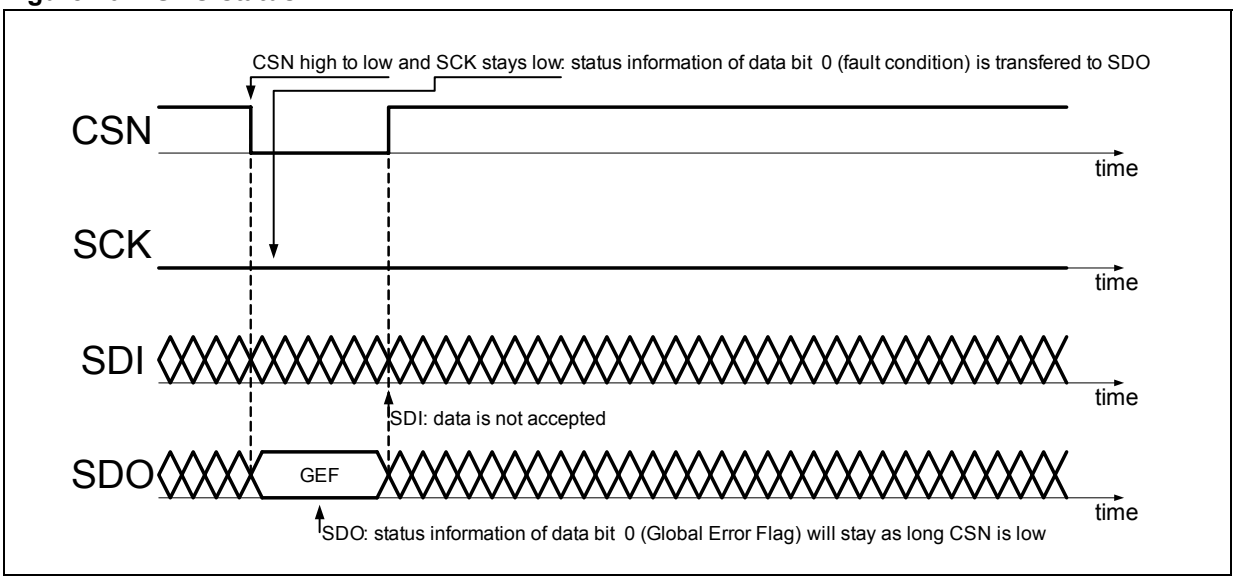
Table 22. Global status byte: description

Name	Polarity	Comment
Global error flag	Active high	Logical OR combination of all failures in the <Global Status Register> (initially set to '1').
Communication error	Active high	Set if the number of clock cycles during CSN low does not match with the specified frame width. SDI stuck at '0' will force the LHOME-bit to be cleared and is not signaled as a communication error. SDI stuck at '1' will lead to a software reset and is therefore not signaled as a communication error. FAIL SAVE is entered in both cases.

Table 22. Global status byte: description (continued)

Name	Polarity	Comment
No (chip reset or communication error)	Active low	Activated by all internal reset events which change the device state or configuration registers (e.g. software reset, VCORE3 undervoltage, etc.). This bit is initially '0' and will be set to '1' by a valid SPI communication to any register.
Over temp/ over load	Active high	Set when over temp and/or over load failure is detected by the diagnosis function
n/a	0	Not implemented
Open-load	Active high	Set when open-load failure is detected by the diagnosis function
STK_ON	Active high	Set when SHORT TO BATTERY is detected by the diagnosis function (OFF state diagnosis)
Fail save	Active high	Indicates if the device is in FAIL SAVE (defined state)

Figure 10. SDO status



Note: In case of a status change during an SPI transmission this status will not be read and therefore not cleared in case of a clear command.

Due to the internal mechanism of loading the status data into the shift register a possible inconsistency between the GlobalErrorRegister and the read StatusRegister can occur. In this case, the data in the Status Register is always the more actual data.

6.4 SPI – control and status register

Table 23. RAM memory map

Address	Name	Access	Content
hex00	CTRL	Read/write	Control register
hex01	ON_OFF	Read/write	Switch On or OFF the output
hex02	DEV_TYPE	Read/write	Device type register (write protected if channel ON)
hex03	PWM_EN	Read/write	PWM mode enable register
hex04	CLK_SEL	Read/write	Clock input signal selection register
hex05	ASDT	Read/write	Automatic shutdown register
hex06	DET_DIAG_N	Read/write	Detailed diagnosis disable
hex07	BLK_TIME1	Read/write	Blank time 1 (write protected if channel ON)
hex08	BLK_TIME2	Read/write	Blank time 2 (write protected if channel ON)
hex09	TD_SENSE	Read/write	Td_SENSE (write protected if channel ON)
hex0A	CFR	Read/write	Current feedback ratio register
hex0B	OLOVL_TH1	Read/write	Open-load/Over load 1 threshold settings
hex0C	OLOVL_TH2	Read/write	Open-load/Over load 2 threshold settings
hex10	DUTY_CH 0	Read/write	PWM duty cycle selection – channel O0
hex11	DUTY_CH 1	Read/write	PWM duty cycle selection – channel O1
hex12	DUTY_CH 2	Read/write	PWM duty cycle selection – channel O2
hex13	DUTY_CH 3	Read/write	PWM duty cycle selection – channel O3
hex14	DUTY_CH 4	Read/write	PWM duty cycle selection – channel O4
hex15	DUTY_CH 5	Read/write	PWM duty cycle selection – channel O5
hex16	DUTY_CH 6	Read/write	PWM duty cycle selection – channel O6
hex17	DUTY_CH 7	Read/write	PWM duty cycle selection – channel O7
hex18	PHASE_CH 0	Read/write	Phase shift setting register – channel O0
hex19	PHASE_CH 1	Read/write	Phase shift setting register – channel O1
hex1A	PHASE_CH 2	Read/write	Phase shift setting register – channel O2
hex1B	PHASE_CH 3	Read/write	Phase shift setting register – channel O3
hex1C	PHASE_CH 4	Read/write	Phase shift setting register – channel O4
hex1D	PHASE_CH 5	Read/write	Phase shift setting register – channel O5
hex1E	PHASE_CH 6	Read/write	Phase shift setting register – channel O6
hex1F	PHASE_CH 7	Read/write	Phase shift setting register – channel O7
hex2E	CHANNEL_FB	Read	Read back of OUTx state
hex2F	AUX_STATUS	Read/clear	Auxiliary warning flag registers
hex30	OT_FAULT	Read/clear	Overtemperature failure register
hex31	OL_FAULT	Read/clear	Open-load in ON state failure register

Table 23. RAM memory map (continued)

Address	Name	Access	Content
hex32	STK_FAULT	Read/clear	STK ON/OLOFF failure register
hex33	OVL_FAULT	Read/clear	Overload failure register

Table 24. ROM memory map (access with OC0 and OC1 set to '1')

Address	Name	Access	Content
0x00	ID header	Read only	hex43 (device class ASSP, 2 additional information bytes)
0x01	Version	Read only	hex00 (engineering samples) (ST-SPI)
0x02	ProducCode1	Read only	hex25 (ST-SPI)
0x03	ProducCode2	Read only	hex50 (ST-SPI)
0x3E	SPI frame ID	Read only	hex01 SPI-Frame-ID register (ST-SPI)

Table 25. Control register, hex00 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUX_EN	MUX_C	MUX_B	MUX_A	CS_MON1	CS_MON0	-	LHOMEN

MUX_EN 0 the multiplexer MUX ST/CS pin is inactive (tristate)

1 the multiplexer MUX ST/CS pin is active (default)

MUX_A …MUX_C - STATUS/CSENSE multiplexer pin – selection of one signal (ST0/CS0 … ST7/CS7) to MUX ST/CS pin

MUX_C	MUX_B	MUX_A	
0	0	0	ST0/CS0 signal is transferred to MUX ST/CS pin (default)
0	0	1	ST1/CS1 signal is transferred to MUX ST/CS pin
0	1	0	ST2/CS2 signal is transferred to MUX ST/CS pin
0	1	1	ST3/CS3 signal is transferred to MUX ST/CS pin
1	0	0	ST4/CS4 signal is transferred to MUX ST/CS pin
1	0	1	ST5/CS5 signal is transferred to MUX ST/CS pin
1	1	0	ST6/CS6 signal is transferred to MUX ST/CS pin
1	1	1	ST7/CS7 signal is transferred to MUX ST/CS pin

CS_MONITOR1, CS_MONITOR 0: select one out of the 4 different ChipSelectTimeouts, served by CSN. The internal counter is reset by the rising edge of the CSN pin. When a Timeout occurs the device enters FAIL SAFE mode (LimpHome).

CS_MONITOR1	CS_MONITOR0	
0	0	max time for serving the CSN set to 50ms
0	1	max time for serving the CSN set to 100ms (default)

1	0	max time for serving the CSN set to 200ms
1	1	max time for serving the CSN set to 400ms

Table 26. ON_OFF register, hex01 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 Ox channel is switched off (default)

1 Ox channel is switched on

CHx Output Ox

Table 27. DEV_TYPE register, hex02 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 Digital device is connected to device output (default)

1 Analog device is connected to device output

Note: If a channel is in ON-state (ON_OFF reg = '1'), the corresponding DEV_TYPE register is write protected.

Table 28. PWM_EN register, hex03 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 If OUTx in ON_OFF register is 1, OUTx is switched in steady state mode (default)

1 If OUTx in ON_OFF register is 1, OUTx is switched in PWM mode

CHx Enables PWM mode on output Ox

Table 29. CLK_SEL register, hex04 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 The external clock source signal CLK_IN0 is selected for internal generation of PWM signal for OUTx channel. The PWM period is the received clock signal divided by 256 (default).

1 The external clock source signal CLK_IN1 is selected for internal generation of PWM signal for OUTx channel. The PWM period is the received clock signal divided by 256.

CHx PWM input signal selection for Ox channel

Table 30. ASDT register, hex05 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 Automatic shutdown of thermal cycling is switched off

1 Automatic shutdown of thermal cycling is switched on (default)

Setting the ASDT bit to 1 means the automatic shutdown function is switched ON and the channel is switched OFF after setting the OT_FAULT (over temperature or power limitation) bit to 1. This can happen with a digital HSD either reaching the thermal shut down (or power limitation) or detecting ambiguous failure with OT_FAULT.

Note, that the thermal shutdown is detected at 6mA regardless of the current range

After OT_FAULT register is “Read & Cleared” (clear status code, see 6.6), the device activates the corresponding channel after clear according to setting.

Table 31. DET_DIAG register, hex06 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 Automatic detailed diagnosis is disabled.

1 Automatic detailed diagnosis is enabled, switching off is activated when failure in on-state is detected. The purpose is to have short off-state (27 µs typ +/-6us) in order to have detailed information of the failure. The delay between discriminating pulses is 4 ms (default).

Table 32. BLK_TIME1 register, hex07 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7-1	CH7-0	CH6-1	CH6-0	CH5-1	CH5-0	CH4-1	CH4-0

Table 33. BLK_TIME2 register, hex08 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH3-1	CH3-0	CH2-1	CH2-0	CH1-1	CH1-0	CH0-1	CH0-0

BLK_TIME (CHx-1;CHx-0)

0 0 The blank time is not active after activation of the related channel.

0 1 The blank time is active after activation of the related channel and set to 15 ms (minimum).

1 0 The blank time is active after activation of the related channel and set to 70 ms (minimum).

1 1 The blank time is active after activation of the related channel and set to 200ms (minimum) (default).

The duration of the blank time can be set to three different timings in order to avoid any wrong detection of failures during an inrush phase when switching on the load. During this time the diagnostics doesn't report any failures.

Note: The Blanking time is started by turning the selected channel on. Write command to address 0x00 with a '1' (former state '0' => OFF).

If a channel is in on-state (ON_OFF reg = '1'), the corresponding BLK_TIMEx register is write protected.

Table 34. TD_SENSE register, hex09 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 the diagnosis is activated 300 µs(min) after the rising edge of the output OUTx

1 the diagnosis is activated 600 µs(min) after the rising edge of the output OUTx (default)

Note: This blanking time is just used for analog devices and is related to the analog device connected to the device (see VIP specification).

If a channel is in ON-state (ON_OFF reg = '1'), the corresponding TD_SENSE register is write protected.

Table 35. CFR register, hex0A (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

The variable gain of Current sense feedback ratio for ST/CS channels (ST0/CS0 … ST7/CS7). It is applied between the ST/CSx input signal current and both, internal diagnostics and MUX_CS/ST signal current.

CFR 0 the gain of current sense signal to internal current comparator is 1:10 (default)

1 the gain of current sense signal to internal current comparator is 1:1

Table 36. OLOVL_TH_1 register, hex0B (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7-1	CH7-0	CH6-1	CH6-0	CH5-1	CH5-0	CH4-1	CH4-0

Open-load threshold values for ST/CS channels (ST4/CS4 … ST7/CS7).

CH 1,0 0 x 50 µA(CFL=0), 5 µA(CFL=1) (default)

1 0 100 µA(CFL=0), 10 µA(CFL=1)

1 1 400 µA(CFL=0), 40 µA(CFL=1)

Overload threshold values for ST/CS channels (ST4/CS4 … ST7/CS7).

CH 1,0 0 0 1.2 mA(CFL=0), 120 µA(CFL=1) (default)

0 1 2.4 mA(CFL=0), 240 µA(CFL=1)

1 0 3.6 mA(CFL=0), 360 µA(CFL=1)

1 1 6.0 mA(CFL=0), 600 µA(CFL=1)

Table 37. OLOVL_TH_2 register, hex0C (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH3-1	CH3-0	CH2-1	CH2-0	CH1-1	CH1-0	CH0-1	CH0-0

Open-load threshold values for ST/CS channels (ST0/CS0 … ST3/CS3).

CH 1,0 0 x 50 µA(CFL=0), 5 µA(CFL=1) (default)

1 0 100 µA(CFL=0), 10 µA(CFL=1)

1 1 400 µA(CFL=0), 40 µA(CFL=1)

Overload threshold values for ST/CS channels (ST0/CS0 … ST3/CS3).

CH 1,0 0 0 1.2 mA(CFL=0), 120 µA(CFL=1) (default)

0 1 2.4 mA(CFL=0), 240 µA(CFL=1)

1 0 3.6 mA(CFL=0), 360 µA(CFL=1)

1 1 6.0 mA(CFL=0), 600 µA(CFL=1)

Table 38. DUTY_CH 0 – DUTY_CH 7 Registers, hex10 – hex17 (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
b7	b6	b5	b4	b3	b2	b1	b0

Output PWM duty cycle selection, one register per channel. Active only if PWM_EN signal is set for dedicated output.

b7 … b1 - PWM duty cycle of this channel (256 levels, default value – 50% DC, 80H)

Note: The values of the duty cycle and the Phase will be captured and executed with the end of the write command. Be aware, that an unwanted PWM can be generated during this phase.

Table 39. PHASE_CH 0 - PHASE_CH7 Registers, hex18 – hex1F (RW-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
b7	b6	b5	b4	b3	-	-	-

Output PWM phase shift selection, one register per channel. This feature will improve the power net characteristic during PWM mode.

b7 … b3 - phase shift of this channel related to the length of 1 PWM period (5 bits - 32 levels).

Default values:

PHASE_CH0	0x00h	(0/32)
PHASE_CH1	0x20h	(4/32)
PHASE_CH2	0x40h	(8/32)
PHASE_CH3	0x60h	(12/32)
PHASE_CH4	0x80h	(16/32)
PHASE_CH5	0xA0h	(20/32)
PHASE_CH6	0xC0h	(24/32)
PHASE_CH7	0xE0h	(28/32)

Note: The values of the duty cycle and the phase will be captured and executed with the end of the write command. Be aware, that an unwanted PWM can be generated during this phase.

Table 40. CHANNEL_FB Registers, hex2E (R-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 channel CH x is off

1 channel CH x is on

Table 41. AUX_STATUS Registers, hex2F (RC-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CS_time50%	CS_timeout	-	-	CLK_IN1 Warm	CLK_IN0 Warm

CLK_IN0 Warn, CLK_IN1 Warn: the corresponding warn bit is set when the input frequency is below 5kHz (f_{PWMmin_set} = 19 Hz) and reset when the frequency is above 7 kHz f_{PWMmin_reset} = 28 Hz. The hysteresis was implemented not to get a flickering on the PWM output. If the warn bit is set the PWM is generated by an internally generated signal (f = 122 Hz). The warn bit does not set the global error flag.

CLK_INx Warn 0 input clock frequency f_{CLK_INx} > 7 kHz.

1 input clock frequency f_{CLK_INx} < 5 kHz (f_{PWMmin} < 19 Hz). The internal generated PWM clock signal is used.

CS_timeout this bit is set when a CS-timeout occurred. It has to be cleared by a clear command (Op code b10)

CS_time50% this bit is set when 50% of the CS-timeout time is reached.

Table 42. OT_FAULT Registers, hex30 (RC-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 on channel CHx wasn't detected dedicated failure

1 on channel CHx was detected dedicated failure

Note: If a digital device and no detailed diagnosis is selected, also ambiguous failures are reflected in this register (channel is turned off if ASDT is selected).

Table 43. OL_FAULT Registers, hex31 (RC-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 on channel CHx wasn't detected dedicated failure

1 on channel CHx was detected dedicated failure

Note: 1 In digital mode, the OL failure can not be cleared in off-state when detailed diagnosis is disabled. To clear the OL bit, the detailed diagnosis has to be enabled or the failure has to be removed and cleared in on-state.

2 If a digital device and no detailed diagnosis is selected, also ambiguous failures are reflected in this register.

Table 44. STK_FAULT Registers, hex32 (RC-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 on channel CHx wasn't detected dedicated failure

1 on channel CHx was detected dedicated failure

Table 45. OVL_FAULT Registers, hex33 (RC-Type)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHx 0 on channel CHx wasn't detected dedicated failure

1 on channel CHx was detected dedicated failure

7 Package and packing information

7.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

7.2 LQFP32 mechanical data

Figure 11. LQFP32 outline

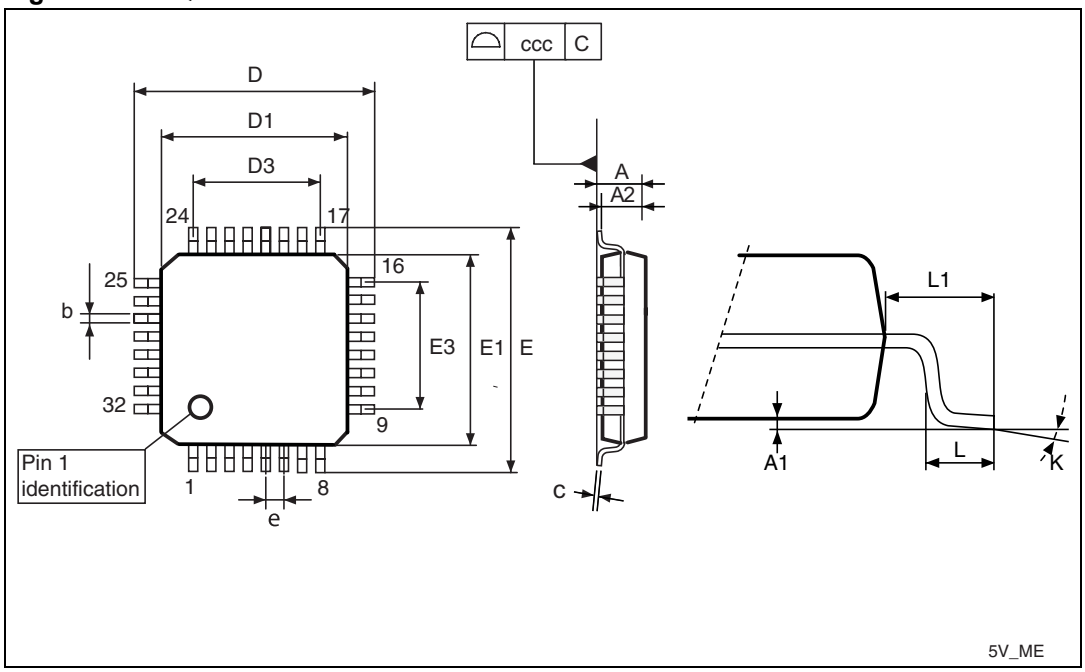


Table 46. LQFP32 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.3	0.37	0.45
c	0.09		0.2
D	8.8	9	9.2
D1	6.8	7	7.2
D3		5.6	

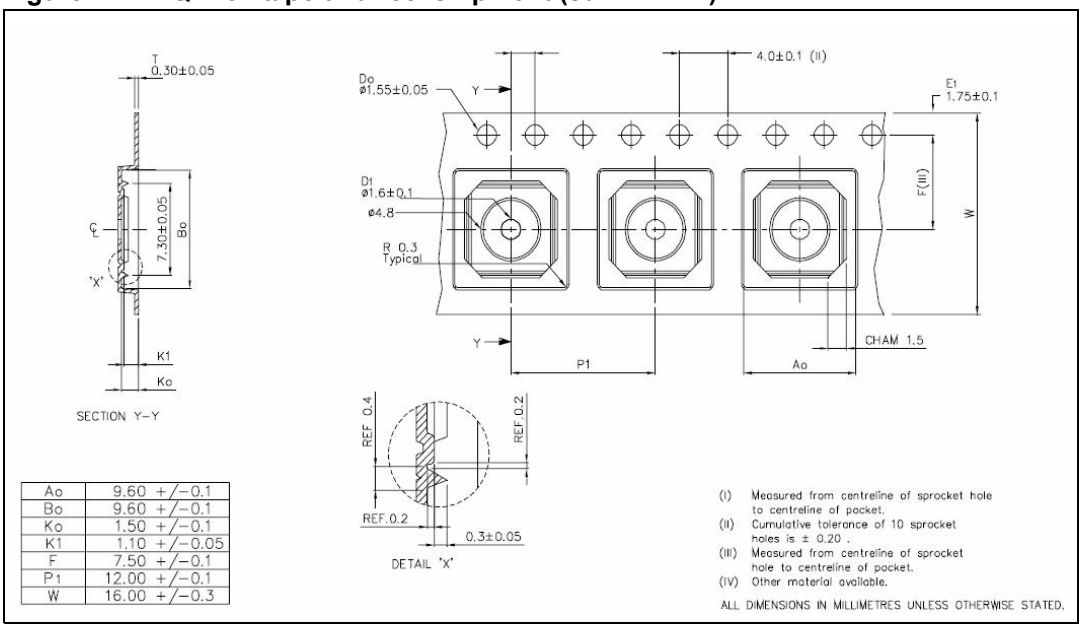
Table 46. LQFP32 mechanical data (continued)

Symbol	millimeters		
	Min	Typ	Max
E	8.8	9	9.2
E1	6.8	7	7.2
E3		5.6	
e		0.8	
L	0.45	0.6	0.75
L1		1	
k	0.0°	3.5°	7.0°
ccc			0.1

7.3 LQFP32 packing information

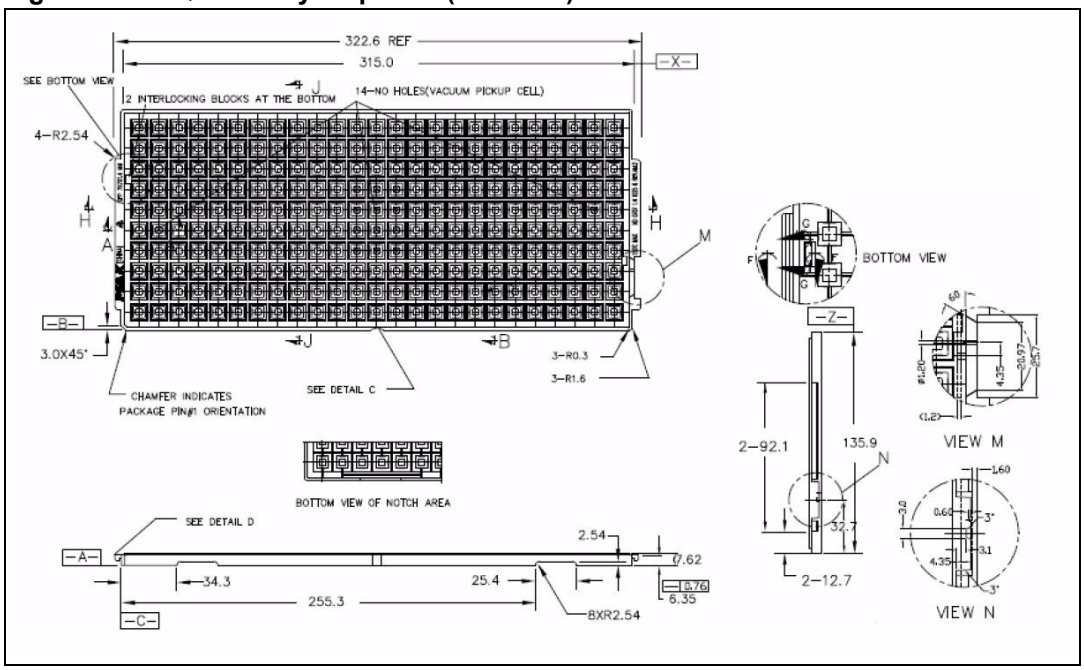
The devices can be packed in tube or tape and reel shipments (see the *Summary device on page 1* for packaging quantities).

Figure 12. LQFP32 tape and reel shipment (suffix “TR”)



Ao	9.60 +/−0.1
Bo	9.60 +/−0.1
Ko	1.50 +/−0.1
K1	1.10 +/−0.05
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Figure 13. LQFP32 tray shipment (no suffix)



8 Revision history

Table 47. Document revision history

Date	Revision	Changes
16-Jun-2009	1	Initial release.
16-Jul-2009	2	Updated *Table 7: Supply*, *Table 11: Current sense/status inputs*, *Table 12: MUX_ST/CS output*, *Table 13: Current MUX_ST/CS ratio*, *Table 14: Current sense diagnostic thresholds* and *Table 16: DC characteristics*.
09-Apr-2010	3	Changed status device from target specification to datasheet.

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