

SN74AUCH32244

32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES412B – SEPTEMBER 2002 – REVISED DECEMBER 2002

- Member of the Texas Instruments Widebus+™ Family
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max t_{pd} of 1.8 ns at 1.8 V
- Low Power Consumption, 40- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 32-bit buffer/driver is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUCH32244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74AUCH32244GKER	MK244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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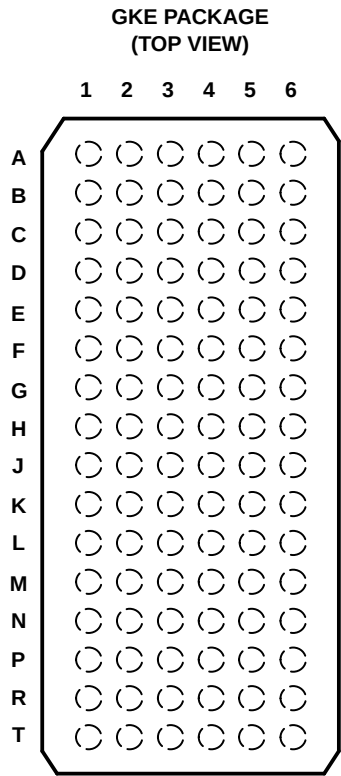
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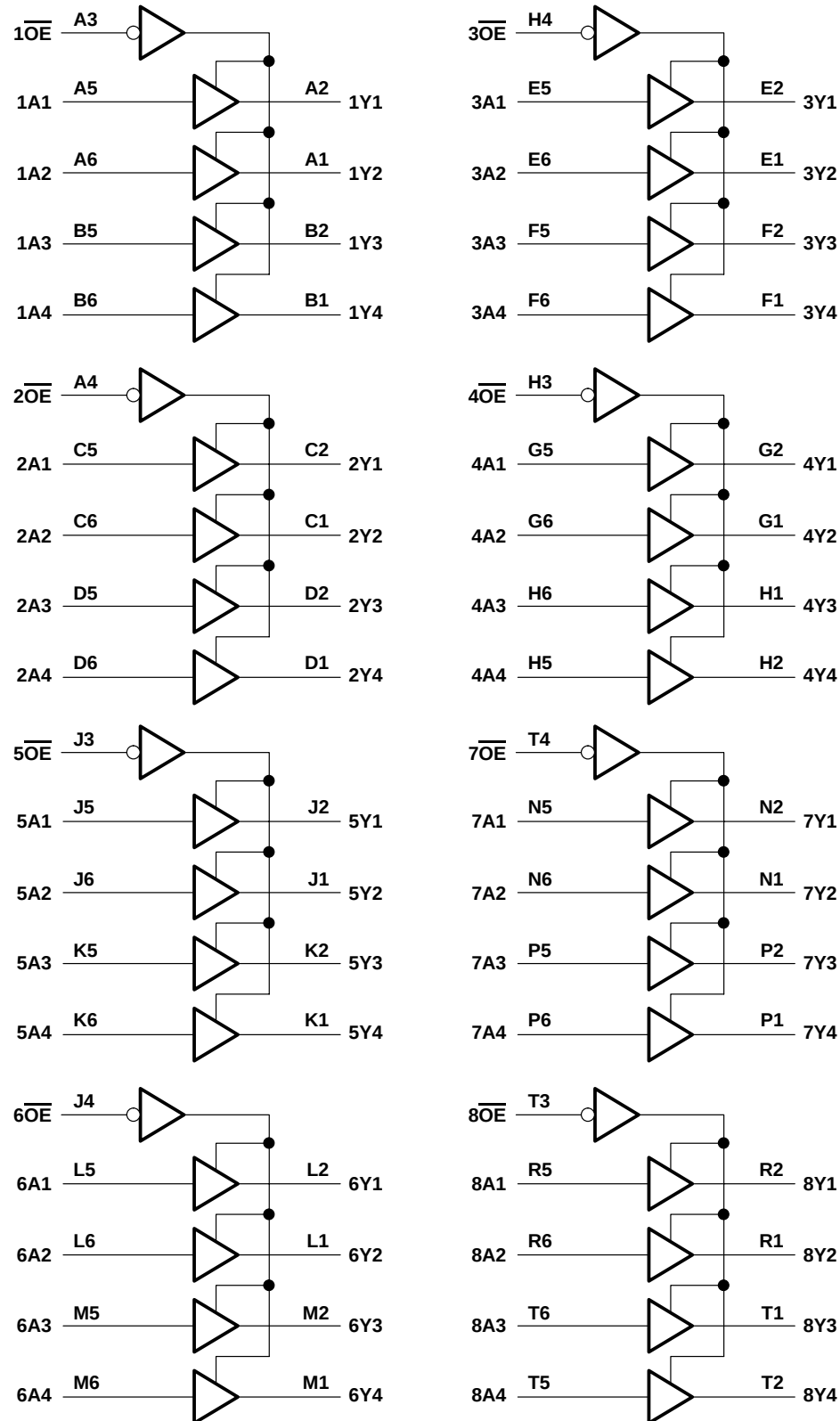
terminal assignments

	1	2	3	4	5	6
A	1Y2	1Y1	1OE	2OE	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	VCC	VCC	2A1	2A2
D	2Y4	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	VCC	VCC	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	4OE	3OE	4A4	4A3
J	5Y2	5Y1	5OE	6OE	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	VCC	VCC	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	VCC	VCC	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	8OE	7OE	8A4	8A3

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



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SCES412B – SEPTEMBER 2002 – REVISED DECEMBER 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 3.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 3.6 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±20 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2)	40°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8$ V	V_{CC}	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8$ V	0	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	Active state	0	V
		3-state	0	
I_{OH}	High-level output current	$V_{CC} = 0.8$ V	–0.7	mA
		$V_{CC} = 1.1$ V	–3	
		$V_{CC} = 1.4$ V	–5	
		$V_{CC} = 1.65$ V	–8	
		$V_{CC} = 2.3$ V	–9	
I_{OL}	Low-level output current	$V_{CC} = 0.8$ V	0.7	mA
		$V_{CC} = 1.1$ V	3	
		$V_{CC} = 1.4$ V	5	
		$V_{CC} = 1.65$ V	8	
		$V_{CC} = 2.3$ V	9	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8$ V	20	ns/V
		$V_{CC} = 1.3$ V	15	
		$V_{CC} = 1.6$ V, 1.95 V, and 2.7 V	10	
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES412B – SEPTEMBER 2002 – REVISED DECEMBER 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = –100 µA		0.8 V to 2.7 V	V _{CC} –0.1			V
	I _{OH} = –0.7 mA		0.8 V	0.55			
	I _{OH} = –3 mA		1.1 V	0.8			
	I _{OH} = –5 mA		1.4 V	1			
	I _{OH} = –8 mA		1.65 V	1.2			
	I _{OH} = –9 mA		2.3 V	1.8			
V _{OL}	I _{OL} = 100 µA		0.8 V to 2.7 V	0.2			V
	I _{OL} = 0.7 mA		0.8 V	0.25			
	I _{OL} = 3 mA		1.1 V	0.3			
	I _{OL} = 5 mA		1.4 V	0.4			
	I _{OL} = 8 mA		1.65 V	0.45			
	I _{OL} = 9 mA		2.3 V	0.6			
I _I	A or $\overline{\text{OE}}$ inputs	V _I = V _{CC} or GND	0 to 2.7 V			±5	µA
I _{BHL} [‡]	V _I = 0.35 V		1.1 V	10			µA
	V _I = 0.47 V		1.4 V	15			
	V _I = 0.57 V		1.65 V	20			
	V _I = 0.7 V		2.3 V	40			
I _{BHH} [§]	V _I = 0.8 V		1.1 V	–10			µA
	V _I = 0.9 V		1.4 V	–15			
	V _I = 1.07 V		1.65 V	–20			
	V _I = 1.7 V		2.3 V	–40			
I _{BHLO} [¶]	V _I = 0 to V _{CC}		1.3 V	75			µA
			1.6 V	125			
			1.95 V	175			
			2.7 V	275			
I _{BHHO} [#]	V _I = 0 to V _{CC}		1.3 V	–75			µA
			1.6 V	–125			
			1.95 V	–175			
			2.7 V	–275			
I _{off}	V _I or V _O = 2.7 V		0			±10	µA
I _{OZ}	V _O = V _{CC} or GND		2.7 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0		0.8 V to 2.7 V			40	µA
C _i	V _I = V _{CC} or GND		2.5 V		3	4.5	pF
C _o	V _O = V _{CC} or GND		2.5 V		4	7	pF

[†] All typical values are at T_A = 25°C.

[‡] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[§] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.



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SCES412B – SEPTEMBER 2002 – REVISED DECEMBER 2002

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

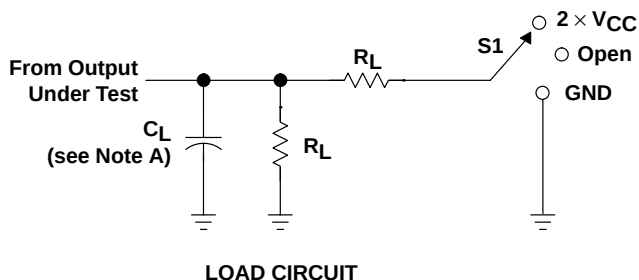
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	5.4	0.8	2.8	0.6	1.9	0.7	1.3	1.8	0.5	1.8	ns
t _{en}	$\overline{\text{OE}}$	Y	8	1	4.4	0.7	2.6	0.8	1.4	2.5	0.6	1.9	ns
t _{dis}	$\overline{\text{OE}}$	Y	12	1.9	4.9	1	4.6	1.5	2.6	4	0.5	2	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	Outputs enabled	f = 10 MHz		21	22	23	25	30	pF
	Outputs disabled			1	1	1	1	1	

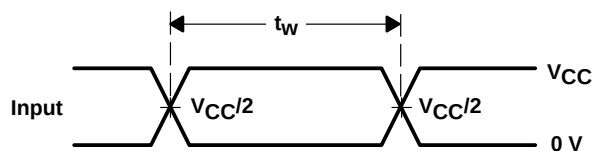


PARAMETER MEASUREMENT INFORMATION

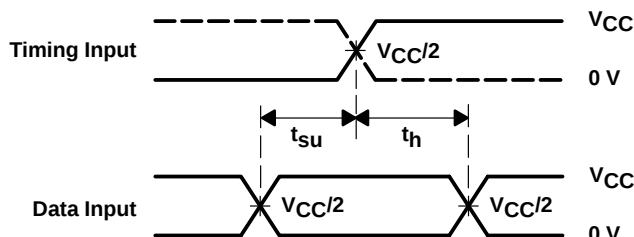


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

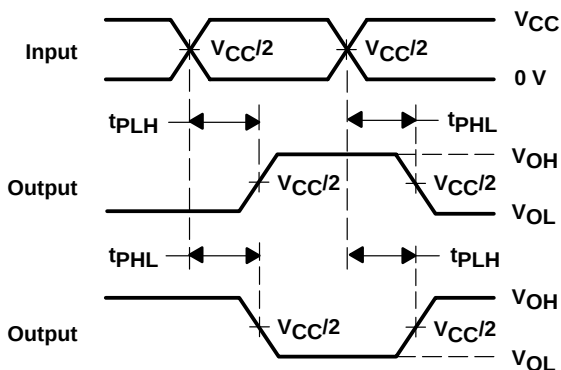
V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



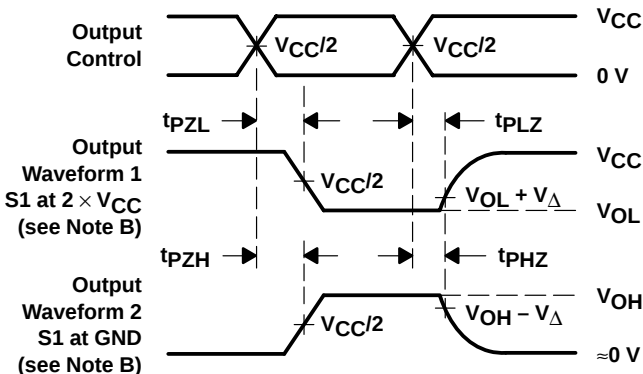
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



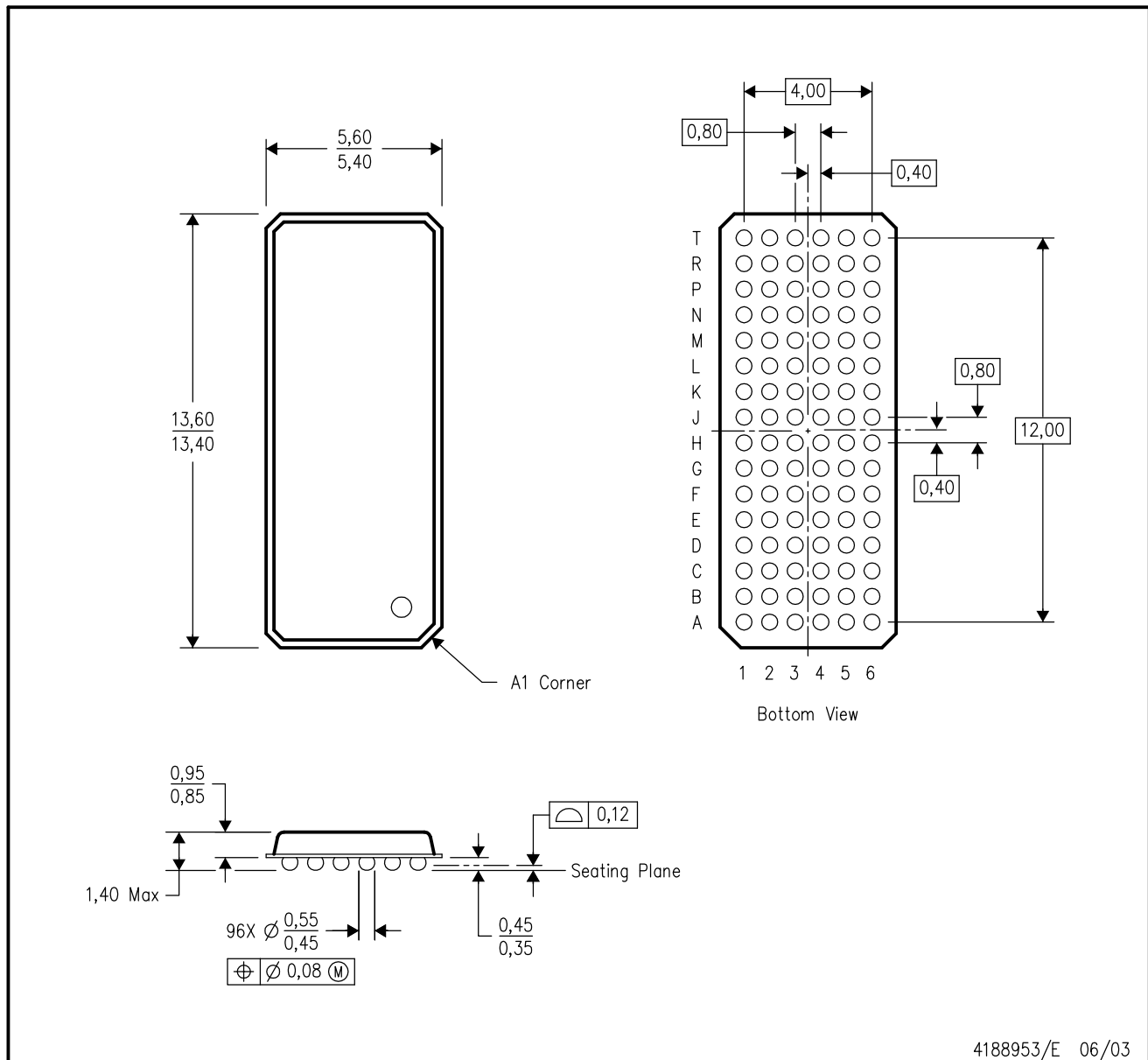
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, slew rate $\geq$ 1 V/ns.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY

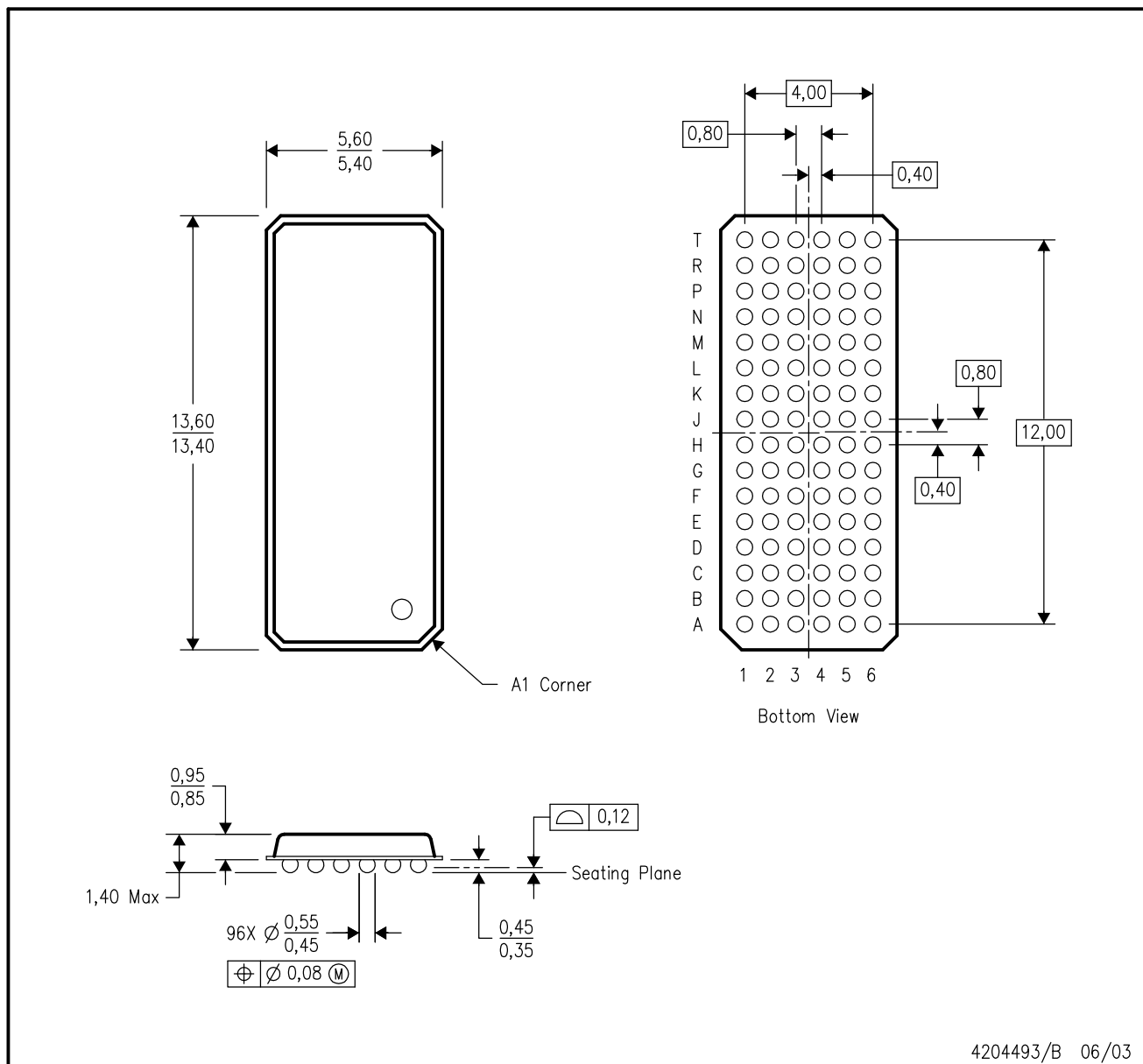


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar BGA™ configuration
 - D. Falls within JEDEC MO-205 variation CC.
 - E. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

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ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar BGA™ configuration
 - D. Falls within JEDEC MO-205 variation CC.
 - E. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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