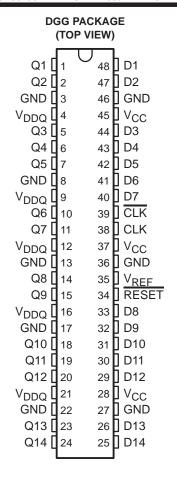


- Supports SSTL_2 Signal Data Inputs and Outputs
- Supports LVTTL Switching Levels on the RESET Pin
- Differential CLK Signal
- Flow-Through Architecture Optimizes PCB Layout
- Meets SSTL_2 Class II Specifications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Packaged in Plastic Thin Shrink Small-Outline Package

description

This 14-bit registered buffer is designed for 2.3-V to 3.6-V V_{CC} operation and SSTL_2 data input and output levels.

All inputs are compatible with the JEDEC Standard for SSTL_2, except the LVCMOS reset (RESET) input. All outputs are SSTL_2, Class II compatible.



When RESET is low, the differential input receivers are disabled, and undriven (floating) data and clock inputs are allowed. In addition, when RESET is low, all registers are reset, and all outputs are forced low. The LVCMOS RESET input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The SN74SSTL16857 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

	INPUTS									
RESET	CLK	CLK	D	Q						
L	Х	Х	Χ	L						
Н	\downarrow	\uparrow	Н	Н						
Н	\downarrow	\uparrow	L	L						
Н	L or H	L or H	Χ	Q_0						

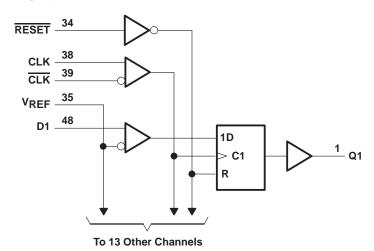


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} or V _{DDQ}	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$)	
Continuous output current, I_O ($V_O = 0$ to V_{DDO})	±50 mA
Continuous current through each V _{CC} , V _{DDO} , or GND	
Package thermal impedance, θ _{JA} (see Note 3)	70°C/W
Storage temperature range, T _{Stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. Current flows only when the output is in the high state and $V_O > V_{DDQ}$.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	V_{DDQ}		3.6	V	
V _{DDQ}	Output supply voltage		2.3		2.7	V
VREF	Reference voltage (V _{REF} = V _{DDQ} /2)		1.15	1.25	1.35	V
VTT	Termination voltage		V _{REF} -40 mV	V _{REF}	V _{REF} +40 mV	V
VI	Input voltage		0		VCC	V
VIH	AC high-level input voltage	Data inputs	V _{REF} +350 mV			V
VIL	AC low-level input voltage	Data inputs			V _{REF} -350 mV	V
VIH	DC high-level input voltage	Data inputs	V _{REF} +180 mV			V
VIL	DC low-level input voltage	Data inputs			V _{REF} -180 mV	V
VIH	High-level input voltage	RESET	2			V
V _{IL}	Low-level input voltage	RESET			0.8	V
VICR	Common-mode input voltage range	CLK, CLK	0.97		1.53	V
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK	360			mV
ІОН	High-level output current				-20	mA
loL	Low-level output current	·		·	20	mA
TA	Operating free-air temperature		0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

F	PARAMETER	TEST CO	ONDITIONS	VCC	MIN	TYP	MAX	UNIT	
VIK		I _I = -18 mA	$I_{I} = -18 \text{ mA}$				-1.2	V	
		I _{OH} = -100 μA		2.3 V to 2.7 V	V _{CC} -0.2				
Vон		I _{OH} = -8 mA		227	1.95			V	
		I _{OH} = -16 mA		2.3 V	1.95				
		I _{OL} = 100 μA		2.3 V to 2.7 V			0.2		
VOL		$I_{OL} = 8 \text{ mA}$		2.3 V			0.35	V	
		I _{OL} = 16 mA		2.3 V			0.35		
		V _I = 1.7 V or 0.8V	V 4.45 V and 25 V	0.7.1/			±5		
	Data innuta	V _I = 2.7 V or 0	V _{REF} = 1.15 V or 1.35 V	2.7 V			±5	4	
	Data inputs	V _I = 1.7 V or 0.8V	V 4.45 V and 25 V	267			±5	μΑ	
		V _I = 2.7 V or 0	V _{REF} = 1.15 V or 1.35 V	3.6 V			±5		
1		V _I = 1.7 V or 0.8V	V 445 V == 4.05 V	0.71/			±1		
١.	OLK OLK	V _I = 2.7 V or 0	V _{REF} = 1.15 V or 1.35 V	2.7 V			±1	mA	
†į	CLK, CLK	V _I = 1.7 V or 0.8V	V 4.45 V and 25 V	261/			IIIA		
		V _I = 2.7 V or 0	V _{REF} = 1.15 V or 1.35 V	3.6 V			±1		
		V. V CND	-	2.7 V			±5		
	RESET	$V_I = V_{CC}$ or GND		3.6 V			±5	^	
	V	V 1 15 V or 1 25 V		2.7 V			±5	μΑ	
	VREF	V _{REF} = 1.15 V or 1.35 V		3.6 V			±5		
		V _I = 1.7 V or 0.8 V	1- 0	2.7 V	90		90		
		V _I = 2.7 V or 0	IO = 0	2.7 V		90		A	
ICC		V _I = 1.7 V or 0.8 V	10 0	3.6 V	90		mA		
		V _I = 2.7 V or 0	IO = 0	3.6 V			90		
	RESET	\/. 4.7\/.or.0.9\/		0.51/#		3			
C.	Data inputs	V _I = 1.7 V or 0.8 V		2.5 V†		2.5		pF	
Ci	RESET	\(\(\frac{1}{2}\)\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	V 47V 00V			3		þΓ	
	Data inputs	V _I = 1.7 V or 0.8 V		3.3 V [‡]		2.5			

[†] All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} =		V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	
fclock	Clock frequency			150		150	MHz
t _W	Pulse duration, CLK, CLK high or low		3.3		3.3		ns
	Catura tima	Data before CLK↑, CLK↓	1.1		1.75		20
t _{su}	Setup time	RESET high before CLK↑, CLK↓	0.6		1.1		ns
th	Hold time, data after CLK↑, CLK↓		0.7		0.7		ns



[‡] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

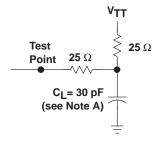
SN74SSTL16857 14-BIT SSTL_2 REGISTERED BUFFER

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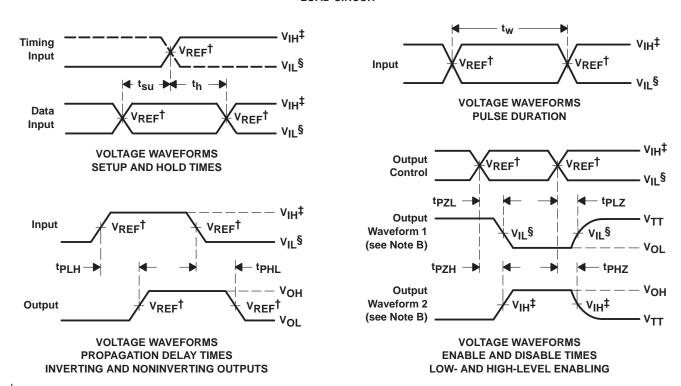
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INDLIT)	FROM TO (INPUT) (OUTPUT)				3.3 V 3 V	UNIT
	(1141 01)	(001101)	MIN	MAX	MIN	MAX	
f _{max}			150		150		MHz
^t pd	CLK and CLK	Q	1.5	3.8	1.4	3.7	ns
^t PHL	RESET	Q	1.5	4.3	1.4	3.5	ns

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V AND V_{CC} = 3.3 V \pm 0.3 V



LOAD CIRCUIT



 $^{^{\}dagger}V_{REF} = V_{DDQ}/2$

NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 1.25 ns/V, t_f \leq 1.25 ns/V.
- D. The outputs are measured one at a time with one transition per measurement.
- E. $V_{TT} = V_{REF} = V_{DDQ}/2$
- F. tpLZ and tpHZ are the same as t_{dis}.
- G. tpzL and tpzH are the same as ten.
- H. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



[‡]V_{IH} = V_{REF} + 350 mV (AC voltage levels)

[§] V_{IL} = V_{REF} − 350 mV (AC voltage levels)





27-Sep-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins I	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74SSTL16857DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74SSTL16857DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74SSTL16857DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

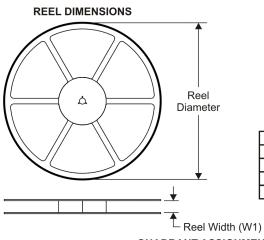
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

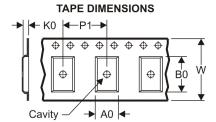
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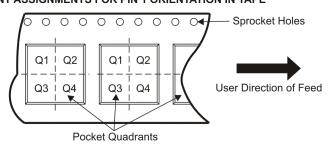
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

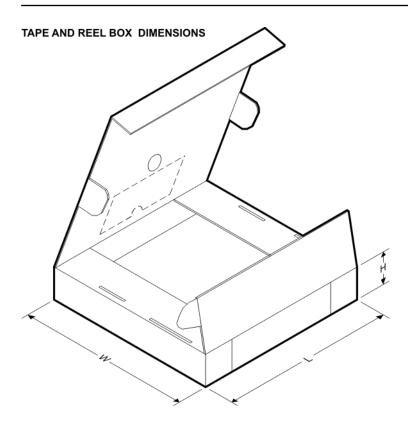
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTL16857DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTL16857DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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