

CN54F251A-X REV 0A0

 Original Creation Date: 06/25/97
 Last Update Date: 07/08/97
 Last Major Revision Date: 06/25/97

8-INPUT MULTIPLEXER WITH TRI-STATE OUTPUTS

General Description

The F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Industry Part Number

54F251A

NS Part Numbers

54F251ADC

Prime Die

M251A

Processing

Quality Conformance Inspection

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+70
3	Static tests at	0
4	Dynamic tests at	+25
5	Dynamic tests at	+70
6	Dynamic tests at	0
7	Functional tests at	+25
8A	Functional tests at	+70
8B	Functional tests at	0
9	Switching tests at	+25
10	Switching tests at	+70
11	Switching tests at	0

Features

- Multifunctional Capability
- On-Chip Select Logic Decoding
- Inverting and Non-Inverting Tri-State Outputs

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0 C to +70 C
Supply Voltage Commercial	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: VCC 4.5V to 5.5V, Temp range: 0°C to +70°C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIH	Input HIGH Voltage	Recognized as a HIGH Signal	1	INPUTS	2.0		V	1, 2, 3
VIL	Input LOW Voltage	Recognized as a LOW Signal	1	INPUTS		0.8	V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IIN=-18mA	2, 3	INPUTS		-1.2	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, IOH=-1.0mA	2, 3	OUTPUTS	2.5		V	1, 2, 3
		VCC=4.5V, IOH=-3.0mA	2, 3	OUTPUTS	2.4		V	1, 2, 3
		VCC=4.75V, IOH=-1.0mA	2, 3	OUTPUTS	2.7		V	1, 2, 3
		VCC=4.75V, IOH=-3.0mA	2, 3	OUTPUTS	2.7		V	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, IOL=24mA	2, 3	OUTPUTS		0.5	V	1, 2, 3
IIH	Input HIGH Current	VCC=5.5V, VIN=2.7V	2, 3	INPUTS		5.0	uA	1, 2, 3
IBVI	Input HIGH Current Breakdown Test	VCC=5.5V, VIN=7.0V	2, 3	INPUTS		7.0	uA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VOUT = VCC	2, 3	OUTPUTS		100	uA	1, 2, 3
VID	Input Leakage Test	VCC = 0.0V, IID = 1.9uA, All other pins grounded	2, 3	INPUTS	4.75		V	1, 2, 3
IOD	Output Leakage Circuit Current	VCC = 0.0V, VIOD = 150mV, All other pins grounded	2, 3	OUTPUTS		4.75	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VIN=0.5V	2, 3	INPUTS		-0.6	mA	1, 2, 3
IOZH	Output Leakage Current	VCC=5.5V, VOUT=2.7V	2, 3	OUTPUTS		50	uA	1, 2, 3
IOZL	Output Leakage Current	VCC=5.5V, VOUT=0.5V	2, 3	OUTPUTS		-50	uA	1, 2, 3
IOS	Output Short Circuit Current	VCC=5.5V, VOUT = 0V	2, 3	OUTPUTS	-60	-150	mA	1, 2, 3
IZZ	Bus Drainage Test	VCC = 0.0V, VOUT = 5.25V	2, 3			500	uA	1, 2, 3
ICCL	Power Supply Current	VCC=5.5V, VO = LOW	2, 3	VCC		22	mA	1, 2, 3
ICCZ	Power Supply Current	VCC=5.5V, VO = HIGH Z	2, 3	VCC		24	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS. Temp Range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	Sn to Z	3.5	9.0	ns	9
			2, 3	Sn to Z	3.5	9.5	ns	10, 11
tpHL(1)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	Sn to Z	3.2	7.5	ns	9, 10, 11
tpLH(2)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	Sn to Z	4.5	10.5	ns	9
			2, 3	Sn to Z	4.5	12.5	ns	10, 11
tpHL(2)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	Sn to Z	4.0	8.5	ns	9
			2, 3	Sn to Z	4.0	9.0	ns	10, 11
tpLH(3)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	In to Z	3.0	6.5	ns	9
			2, 3	In to Z	3.0	7.0	ns	10, 11
tpHL(3)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	In to Z	1.4	4.0	ns	9
			2, 3	In to Z	1.5	5.0	ns	10, 11
tpLH(4)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	In to Z	3.5	7.0	ns	9
			2, 3	In to Z	2.5	8.0	ns	10, 11
tpHL(4)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	In to Z	3.5	7.0	ns	9
			2, 3	In to Z	3.5	7.5	ns	10, 11
tpZH(1)	Output Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	2.5	6.0	ns	9
			2, 3	OE to Z	2.5	7.0	ns	10, 11
tpZL(1)	Output Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	2.5	6.0	ns	9
			2, 3	OE to Z	2.5	6.5	ns	10, 11
tpHZ(1)	Output Disable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	2.5	5.5	ns	9
			2, 3	OE to Z	2.5	6.0	ns	10, 11
tpLZ(1)	Output Disable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	1.5	4.5	ns	9, 10, 11
tpZH(2)	Output Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	3.5	7.0	ns	9
			2, 3	OE to Z	3.0	7.5	ns	10, 11
tpZL(2)	Output Enable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	3.5	7.5	ns	9
			2, 3	OE to Z	3.5	8.0	ns	10, 11
tpHZ(2)	Output Disable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	2.0	5.5	ns	9, 10, 11
tpLZ(2)	Output Disable Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	OE to Z	1.5	4.5	ns	9, 10, 11

Note 1: Guaranteed by applying specific input condition and testing VOL & VOH.

(Continued)

Note 2: Screen tested 100% on each device at +75C temperature only, subgroups A2 & A10.

Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +75C temperature only, subgroups A2 & A10.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0001726	07/08/97	Linda Collins	Legal issue with Fairchild, due to the Fairchild/National split, is forcing the change from CN74F which is 'Fairchilds' product code to CN54F which is 'Nationals' product code.