*Click **here** for production status of specific part numbers.*

MAX14915

Compact Industrial Octal High-Side Switch with Diagnostics

General Description

The MAX14915 has eight high-side switches specified to deliver up to 700mA continuous current. The high-side switches have on-resistance of 250mΩ (max) at 125°C ambient temperature.

The SPI interface has a built-in chip addressing decoder, allowing communication with multiple MAX14915s utilizing a common SPI chip select ($\overline{CS}$).

The SPI interface provides flexibility for global and per-channel configuration and diagnostic, including over and undervoltage detection, open wire/load detection, overload and current limiting reporting, thermal conditions reporting, and more.

Open load detection detects both open-wire/open-load conditions with switches in the on and off states. LED drivers provide indication of per-channel fault, status, and supply undervoltage conditions. Internal active clamps allow for fast turn-off of inductive loads.

Integrated line-to-ground and line-to-line surge protection only requires a TVS on V_{DD}.

The MAX14915 is available in a compact 48-pin 6mm x 6mm QFN package.

Applications

- Industrial Digital Outputs
- PLC Systems

Benefits and Features

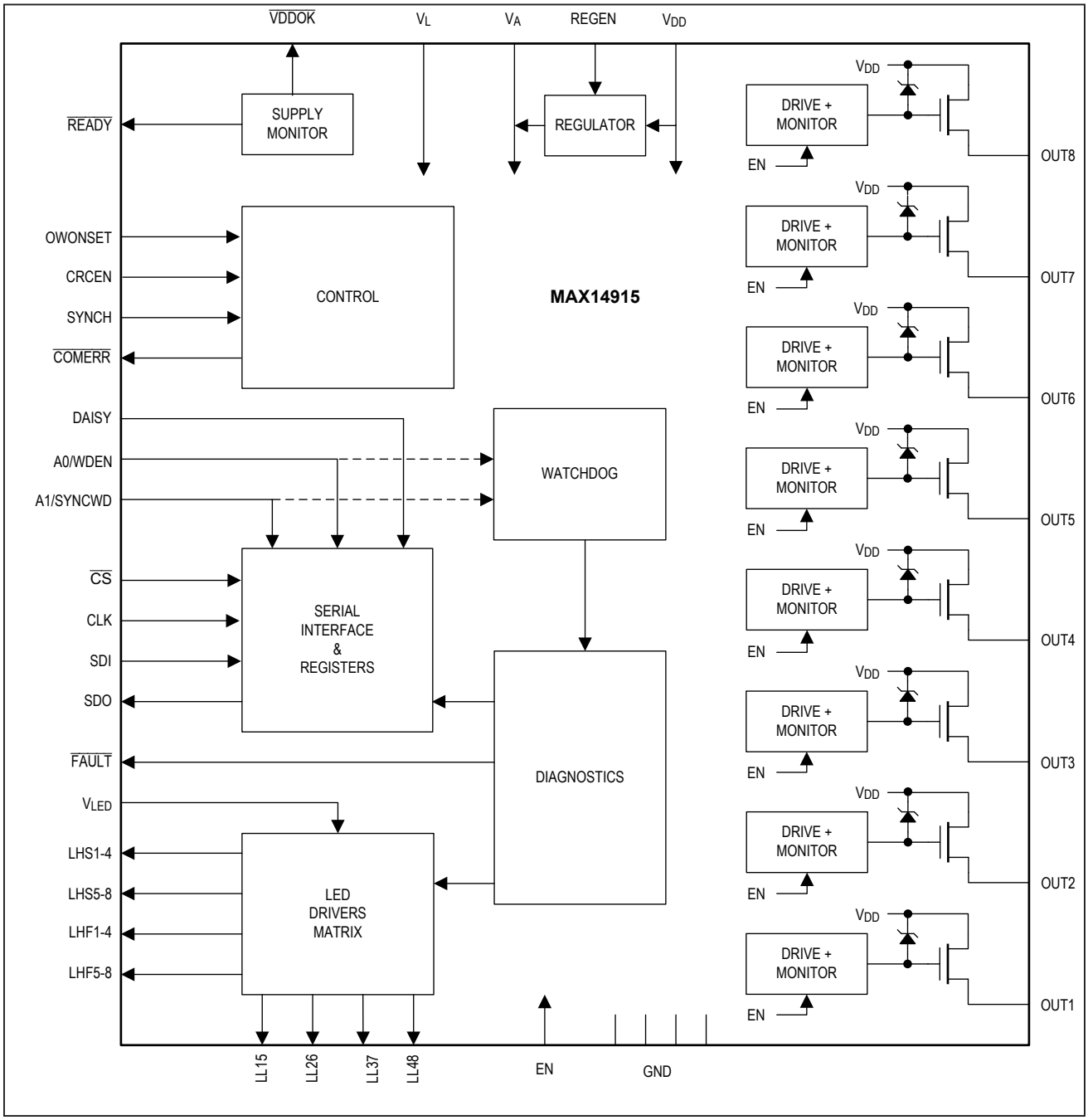
- Robustness and Smart Diagnostics
  - 65V Absolute Maximum Supply Range
  - Internal Clamps for Fast Inductive Load Demagnetization
  - CRC Error Checking on the SPI Interface
  - Watchdog Timer for Diagnostics Checking
  - Open-Wire Detection, Both with Switches On and Off
  - Undervoltage Detection with UVLO
  - Loss of V_{DD} or GND Protection
  - Thermal Shutdown Protection
  - Integrated ±1kV/42Ω IEC61000-4-5 Surge Protection
  - -40°C to +125°C Operating Ambient Temperature
- Reduces Power and Heat Dissipation
  - 250mΩ (Max) On-Resistance at T_A = 125°C
  - 2mA (typ) Supply Current
  - Accurate Output Current Limiting
- Flexibility
  - Addressable SPI Interface Reduces Isolation Cost
  - SYNCH Input for Simultaneous Update of Switches
  - LED Driver Matrix for 16 LEDs, Powered by 24V, 5V, or 3.3V
  - Flexible Logic Voltage Interface from 2.5V to 5.5V
- Compact 6mm x 6mm QFN Package

***Ordering Information** appears at end of data sheet.*

19-100231; Rev 2; 10/18

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

V_{DD} ..... -0.3V to +65V
OUT_ ..... (V_{DD} - 49)V to (V_{DD} + 0.3)V
V_A, V_L ..... -0.3V to +6V
SDO, $\overline{READY}$, $\overline{COMERR}$ ..... -0.3V to (V_L + 0.3)V
REGEN, OWONSET ..... -0.3V to +6V
$\overline{FAULT}$ ..... -0.3V to 6V
SDI, $\overline{CS}$, CLK, EN, ADD0/WDEN, ADD1, SYNCH, CRCEN, DAISY ..... -0.3V to 6V
V_{LED} ..... -0.3V to +70V
LH_, LL_, $\overline{VDDOK}$ ..... -0.3V to (V_{LED} + 0.3)V
OUT_ Load Current ..... Internally Limited
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 50mW/°C above +70°C) 3900mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... 260°C

Note 1: All voltages relative to GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Flip Chip QFN

Package Code	F486A6F-1
Outline Number	**21-100232**
Land Pattern Number	**90-100077**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	20.5°C/W
Junction to Case (θ_{JC})	0.39°C/W (bottom)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS/SUPPLY						
V_{DD} Supply Voltage	V_{DD}		10		36	V
V_{DD} Supply Current	I_{DD}	EN = high, OUT_ switches on, no load, V_A and V_L supplied externally		2	3	mA
		EN = low			3	
V_{DD} UVLO Rise Threshold	$V_{DD\_UVLO\_R}$	V_{DD} rising			9.6	V
V_{DD} UVLO Fall Threshold	$V_{DD\_UVLO\_F}$	V_{DD} falling, OUT_ disabled, VddUvlo bit set	7.9			V
V_{DD} UVLO Hysteresis	$V_{DD\_UVLO\_H}$			0.35		V
V_{DD} Warn Rise Threshold	$V_{DD\_WARN\_R}$	V_{DD} rising			14	V
V_{DD} Warn Fall Threshold	$V_{DD\_WARN\_F}$	V_{DD} falling, VddWarn bit set, $\overline{VDDOK}$ pin set HiZ	12			V
V_{DD} Warn Hysteresis	$V_{DD\_WARN\_H}$			0.4		V
V_{DD} Good Rise Threshold	$V_{DD\_GOOD\_R}$	V_{DD} rising, VddNotGood bit set, $\overline{VDDOK}$ pin set HiZ			17	V
V_{DD} Good Fall Threshold	$V_{DD\_GOOD\_F}$	V_{DD} falling	15			V
V_{DD} Good Hysteresis	$V_{DD\_GOOD\_H}$			0.4		V
V_{DD} POR Rise Threshold	$V_{DD\_POR\_R}$	V_{DD} rising			6.8	V
V_{DD} POR Falling Threshold	$V_{DD\_POR\_F}$	V_{DD} falling	5.6			V
V_A Supply Voltage	V_{VA}	When V_A is supplied externally; REGEN = GND.	3.0		5.5	V
V_A Supply Current	I_{VA}	EN = high, OUT_ are turned on, no load, no LEDs connected		0.5	0.85	mA
V_A Undervoltage Lockout Threshold	V_{VA_UV}	V_{DD} = 24V, VA falling	2.35		2.8	V
V_A Undervoltage Lockout Hysteresis	V_{VA_UVHYST}	V_{DD} = 24V		0.1		V
V_L Supply Voltage	V_{VL}		2.5		5.5	V
V_L Supply Current	I_{VL}	All logic inputs high or low		13	34	µA
V_L POR Threshold	V_{L_POR}	V_L falling	0.87	1.32	1.5	V
DC CHARACTERISTICS/SWITCH OUTPUTs (OUT_)						
On-Resistance	R_{OUT_HS}	$I_{OUT\_}$ = -600mA		120	250	mΩ
Current Limit	I_{LIM}		0.7	1	1.3	A
Off Leakage Current	I_{LKG}	OL detect = off, switch off, OUT_ = 0V	-10		10	µA

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS/LINEAR REGULATOR						
Output Voltage	V_{VA}	REGEN open, Cload = 1µF, 0mA < I_{VA} < 20mA	3.0	3.3	3.6	V
Current Limit	I_{CL_VA}	REGEN open	25			mA
Short Current	I_{SHRT_VA}	REGEN open, V_A = 0V			60	mA
Load Regulation		0mA < I_{VA} < 20mA		0.1		mV/mA
REGEN Threshold	VT_{REGEN}		0.2			V
REGEN Leakage Current	I_{LK_REGEN}	REGEN = 0V	-50			µA
DC CHARACTERISTICS/OFF STATE DIAGNOSTICS (OUT_)						
Pullup Current, OWOFF	I_{PU_OWOFF1}	OWOff_ = 1, $V_{OUT\_}$ < 5V, OffCurr1 = 0, OffCurr0 = 0	10	20	32	µA
	I_{PU_OWOFF2}	OWOff_ = 1, $V_{OUT\_}$ < 5V, OffCurr1 = 0, OffCurr0 = 1	65	100	135	
	I_{PU_OWOFF3}	OWOff_ = 1, $V_{OUT\_}$ < 5V, OffCurr1 = 1, OffCurr0 = 0	230	300	370	
	I_{PU_OWOFF4}	OWOff_ = 1, $V_{OUT\_}$ < 5V, OffCurr1 = 1, OffCurr0 = 1	480	600	720	
OUT_ Voltage, OWOFF	V_{OUT_OFF}	OWOff_ = 1, $I_{OUT\_}$ = 0mA	5.7	6.7	7.8	V
Open Wire Detect Threshold, OWOFF	V_{TH_OWOFF}	OWOff_ = 1	5		5.8	V
Short to V_{DD} Detect Threshold	V_{TH_SHVDD}	ShVddEn_ = 1, ShrtVddThr1 = 0, ShrtVddThr0 = 0	8.2	9.0	10.0	V
		ShVddEn_ = 1, ShrtVddThr1 = 0, ShrtVddThr0 = 1	9.1	10	10.9	
		ShVddEn_ = 1, ShrtVddThr1 = 1, ShrtVddThr0 = 0	11	12	13	
		ShVddEn_ = 1, ShrtVddThr1 = 1, ShrtVddThr0 = 1	13	14	15	
DC CHARACTERISTICS/ON STATE DIAGNOSTICS						
Open Wire Detect Threshold Current, On	I_{TH_OWON}	OWOn_ = 1, $R_{OWONSET}$ = 500kΩ	0.05	0.13	0.2	mA
		OWOn_ = 1, $R_{OWONSET}$ = 160kΩ	0.25	0.35	0.55	
		OWON_ = 1, $R_{OWONSET}$ = 30kΩ	1.8	2.4	2.9	
DC CHARACTERISTICS/LOGIC I/O						
Input Voltage High	V_{IH}		0.7xV_L			V
Input Voltage Low	V_{IL}				0.3xV_L	V
Input Threshold Hysteresis	V_{IHYS}			0.11xV_L		V
Input Pulldown Resistor	R_{IN_PD}	See logic pin descriptions for applicable pins		200		kW
Input Pullup Resistor	R_{IN_PU}	See logic pin descriptions for applicable pins		200		kW
Output Logic-High (SDO)	V_{OH}	I_{LOAD} = -5mA	V_L - 0.6			V

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-Low	V_{OL}	I_{LOAD} = +5mA			0.33	V
SDO Output Tristate Leakage	I_{L_SDO}	$\overline{CS}$ = high	-1		+1	µA
DC CHARACTERISTICS/OPEN-DRAIN OUTPUT ($\overline{FAULT}$, $\overline{COMERR}$, $\overline{READY}$)						
READY Output Logic-High	V_{ODH}	I_{LOAD} = -5mA	V_L - 0.6			V
Output Logic-Low	V_{ODL}	I_{LOAD} = +5mA			0.33	V
Leakage	I_{ODL}	Open-drain output off, V = 5.5V	-1		+1	µA
DC CHARACTERISTICS/LED Drivers (LH_, LL_, $\overline{VDDOK}$)						
LED Supply Voltage	V_{LED}		3.0		V_{DD}	V
LH Voltage High	V_{OH_LH}	LH = on, I_{LEDH} = -5mA	V_{LED} - 0.3			V
LH Off Leakage Current	I_{L_LH}	LH_ = off, V_{LEDH} = 0V			5	µA
LL Output Voltage Low	V_{OH_LL}	LL = on, I_{LDL} = 5mA			0.3	V
LL Off Leakage Current	I_{L_LL}	LL = off, V_{LL} = VLED	-1		+1	µA
DC CHARACTERISTICS/PROTECTION						
OUT_ Clamp Voltage	V_{CL}	V_{CL} = V_{DD} - OUT, $I_{OUT\_}$ = -500mA, OUT_ is off	49	56		V
Channel Thermal Shutdown Temperature	T_{JSHDN}	Junction temperature rising. Per channel.		150		°C
Channel Thermal Shutdown Hysteresis	T_{JSHDN_HYST}			15		°C
Chip Thermal Shutdown	T_{CSHDN}	Temperature rising.		150		°C
Chip Thermal Shutdown Hysteresis	T_{CSHDN_HYST}			10		°C
TIMING CHARACTERISTICS/OUT_						
Prop Delay LH	t_{PD_LH}	Delay from rising SYNCH edge to OUT_ rising to 90%. R_L = 48Ω. V_{DD} = 24V. Figure 2		11	30	µs
Prop Delay HL	t_{PD_HL}	Delay from rising SYNCH edge to OUT_ falling to 10% of V_{DD}, V_{DD} = 24V, R_L = 48Ω, Figure 2		11	30	µs
Rise-Time	t_R	20% to 80% V_{DD}, V_{DD} = 24V, R_L = 48Ω, Figure 2		8		µs
Fall-Time	t_F	80% to 20% V_{DD}, V_{DD} = 24V, R_L = 48Ω, Figure 2		8		µs

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_{LED} = +3.0V to 36V, V_A = +3.0V to +5.5V, V_L = +2.5V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{LED} = 24V, V_A = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS/WATCHDOG						
Watchdog Timeout	t_{WD}	WDTo[1:0] = 01b		200		ms
		WDTo[1:0] = 10b		600		
		WDTo[1:0] = 11b		1200		
Watchdogs Timeout Accuracy	t_{WD_ACC}	WDEN = 1, SynchWDEn = 1, see Config2 register for watchdog timeout	-30		+30	%
TIMING CHARACTERISTICS/LED Matrix						
LED Driver Scan rate	FLED	Update rate for each LED		1		kHz
TIMING CHARACTERISTICS/SPI Figure 1						
CLK Clock Period	t_{CH+CL}		100			ns
CLK Pulse Width High	t_{CH}		40			ns
CLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to CLK Rise Time	t_{CSS}		40			ns
SDI Hold Time	t_{DH}		10			ns
SDI Setup Time	t_{DS}		10			ns
SDO Propagation Delay	t_{DO}	Cload = 10pF, CLK falling edge to SDO stable			30	ns
SDO Rise and Fall Times	t_{FT}			1		ns
$\overline{CS}$ Hold Time	t_{CSH}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	Note 3	40			ns
EMC						
ESD IEC Contact Discharge	V_{ESD_C}	OUT_ to GND, IEC61000-4-2		±7		kV
ESD IEC Air Discharge	V_{ESD_A}	OUT_ to GND, IEC61000-4-2		±30		kV
ESD	V_{ESD}	All other pins. Human Body Model (Note 4)		±2		kV
Surge Tolerance	V_{SURGE}	OUT_ to GND, IEC61000-4-5 with 42Ω, TVS on V_{DD}. (Note 5)		±1		kV

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: All logic input pins except CS have a pulldown resistor. CS has a pullup resistor.
Note 4: Bypass V_{DD} pin to GND with 1µF capacitor as close as possible to the device for high ESD protection.
Note 5: At typical application value of V_{DD} = 24V, with a TVS proection on V_{DD} to GND.

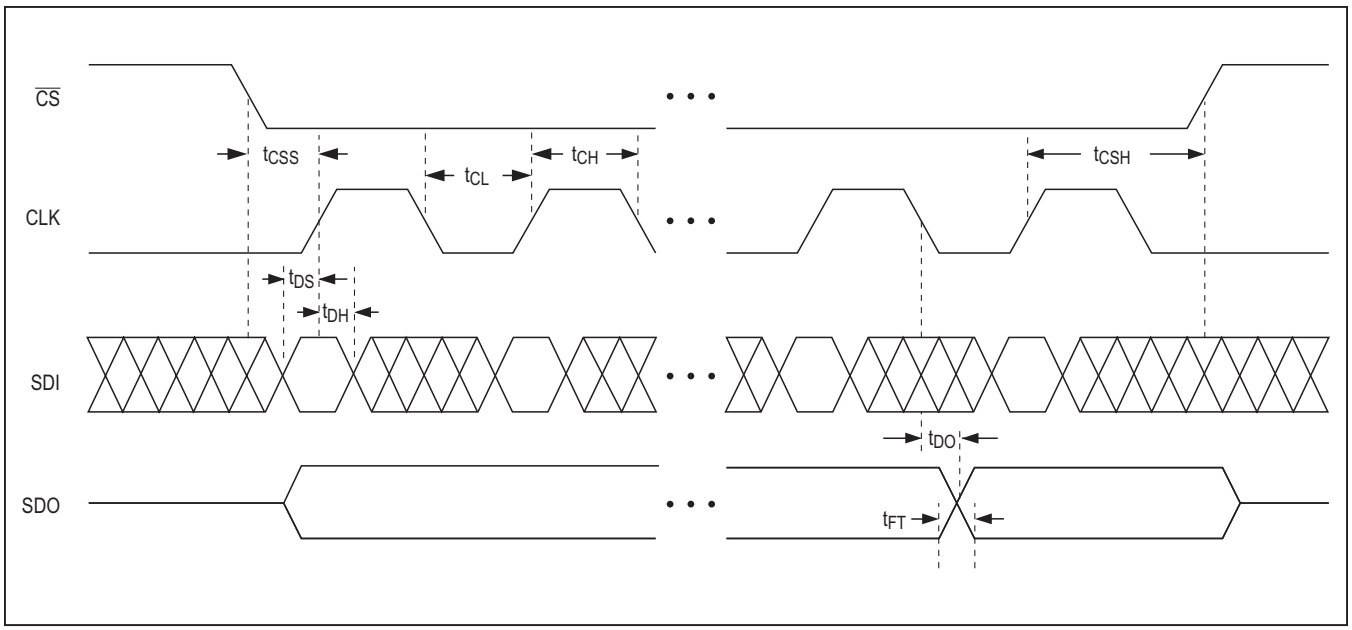


Figure 1. SPI Timing Diagram.

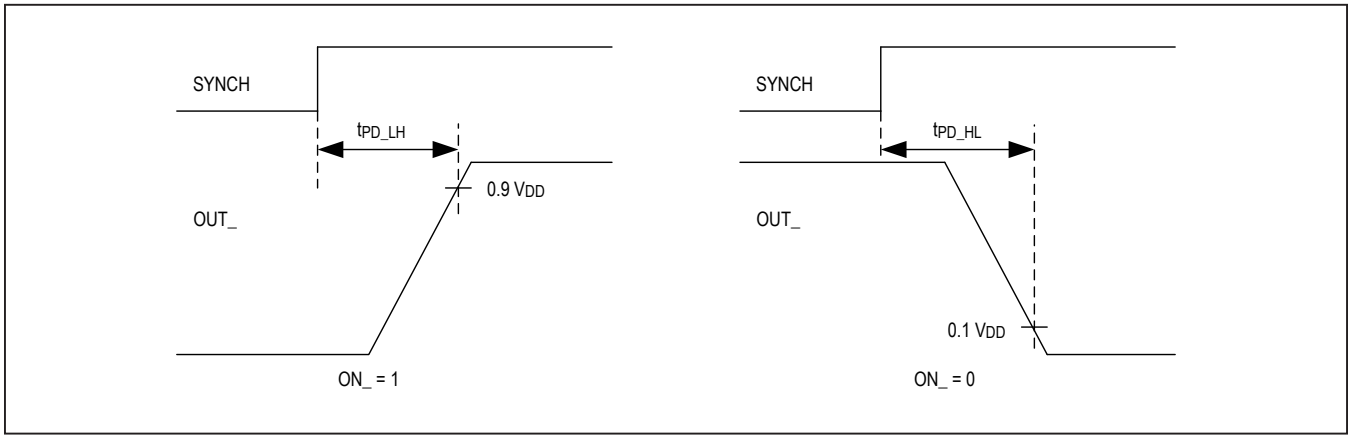
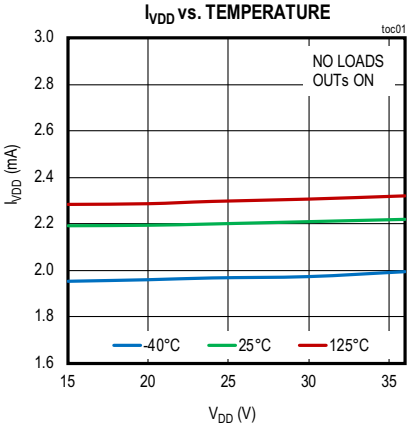


Figure 2. Propagation Delay Timing Characteristics

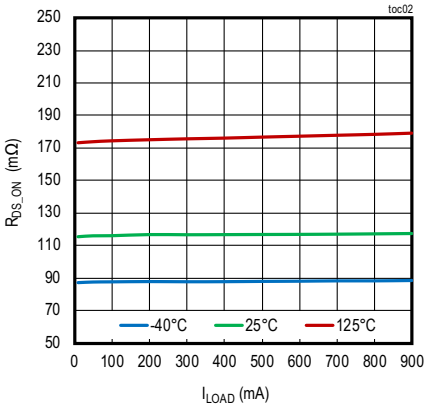
Typical Operating Characteristics

(V_{DD} = +24V, REGEN = open, V_L = +3.3V, T_A = +25°C, unless otherwise noted)

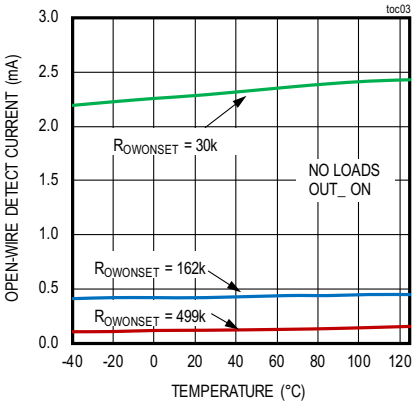
I_{VDD} vs. TEMPERATURE



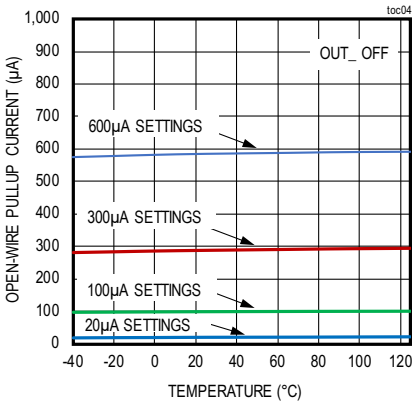
R_{DS_ON} vs. LOAD CURRENT



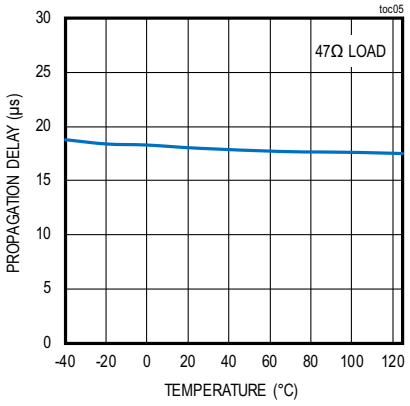
OPEN-WIRE DETECT CURRENT vs. TEMPERATURE



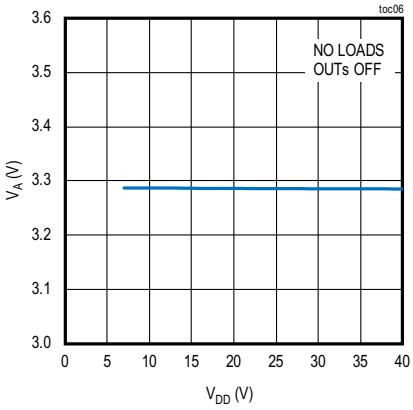
OPEN-WIRE PULLUP CURRENT vs. TEMPERATURE



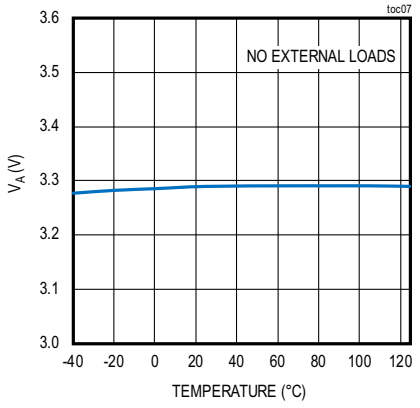
TURN-ON PROPAGATION DELAY vs. TEMPERATURE



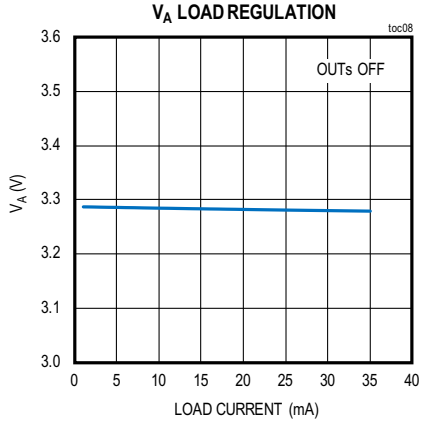
V_A LINE REGULATION



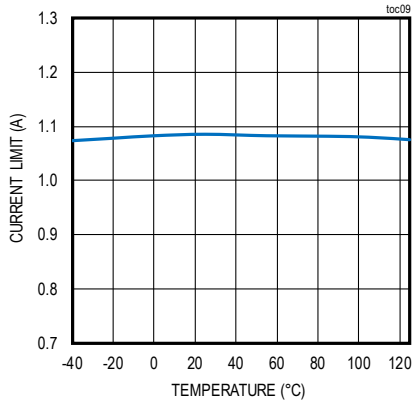
V_A vs. TEMPERATURE



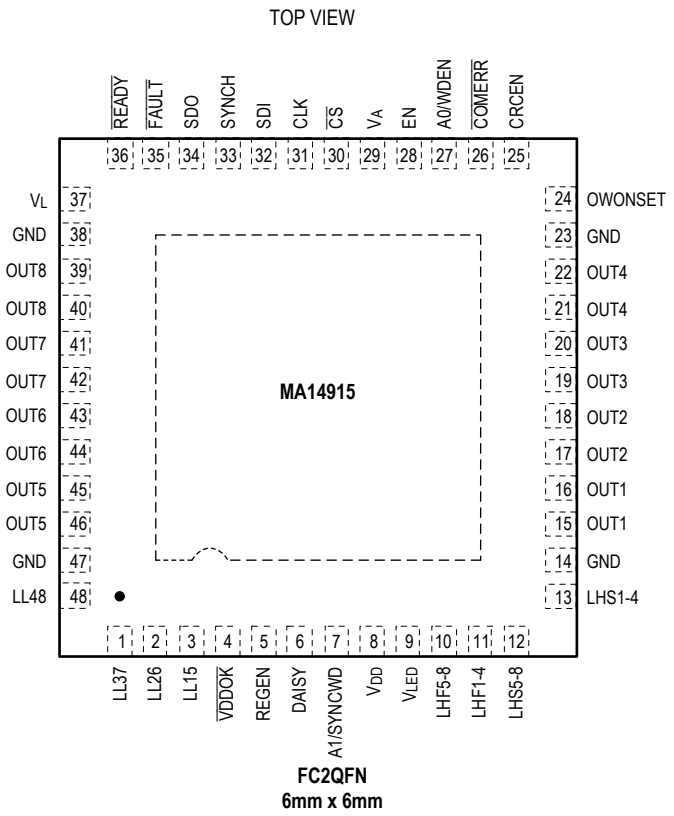
V_A LOAD REGULATION



CURRENT LIMIT vs. TEMPERATURE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
POWER SUPPLY				
EP, 8	V_{DD}	Supply Voltage, Nominally 24V. Connect all V_{DD} together. Bypass V_{DD} to GND through a 1µF capacitor.	GND	Supply
29	V_A	Analog Supply Input. Connect an external 3.0V to 5.5V supply to V_A or use the internal linear regulator by leaving REGEN open. Bypass V_A to GND through a 1µF ceramic capacitor.	GND	Supply
5	REGEN	V_A Regulator Enable Input. Connect REGEN to GND to disable V_A regulator. Leave REGEN open to enable V_A regulator, which internally supplies V_A with 3.3V.	GND	Supply
14, 23, 38, 47	GND	Ground. Connect all GND pins together.	GND	GND
37	V_L	Logic Supply Input. V_L defines the logic levels on all logic interface pins. Bypass V_L to GND through a 100nF ceramic capacitor.	GND	Supply
4	$\overline{VDDOK}$	$\overline{VDDOK}$ is an active-low, open-drain logic output that indicates when the V_{DD} supply is OK. $\overline{VDDOK}$ turns on low when V_{DD} rises to > 16V(typ) and turns off when V_{DD} falls to < 13V (typ). Connect a LED with a pullup resistor to a voltage between 3.3V and V_{DD}.	GND	Logic

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
SWITCH OUTPUTS				
15, 16	OUT1	High-Side Switch Output 1	V_{DD}	Power
17, 18	OUT2	High-Side Switch Output 2	V_{DD}	Power
19, 20	OUT3	High-Side Switch Output 3	V_{DD}	Power
21, 22	OUT4	High-Side Switch Output 4	V_{DD}	Power
45, 46	OUT5	High-Side Switch Output 5	V_{DD}	Power
43, 44	OUT6	High-Side Switch Output 6	V_{DD}	Power
41, 42	OUT7	High-Side Switch Output 7	V_{DD}	Power
39, 40	OUT8	High-Side Switch Output 8	V_{DD}	Power
DIAGNOSTIC SETTING				
24	OWON-SET	Open-Wire Detection Threshold Current Set. Connect a resistor between OWONSET and GND to define the threshold current for open-wire detection when the OUT_ switches are closed.	V_A	Analog
Control Interface				
28	EN	Enable Logic Input. Drive EN high for normal operation. Drive EN low to disable/three-state all OUT_ drivers. Internal weak pulldown.	V_L	Logic
35	$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$Global Diagnostics Open-Drain Output. The $\overline{\text{FAULT}}$ transistor turns on low under conditions defined in the Interrupt register. Connect a pullup resistor to V_L.	V_L	Logic
33	SYNCH	SYNCH Input. All eight output switches are updated simultaneously on the rising edge of SYNCH, as determined by the contents of the SPI register. The OUT_ states do not change when SYNCH is held low. When SYNCH is high, the output states change immediately when a new value is written into the SetOUT register. Internal weak pullup.	V_L	Logic
25	CRCEN	CRC Enable Select Input. Drive CRCEN high to enable CRC generation and error detection on the serial data. CRC has a weak pulldown.	V_L	Logic
36	$\overline{\text{READY}}$	$\overline{\text{READY}}$is an open-drain output that is passive low when the internal logic chip supply and V_L I/O supply are both higher than their respective UVLO thresholds, indicating that the part is ready for SPI communication. When the internal register supply falls below the UVLO threshold the register contents are lost and $\overline{\text{READY}}$transitions active-high. Connect a pulldown resistor to $\overline{\text{READY}}$.	V_L	Logic
26	$\overline{\text{COMERR}}$	SPI Error Open-Drain Output. The $\overline{\text{COMERR}}$ transistor turns on low when an error occurs during a SPI transaction. Connect a pullup resistor to V_L.	V_L	Logic

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
SERIAL INTERFACE				
32	SDI	Serial Data Input. SPI MOSI data from controller. SDI has a weak pulldown.	V_L	Logic
34	SDO	Serial Data Output. SPI MISO data output to controller.	V_L	Logic
31	CLK	Serial Clock Input from SPI Controller. CLK has a weak pulldown.	V_L	Logic
30	$\overline{CS}$	Chip Select Input from Controller. $\overline{CS}$ has a weak pullup.	V_L	Logic
27	A0/WDEN	Chip address LSB for addressable SPI or SPI watchdog enable input for daisy-chain SPI. AO/WDEN has a weak pulldown.	V_L	Logic
7	A1/SYN-CWD	Chip Address MSB for Addressable SPI. SYNCH pin watchdog enable input for daisy-chain SPI. A1/SYNCWD has a weak pulldown.	V_L	Logic
6	DAISY	Daisy-Chain Enable Select Input. Drive DAISY high to enable daisy-chained SPI mode. DAISY has a weak pulldown.	V_L	Logic
LED DRIVER MATRIX				
9	V_{LED}	Supply for LED Drivers. Apply supply voltage of 3.0V to V_{DD}.		
3	LL15	OUTs 1, 5 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
2	LL26	OUTs 2, 6 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
1	LL37	OUTs 3, 7 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
48	LL48	OUTs 4, 8 Status/Fault LED Cathode Output (Open-Drain Low-Side). Connect a resistor in series to set the LED current.		
13	LHS1-4	OUTs 1-4 Status LED Anode Outputs (Open-Drain High-Side). Connect a resistor in series to set the LED current.		
12	LHS5-8	OUTs 5-8 Status LED Anode Outputs (Open-Drain High-Side). Connect a resistor in series to set the LED current.		
11	LHF1-4	OUTs 1-4 Fault LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the LED current		
10	LHF5-8	OUTs 5-8 Fault LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the LED current.		

Detailed Description

The MAX14915 is an octal high-side switch. The OUT_ high-side switches have 250mΩ (max) on-resistance at 600mA and T_A = 125°C. Extensive diagnostics can be enabled through SPI to indicate wire-break, overload, current limiting, output short to V_{DD}, low supply voltage, and high chip temperature conditions. Active clamping limits the negative OUT_ voltage to (V_{DD} - V_{CL}) and allows for freewheeling currents to demagnetize the inductive loads quickly. A watchdog timer monitors SPI activity and automatically switches the OUT_ switches off in case of missing SPI activity.

Synchronization

On the rising edge of the SYNCH logic input, all OUT_ switches change to the new state previously programmed into the SetOUT register. If SYNCH is held high, then the OUT_ change state immediately when the SetOUT register is written to (transparent mode).

When EN pin is low, all OUT_ are off independent of the SYNCH pin state and the SetOUT register value.

Power-Up and Undervoltage Lockout

When the V_{DD}, V_A, V_L, or V_{INT} supply voltages are under their respective UVLO thresholds, all OUT_ switches are off and the open wire detect current sources are turned off. V_{INT} is an internal supply for the registers and logic that is derived from the V_A or V_{DD} supply.

When the V_{DD} supply or V_A supply rises, the internal logic supply, V_{INT}, rises. If V_L and V_{INT} are both above their UVLO thresholds, the chip is ready for communication and the $\overline{READY}$ pin becomes passive low to indicate that the part is ready to communicate through the SPI interface.

In addressed SPI mode (DAISY pin is low) the VddUvlo, VddNotGood, VddWarn, Vint_UV, and VA_UVLO bits are set = 1 and the $\overline{FAULT}$ output is set active-low. These bits and the $\overline{FAULT}$ pin only clear once the GlobalErr register is read.

The register contents are lost when both V_A and V_{DD} drop low and the internal register supply, V_{INT}, falls below its undervoltage lockout threshold.

The Vint_UV bit = 1 signals that the register contents are in power-on-reset state and any custom configuration can be programmed or needs to be reprogrammed after a power reset event.

When V_{DD} rises above $V_{DD\_UVLO\_R}$ (with VDDOnTh = 0) or above $V_{DD\_GOOD\_R}$ (with VDDOnThr = 1) the $\overline{VDDOK}$ pin is turned active-low, indicating that the V_{DD} supply is high enough so the OUT_ switches can be operated normally.

When V_{DD} falls below $V_{DD\_WARN\_F}$ (~13V), the VDDWarn bit (if VddOKM = 0) and, thus, $\overline{FAULT}$ are set but the OUT_ switches continue operating normally.

When V_{DD} falls further below $V_{DD\_UVLO\_F}$, the VDD_UVLO bit is set and the OUT_ switches are turned off.

In daisy-chain mode (DAISY pin high), the $\overline{READY}$ and $\overline{VDDOK}$ pins are active, but the $\overline{FAULT}$ pin does not signal supply conditions.

Chip Thermal Protection

When the chip temperature rises to above the thermal shutdown threshold of 150°C, the chip enters shutdown protection and all overloaded OUT switches are kept off until chip temperature drops below 140°C. The ThrmShut bit and $\overline{FAULT}$ output are set.

If the chip temperature rises above 165°C due to a short, an overload on the V_A regulator, or LED matrix, the internal V_A linear regulator, all OUT switches, and the LED matrix are shutdown to prevent part damage. In this condition, the ThrmShut bit and $\overline{FAULT}$ output are already set and in daisy-chain mode the F-bits in SDO are all set to 1. The register contents are not lost in thermal shutdown if V_{DD} supply is present.

When the chip temperature then falls by the hysteresis amount, the V_A regulator turns on, LED matrix and OUT switches are restored to normal operation.

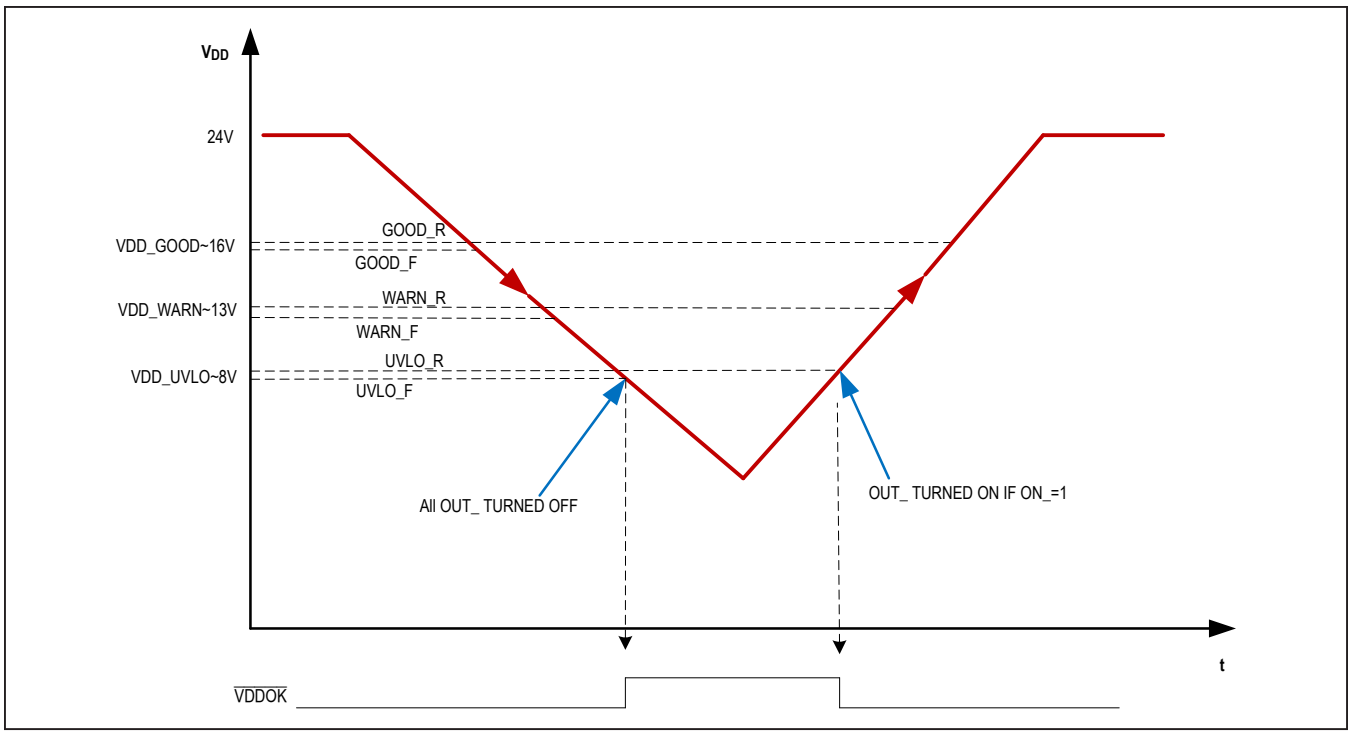


Figure 3. V_{DD} Monitoring with VDDOnThr = 0

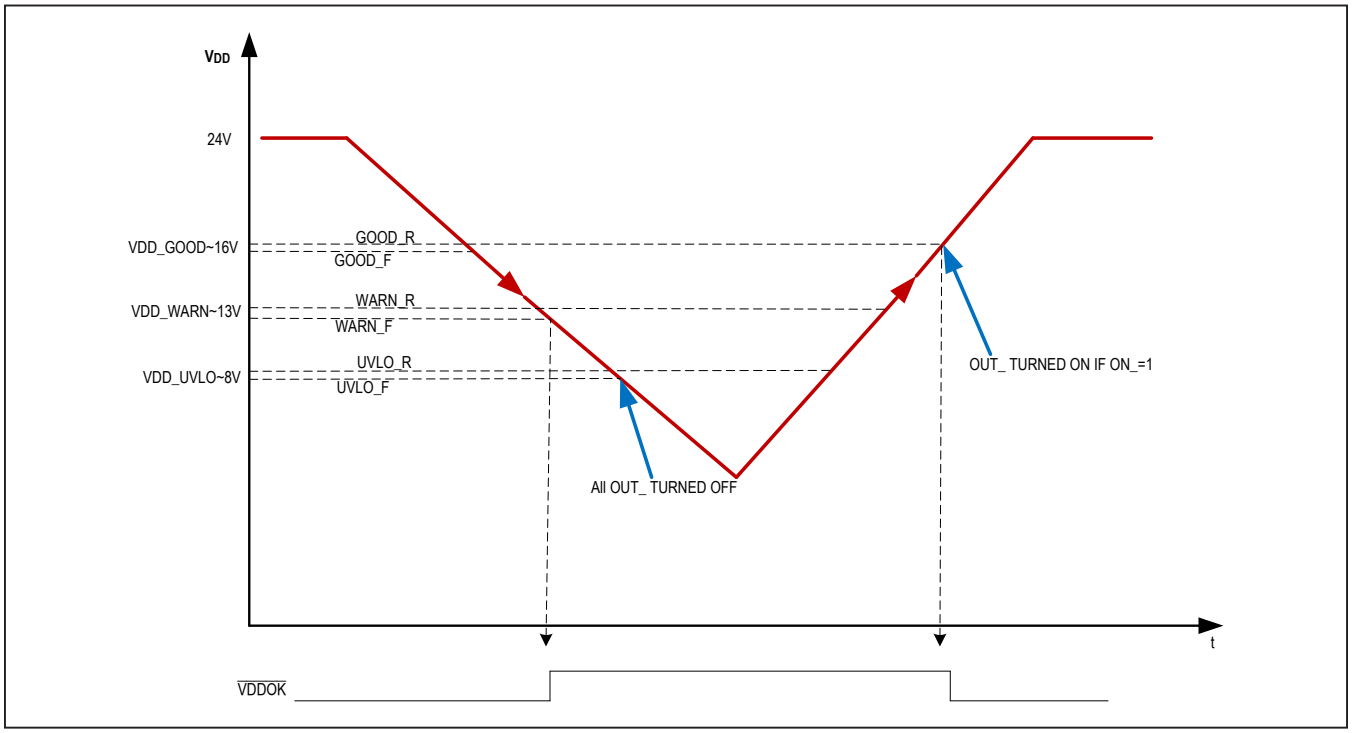


Figure 4. V_{DD} Monitoring with VDDOnThr = 1

Channel Thermal Management

Every driver's temperature is constantly monitored. If the temperature of a driver rises above the thermal shutdown threshold of 150°C (typ), that channel is automatically turned off for protection. After the temperature drops by 15°C, the driver will be turned on again.

When a driver turns off due to thermal shutdown, the per-channel overload bits, OVL_, the interrupt OverLdFault bit and $\overline{\text{FAULT}}$ pin indicate this condition, if enabled. See *Register Map*.

Current Limiting

Each high-side switch features active current limiting. When the load current exceeds 1A (typ), the load current is limited by the high-side switch. If the load impedance tries to draw higher current, the voltage across the high-side FET switch increases and the temperature of the FET increases in accordance with the FET's power dissipation. When an OUT_ channel shows an overcurrent, the CL_ bit is set in the CurrLimF register.

Lamp Load Turn On

Incandescent lamps initially draw high currents while their filament is cold, and this turn-on current reduces as the filament heats up. The MAX14915 has a scheme that automatically detects the presence of a lamps loads. When a lamp load is detected the overtemperature and overload messages are avoided for a duration of 200ms. The lamp load detection is transparent to the user and is not signaled to the user.

Diagnostics

Table 2 lists the per channel diagnostics made available by the MAX14915. The state of the high-side switch for which diagnostics are determined is shown in the Table 1.

Table 2 summarizes the global diagnostics.

Table 1. Per-Channel Diagnostics

PER CHANNEL DIAGNOSTIC	SWITCH STATE	ENABLED	INTERRUPT MASK ENABLED
Overload	Closed	By default	By OverldM
Overcurrent	Closed	By default	By CurrLimM
Open Wire On	Closed	Per channel	By OWOnM
Open WIre Off	Open	Per channel	By OWOffM
Short to VDD	Open	Per channel	By ShtVddM

Table 2. Global Diagnostics

GLOBAL DIAGNOSTICS	FUNCTION	ENABLED	FAULT INTERRUPT MASK
ThrmShut	Chip thermal shutdown	Always On	None
Vint_UV	Undervoltage on the internal supply for the SPI registers	Always On	None
VA_UVLO	VA was in undervoltage	Always On	SupplyErrM
VDD_Warn	Low VDD warning	Always On	VddOKM
VddUvlo	VDD supply in UVLO, all OUT_ switches turned off	Always On	SupplyErrM
VddNotGood	Not Good VDD warning	Always On	VddOKM
WDErr	SPI has no activity for the timeout period	by WDTo[1:0] (DAISY = Low) by A0/WDEN (DAISY = High)	ComErrM
SynchErr	SYNCH input stuck low for the timeout period	by SynchWDEn (DAISY = Low) by A1/SWDEN (DAISY = High)	ComErrM
ComErr	SPI CRC or Communication error	by CRCEN pin	ComErrM

Diagnostics Filtering

Open-wire detection and short-to-V_{DD} detection, in conjunction with reactive loads, can take many milliseconds to settle to stable conditions after a change of high-side switch state. During this time, diagnostic detection would not generate reliable results. Therefore, after the OUT_ switching instant, a blanking period of 4ms (optionally 8ms through register bit) is observed, during which these diagnostics are not evaluated. After this 4ms blanking time, an averaging filter is engaged for 4ms, after which the short-to-V_{DD} and open-wire diagnostics are determined and updated as per channel diagnostics in the OwOffChF, OwOnChF, and ShtVDDChF registers. Consequentially, the Interrupt register, FLEDs (if FLEDSet = 0), and diagnostic bits in the SDO data (if read).

When an OUT_ switch changes On/Off state, the diagnostic state for the previous state is cleared internally. The registers diagnostic bits are cleared if FLatchEn = 0. If FLatchEn = 1, the diagnostic bits are cleared by an SPI read command.

For the overload and overcurrent diagnostics detection, a 54µs filter time is employed and there is no blanking time. If a lamp load is detected on an OUT_, this is seen as a normal load and, therefore, overload and overcurrent diagnostics are not set during the lamp-load detect time.

Open-Wire Detection

Monitoring of an open wire/open load condition can be enabled on a per-channel basis through serial configuration. Open-wire detection can be selected for either, or both, of the cases with a high-side switch in the on or/and the off state.

Open-Wire Detection with Switch On

Open load detection can be enabled on any OUT_ switch through the OwOnEN_ bits. When the HS switch is on, the load current flowing out of the high-side switch is monitored. If this current drops to below a threshold value set through the resistor connected to the OWONSET, an open load detection fault is reported.

The OWONSET resistor allows selecting a load current threshold in the range of 0.35mA (typ) to 2.5mA (typ)

Open-Wire Detection with Switch Off

Monitoring of an open-wire condition in the switch off-state can be enabled on individual channels through the OWOffEn_ bits. When the HS switch is off, a weak current source, IOL, is enabled that pulls OUT_ to 6.7V during a wire break. If the OUT_ voltage is above 5V(min) and below the V_{TH_SHVDD} (9V-14V) voltage threshold, an open load is signaled.

Short to V_{DD} Detection

The MAX14915 can detect shorts to V_{DD}, if enabled through SPI. This only operates when an OUT_ switch is off. If the OUT_ voltage is higher than the threshold voltage set by the ShrtVddThr0 and ShrtVddThr1 bits, a ShtVddFault is indicated in the GloblErr and ShtVddChF registers, as well as the $\overline{FAULT}$ output pin (if not masked). The bits allow setting a V_{TH_SHVDD} threshold in the range of 9V to 14V when V_{DD} is above VDD_GOOD threshold. For V_{DD} below 16V (typ), the V_{TH_SHVDD} is always set to 9V independently by the ShtVddChF bits.

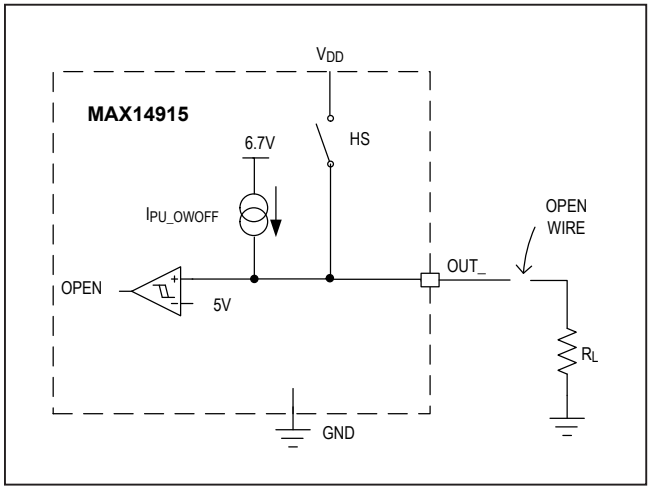


Figure 5. Open Wire Detection Scheme

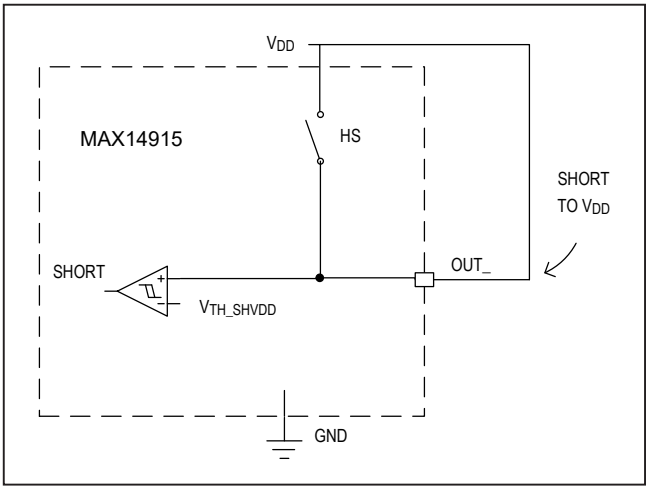


Figure 6. Short to V_{DD} Detection Scheme

Diagnostic Bit Behavior

The per channel diagnostic bits (OVL_, CL_, OWOff_, OWOn_, SHVDD_) can be configured to be latched or real-time through the FLatchEn bit in the Config1 register. When latched diagnostics are enabled (FLatchEn = 1), the diagnostic bits are set = 1 when a fault is detected and remains = 1, even if the fault disappears. This bit is only reset to = 0 when the cause of the fault has disappeared AND the relevant fault register is read through SPI — in address SPI mode. If the cause of the fault has not disappeared, the diagnostic bit remains = 1.

In daisy-chain mode, the $\overline{FAULT}$ pin and the F-bits in SDO are cleared on the following SPI cycle if the fault condition was removed.

The per-channel faults in each of the five error registers are logically or'ed together to produce the fault bits in the Interrupt register. This is shown in the following diagram on the basis of overload diagnostics.

$\overline{FAULT}$ Pin Signalling

The $\overline{FAULT}$pin is an open-drain logic output that transitions active low when a fault condition is detected. The source of faults are the eight bits in the Interrupt register: per-channel faults and global faults. The source of $\overline{FAULT}$ can be masked through the Mask register.

In addressed SPI mode, the diagnostics can be latched (FLatchEn = 1), in which case the $\overline{FAULT}$pin can only be cleared by reading the Interrupt register AND the corresponding fault register(s), whose fault is latched in the Interrupt register. In latched diagnostics mode, $\overline{FAULT}$cannot be cleared by only reading the Interrupt register. If FLatch = 0, then the diagnostic bits, the Interrupt register bits and the $\overline{FAULT}$pin are not latched, so are real time.

In daisy-chain mode, the $\overline{FAULT}$pin is latched, so is cleared on the next SPI cycle, if the cause of the fault has disappeared.

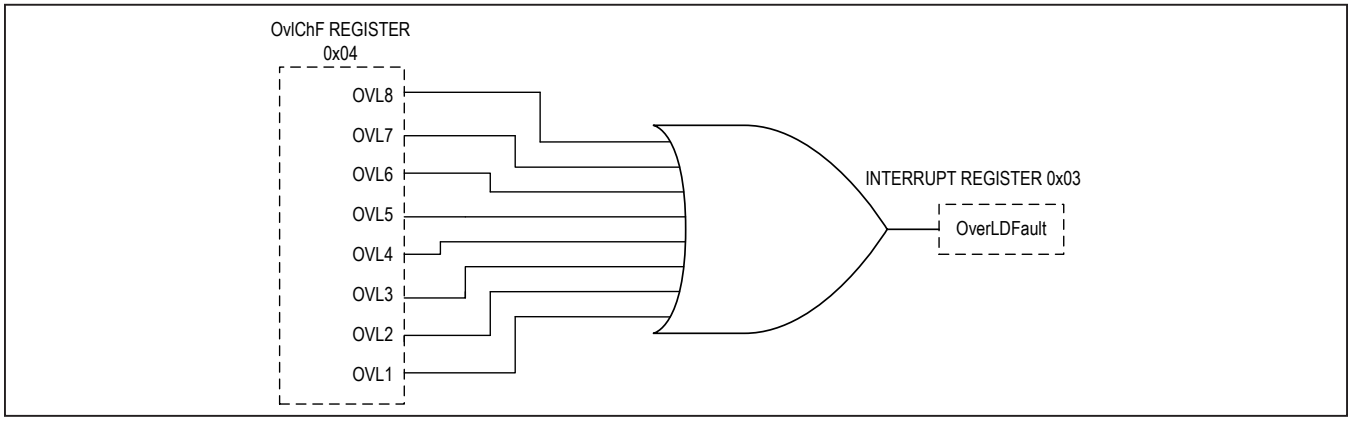


Figure 7. Overload Interrupt Diagnostic Scheme

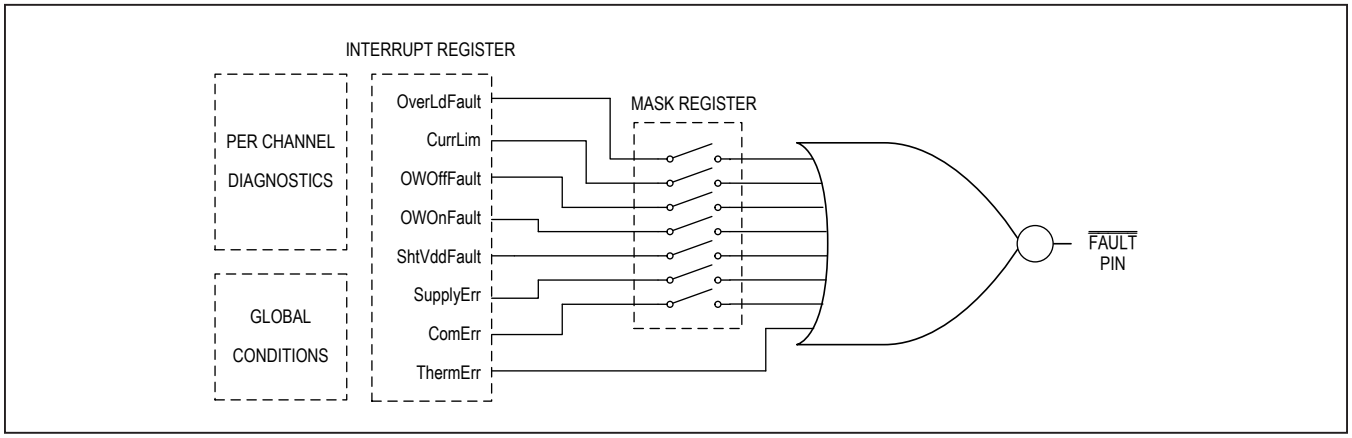


Figure 8. $\overline{FAULT}$ Signaling Scheme

Watchdog

MAX14915 provides two watchdog timers to allow monitoring activity on the SPI interface and on SYNCH pin. In daisy-chain SPI mode, drive A0/WDEN and/or A1/SYNCWD high to enable the watchdog for SPI and/or SYNCH pin. In addressed SPI mode, the watchdog timer is enabled through the WDTo_ bits. If enabled, it will monitor and expect clock activity on the CLK and $\overline{CS}$ inputs. At least one valid SPI cycle must be detected in the WD-timeout period. This means that the CLK input must have a multiple of 8 clock cycles during a $\overline{CS}$ low period.

The SYNCH pin watchdog can be enabled by SynchWDEn bit and it will monitor the SYNCH pin if it is not stuck low. At least a 1µs SYNCH pin high must be detected in the WD-timeout period to avoid SYNCH pin watchdog error.

If the watchdog criterion is not met, all OUT_ switches are automatically turned off and the $\overline{FAULT}$ pin is set active-low. In addressed SPI mode, the WDErr and ComErr bits are set to 1.

In addresses SPI mode, SYNCH and SPI watchdog timeout can be selected through the WDTo_ bits in the Config2 register. In daisy-chain SPI mode, the watchdog timeout for both SPI and SYNCH pin is 1.2s.

LED Drivers

The 4x4 LED driver crossbar matrix offers an efficient configuration for driving up to 16 LEDs. The LEDs can either be turned on/off by the SPI master by setting the SetSLED and/or SetFLED register bits in addressed SPI mode, or can be controlled by the MAX14915 autonomously to indicate per-channel status and fault conditions, depending on configuration in the Config1 register.

If controlled internally (SLEDSet = 0 or FLEDSet = 0), a channel's status LED will automatically be turned on when the corresponding OUT_ switch is on and there is no fault condition. If diagnostics detection is enabled on any OUT_ switch and a fault is detected, its associated fault LED (FLED) is turned on and its associated status LED (SLED) is automatically turned off. This means that for any OUT_ channel, its SLED and its FLED will never be on simultaneously.

If FLEDSet = 0, diagnostics that are enabled (ShtVdd, OWOnCh, OWOff, CL, OVL) will result in FLEDs turning on when a fault is detected. Only overcurrent detection can be masked from driving the FLEDs through the LEDCurrLim bit.

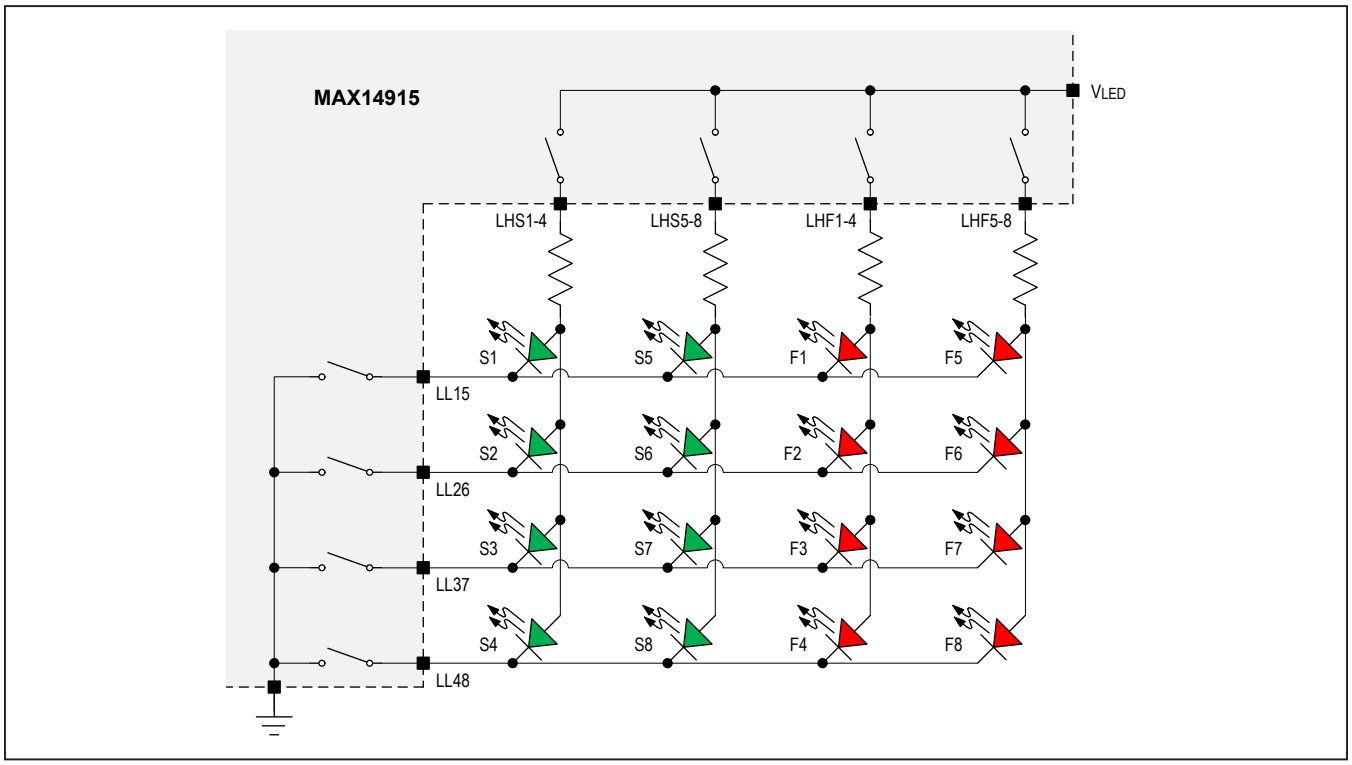


Figure 9. LED Matrix Scheme

When a lamp load is detected during OUT_ turn-on, its SLED is turned on and its FLED stays off.

If the FLEDs are controlled internally, they are always filtered, both in daisy chain and addressed SPI modes. When controlled internally, the FLED minimum on-time can be programmed through the two FLEDStretch_ bits. The SLEDs are real-time when controlled internally.

The LED matrix is powered through the V_{LED} supply input, which can be in the range of the 3.0V (min) up to the V_{DD} field supply voltage.

If daisy-chain mode is selected (DAISY pin high) the LED matrix is always controlled by MAX14915. FAULT LEDs signal only OVL faults and they are stretched by 2s.

For every current limiting resistor, R, each of the four LEDs in a column string is pulsed for a quarter of the time, so that current only flows through one LED and resistor at any one time. Thus the resistors, R, determine the LED current through one LED during the pulse. Each LED is pulsed on at a rate of 1kHz (typ) and is on for 25% of the 1ms period. Thus the average current flowing through a LED that is turned on, is about 0.25 x (V_{LED} - V_F)/R. V_F is the forward voltage of the LED. The resistor value should be chosen according to the LED's current/light intensity requirements.

Serial Interface

The MAX14915 communicates with the host controller through a high-speed SPI serial interface. The interface has three logic inputs: clock (CLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is three-stated when $\overline{CS}$ is high. The maximum SPI clock rate is 10MHz. The SPI interface logic complies with SPI clock polarity CPOL = 0 and clock phase CPHA = 0.

The MAX14915 SPI can either be operated in addressed SPI mode or in daisy-chain mode. Addressed SPI (DAISY = low) allows direct communication with up to four MAX14915 on a shared SPI using a single, shared $\overline{CS}$signal. Addressed SPI offers the advantage direct chip access and getting global diagnostics in the same SPI cycle. Addressed SPI supports both single cycle and burst mode read/writing.

Daisy chained SPI is enabled by driving DAISY = high. In daisy-chain mode, the first SDO byte provides the channel diagnostics based only on driver overload. Daisy-chain mode provides limited features like reduced diagnostics and configuration.

Since the power-on default configuration is different in daisy-chain mode versus addressed SPI modes, the MAX14915 does not support dynamic switching between daisy-chain and addressed SPI modes during operation.

Addressed SPI Chip Addressing (A1, A0)

In addressed SPI mode, a SPI master can communicate with up to four MAX14915 devices on a shared, non-daisy-chained SPI bus with one single/shared $\overline{CS}$ through chip addressing. Each chip on the shared SPI is assigned an individual chip address through the logic input pins A1 and A0, see Table 3.

The SPI master addresses a specific chip by sending the appropriate A1, A0 logic in the first and second bits of the SPI read/write command. The MAX14915 monitors the SPI-address in each SPI read/write cycle and responds appropriately when the address matches the programmed address for that IC.

Addressed SPI In-Band Diagnostic Fault Signaling

In every addressed SPI cycle, the MAX14915 returns six bits in SDO within the first eight SPI CLK cycles. These six bits include the global short-to-V_{DD}, wire-break-on, wire-break-off, overload, overcurrent as well as a global diagnostics bit. The global fault bit, GlobIF, is the logic OR of the ComErr, SupplyErr and ThErr bits. These five diagnostic bits allows for fast identification of the specific channel in fault or global fault condition.

During an SPI write cycle, the second SDO byte returns eight fault bits, one bit associated with each OUT channel. These bits are the logic OR of the diagnostic faults.

Table 3. SPI Device Address Selection

A1	A0	DEVICE ADDRESS
LOW	LOW	00
LOW	HIGH	01
HIGH	LOW	10
HIGH	HIGH	11

Single-Cycle Addressed SPI Read

The following shows the SPI read command in addressed SPI mode (DAISY = low).

Single-Cycle Addressed SPI Write

The following shows the SPI write command in SPI addressed mode (DAISY = low):

The F_ bits in the second byte of SDO write cycle are the per-channel fault bits. These are the logic OR of the channel fault bits in the OvlChF, CurrLimChF, OwOffChF, OwOnChF and ShtVDDChF registers. If only one OUT channel has diagnostic fault(s), then an SPI Write command provides full diagnostic information: the channel and the all faults. The only reason to subsequently read the diagnostic registers is to reset the diagnostic bits.

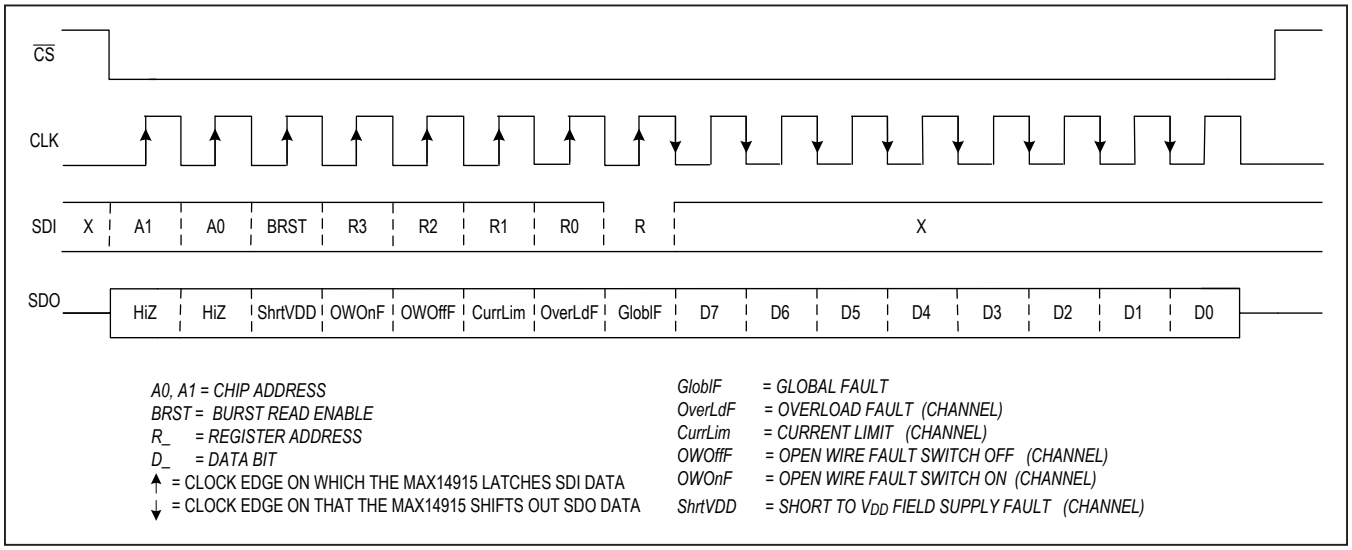


Figure 10. Addressed SPI Single Read Command

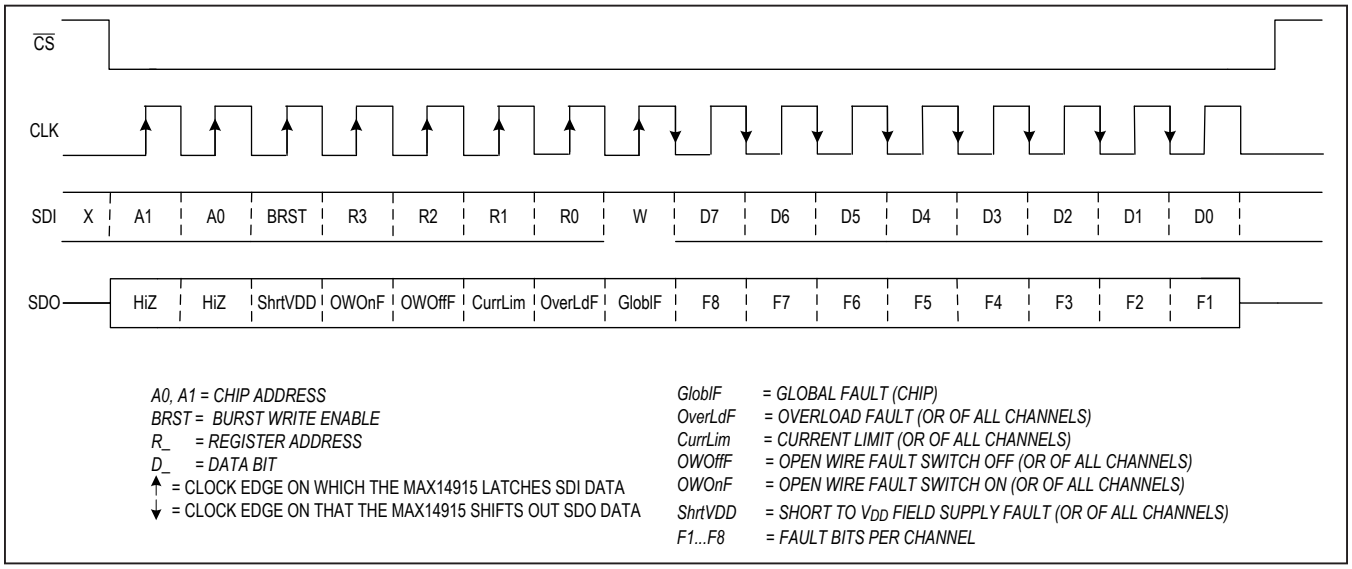


Figure 11. Addressed SPI Single Cycle Write Command

SPI Burst Write

In addressed SPI mode (DAISY = low), burst SPI writing is supported. This allows efficient writing of registers that are commonly accessed: SetOUT, SetSLED and SetFLED. Burst SPI uses one SPI cycle and one register address to write to multiple consecutive registers. A burst write is enabled through the BRST bit in the SDI command byte. If the BRST bit is set, the MAX14915 expects an SPI write cycle writing to 2 or 3 registers. The chip-select input ($\overline{CS}$) must be held low during the entire burst write cycle. The SPI clock continues clocking throughout the burst cycle. Only the initial register address (0x00) is specified in the SDI command byte, followed by two or three bytes of data. The burst length is defined by the number of CLK clocks in the SPI cycle: for a 2 register burst write, 24 clocks are needed if CRC is not used, and 32 clocks are needed with CRC. For a 3 register burst write, 32 SPI clocks are needed without CRC enabled, and 40 clocks with CRC. The burst cycle ends when the $\overline{CS}$ is driven high.

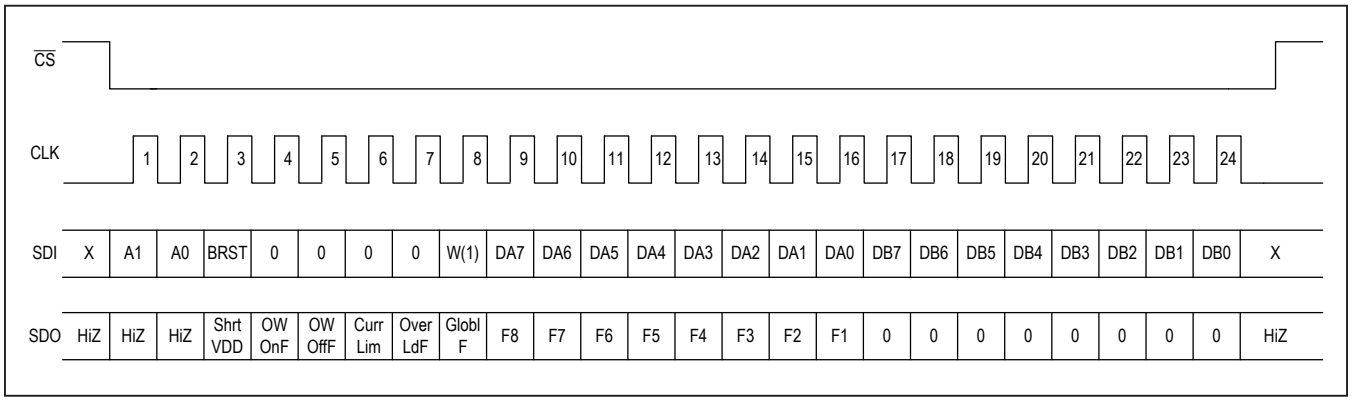


Figure 12. Addressed SPI Single Cycle Write Command

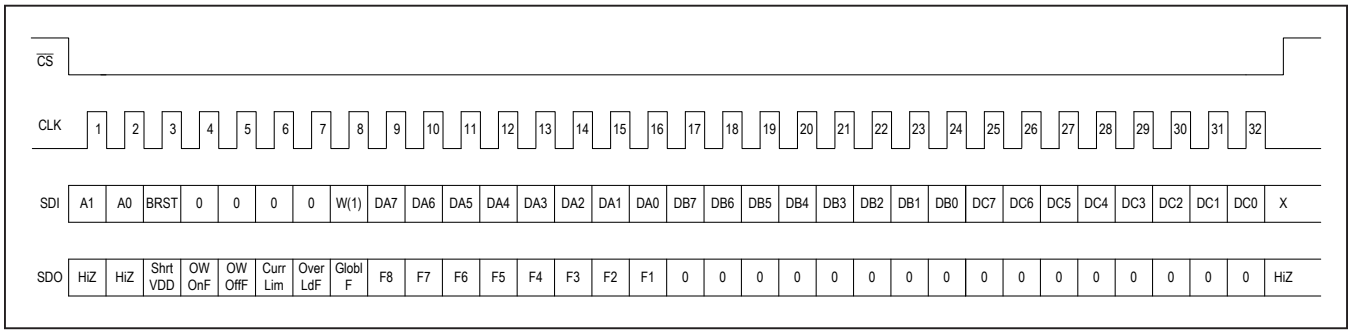


Figure 13. Addressed SPI Three Bytes Burst Write Command

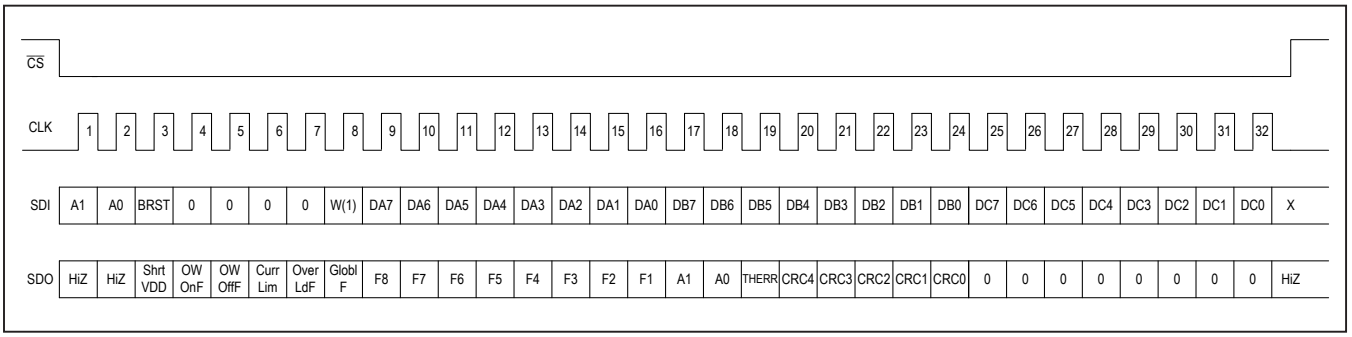


Figure 14. Addressed SPI Two Bytes Burst Write Command with CRC

(*) CRC_ bit are calculated on all the data send before CRC_ bits.

SPI Burst Read

In addressed SPI mode (DAISY = low), burst SPI reading is supported. Burst SPI reading allows efficient reading of multiple registers in one SPI cycle. The MAX14915 only supports burst reading of the diagnostic registers OvlChF, CurrLimF, OwOffChF, OwOnChF, ShtVDDChF, GloblErr.

Set the BRST bit in the SDI command byte to signal a burst SPI cycle. The first register address must be 0x04 (OvlChF register) and it must end with the register 0x09 (GloblErr register). Total of six consecutive registers can be read within the burst read cycle. If the burst read command ends before the GloblErr register, a communication error is signaled on $\overline{\text{COMERR}}$ pin.

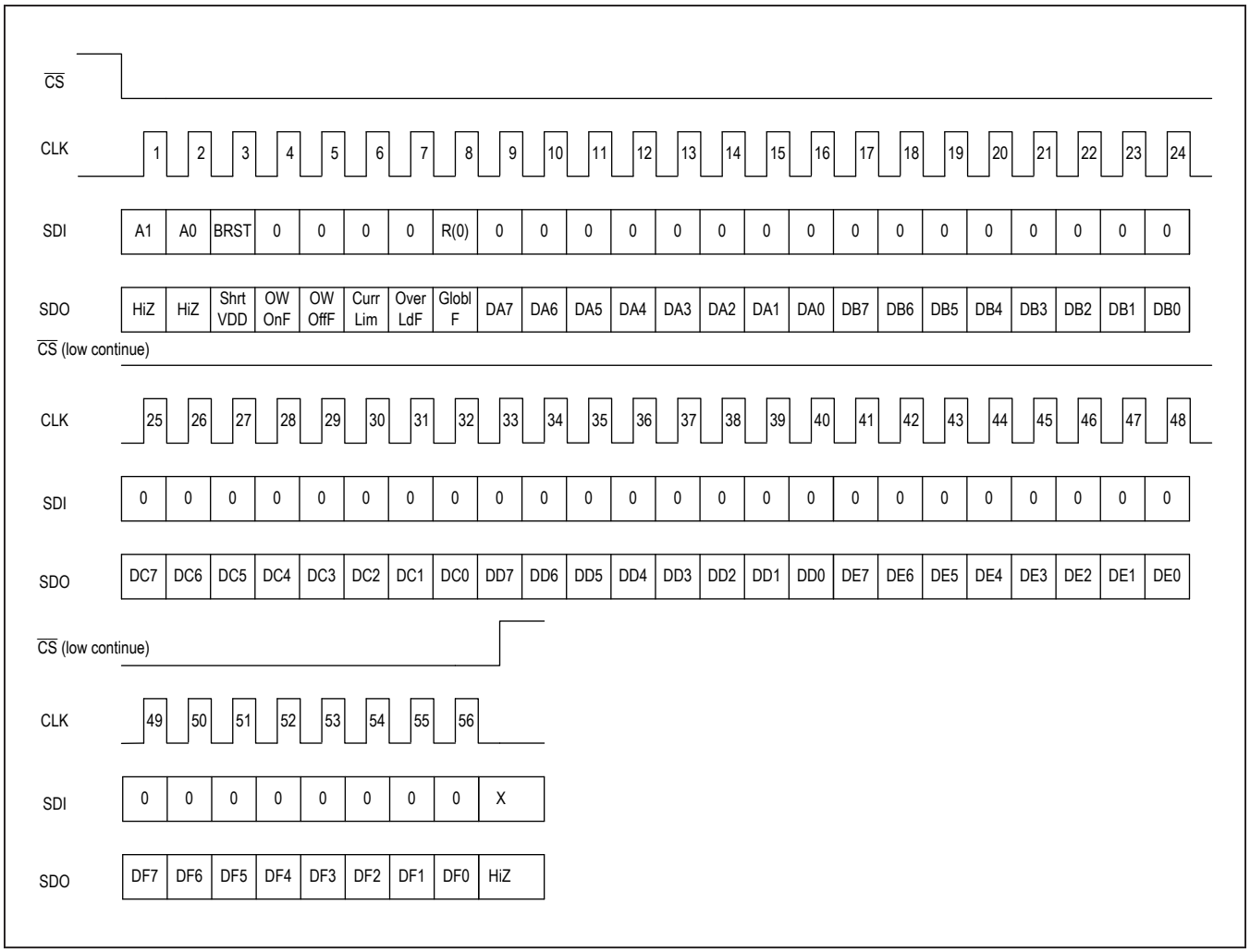


Figure 15. Addressed SPI Six Bytes Burst Read Command

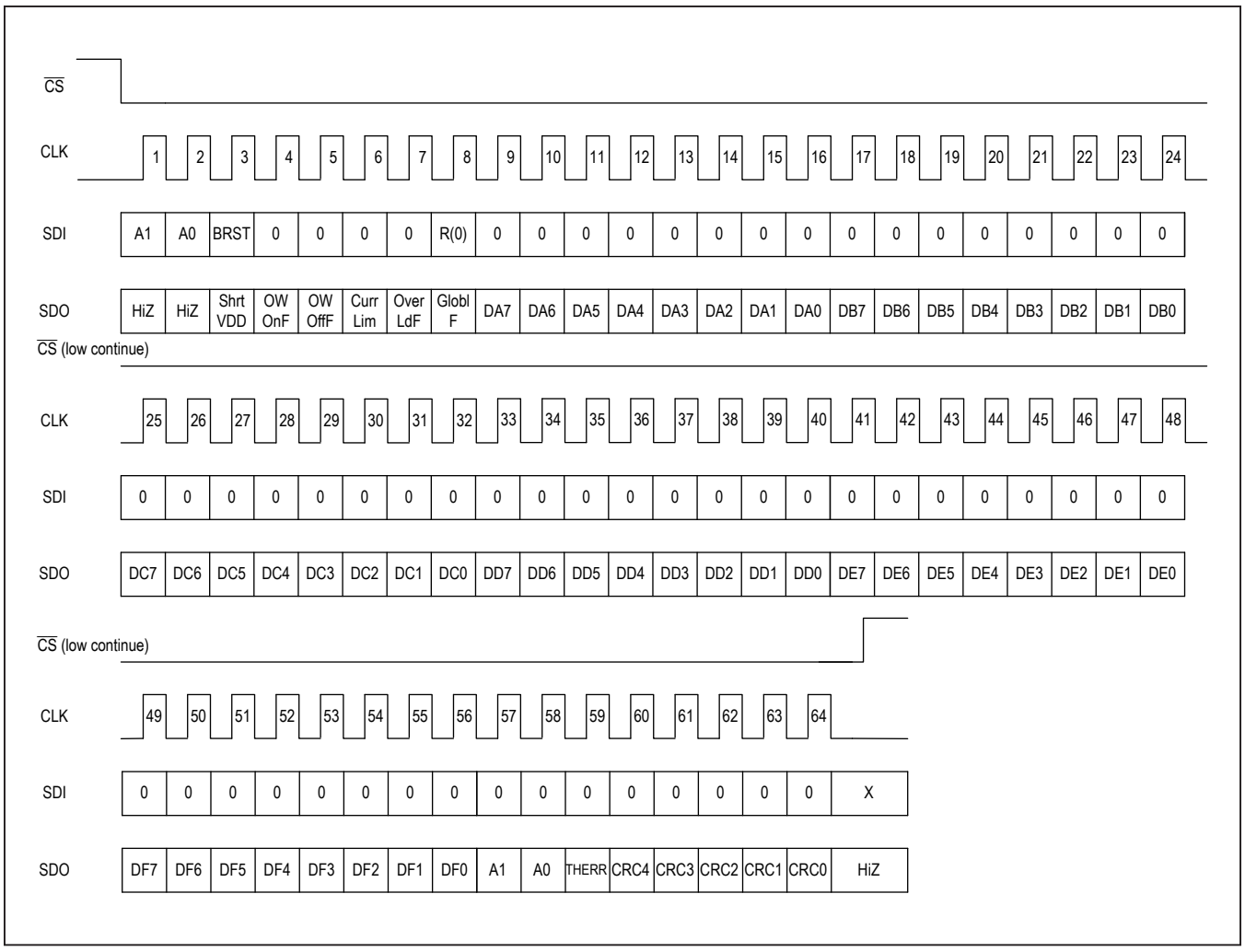


Figure 16. Addressed SPI Six Bytes Burst Read Command with CRC

Daisy-Chained SPI

Daisy-chained SPI mode (DAISY = high) allows communication with multiple MAX14915 with one $\overline{CS}$signal in one SPI cycle. In daisy-chain mode, register access is not possible. Switching between daisy chain and addressed modes is not supported. Daisy-chain mode only allows turning the OUT_ switches on/off and reading per channel thermal overload diagnostics as well as chip thermal shutdown.

The following shows a single daisy chain mode SPI cycle without CRC enabled (CRCEN = low), based on only one device in the SPI chain:

The ON_ bits turn the OUT_ switches on. The F_ bits are per-channel diagnostics, and are the same as the OVL_ bits in the OvlChF register. The F_ bits are latched and are, therefore, only cleared on the following SPI cycle if the fault has disappeared before the following SPI cycle. The F_ bits are filtered, so do not go active when a lamp load is detected. In thermal chip shutdown, all F_ bits are set to 1.

Daisy-chain SPI mode also supports CRC error detection/correction, which lengthens the minimum SPI cycle to 16 CLK clocks per MAX14915.

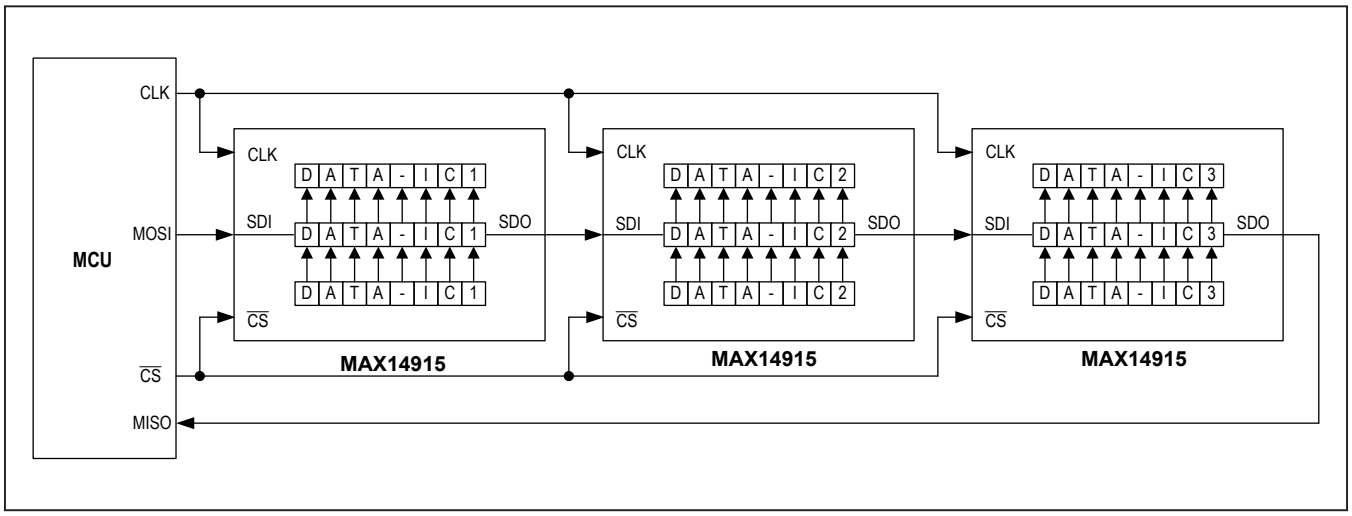


Figure 17. Daisy-Chaining Diagram of Three MAX14915

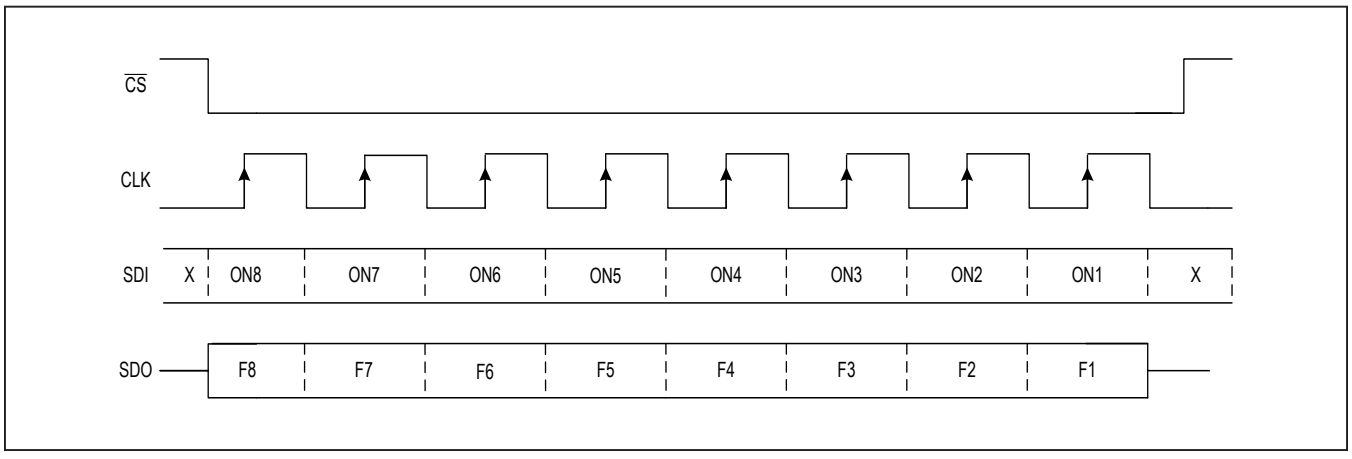


Figure 18. Single Daisy-Chain SPI Command

Checking of Clocks on the Serial Interface

In addressed SPI and daisy-chain SPI modes, the MAX14915 checks that the number of clock cycles in one SPI cycle (from falling edge of $\overline{CS}$ to rising edge of $\overline{CS}$) is a multiple of 8, with 8 clocks minimum for daisy-chain mode and 16 clocks minimum for addressed SPI modes. The expected number of clocks is scaled according to CRCEN setting and Burst mode settings. If the number of clock cycles differs from the expected, then the SPI command is not executed and an SPI error is signaled through the $\overline{COMERR}$ pin.

CRC Error Detection on the Serial Interface

CRC error detection of the serial data can be enabled to minimize incorrect operation/misinformation due to data corruption of the SDI/SDO signals. If error detection is enabled, then the MAX14915:

1) Performs error detection on the SDI data that it receives from the controller, and
2) Calculates a CRC on the SDO data and appends a check byte to the SDO diagnostics/status data that it sends to the controller.

This ensures that both the data that it receives from the controller (setting/configuration) and the data that it sends to the controller (diagnostics/status) have a low likelihood of undetected errors.

Setting the CRCEN input high enables CRC error detection. A CRC Frame Check Sequence (FCS) is then sent along with each serial transaction. The 5-bit FCS is based on the generator polynomial X5 + X4 + X2 + 1 with CRC starting value = 11111.

When CRC is enabled, the MAX14915 expects a check byte appended to the SDI program/configure data that it receives. The check byte has the following format:

Table 4. Valid Data Length

DAISY	CRCEN	R/W BIT	BRST BIT	VALID DATA LENGTH (*)
0	0	1	0	16
0	0	1	1	24 or 32
0	1	1	0	24
0	1	1	1	32 or 40
0	0	0	0	16
0	0	0	1	56
0	1	0	0	24
0	1	0	1	64
1	0	x	x	8xN (**)
1	1	x	x	16xN (**)

(*) This is the number of CLK rising edges between $\overline{CS}$ falling and rising edges

(**) N is an integer number of daisy-chained devices

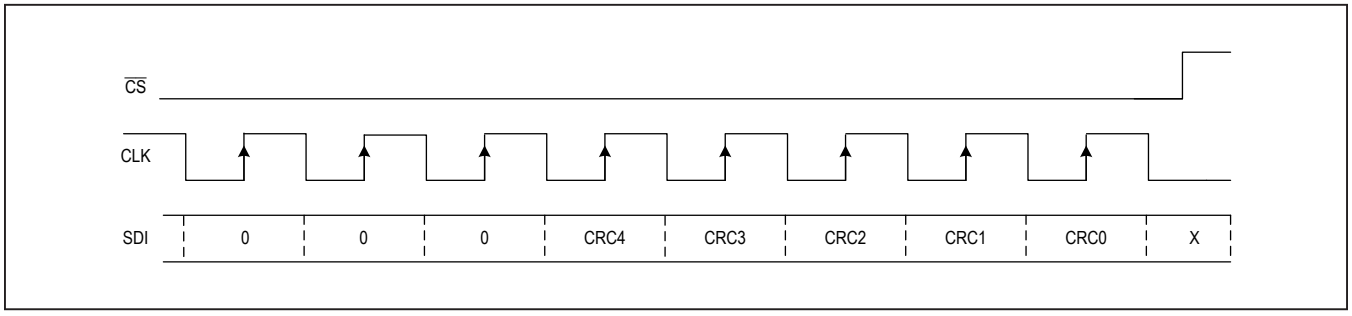


Figure 19. FCS Byte Expected from the SPI Master

The five FCS bits (CR_) are calculated on all the data sent in one SPI command including the three “0” in the MSBs of the check byte. Therefore, the CRC is calculated from 8 + 3 bits up to 56 + 3 bits in case of burst command. CR0 is the LSB of the FCS.

The MAX14915 verifies the received FCS. If no error is detected, the MAX14915 sets the OUT_ output switches and/or changes configuration per the SDI data. If a CRC error is detected, then the MAX14915 does not change the OUT_ outputs and/or does not change its configuration. Instead, the MAX14915 sets the $\overline{\text{COMERR}}$ logic output low (i.e., the open-drain COMERR NMOS output transistor is turned on).

The check byte that the MAX14915 appends to the SDO data has the format seen in Figure 20 when the DAISY pin is low.

A1 and A0 are the level for A1/A0 pins while THERR bit is set when a chip thermal shutdown event has occurred.

CR_ are the CRC bits that the MAX14915 calculates on the SDO data, including the A1, A0, and THERR bits. This allows the controller to check for errors on the SDO data received from the MAX14915.

The CMERR is set when either a SPI or SYNCH pin WatchDog event has occurred.

The THERR bit is set when either the thermal warning or the thermal shutdown occurs. The VERR bit in FCS byte corresponds to the SupplyErr bit in the Interrupt register.

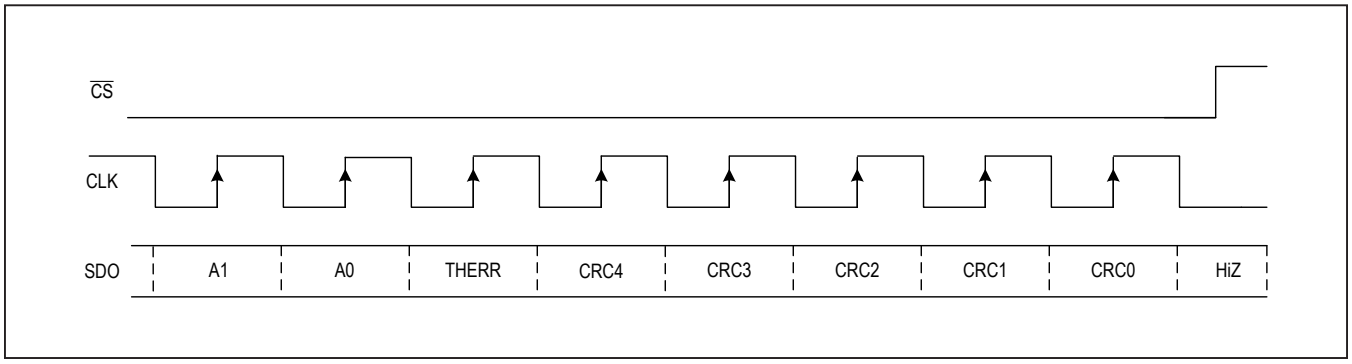


Figure 20. FCS Byte Sent by the MAX14915 to SPI Master (SPI Addressed Mode)

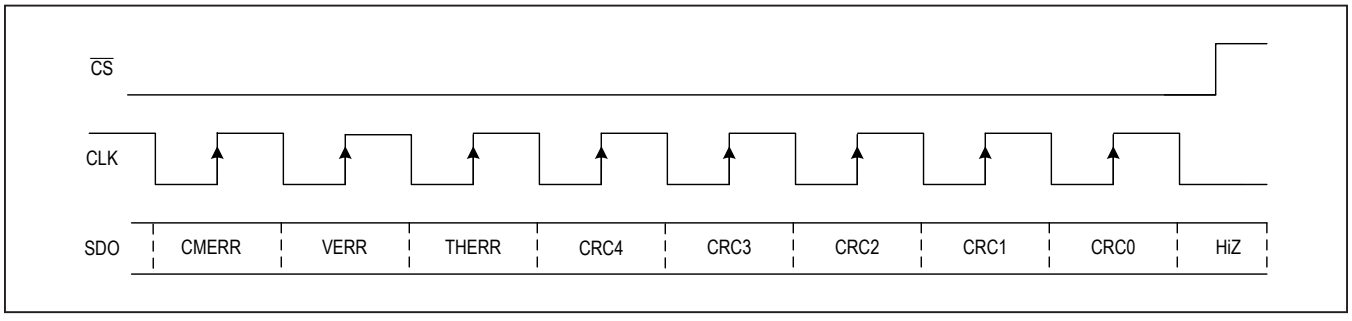


Figure 21. FCS Byte Sent by the MAX14915 to SPI Master in Daisy-Chain Mode

Register Map

	REGISTER ADDRESS	ACCESS TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SetOUT	0x00	R/W	On8	On7	On6	On5	On4	On3	On2	On1
SetFLED	0x01	R/W	FLED8	FLED7	FLED6	FLED5	FLED4	FLED3	FLED2	FLED1
SetSLED	0x02	R/W	SLED8	SLED7	SLED6	SLED5	SLED4	SLED3	SLED2	SLED1
Interrupt	0x03	R	ComErr	SupplyErr	ThErr	ShtVdd-Fault	OWOn-Fault	OWOff-Fault	CurrLim	OverLd-Fault
OvlChF	0x04	R	OVL8	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1
CurrLim	0x05	R	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1
OwOffChF	0x06	R	OWOff8	OWOff7	OWOff6	OWOff5	OWOff4	OWOff3	OWOff2	OWOff1
OwOnChF	0x07	R	OWOn8	OWOn7	OWOn6	OWOn5	OWOn4	OWOn3	OWOn2	OWOn1
ShtVD-DChF	0x08	R	SHVDD8	SHVDD7	SHVDD6	SHVDD5	SHVDD4	SHVDD3	SHVDD2	SHVDD1
GlobalErr	0x09	R	WDErr	SynchErr	ThrmShutd	VddUvlo	VddWarn	VddNot-Good	VA_UVLO	Vint_UV
OwOffEn	0x0A	R/W	OwOffEn8	OwOffEn7	OwOffEn6	OwOffEn5	OwOffEn4	OwOffEn3	OwOffEn2	OwOffEn1
OwOnEn	0x0B	R/W	OwOnEn8	OwOnEn7	OwOnEn6	OwOnEn5	OwOnEn4	OwOnEn3	OwOnEn2	OwOnEn1
ShtVddEn	0x0C	R/W	ShtVdd En8	ShtVdd En7	ShtVdd En6	ShtVdd En5	ShtVdd En4	ShtVdd En3	ShtVdd En2	ShtVdd En1
Config1	0x0D	R/W	LEDCur-rLim	FLatchEn	FiltrLong	FFilterEn	FLED-Strech0	FLED-Strech0	SLEDSet	FLEDSet
Config2	0x0E	R/W	WDTo1	WDTo0	OWOffCs1	OWOffCs0	ShtVdd Thr1	ShtVdd Thr0	Synch-WDEn	VDDOnThr
Mask	0x0F	R/W	ComErrM	Supply-ErrM	VddOKM	ShtVddM	OWOnM	OWOffM	CurrLimM	OverLdM

SetOUT Register (0x00)

SetOUT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	On8	On7	On6	On5	On4	On3	On2	On1
POR Addrss	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

On_

Set On_ = 1 to close the associated OUT_ high-side switch. Set On_ = 0 to open the high-side switch.

SetFLED Register (0x01)

SetFLED	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	FLED8	FLED7	FLED6	FLED5	FLED4	FLED3	FLED2	FLED1
POR Addrss	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FLED_

Set FLEDx = 0 turn FLEDx fault LED off. The FLED register bits only operate if the FLEDSet bits is set in the Config1 register.

SetSLED Register (0x02)

SetSLED	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	SLED8	SLED7	SLED6	SLED5	SLED4	SLED3	SLED2	SLED1
POR Addrss	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SLED_

Set SLEDx = 1 to turn on the SLEDx status LED. Set SLEDx = 0 turn status LED SLEDx off. The SLED register bits only operate if the SLEDSet bits is set in the Config1 register.

Interrupt Register (0x03)

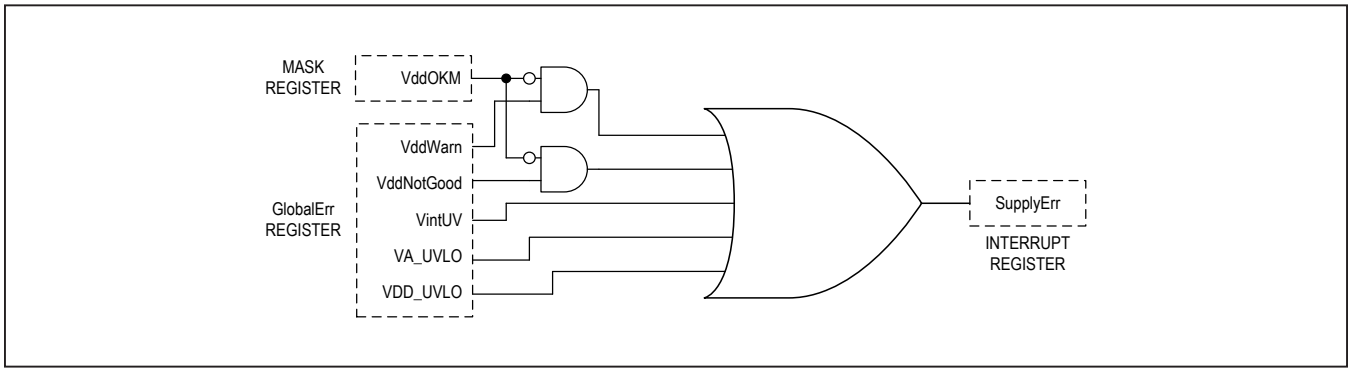
Interupt	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	ComErr	SupplyErr	ThrmErr	ShtVddFault	OWOnFault	OWOffFault	CurrLim-Fault	OverLdFault
POR	0	1	0	0	0	0	0	0
Read / Write	R	R	R	R	R	R	R	R

ComErr

ComErr is set = 1 when a watchdog timeout for SPI interface or SYNCH pin is detected. If the errors are latched (FLatchEn = 1), the ComErr bit is cleared when GlobalErr register is read and the event has disappeared.

SupplyErr

SupplyErr is the logic OR of the VA_UVLO, Vint_UV and SupplyInt bits in the GlobalErr register. If the errors are latched (FLatchEn = 1), the SupplyErr bit is cleared when GlobalErr register is read and the event has disappeared.



ThermErr

ThermErr is set = 1 after MAX14915 enters chip thermal shutdown.

ShrtVddFault

ShrtVddFault = 1 when a short to Vdd error was detected on any OUT_. The detailed channel can be found in the ShrtVddChF register.

OWOnFault

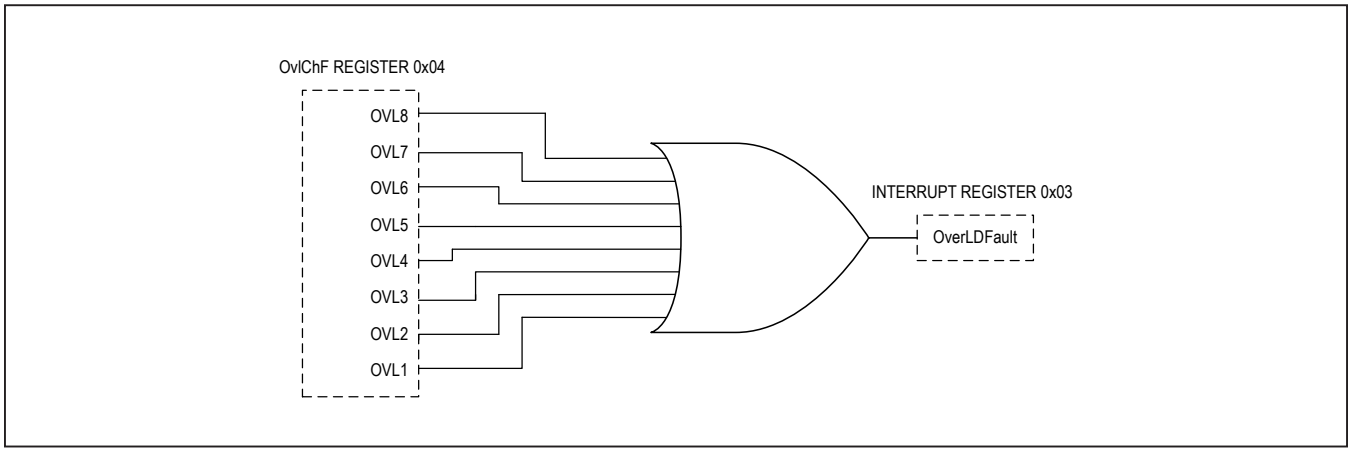
OWOnFault = 1 when an open wire fault in On state is detected on any OUT_. The detailed channel can be found in the OwOnChF register.

OWOffFault

OLOffFault = 1 when an open wire fault in Off state is detected on any OUT_. The detailed channel can be found in the OwOffChF register.

OverLdFault

OverLdFault = 1 when an overload occurs on any OUT_. The detailed channel can be found in the OvlChF register.



OvlChF (0x04)

OvlChF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	OVL8	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1
POR Addrs	0	0	0	0	0	0	0	0
Read / Write	R	R	R	R	R	R	R	R
Reset upon Read	Y	Y	Y	Y	Y	Y	Y	Y
Latched	Y	Y	Y	Y	Y	Y	Y	Y

OVL_

OVL_ = 1 when a thermal overload is detected on OUT_. All bits are latched, and are only reset when OvlChF is read AND the overload condition is not present.

CurrLimF (0x05)

CurrLim	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1
POR Addrs	0	0	0	0	0	0	0	0
Read / Write	R	R	R	R	R	R	R	R
Latched	Y	Y	Y	Y	Y	Y	Y	Y

CL_

CL_ = 1 when a current limit is detected on an OUT_ switch while the switch is on. All bits are latched, and are only reset when the CurrLimF register is read AND a current limit condition is not present.

OwOffChF (0x06)

CurrLim	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	OWOff8	OWOff7	OWOff6	OWOff5	OWOff4	OWOff3	OWOff2	OWOff1
POR	0	0	0	0	0	0	0	0
Read / Write	R	R	R	R	R	R	R	R
Latched	Y	Y	Y	Y	Y	Y	Y	Y

OWOff_

OWOff_ = 1 when an open wire fault is detected on OUT_ in the off state. All bits are latched, and are only reset when OwOffChF register is read AND the fault condition is removed.

OwOnChF (0x07)

OwOnChF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	OWOn8	OWOn7	OWOn6	OWOn5	OWOn4	OWOn3	OWOn2	OWOn1
POR	0	0	0	0	0	0	0	0
Read / Write	R	R	R	R	R	R	R	R
Latched	Y	Y	Y	Y	Y	Y	Y	Y

OWOn_

OWOn_ = 1 when an open wire fault is detected on OUT_ in the on state. All bits are latched, and are only reset when OwOnChF register is read AND the fault condition is removed.

ShtVDDChF (0x08)

OwOffEn	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	SHVDD8	SHVDD7	SHVDD6	SHVDD5	SHVDD4	SHVDD3	SHVDD2	SHVDD1
POR	0	0	0	0	0	0	0	0
Read / Write	R	R	R	R	R	R	R	R
Latched	Y	Y	Y	Y	Y	Y	Y	Y

SHVDD_SHVDDx = 1 when an OUTx short to VDD fault in the off state occurred. All bits are latched, and bits are only reset when ShtVDDChF register is read AND the fault condition is removed.

GlobalErr (0x09)

GlobalErr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	WDErr	SynchErr	ThrmShutd	VddUvlo	VddWarn	VddNot-Good	VA_UVLO	Vint_UV
POR	0	0	0	1	1	1	1	1
Read / Write	R	R	R	R	R	R	R	R
Latched	Y	Y	Y	Y	Y	Y	Y	Y

WDErr

WDErr is set = 1 when a watchdog timeout is detected, if the watchdog function is enabled through the WDTo_ bits. This bit is mapped to the ComErr bit in the Interrupt register .

SynchErr

SynchErr is set = 1 when a watchdog timeout for SYNCH pin is detected, if the SYNCH pin watchdog function is enabled through the SynchWDEn bit. This bit is mapped to the ComErr bit in the Interrupt register.

ThrmShutdThrmShutd is set = 1 after the MAX14915 enters thermal shutdown. This bit is mapped to the ThErr bit in the Interrupt register.

VddUvlo

VddUvlo bit is set =1 any time V_{DD} drops below UVLO_VDD voltage threshold.VddUvlo bit can be cleared by reading GlobalErr register only if V_{DD} voltage exceeds the VDD_UVLO voltage threshold.

If SupplyErrM bit is 1, V_{DD} falling below UVLO_VDD event triggers the VddUvlo bit and the SupplyErr bit (or VERR bit in SDO signal if daisy-chain mode with CRC operation is selected) in but it will not be signaled by $\overline{FAULT}$ pin.

VddWarn

VddWarn bit is set = 1 any time V_{DD} drops below VDD_WARN voltage threshold.VddWarn bit can be cleared by reading GlobalErr register only if V_{DD} voltage exceeds the VDD_WARN threshold. If VddOKM bit is 1, V_{DD} falling below WARN_V_{DD} events triggers the VddWarn bit, but they will not be signaled by SupplyErr bit and $\overline{FAULT}$ pin.

VddNotGood

VddNotGood bit is set =1 any time V_{DD} drops below VDD_GOOD voltage threshold. VddNotGood bit can be cleared by reading GlobalErr register only if V_{DD} voltage exceeds the VDD_GOOD threshold. If VddOKM bit is 1, V_{DD} falling below VDD_GOOD threshold events triggers the VddNotGood bit but they will not be signaled by SupplyErr bit and $\overline{FAULT}$ pin.

VA_UVLO

VA_UVLO is set to 1 when the VA voltage input falls under the VA_UVLO threshold. If VA_UVLO is = 1, it can be set = 0 by reading the GlobalErr register when the VA voltage exceeds the VA_UVLO threshold.

If SupplyErrM bit is 1, VA falling below VA_UVLO threshold event will trigger the VA_UVLO flag and the SupplyErr bit but it will not be signaled by $\overline{\text{FAULT}}$ pin.

Vint_UV

Vint_UV is set to 1 on initial power-up and after the internal supply to the registers falls to a level where the register contents are lost. This signals that a power-on reset has occurred and informs that all register contents were reset. After power-up Vint_UV = 1 and can be set = 0 by reading the GlobalErr register.

Vint falling below Vint_UVLO threshold event will always trigger the Vint_UV flag, the SupplyErr bit and it will be signaled by $\overline{\text{FAULT}}$ pin and $\overline{\text{READY}}$ pin.

OwOffEn (0x0A)

OwOffEn	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	OwOffEn8	OwOffEn7	OwOffEn6	OwOffEn5	OwOffEn4	OwOffEn3	OwOffEn2	OwOffEn1
POR	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OwOffEn_

Set OwOffEn_ = 1 to enable open wire detection with OUT_ switch in off state. Set OwOffEn_ = 0 to disable open wire detection on OUT_ switch in off state. If OwOffEn_ = 0, the pullup current source is disabled.

OwOnEn (0x0B)

OwOnEn	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	OwOnEn8	OwOnEn7	OwOnEn6	OwOnEn5	OwOnEn4	OwOnEn3	OwOnEn2	OwOnEn1
POR	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OwOnEn_

Set OwOnEn_ = 1 to enable open wire detection with OUT_ switch ON. Set OwOnEn_ = 0 to disable open wire on detection on corresponding OUT_ pin.

ShtVddEn (0x0C)

ShtVddEn	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	ShVddEn8	ShVddEn7	ShVddEn6	ShVddEn5	ShVddEn4	ShVddEn3	ShVddEn2	ShVddEn1
POR	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ShVddEn_

Set ShVddEn_ = 1 to enable detection of a short to VDD on OUT_. Set ShVddEn_ = 0 to disable short to VDD detection on corresponding OUT_ pin.

Config1 Register (0x0D)

Config1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	LEDCurrLim	FLatchEn	FiltrLong	FFilterEn	FLED-Strech1	FLED-Strech0	SLEDSet	FLEDSet
POR	0	1	0	1	0	0	1	1
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEDCurrLim

Set LEDCurrLim = 1 to mask the FLEDs signaling current limiting on a channel when the internal FLED control is active (FLEDSet = 0).

When DAISY is high FLEDs do not show current limiting condition on channel.

FLatchEn

Set FLatchEn = 1 enable latching of diagnostic fault bits in the OvlChF, CurrLimF, OwOffChF, OwOnChF, ShtVDDChF registers. When the Fault LEDs are controlled internally (FLEDSet = 0), the LED on-time is not affected by this bit, but has a minimum on-time defined by the FLEDStrech_ bits and is turned off when the fault disappears, if longer than FLEDStech_ timing.

FiltrLong

Set FiltrLong = 1 to select long blanking time (8ms instead of 4ms) of the diagnostics fault bits in the OwOffChF, OwOnChF, ShtVDDChF. This bit also affects the fault LED turn-on when controlled internally (FLEDSet = 0).

FFilterEn

Set FFilterEn = 1 to enable blanking and filtering of the short-to-VDD, open-wire-on, open-wire-off diagnostic bits in the OwOffChF, OwOnChF, ShtVDDChF registers. If FFilterEn = 0, the diagnostics are all real-time (only filtered by 50us filter) and filtering is left to application software. The internal fault LED control (FLEDSet = 0) always uses filtering, this cannot be disabled through FFilterEn.

FLEDStrech0, FLEDStrech1

The LEDStretch bits select the minimum on-time for the FLEDs, if controlled internally (FLEDSet = 0), so the eye can catch short events.

FLEDStrech1	FLEDStrech0	MINIMUM LED ON TIME
0	0	Disable
0	1	1s
1	0	2s
1	1	3s

When DAISY pin is high the minimum on-time for the FLED is configured to 2s.

SLEDSet

Set SLEDSet = 1 so that the eight status LEDs (SLEDs) are controlled by SetSLED register bits. If SLEDSet = 0, then the eight FLEDs as controlled autonomously by the MAX14915.

When DAISY pin is high the SLEDs are always controlled by the MAX14915.

FLEDSet

Set FLEDSet = 1 for the eight fault FLEDs to be controlled by SetFLED register bits. If FLEDSet = 0, then the FLEDs are controlled by the internal fault diagnostics detection: overload, over-current, open-wire and short-to-VDD (if enabled).

When DAISY pin is high the FLEDs are always controlled by the internal overload fault diagnostics detection.

Config2 Register (0x0E)

Config2	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	WDTo1	WDTo0	OWOffCs1	OWOffCs0	ShtVddThr1	ShrtVdd Thr0	Synch-WDEn	VDDOnThr
POR	0	0	0	0	0	0	0	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WDTo1, WDTo0

The WDTo_ bits enable and set the timeout of the watchdog timer for both SPI and SYNCH.

WDTo1	WDTo0	SPI WATCHDOG TIMEOUT	SYNCH WATCHDOG TIMEOUT
0	0	Disabled	600ms
0	1	200ms	200ms
1	0	600ms	600ms
1	1	1.2s	1.2s

When DAISY pin is high, SPI and SYNCH watchdog timers are both configured to 1.2s and can be enable shorting to VL respectively pins A0 and A1.

OWOffCs1, OWOffCs0

The OWOffCs_ bits select the pull-up current source current magnitude used for the open wire off detection.

OWOffCs1	OWOffCs0	CURRENT (TYP)
0	0	20µA
0	1	100µA
1	0	300µA
1	1	600µA

ShrtVddThr1, ShrtVddThr0

The ShrtVddThr_ bits select the voltage threshold for Short to VDD detection.

ShrtVddThr1	ShrtVddThr0	CURRENT (TYP)
0	0	9V
0	1	10V
1	0	12V
1	1	14V

VDDOnThr

Set VDDOnThr = 1 to select VDD_GOOD_R voltage threshold (16V typ) instead of UVLO_VDD_R voltage threshold (9V typ) for OUT_ switch turn-on when VDD rises after a VDD UVLO event.

VDD_GOOD_R is used if DAISY pin is high.

Mask Register (0x0F)

Mask	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	ComErrM	SupplyErrM	VddOKM	ShtVddM	OWOnM	OWOffM	CurrLimM	OverLdM
POR	1	0	1	1	1	1	1	0
Read / Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ComErrM

Set ComErrM = 1 to disable SPI and SYNCH pin watchdog timeout (if enabled through WDTo_ and SynchWDEn bits) being signaled on the $\overline{FAULT}$ output pin. Independent of the ComErrM bit, these conditions will still be shown in the ComErr bit in the Interrupt register and the GlobIF bit in the SDO signal.

If DAISY pin is high, SPI and SYNCH pin watchdog timeout can be enabled by A0/WDEN or/and A1/SWDEN pins. Any watchdog event is signaled in ComErr bit (available if CRCEN is high) while $\overline{FAULT}$ pin will not be impacted by ComErr detection.

SupplyErrM

Set SupplyErrM = 1 to disable any supply errors and warnings being signaling on the $\overline{FAULT}$ output. Independent of the SupplyErrM bit, these conditions will still be shown in the SupplyErr bit in the Interrupt register and the GlobIF bit and in the SDO signal.

If DAISY pin is high, supply errors are not signaled on $\overline{FAULT}$ output and information is available only on VERR bit in SDO signal when CRC byte is enabled.

VddOKM

Set VddOKM = 1 to disable signaling of VddNotGood and VddWarn bits in SupplyErr bit (and hence also the FAULT output, if enabled through SuplyErrM). The SupplyErr bit is always active and not affected by the VddOKM bit setting.

If DAISY pin is high supply VddNotGood and VddWarn bits do not affect VERR bit in SDO signal.

ShtVddM

Set ShtVddM = 1 to disable per channel short-to-VDD faults being signaling on the $\overline{FAULT}$ output. If the Short-to-VDD detection is enabled in the ShtVddEn register, short-to-VDD conditions are still signaled in the ShtVddFault bit and the SPI SDO data, when they occur.

If DAISY pin is high short-to-VDD fault detection is disabled.

OWOnM

Set OWOnM = 1 to disable per channel open-wire-on faults being signaled on the $\overline{FAULT}$ output. If open-wire-on detection is enabled in the OwOnEn register, open-wire-on conditions will still be signaled in the OWOnFault bit and the SPI SDO data, when they occur.

If DAISY pin is high open-wire-on faults detection is disabled.

OWOffM

Set OWOffM = 1 to disable per channel open-wire-off faults being signaled on the $\overline{FAULT}$ output. If open-wire-off detection is enabled in the OwOffEn register, open-wire-off conditions will still be signaled in the OWOffFault bit and the SPI SDO data when they occur.

If DAISY pin is high open-wire-off faults detection is disabled.

CurrLimM

Set CurrLimM = 1 to disable per channel over-current conditions being signaled on the $\overline{FAULT}$ output. Independent of the CurrLimM bit setting, overcurrent conditions will always be signaled in the CurrLim bit and the SPI SDO data when they occur.

If DAISY pin is high overcurrent condition is not signaled.

OverLdM

Set OverLdM = 1 to disable per-channel overload faults being signaled on the $\overline{FAULT}$ output. Independent of the OverLd bit setting, overload faults will always be signaled in the OverLdFault bit and the OvldF bit in the SPI SDO data when they occur.

Applications Information

Inductive Load Turn-off Energy Clamping

During turn-off of inductive loads, the free-wheel energy is clamped by the internal V_{CL} clamps. This energy must be limited to 150mJ (max) at T_J = +125°C and $I_{OUT\_}$ = -600mA per channel, all channels switching simultaneously.

Surge Protection

The MAX14915 has internal protection against ±1kV 42Ω/0.5µF 1.2µs/50µs surges on the OUT_ pins to GND, if the VDD pins are protected with one TVS. Ensure that the peak voltage of the VDD TVS is below 65V.

RF Conducted Immunity

To ensure that the OUT_ pins do not produce wrong logic conditions while being off, during IEC61000-4-6 RF immunity testing, connect 10nF capacitors at each OUT_ to GND.

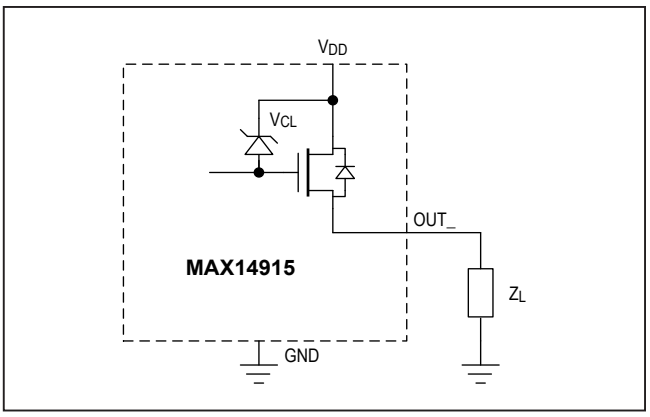


Figure 22. Inductive Load Clamping Scheme

Reverse Currents into OUT_

If currents flow into the OUT_ pins, the device heats up due to internal currents that flow through the device from V_{DD} to GND. The internal currents are proportional to the reverse current into OUT_. The allowed reverse OUT_ current depends on V_{DD}, the ambient temperature and the thermal resistance. At 25°C ambient temperature the reverse current into one OUT should be limited to 1A at V_{DD} = 36V and 1.5A at V_{DD} = 24V. Driving higher currents into OUT_ can destroy the device thermally.

Typical Application Circuit

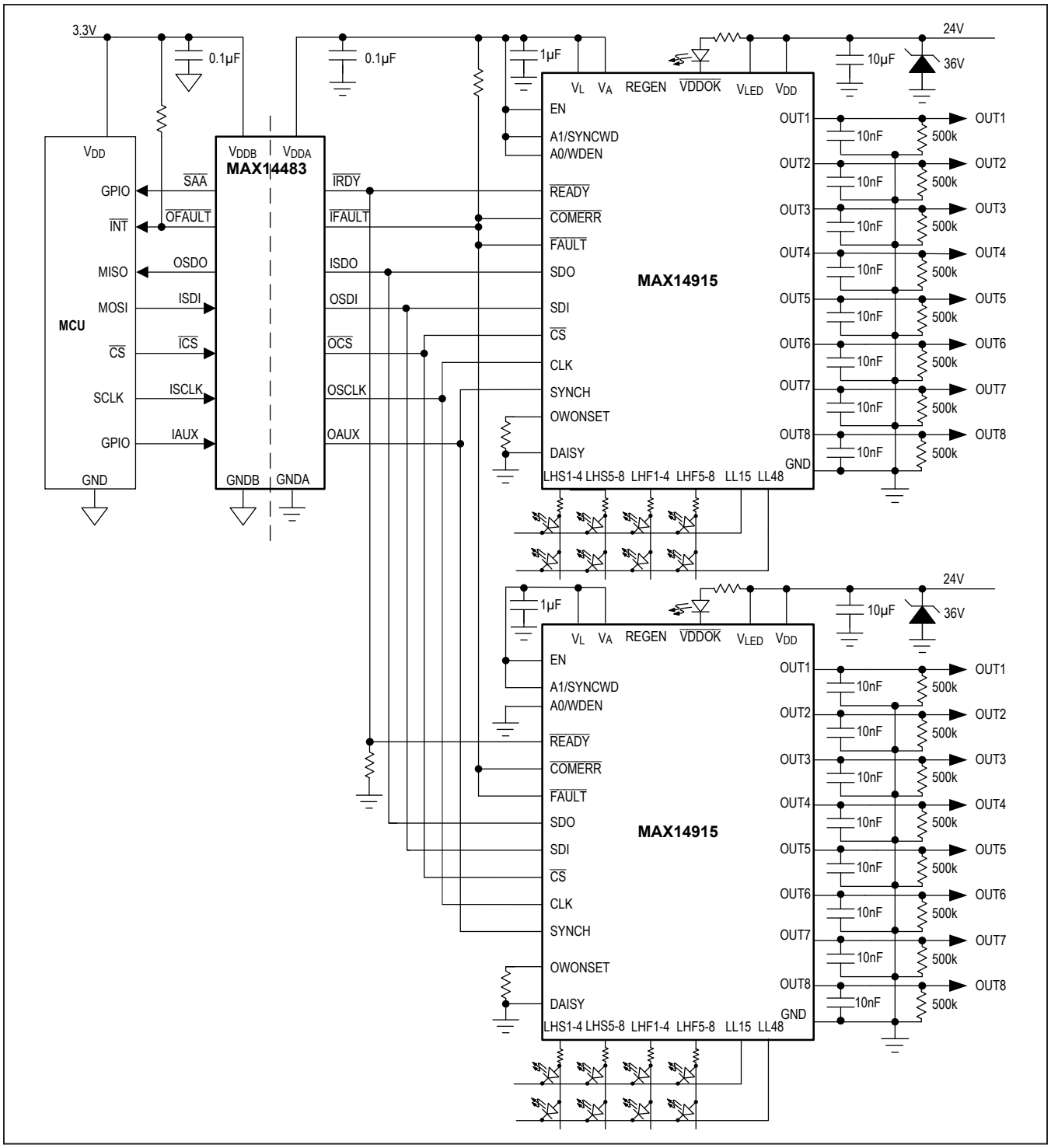


Figure 23. 16-Channel Isolated DO Application Using 6-Channel Digital Isolator

Ordering Information

PART	TEMP RANGE	PACKAGE	TOP MARKING	LEAD PITCH
MAX14915AFM+T	-40°C to +125°C	6x6 QFN48	MAX14915AFM	0.4mm
MAX14915AFM+	-40°C to +125°C	6x6 QFN48	MAX14915AFM	0.4mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/18	Initial release	—
1	9/18	Updated the *Simplified Diagram*, *Package Information* table, *Electrical Characteristics* table, *Pin Configuration*, Figure 7 caption, and *Interrupt Register (0x03)* ; Added new Figures 1–2 and renumbered remaining figures; Replaced Figure 14 and 18.	2–3, 7, 9, 16, 23, 27, 36
2	10/18	Updated TOC01–TOC02, and corrected subscripts, formatting, and grammar	1–2, 4–20, 24 29, 31, 36–37

