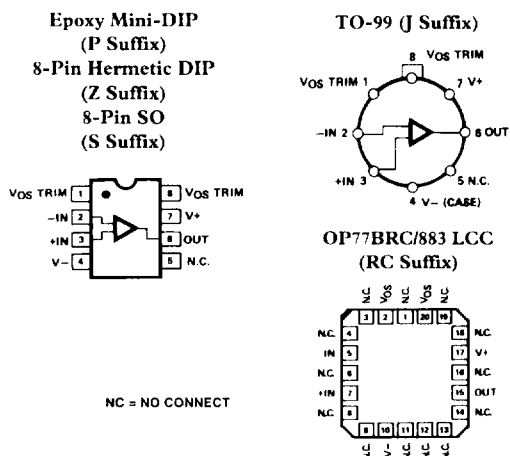


FEATURES

Outstanding Gain Linearity
Ultrahigh Gain: 5000 V/mV min
Low V_{OS} Over Temperature: 60 μ V max
Excellent TCV_{OS} : 0.3 μ V/ $^{\circ}$ C max
High PSRR: 3 μ V/V max
Low Power Consumption: 60 mW max
Fits OP07, 725, 108A/308A, 741 Sockets
Available in Die Form

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The OP77 significantly advances the state-of-the-art in precision op amps. The OP77's outstanding gain of 10,000,000 or more is maintained over the full ± 10 V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications. Low initial V_{OS} drift and rapid stabilization time, combined with only 50 mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3 μ V/ $^{\circ}$ C maximum and the low V_{OS} of 25 μ V maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3 μ V/V (110 dB) and CMRR of 1.0 μ V/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP77 ideally suited for high-resolution instrumentation and other tight error budget systems.

This product is available in six standard grades and five standard packages: the TO-99 can, the 8-pin mini-DIP in ceramic, SO or epoxy, and the 20-contact LCC.

The OP77 is a direct or upgrade replacement for the OP07, 05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot. For higher precision performance refer to OP177.

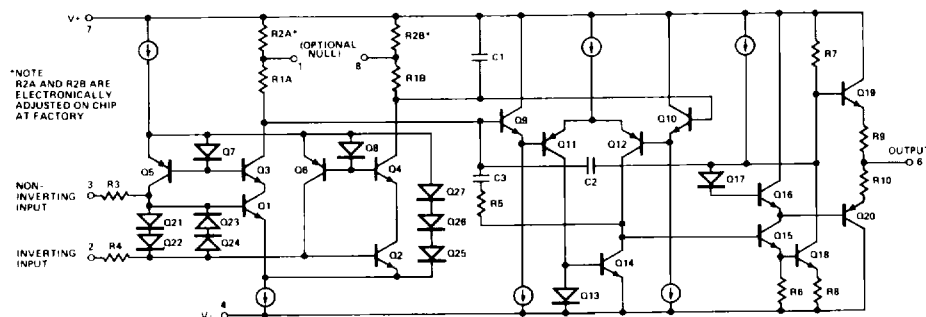


Figure 1. Simplified Schematic

OP77—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15$ V, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	OP77A Typ	Max	Min	OP77B Typ	Max	Units
Input Offset Voltage	V_{OS}			10	25		20	60	μV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)		0.2			0.2		$\mu\text{V}/\text{Mo}$
Input Offset Current	I_{OS}			0.3	1.5		0.3	2.8	nA
Input Bias Current	I_B		0.2	1.2	2.0	0.2	1.2	2.8	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz^2 $f_n = 10 \text{ Hz}^2$		0.35	0.6		0.35	0.6	$\mu\text{V p-p}$
		$f_n = 100 \text{ Hz}^2$		10.3	18.0		10.3	18.0	$\mu\text{V p-p}$
Input Noise Voltage Density	e_n	$f_n = 1000 \text{ Hz}^2$		10.0	13.0		10.0	13.0	$\text{V}/\sqrt{\text{Hz}}$
		$f_n = 1000 \text{ Hz}^2$		9.6	11.0		9.6	11.0	$\text{V}/\sqrt{\text{Hz}}$
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz^2 $f_n = 10 \text{ Hz}^2$		14	30		14	30	pA p-p
		$f_n = 100 \text{ Hz}^2$		0.32	0.80		0.32	0.80	pA p-p
Input Noise Current Density	i_n	$f_n = 100 \text{ Hz}^2$		0.14	0.23		0.14	0.23	$\text{pA}/\sqrt{\text{Hz}}$
		$f_n = 1000 \text{ Hz}^2$		0.12	0.17		0.12	0.17	$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance—Differential-Mode	R_{IN}	(Note 3)	20	15		18.5	45		M Ω
Input Resistance—Common-Mode	R_{INCM}			200			200		G Ω
Input Voltage Range	IVR		± 13	± 14		± 13	± 14		V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13$ V		0.1	1.0		0.1	1.0	$\mu\text{V}/\text{V}$
Power Supply Rejection Ratio	PSRR	$V_S = +3$ V to -18 V		0.7	3		0.7	3	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VOL}	$R_L \geq 2 \text{ k}\Omega$, $V_O = \pm 10$ V	5000	12000		2000	8000		V/mV
Output Voltage Swing	V_{O1}	$R_L \geq 10 \text{ k}\Omega$ $R_L \geq 2 \text{ k}\Omega$	± 13.5 ± 12.5	± 14.0 ± 13.0		± 13.5 ± 12.5	± 14.0 ± 13.0		V
		$R_L \geq 1 \text{ k}\Omega$	± 12.0	± 12.5		± 12.0	± 12.5		V
Slew Rate	SR	$R_L \geq 2 \text{ k}\Omega^2$	0.1	0.3		0.1	0.3		V/ μs
Closed-Loop Bandwidth	BW	$A_{VOL} = +1^2$	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O			60			60		Ω
Power Consumption	P_T	$V_S = \pm 15$ V, No Load		50	60		50	60	mW
Offset Adjustment Range		$V_S = +3$ V, No Load $R_P = 20 \text{ k}\Omega$		3.5	4.5		3.5	4.5	mV

NOTES

¹Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV .

²Sample tested.

³Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	± 22 V
Differential Input Voltage	± 30 V
Input Voltage ²	± 22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, Z, and RC Packages	-65°C to $+150^\circ\text{C}$
P Package	-65°C to $+125^\circ\text{C}$
Operating Temperature Range	
OP77A, OP77B (J, Z, RC)	-55°C to $+125^\circ\text{C}$
OP77E, OP77F (J, Z)	-25°C to $+85^\circ\text{C}$
OP77E, OP77F, OP77G (P, S)	0°C to $+70^\circ\text{C}$
OP77H (P, S)	-40°C to $+85^\circ\text{C}$
Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

Package Type	θ_{JA}^1	θ_{JC}	Units
TO-99 (J)	150	18	$^\circ\text{C}/\text{W}$
8-Pin Hermetic DIP (Z)	148	16	$^\circ\text{C}/\text{W}$
8-Pin Plastic DIP (P)	103	43	$^\circ\text{C}/\text{W}$
20-Contact LCC (RC, TC)	98	38	$^\circ\text{C}/\text{W}$
8-Pin SO (S)	158	43	$^\circ\text{C}/\text{W}$

NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

²For supply voltages less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

³ θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, Cerdip, P, DIP, and LCC packages; θ_{JC} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE¹

Model	Temperature Range	Package Option ²
OP77AJ ³	-55°C to $+125^\circ\text{C}$	TO-99
OP77AZ ³	-55°C to $+125^\circ\text{C}$	8-Pin Cerdip
OP77EJ	-25°C to $+85^\circ\text{C}$	TO-99
OP77EZ	-25°C to $+85^\circ\text{C}$	8-Pin Cerdip
OP77EP	0°C to $+70^\circ\text{C}$	8-Pin Plastic DIP
OP77BJ	-55°C to $+125^\circ\text{C}$	TO-99
OP77BRC/883C	-55°C to $+125^\circ\text{C}$	20-Contact LCC
OP77FJ	-25°C to $+85^\circ\text{C}$	TO-99
OP77FZ	-25°C to $+85^\circ\text{C}$	8-Pin Cerdip
OP77FP	0°C to $+70^\circ\text{C}$	8-Pin Plastic DIP
OP77GP	0°C to $+70^\circ\text{C}$	8-Pin Plastic DIP
OP77GS ⁴	0°C to $+70^\circ\text{C}$	8-Pin SO
OP77GS-REEL	0°C to $+70^\circ\text{C}$	8-Pin SO
OP77GS-REEL7 ⁴	0°C to $+70^\circ\text{C}$	8-Pin SO
OP77HS ⁴	-40°C to $+85^\circ\text{C}$	8-Pin SO
OP77HS-REEL	-40°C to $+85^\circ\text{C}$	8-Pin SO
OP77HS-REEL7 ⁴	-40°C to $+85^\circ\text{C}$	8-Pin SO

NOTES

¹Burn-in is available on commercial and industrial temperature range parts in Cerdip, Plastic DIP, and TO-can packages.

²For outline information see Package Information section.

³For devices processed in total compliance to MIL-STD 883, add 883 after part number. Consult factory for 883 data sheet.

⁴For availability and burn-in information on SO and PLCC packages, contact your local sales office.