SNx4ACT244 Octal Buffers and Drivers With 3-State Outputs

1 Features

- 4.5-V to 5.5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Maximum t_{pd} of 9.5 ns at 5 V
- Inputs are TTL compatible
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- LED displays
- Servers and telecommunication
- Switching networks

3 Description

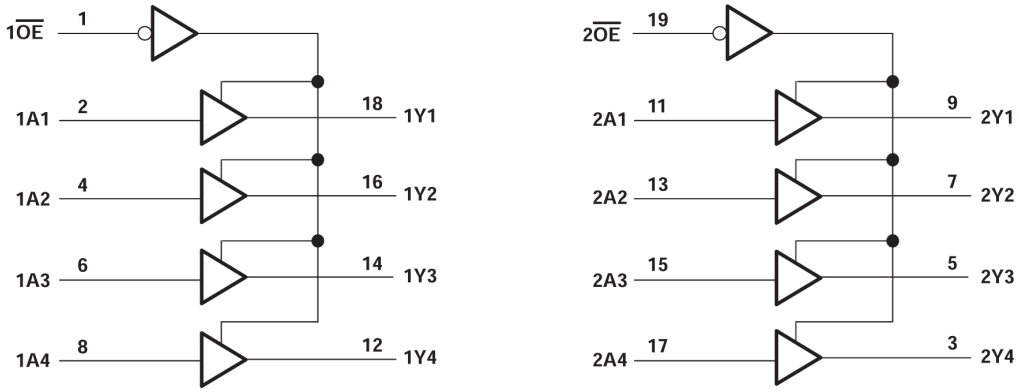
These SNx4ACT244 octal buffers and drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SNx4ACT244 devices are organized as two 4-bit buffers and drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes non-inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)(2)	PACKAGE SIZE(3)
SN74ACT244	DB (SSOP, 20)	7.2 mm × 5.3 mm	7.2 mm × 7.8 mm
	DW (SOIC, 20)	12.8 mm × 7.5 mm	12.8 mm × 10.3 mm
	N (PDIP, 20)	24.33 mm × 6.35 mm	24.33 mm × 9.4 mm
	NS (SO, 20)	12.6 mm × 5.3 mm	12.6 mm × 7.8 mm
	PW (TSSOP, 20)	6.5 mm × 4.4 mm	6.5 mm × 6.4 mm
	RKS (VQFN, 20)	4.5 mm × 2.5 mm	4.5 mm × 2.5 mm
SN54ACT244	J (CDIP, 20)	24.2 mm × 6.92 mm	24.2 mm × 6.92 mm
	W (CFP, 20)	13.09 mm × 6.92 mm	13.09 mm × 6.92 mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The body size (length × width) is a nominal value and does not include pins.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2016) to Revision E (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Device Information* table to include body and package lead size	1
• Add RKS Package information	1

Changes from Revision C (October 2002) to Revision D (January 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

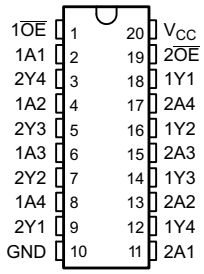


Figure 5-1. SN54ACT244: J or W Packages, 20-Pin CDIP or CFP (Top View)

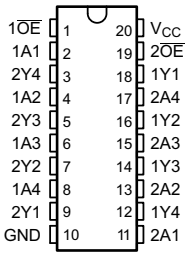


Figure 5-2. SN74ACT244: DB, DW, N, NS, or PW Packages, 20-Pin SSOP, SOIC, PDIP, SO, or TSSOP (Top View)

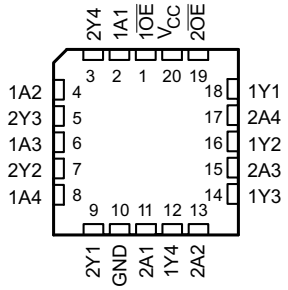


Figure 5-3. SN54ACT244: FK Package 20-Pin LCCC (Top View)

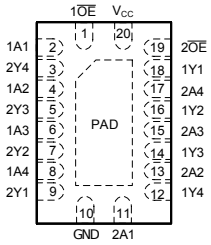


Figure 5-4. SN74ACT244: RKS Packages, 20-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	1 Active low Output enable
2	1A1	I	1A1 input
3	2Y4	O	2Y4 output
4	1A2	I	1A2 input
5	2Y3	O	2Y3 Output
6	1A3	I	1A3 input
7	2Y2	O	2Y2 Output
8	1A4	I	1A4 input
9	2Y1	O	2Y1 Output
10	GND	—	Ground
11	2A1	I	2A1 input
12	1Y4	O	1Y4 output
13	2A2	I	2A2 input
14	1Y3	O	1Y3 Output
15	2A3	I	2A3 input
16	1Y2	O	1Y2 Output
17	2A4	I	2A4 input
18	1Y1	O	1Y1 Output
19	2 $\overline{OE}$	I	2 Active low Output enable
20	V_{CC}	—	Power

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_J	Absolute Maximum Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
SN74ACT244 in DW Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	
SN54ACT244 in J, W, DB, N, NS, PW, FK Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
Δt/Δv	Input transition rise or fall rate			8	ns/V
T_A	Operating free-air temperature	SN54ACT244	–55	125	°C
		SN74ACT244	–40	85	

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC[1]		SN74ACT244						UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.1	81.4	48.1	76.4	103	67.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.6	46.8	34.1	42.6	37.7	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.3	49.3	29	43.9	54	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.8	20	19.5	18.8	2.8	10.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	48.8	28.9	43.5	53.5	40.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	24.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	T_A = 25°C	4.5 V	4.4	4.49		V
		SN54ACT244		4.4			
		SN74ACT244		4.4			
		T_A = 25°C	5.5 V	5.4	5.49		
		SN54ACT244		5.4			
		SN74ACT244		5.4			
	I_{OH} = –24 mA	T_A = 25°C	4.5 V	3.86			
		SN54ACT244		3.7			
		SN74ACT244		3.76			
		T_A = 25°C	5.5 V	4.86			
		SN54ACT244		4.7			
		SN74ACT244		4.76			
	I_{OH} = –50 mA[1]	SN54ACT244	5.5 V	3.85			
	I_{OH} = –75 mA[1]	SN74ACT244	5.5 V	3.85			

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	I_{OL} = 50 µA	T_A = 25°C	4.5 V		0.001	0.1	V
		SN54ACT244				0.1	
		SN74ACT244				0.1	
		T_A = 25°C	5.5 V		0.001	0.1	
		SN54ACT244				0.1	
		SN74ACT244				0.1	
	I_{OL} = 24 mA	T_A = 25°C	4.5 V			0.36	
		SN54ACT244				0.5	
		SN74ACT244				0.44	
		T_A = 25°C	5.5 V			0.36	
		SN54ACT244				0.5	
		SN74ACT244				0.44	
	I_{OL} = 50 mA(1)	SN54ACT244	5.5 V			1.65	
	I_{OL} = 75 mA(1)	SN74ACT244	5.5 V			1.65	
I_{OZ}	V_O = V_{CC} or GND	T_A = 25°C	5.5 V			±0.25	µA
		SN54ACT244				±5	
		SN74ACT244				±2.5	
I_I	V_I = V_{CC} or GND	T_A = 25°C	5.5 V			±0.1	µA
		SN54ACT244				±1	
		SN74ACT244				±1	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	T_A = 25°C	5.5 V			4	µA
		SN54ACT244				80	
		SN74ACT244				40	
ΔI_{CC} (2)	One input at 3.4 V, Other inputs at GND or V_{CC}	T_A = 25°C	5.5 V		0.6		mA
		SN54ACT244				1.6	
		SN74ACT244				1.5	
C_I	V_I = V_{CC} or GND	T_A = 25°C	5 V		2.5		pF
C_o	V_I = V_{CC} or GND	T_A = 25°C	5 V		8		pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	T_A = 25°C	2	6.5	9	ns
			SN54ACT244	1		10	
			SN74ACT244	1.5		10	
t_{PHL}			T_A = 25°C	2	7	9	
			SN54ACT244	1		10	
			SN74ACT244	1.5		10	

6.6 Switching Characteristics (continued)

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PZH}	$\overline{OE}$	Y	T_A = 25°C	1.5	7	8.5	ns
			SN54ACT244	1		9.5	
			SN74ACT244	1		9.5	
t_{PZL}			T_A = 25°C	2	7	9.5	
			SN54ACT244	1		11	
			SN74ACT244	1.5		10.5	
t_{PHZ}	$\overline{OE}$	Y	T_A = 25°C	2	8	9.5	ns
			SN54ACT244	1		11	
			SN74ACT244	1.5		10.5	
t_{PLZ}			T_A = 25°C	2.5	7.5	10	
			SN54ACT244	1		11.5	
			SN74ACT244	2		10.5	

6.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	C_L = 50 pF,	f = 1 MHz	45	pF

6.8 Typical Characteristics

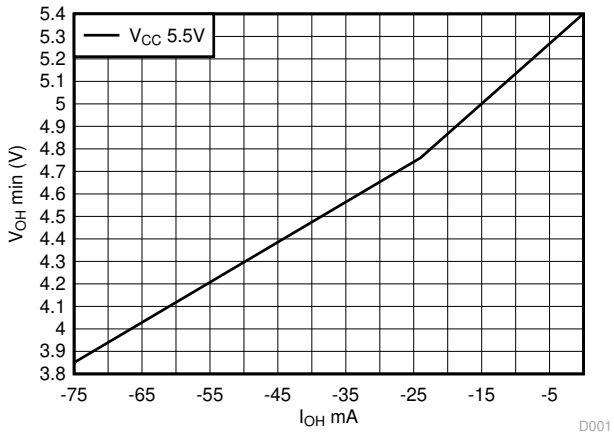
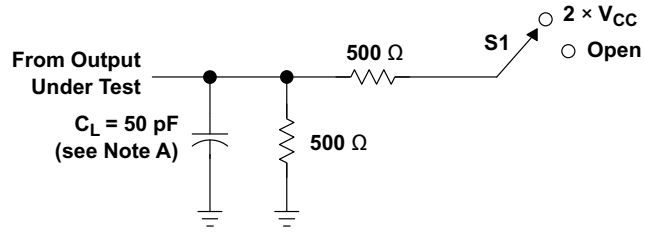


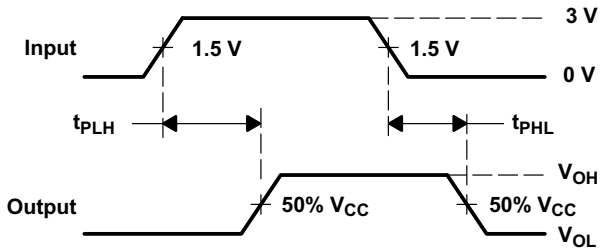
Figure 6-1. V_{OH} Vs I_{OH}

7 Parameter Measurement Information

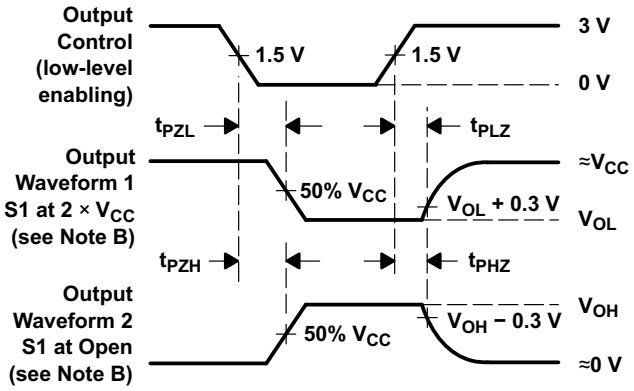


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4ACT244 devices are buffer drivers with separate output enable inputs. The active low output enable sets the output to high impedance when a logic high is applied. For the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

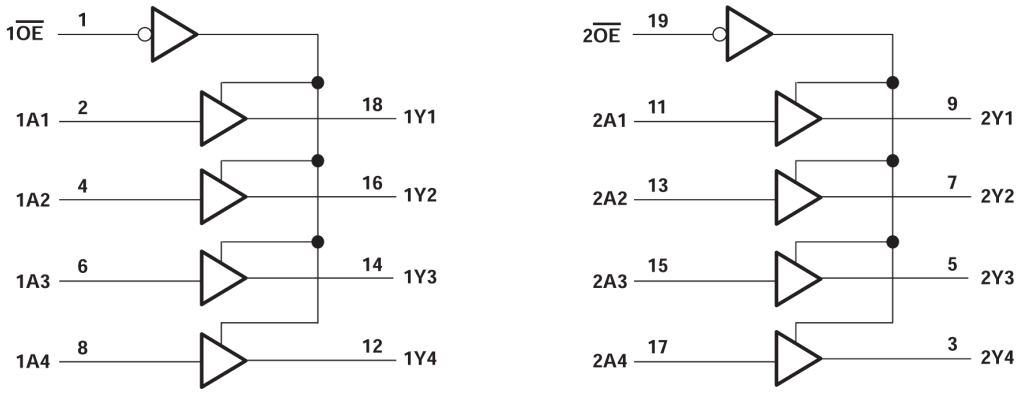


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The SNx4ACT244 devices are recommended for 4.5 V to 5.5-V V_{CC} range under normal operating conditions. The inputs are TTL compatible accepting 2-V minimum high at 5-V V_{CC}.

8.4 Device Functional Modes

Table 8-1 lists the functions of the device.

Table 8-1. Function Table (Each Buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Hi-Z

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx4ACT244 is high-drive buffer drivers providing 24-mA current drive per channel at nominal operating specifications. It can be used as LED driver with appropriate current-limiting resistors to ground or V_{CC} withing the device's and LEDs operating characteristics.

9.2 Typical Application

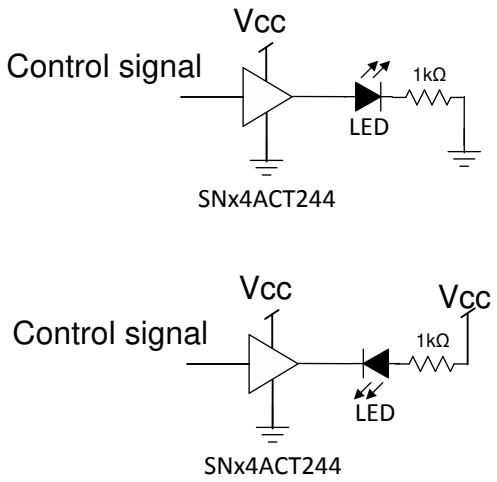


Figure 9-1. Typical LED driving application

9.2.1 Design Requirements

The pullup and pull-down current limiting resistors are chosen to operate within the LED and the SNx4ACT244 device operating specifications. A 1-kΩ resistor, limits the current to less than 5 mA at 5-V V_{CC} operation.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For the specified high and low levels See (V_{IH} and V_{IL}) in the *Section 6.3*.
   - Inputs are not overvoltage tolerant and must be limited to V_{CC}.
2. Recommended output conditions:
   - Limit the output voltage to V_{CC}.
   - Choose the current-limiting resistor for the LED to limit the output current to I_O as per the *Section 6.3*.

9.2.3 Application Curve

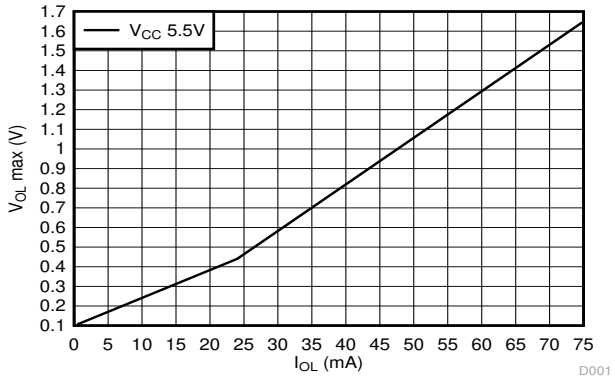


Figure 9-2. V_{OL} vs I_{OL}

9.3 Power Supply Recommendations

The power supply may be any voltage between the MIN and MAX supply voltage rating located in the *Section 6.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

9.4 Layout

9.4.1 Layout Guidelines

Inputs should not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in the Figure 9-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

9.4.2 Layout Example

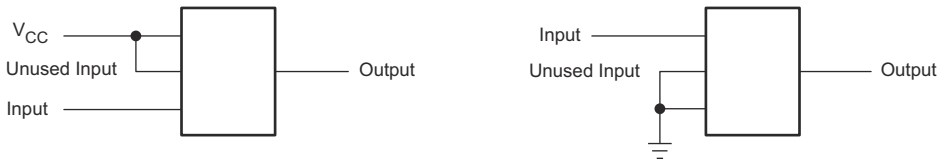


Figure 9-3. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8776001M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001M2A SNJ54ACT 244FK	Samples
5962-8776001MRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001MR A SNJ54ACT244J	Samples
5962-8776001MSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001MS A SNJ54ACT244W	Samples
5962-8776001SRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001SR A SNV54ACT244J	Samples
5962-8776001SSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001SS A SNV54ACT244W	Samples
SN74ACT244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244	Samples
SN74ACT244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244	Samples
SN74ACT244DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244	Samples
SN74ACT244DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244	Samples
SN74ACT244N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT244N	Samples
SN74ACT244NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT244N	Samples
SN74ACT244NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244	Samples
SN74ACT244NSRG4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244	Samples
SN74ACT244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	AD244	Samples
SN74ACT244PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244	Samples
SN74ACT244PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT244RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 125	ACT244	Samples
SNJ54ACT244FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001M2A SNJ54ACT 244FK	Samples
SNJ54ACT244J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001MR A SNJ54ACT244J	Samples
SNJ54ACT244W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8776001MS A SNJ54ACT244W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54ACT244, SN54ACT244-SP, SN74ACT244 :

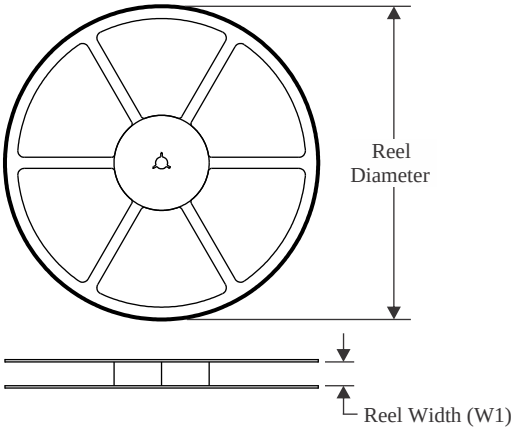
- Catalog : SN74ACT244, SN54ACT244
- Automotive : SN74ACT244-Q1, SN74ACT244-Q1
- Enhanced Product : SN74ACT244-EP, SN74ACT244-EP
- Military : SN54ACT244
- Space : SN54ACT244-SP

NOTE: Qualified Version Definitions:

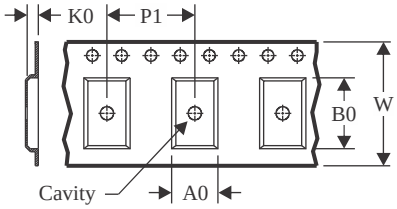
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

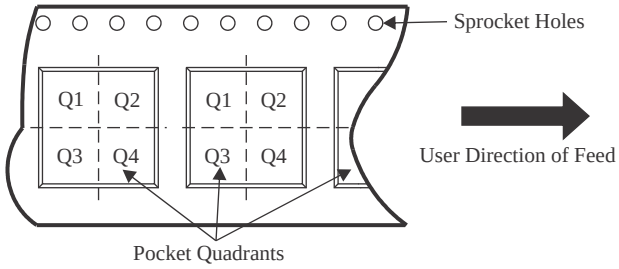


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

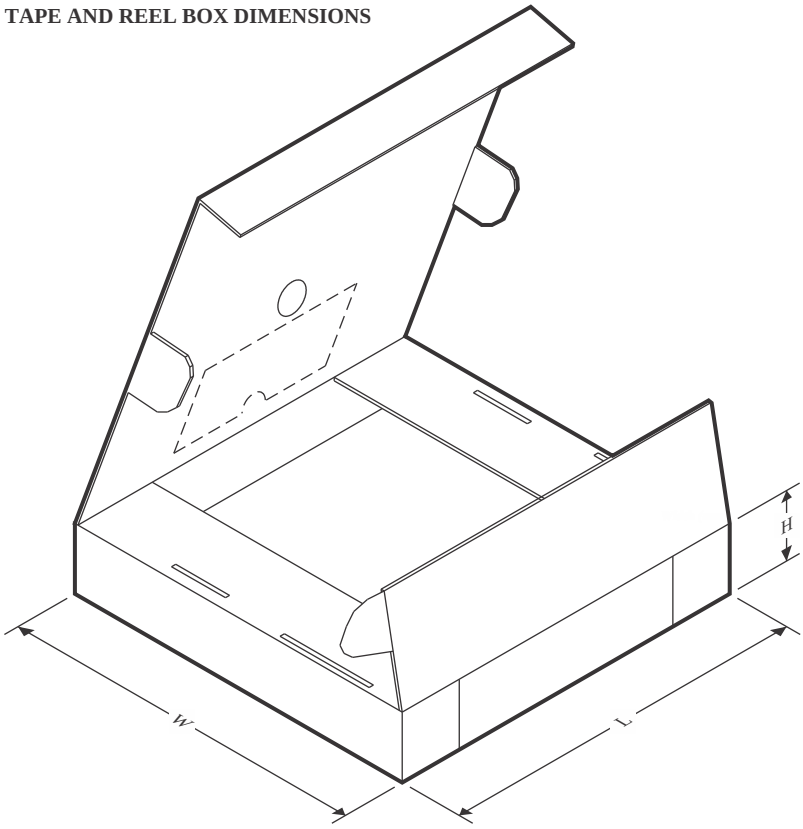
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74ACT244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74ACT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT244RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

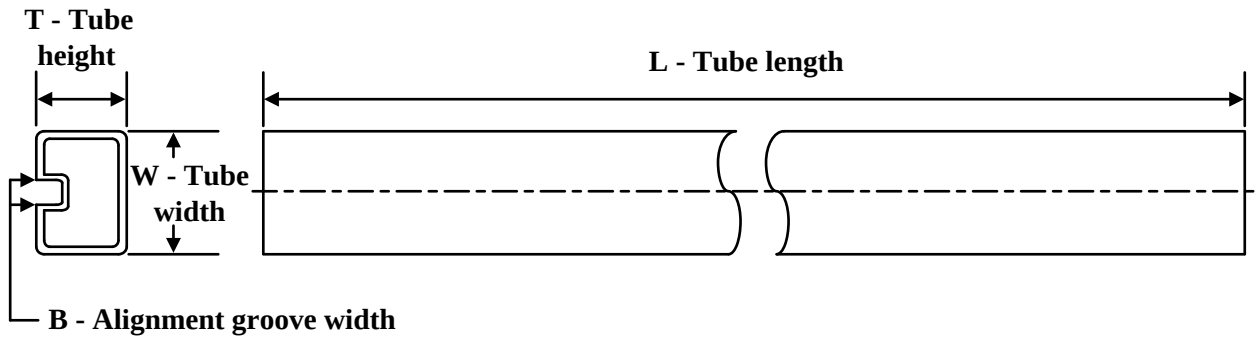
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ACT244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ACT244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ACT244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74ACT244PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74ACT244PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74ACT244RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8776001M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-8776001MSA	W	CFP	20	1	506.98	26.16	6220	NA
5962-8776001SSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74ACT244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ACT244FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54ACT244W	W	CFP	20	1	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

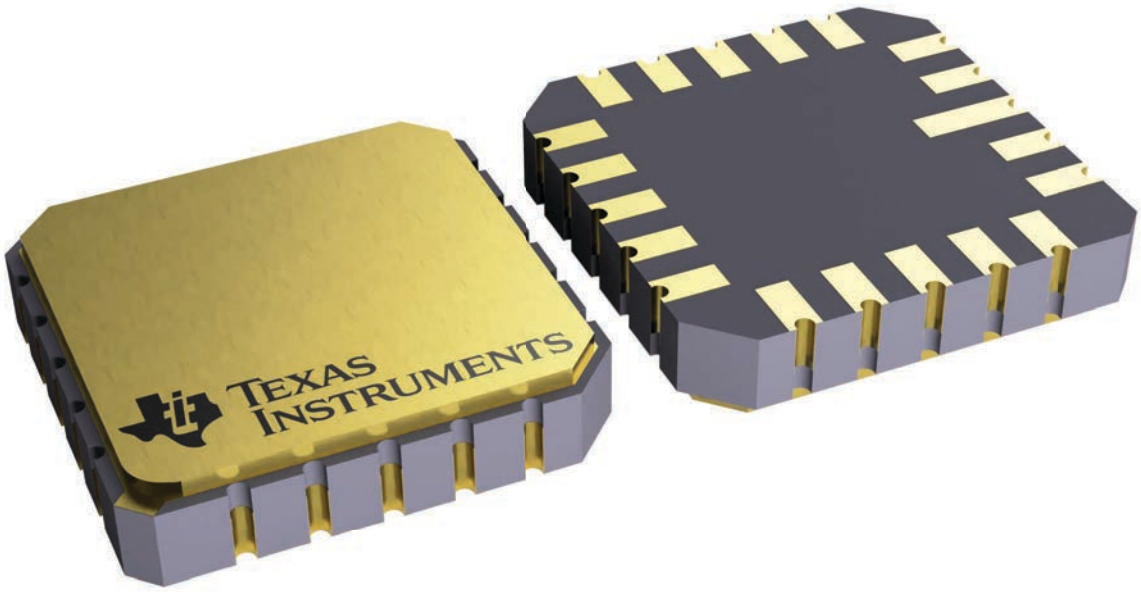
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

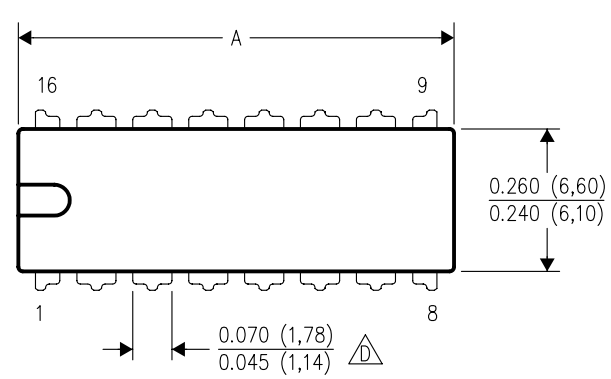


4229370VA\

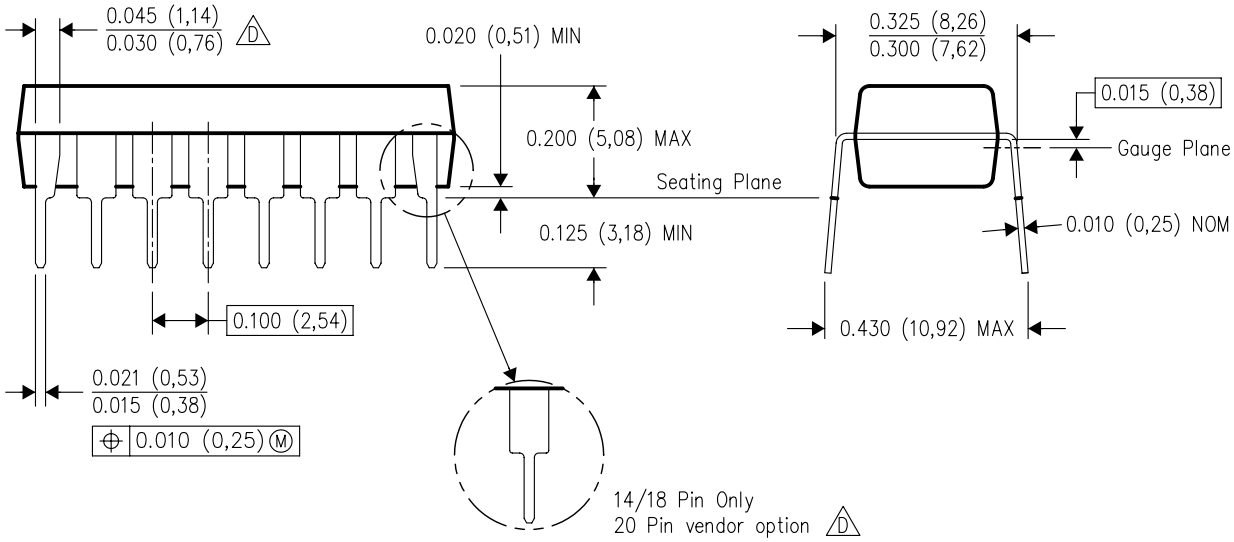
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

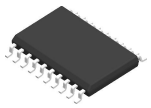


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

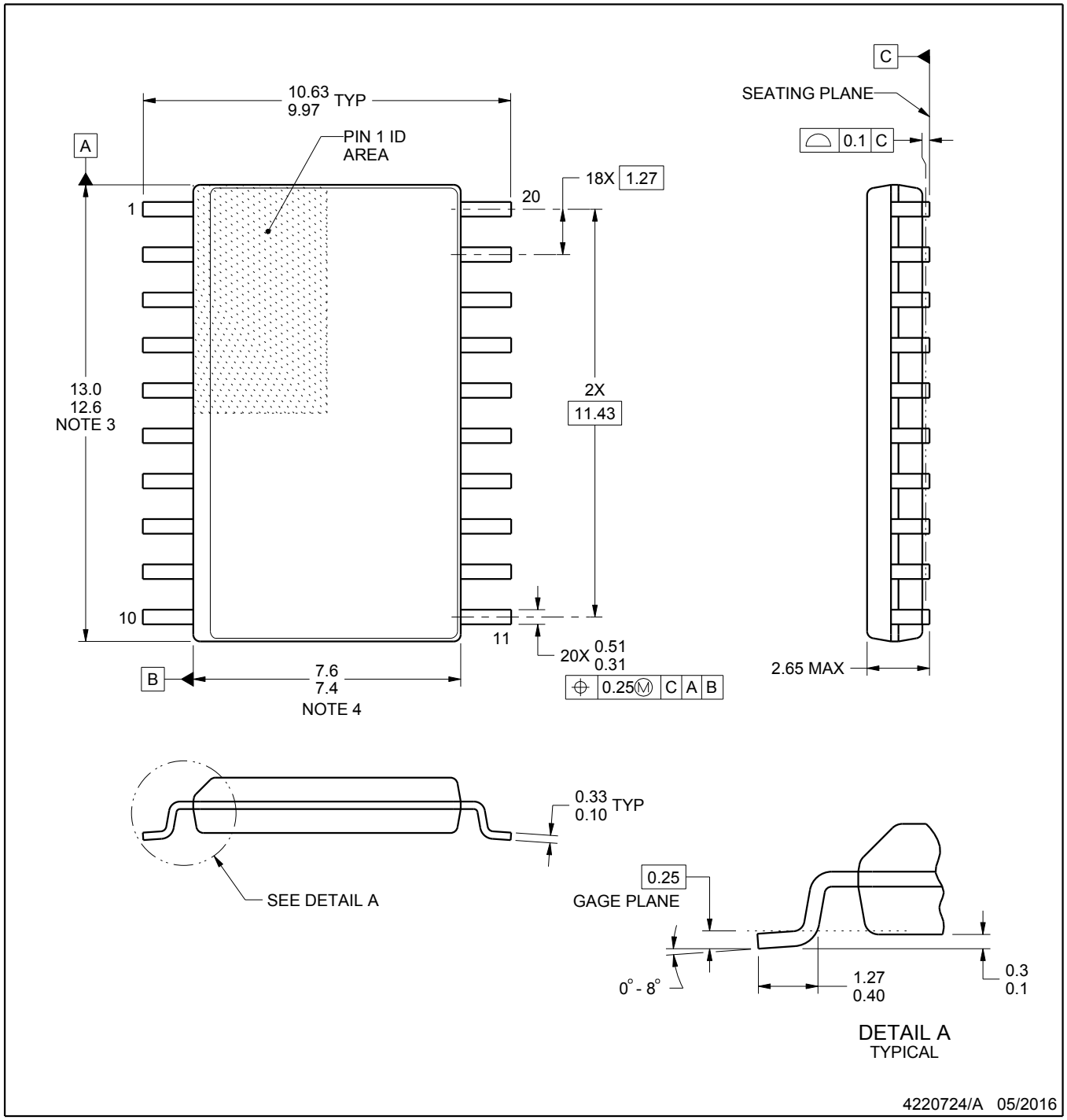


PACKAGE OUTLINE

DW0020A

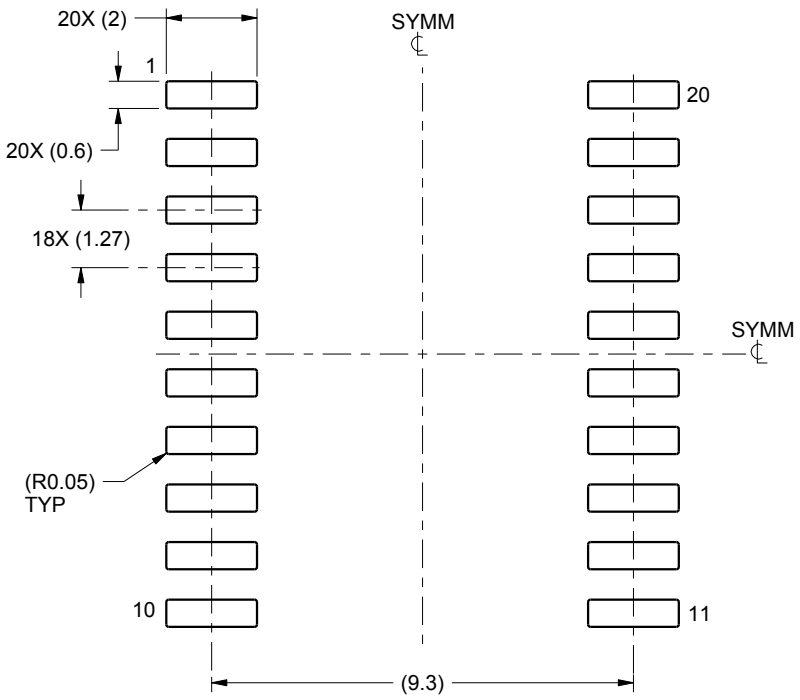
SOIC - 2.65 mm max height

SOIC

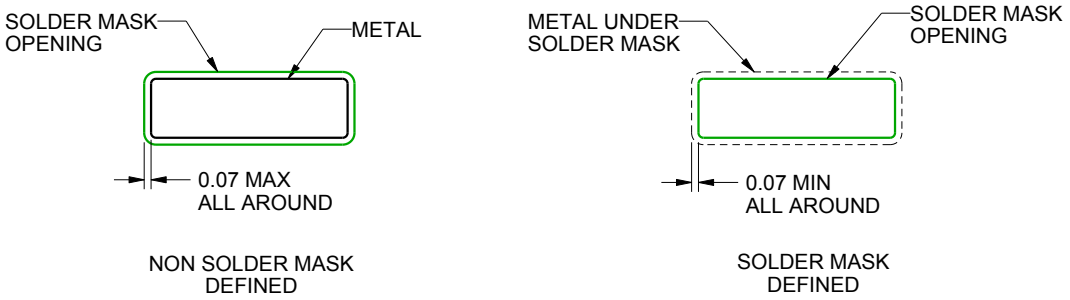


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

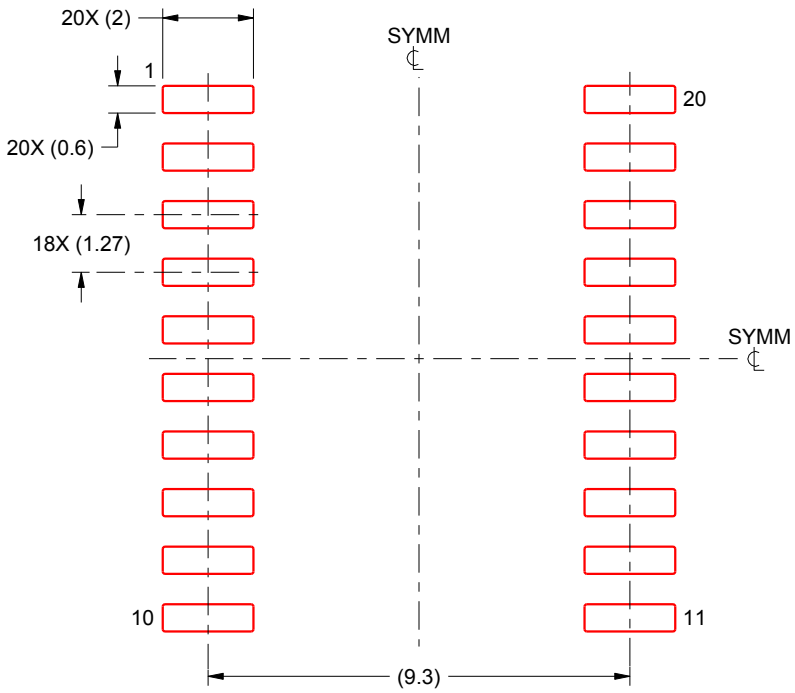


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



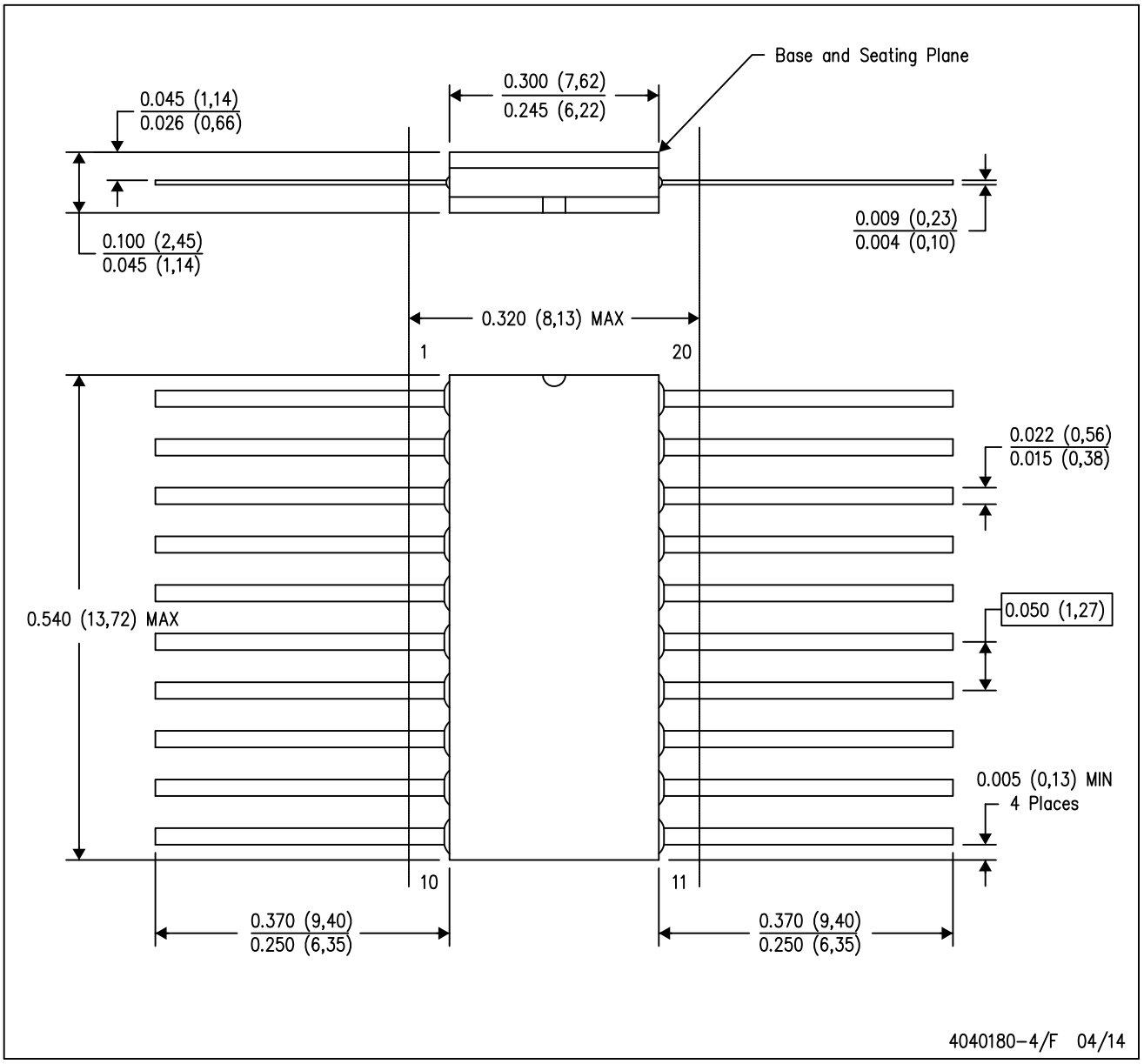
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



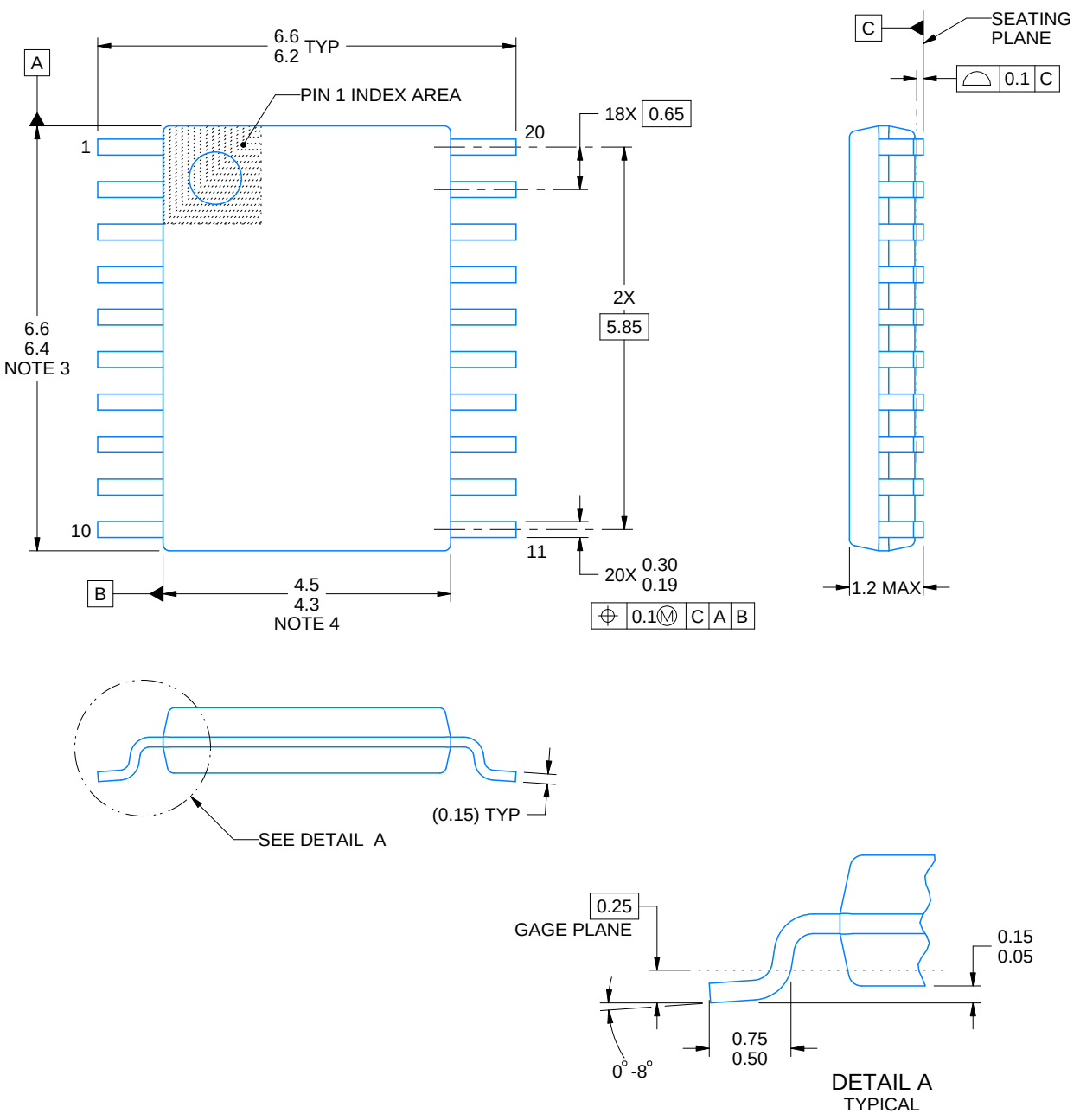
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

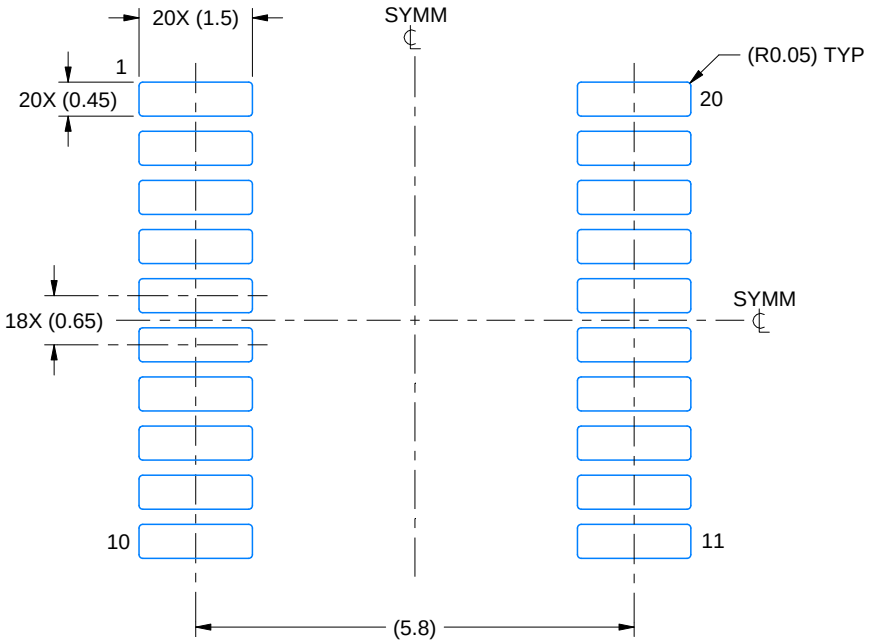
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



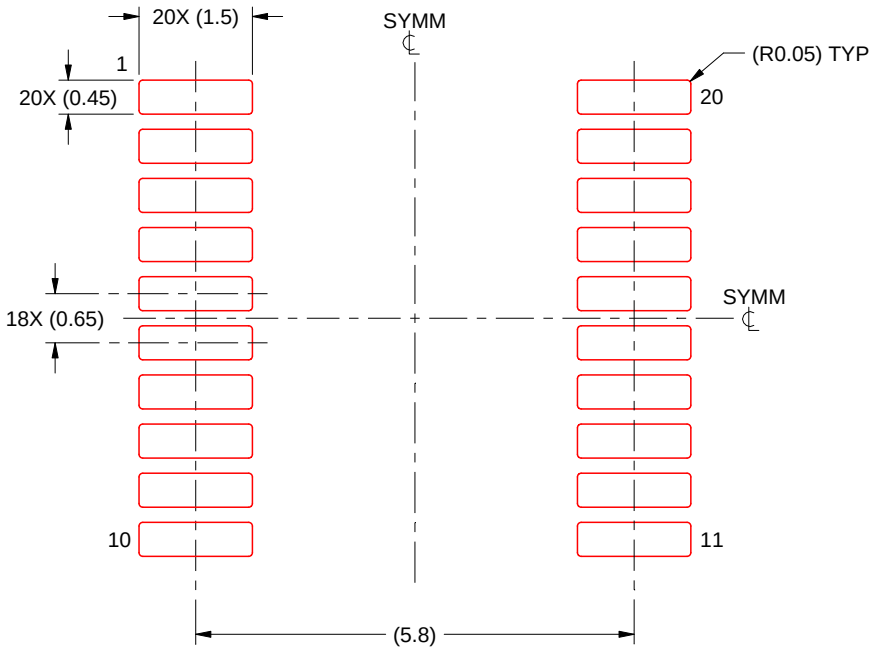
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



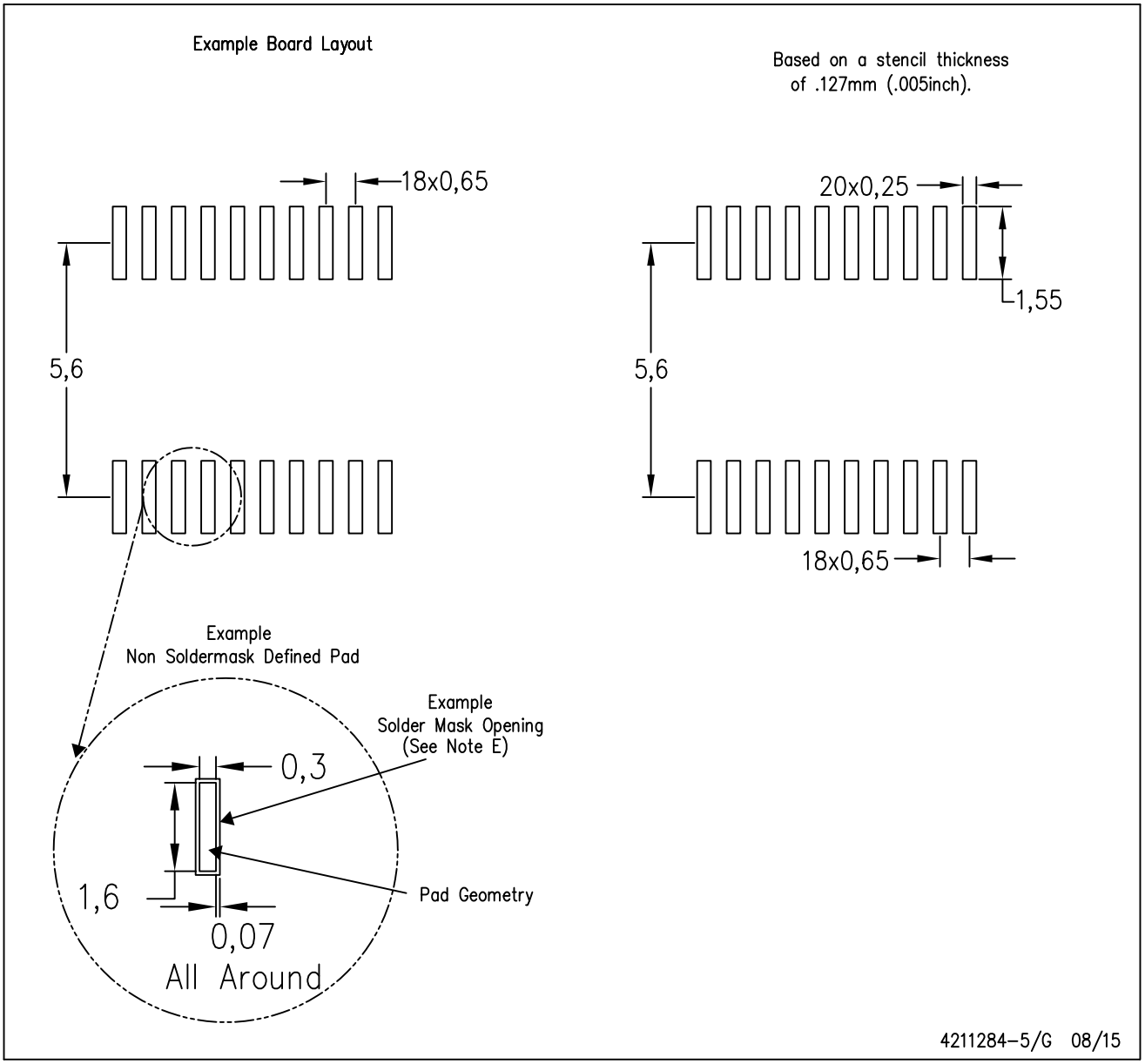
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



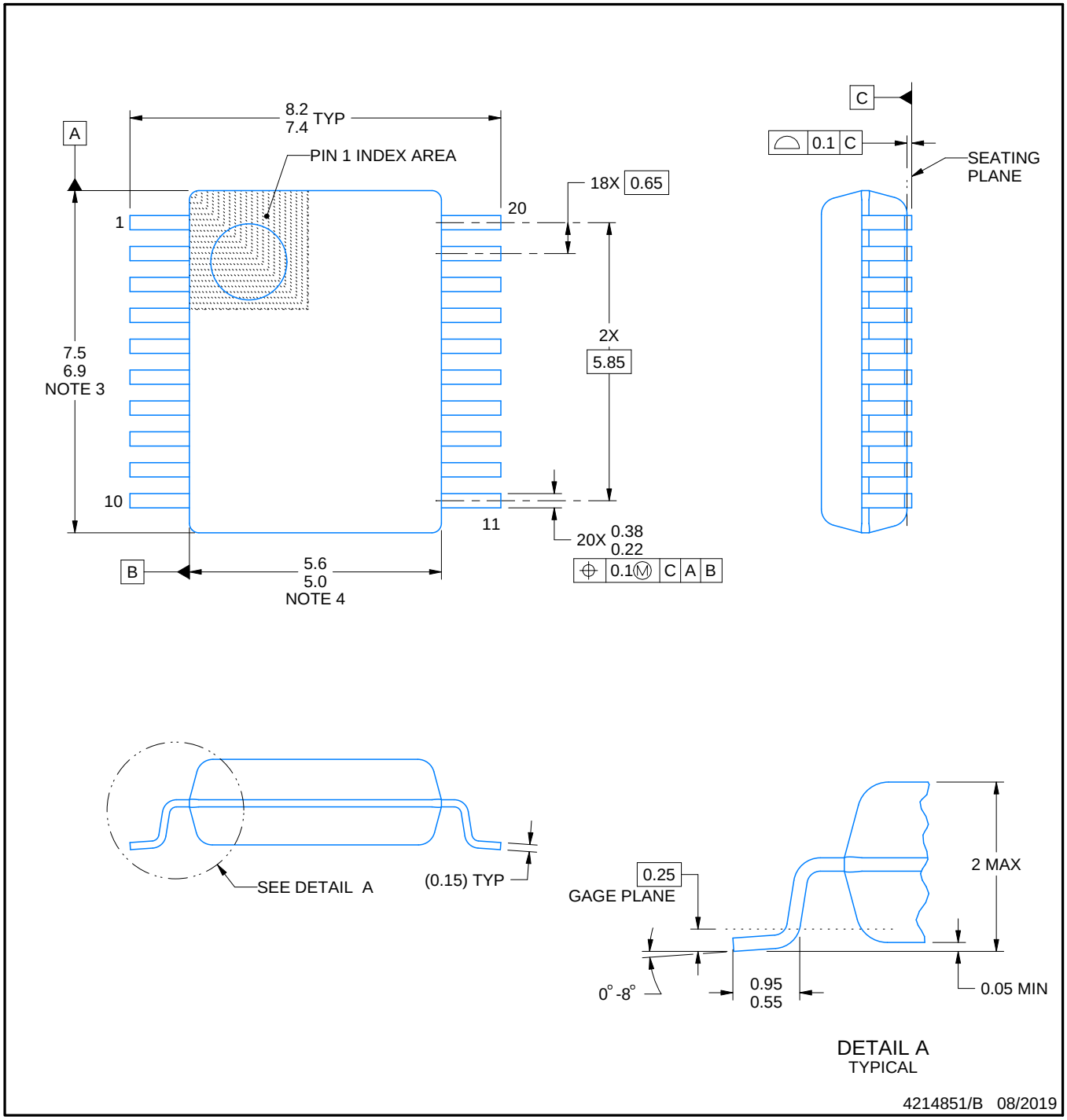
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0020A

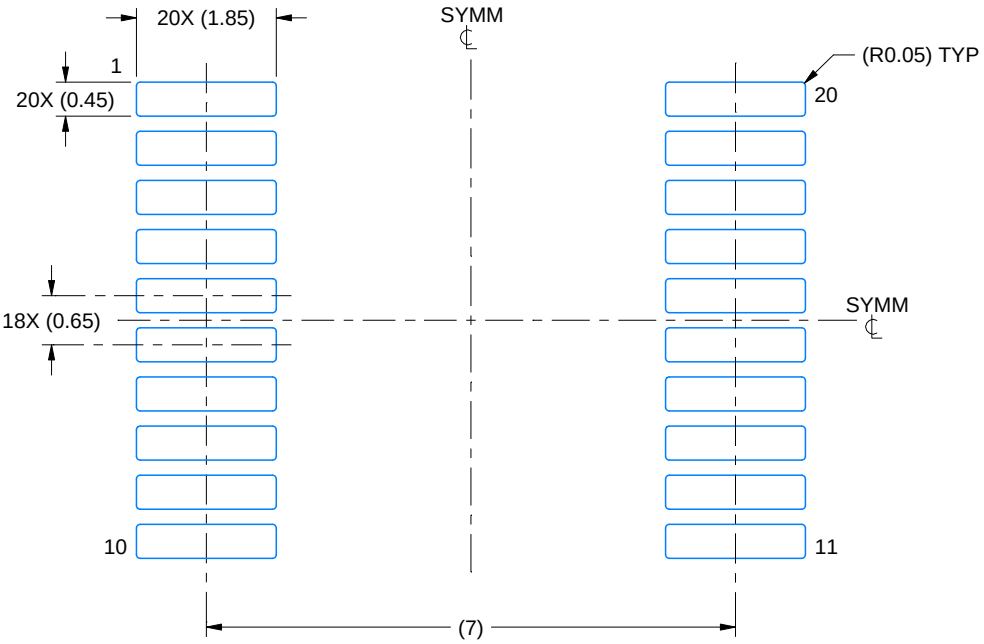
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

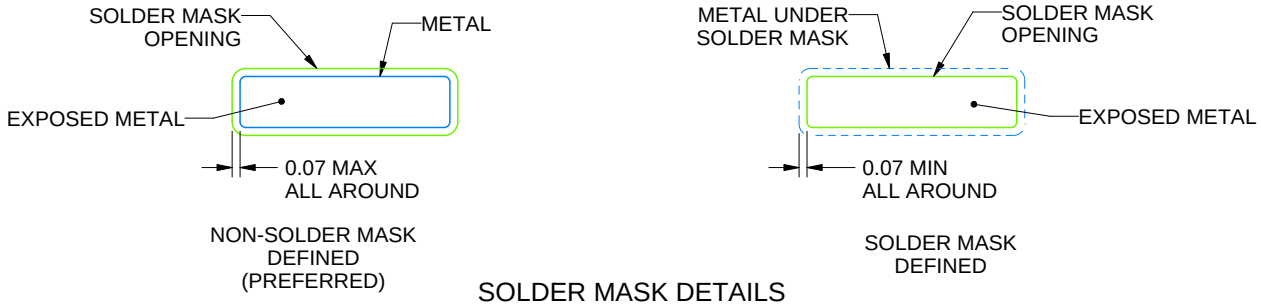


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

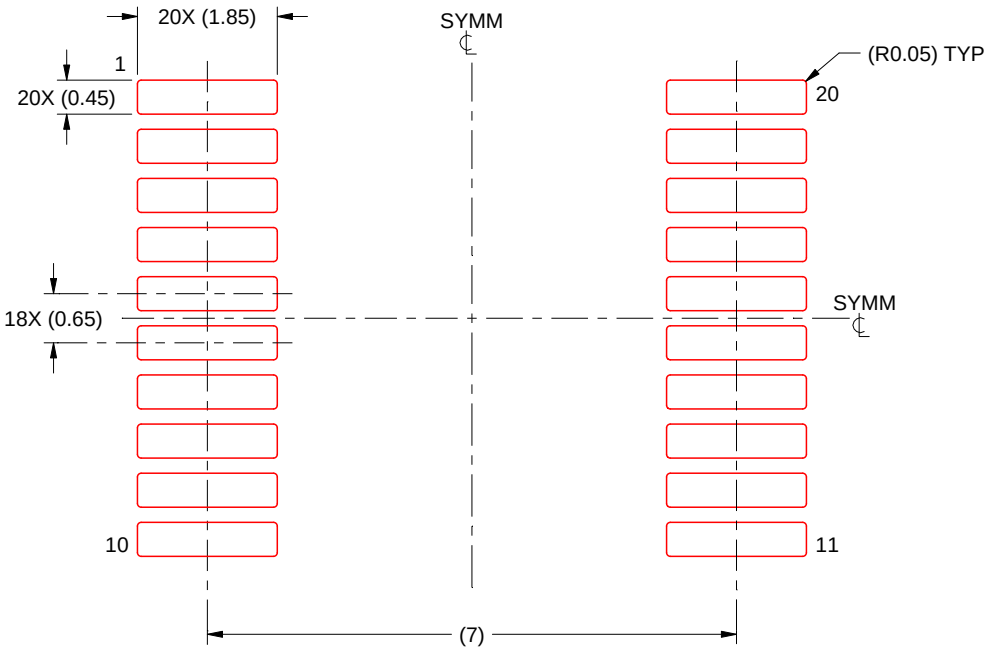
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

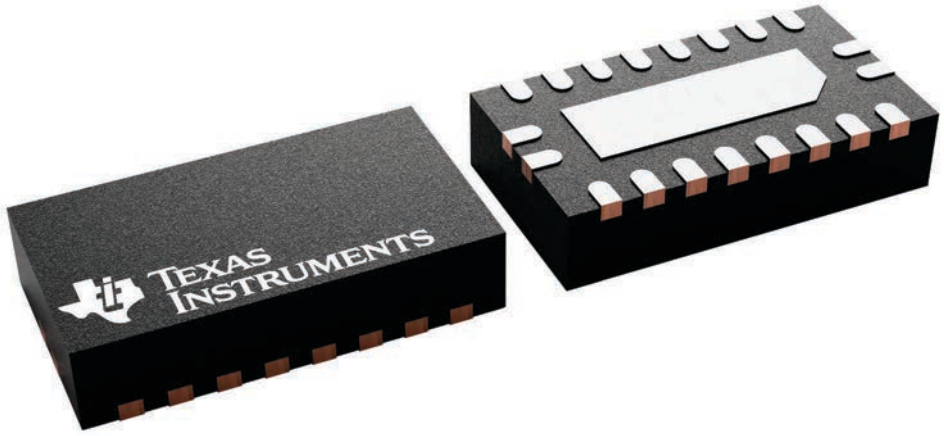
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

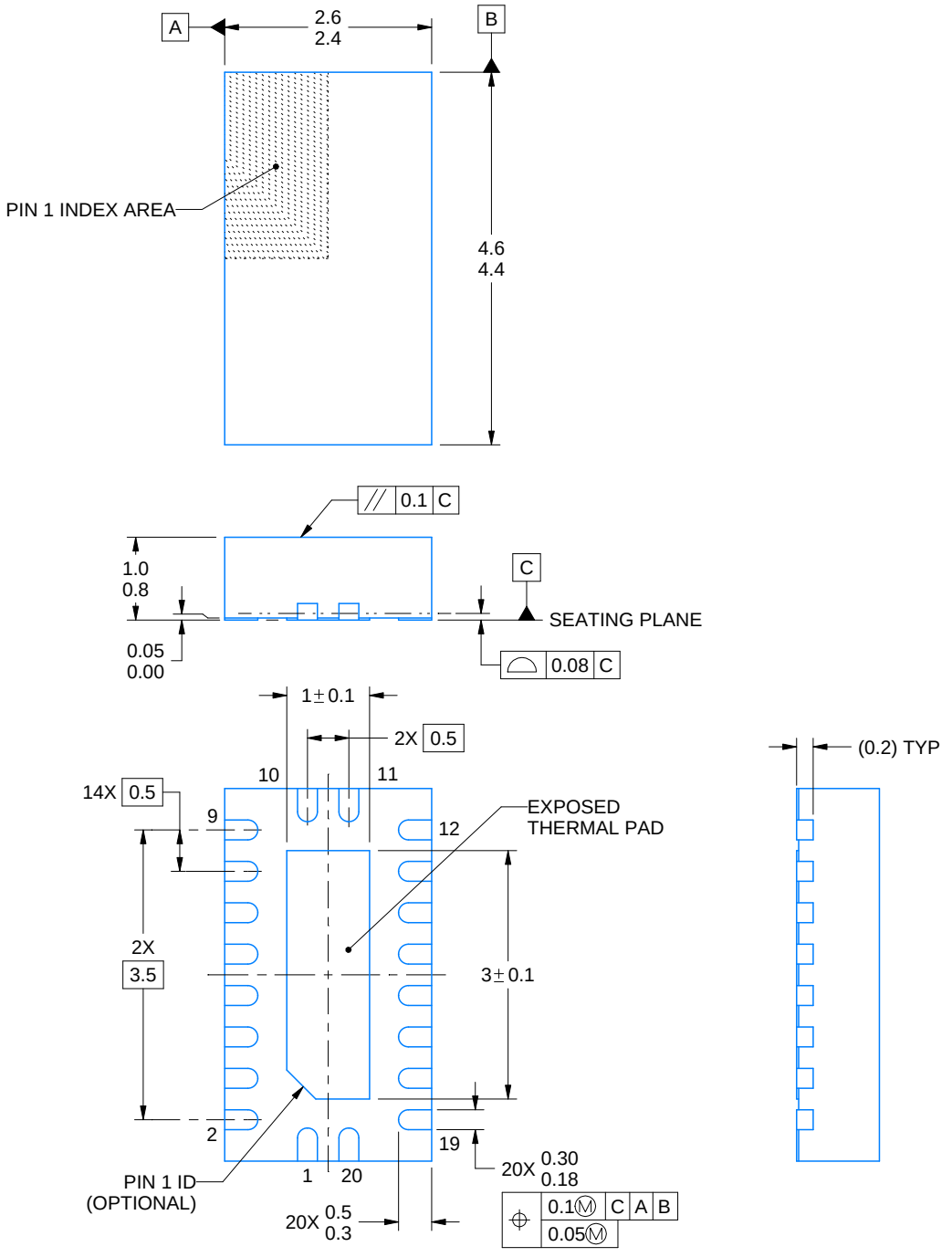


PACKAGE OUTLINE

RKS0020A

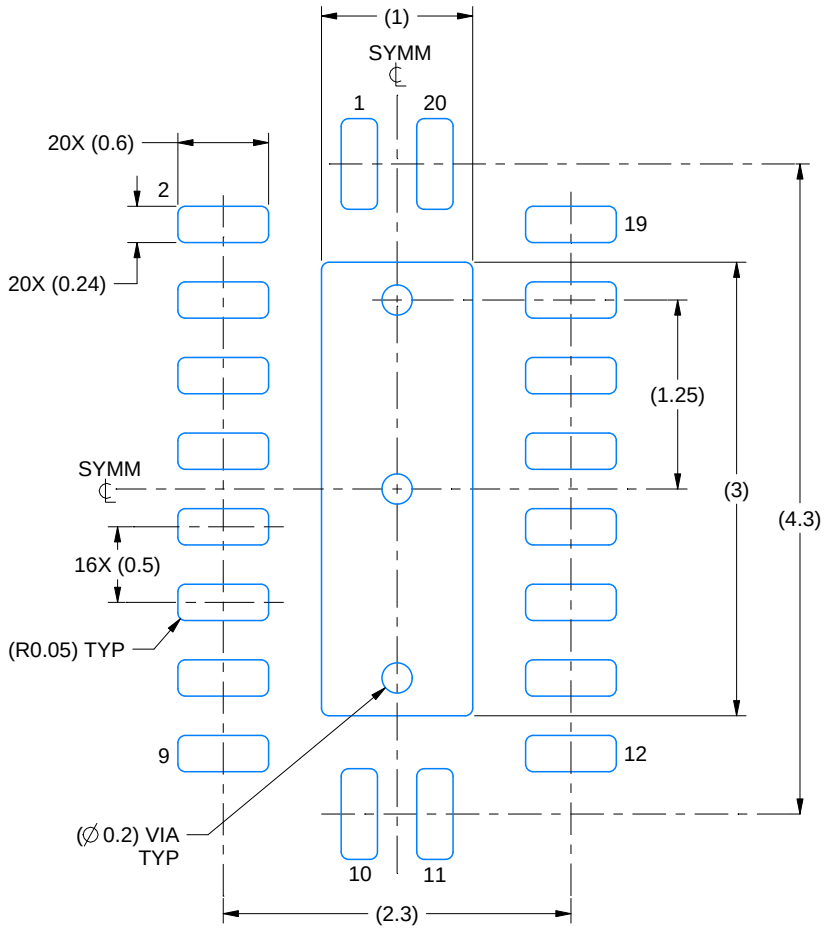
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

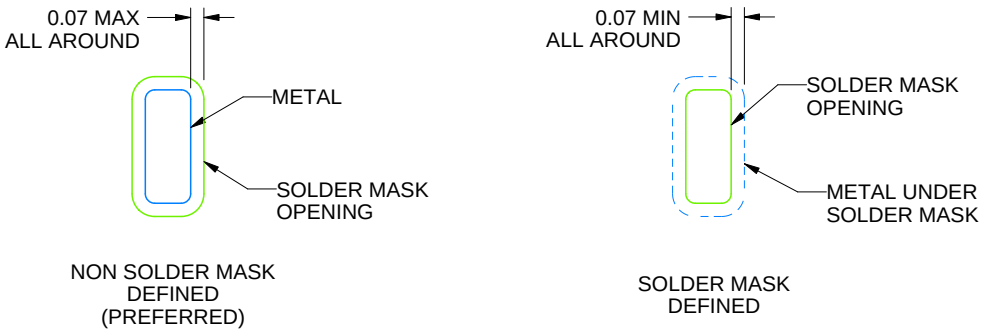


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

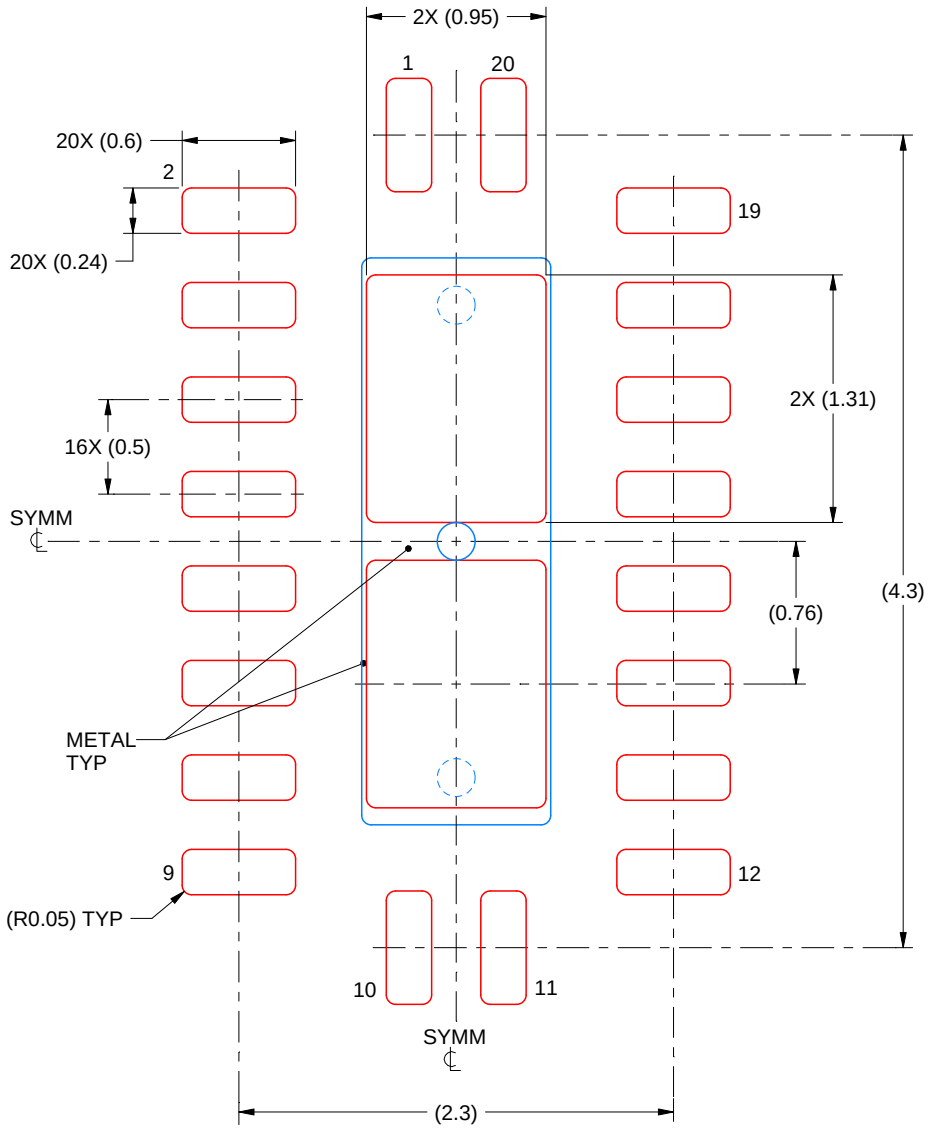


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

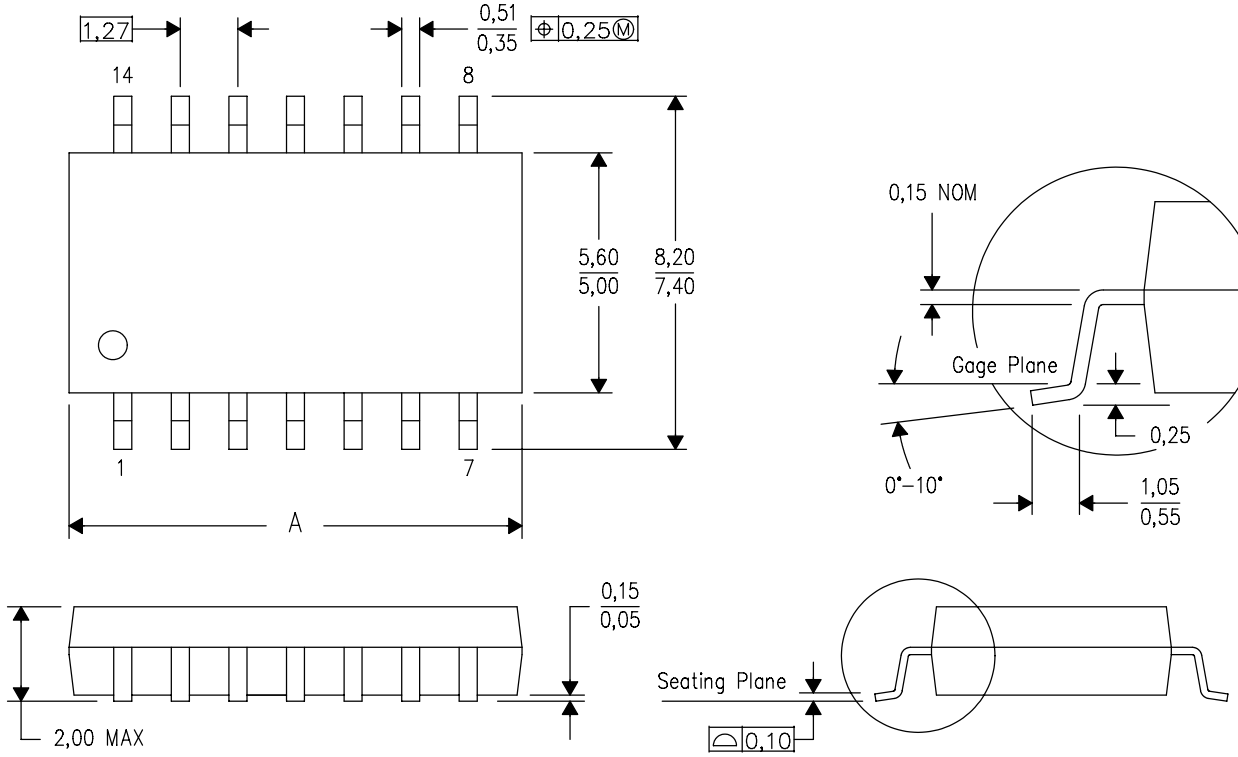
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

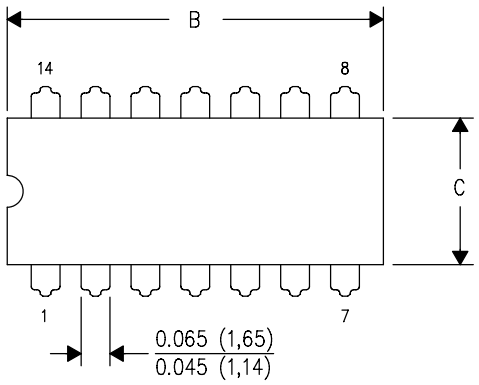
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

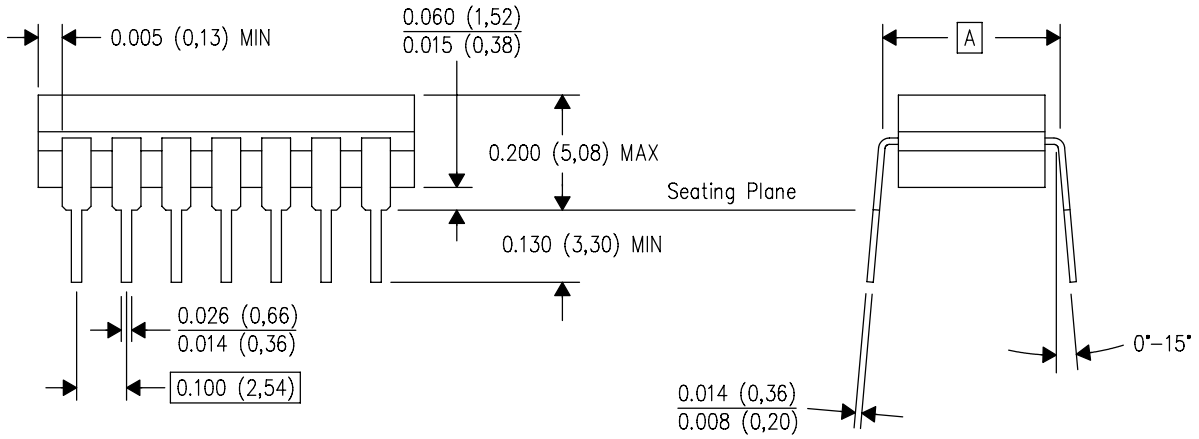
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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