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NTE74HC109
Integrated Circuit
TTL – High Speed CMOS,
Dual J–$\overline{K}$ Positive Edge Triggered
Flip–Flop w/Set & Reset

Description:

The NTE74HC109 is a dual J–K flip–flip with set and reset in a 16–Lead plastic DIP type package. The flip–flop changes state with the positive transition of Clock (1CP and 2CP).

The flip–flip is set and reset by active–low $\overline{S}$ and $\overline{R}$, respectively. A low on both the set and reset inputs simultaneously will force both Q and $\overline{Q}$ outputs high. However, both set and reset going high simultaneously results in an unpredictable output condition.

Features:

- Asynchronous Set and Reset
- Schmitt Trigger Clock Inputs
- Typical Propagation Delay: 18ns (typ)
- Fanout (Over Temperature Range):
  Standard Outputs . . . . . 10 LS–TTL Loads
  Bus Driver Outputs . . . . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Maximum Junction Temperature, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient (Note 3), R_{thJA} . . . . . 90°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the Recommended Operating Conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the Recommended Operating Conditions may effect device reliability. The Absolute Maximum Ratings are stress ratings only.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. R_{thJA} is measured with the component mounted on an evaluation PC board in free air.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–55	–	+125	°C
C_P Input Rise or Fall Times	t_r, t_f				
V_{CC} = 2.0V		–	–	1.0	ms
V_{CC} = 4.5V		–	–	1.0	ms
V_{CC} = 6.0V		–	–	1.0	ms
Input Rise or Fall Times (All Inputs Except C_P)	t_r, t_f				
V_{CC} = 2.0V		–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
High Level Input Voltage	V_{IH}		2.0	1.5	–	–	1.5	–	1.5	–	V
			4.5	3.15	–	–	3.15	–	3.15	–	V
			6.0	4.2	–	–	4.2	–	4.2	–	V
Low Level Input Voltage	V_{IH}		2.0	–	–	0.5	–	0.5	–	0.5	V
			4.5	–	–	1.35	–	1.35	–	1.35	V
			6.0	–	–	1.8	–	1.8	–	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IN} = V_{IH} or V_{IL}, I_O = –0.02mA	2.0	1.9	–	–	1.9	–	1.9	–	V
			4.5	4.4	–	–	4.4	–	4.4	–	V
			6.0	5.9	–	–	5.9	–	5.9	–	V
TTL Loads		V_I = V_{IH} or V_{IL}, I_O = –4mA	4.5	3.98	–	–	3.84	–	3.7	–	V
		V_I = V_{IH} or V_{IL}, I_O = –5.2mA	6.0	5.48	–	–	5.34	–	5.2	–	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IN} = V_{IH} or V_{IL}, I_O = 0.02mA	2.0	–	–	0.1	–	0.1	–	0.1	V
			4.5	–	–	0.1	–	0.1	–	0.1	V
			6.0	–	–	0.1	–	0.1	–	0.1	V
TTL Loads		V_{IN} = V_{IH} or V_{IL}, I_O = 4mA	4.5	–	–	0.26	–	0.33	–	0.4	V
		V_{IN} = V_{IH} or V_{IL}, I_O = –5.2mA	6.0	–	–	0.26	–	0.33	–	0.4	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	µA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_O = 0mA	6.0	–	–	4.0	–	40	–	80	µA

Prerequisite for Switching Characteristics:

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			–40° to +85°C		–55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Setup Time J, $\overline{K}$, to CP	t_{SU}		2.0	80	–	–	100	–	120	–	ns
			4.5	16	–	–	20	–	24	–	ns
			6.0	14	–	–	17	–	20	–	ns

Prerequisite for Switching Characteristics (Cont'd):

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			−40° to +85°C		−55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Hold Time J, $\overline{K}$, to CP	t_H		2.0	5	–	–	5	–	5	–	ns
			4.5	5	–	–	5	–	5	–	ns
			6.0	5	–	–	5	–	5	–	ns
Removal Time $\overline{R}$, $\overline{S}$, to CP	t_{REM}		2.0	80	–	–	100	–	120	–	ns
			4.5	16	–	–	20	–	24	–	ns
			6.0	14	–	–	17	–	20	–	ns
Pulse Width CP, $\overline{R}$, $\overline{S}$	t_W		2.0	80	–	–	100	–	120	–	ns
			4.5	16	–	–	20	–	24	–	ns
			6.0	14	–	–	17	–	20	–	ns
CP Frequency	f_{MAX}		2.0	6	–	–	5	–	4	–	MHz
			4.5	30	–	–	25	–	20	–	MHz
			6.0	35	–	–	29	–	23	–	MHz

Switching Characteristics: ($t_r = t_f = 6ns$)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			−40° to +85°C		−55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Propagation Delay, CP to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	175	–	220	–	265	ns
		C_L = 50pF	4.5	–	–	35	–	44	–	53	ns
		C_L = 15pF	5.0	–	14	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	30	–	37	–	45	ns
Propagation Delay, $\overline{S}$ to Q	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	120	–	150	–	180	ns
		C_L = 50pF	4.5	–	–	24	–	30	–	36	ns
		C_L = 15pF	5.0	–	9	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	20	–	26	–	31	ns
Propagation Delay, $\overline{S}$ to $\overline{Q}$	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	155	–	195	–	235	ns
		C_L = 50pF	4.5	–	–	31	–	39	–	47	ns
		C_L = 15pF	5.0	–	13	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	26	–	33	–	40	ns
Propagation Delay, $\overline{R}$ to Q	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	185	–	230	–	280	ns
		C_L = 50pF	4.5	–	–	37	–	46	–	56	ns
		C_L = 15pF	5.0	–	15	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	31	–	39	–	48	ns
Propagation Delay, $\overline{R}$ to $\overline{Q}$	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	–	170	–	215	–	255	ns
		C_L = 50pF	4.5	–	–	34	–	43	–	51	ns
		C_L = 15pF	5.0	–	14	–	–	–	–	–	ns
		C_L = 50pF	6.0	–	–	29	–	37	–	43	ns
Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	–	75	–	95	–	110	ns
			4.5	–	–	15	–	19	–	22	ns
			6.0	–	–	13	–	16	–	19	ns

Switching Characteristics (Cont'd): ($t_r = t_f = 6ns$)

Parameter	Symbol	Test Conditions	V_{CC} (V)	+25°C			−40° to +85°C		−55° to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Input Capacitance	C_{IN}		–	–	–	10	–	10	–	10	pF
CP Frequency	f_{MAX}	C_L = 15pF	5.0	–	60	–	–	–	–	–	MHz
Power Dissipation Capacitance	C_{PD}	Note 4	5.0	–	30	–	–	–	–	–	pF

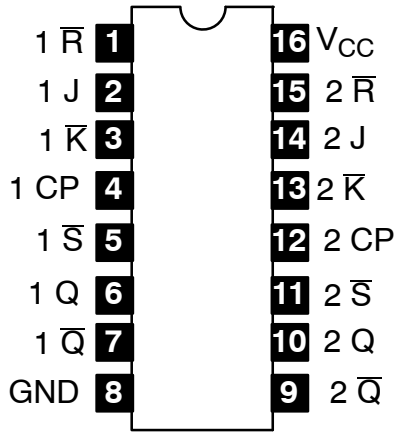
Note 4. C_{PD} is used to determine the dynamic power consumption, per flip−flop.
$P_D = V_{CC}^2 f_I + \Sigma + C_L f_O$ where f_I = input frequency, f_O = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

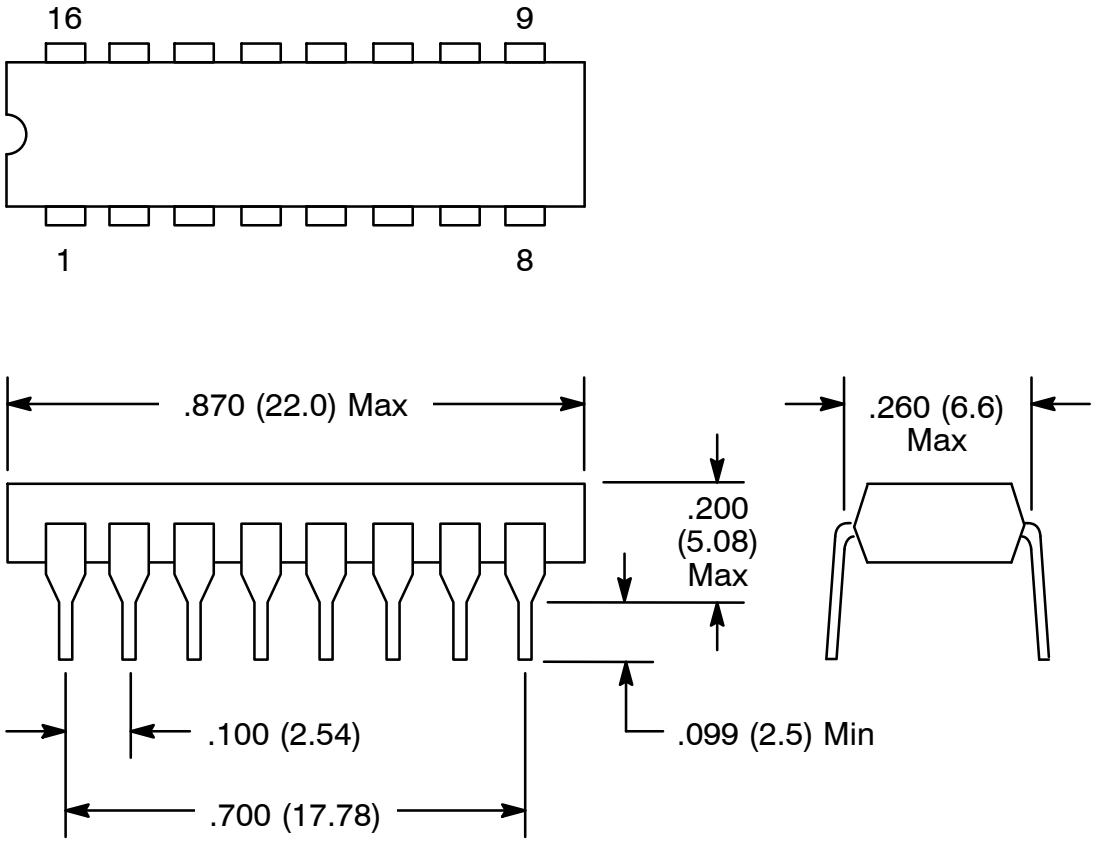
Truth Table:

Inputs					Output	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (NOTE)	H (NOTE)
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	No Change	
H	H	↑	H	H	H	L
H	H	L	X	X	No Change	

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
↑ = Low−to−High Transition
NOTE: Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously.

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)