

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT  
**μPD78F9221CS, 78F9222CS**

**8-BIT SINGLE-CHIP MICROCONTROLLER**

The μPD78F9221CS, 78F9222CS are 8-bit single-chip microcontrollers of the 78K0S series. These microcontrollers feature Single-voltage Self-programming Flash memory and many peripherals.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

78K0S/KA1+ User's Manual: U16898E  
 78K/0S Series User's Manual Instruction: U11047E

**FEATURES**

- Minimum instruction execution time selectable from high speed (0.2 μs) to low speed (3.2 μs) (with CPU clock of 10 MHz)
- General-purpose registers: 8 bits × 8 registers
- ROM and RAM capacities

Part number \ Item	Program Memory (Flash Memory)	Memory (Internal High-Speed RAM)
μPD78F9221CS	2 KB	128 bytes
μPD78F9222CS	4 KB	256 bytes

- On-chip power-on clear (POC) circuit and low voltage detector (LVI)
- On-chip watchdog timer (operable on internal low-speed internal oscillator clock)
- I/O ports: 17
- Timer: 4 channels
  - 16-bit timer/event counter: 1 channel
  - 8-bit timer: 2 channels
  - Watchdog timer: 1 channel
- Serial interface: UART (LIN (Local Interconnect Network) bus supported) 1 channel
- 10-bit resolution A/D converter: 4 channels
- Supply voltage: V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note</sup>
- Operating temperature range: T<sub>A</sub> = -40 to +85°C

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on clear (POC) circuit is 2.1 V ±0.1 V.

The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

**APPLICATIONS**

Automotive electronics, household appliances, toys, and industrial equipment

**ORDERING INFORMATION**

Part Number	Package
$\mu$ PD78F9221CS-CAC-A	20-pin plastic SDIP (7.62 mm (300))
$\mu$ PD78F9222CS-CAC-A	20-pin plastic SDIP (7.62 mm (300))

**Remark** Products with -A at the end of the part number are lead-free products.

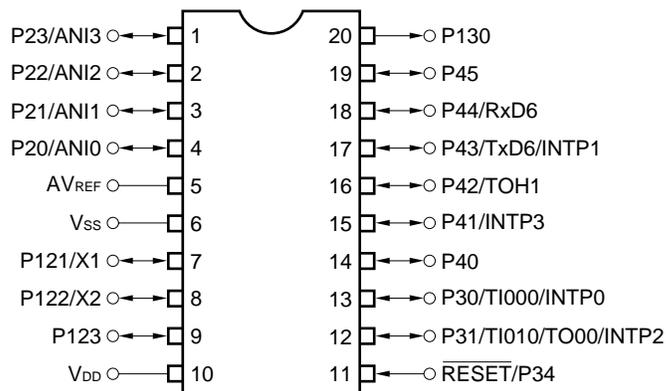
OVERVIEW OF FUNCTIONS

Item		μPD78F9221CS	μPD78F9222CS
Internal memory	Flash memory	2 KB	4 KB
	High-speed RAM	128 bytes	256 bytes
Memory space		64 KB	
X1 input clock (oscillation frequency)		Crystal/ceramic/external clock input: 10 MHz (V <sub>DD</sub> = 2.0 to 5.5 V)	
Internal oscillation clock	High speed (oscillation frequency)	Internal oscillation: 8 MHz (TYP.)	
	Low speed (for TMH1 and WDT)	Internal oscillation: 240 kHz (TYP.)	
General-purpose registers		8 bits × 8 registers	
Instruction execution time		0.2 μs/0.4 μs/0.8 μs/1.6 μs/3.2 μs (X1 input clock: f <sub>x</sub> = 10 MHz)	
I/O port		Total: 17 pins CMOS I/O: 15 pins CMOS input: 1 pin CMOS output: 1 pin	
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter: 1 channel</li> <li>• 8-bit timer (timer H1): 1 channel</li> <li>• 8-bit timer (timer 80): 1 channel</li> <li>• Watchdog timer: 1 channel</li> </ul>	
	Timer output	2 pins (PWM: 1 pin)	
A/D converter		10-bit resolution × 4 channels	
Serial interface		LIN-bus-supporting UART mode: 1 channel	
Vectored interrupt sources	External	4	
	Internal	9	
Reset		<ul style="list-style-type: none"> <li>• Reset by RESET pin</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by power-on clear</li> <li>• Internal reset by low-voltage detector</li> </ul>	
Supply voltage		V <sub>DD</sub> = 2.0 to 5.5 V <sup>Note</sup>	
Operating temperature range		T <sub>A</sub> = -40 to +85°C	
Package		20-pin plastic SDIP	

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>Poc</sub>) of the power-on- clear (POC) circuit is 2.1 V ±0.1 V.

**PIN CONFIGURATION (Top View)**

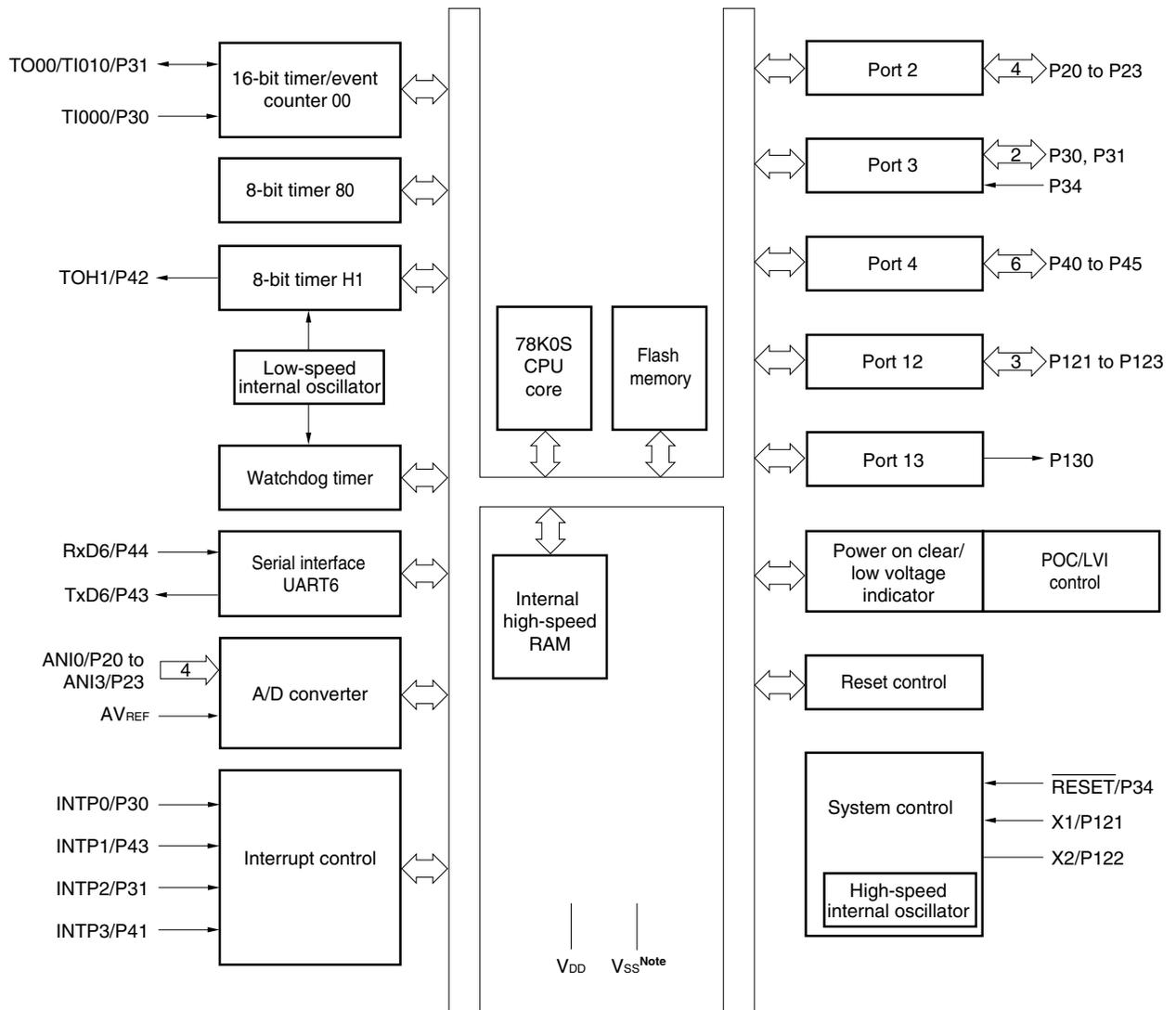
- 20-pin plastic SDIP



**Note** In the μ PD78F9221CS, 78F9222CS, V<sub>SS</sub> functions alternately as the ground potential of the A/D converter. Be sure to connect V<sub>SS</sub> to a stabilized GND (= 0 V).

ANI0 to ANI3:	Analog input	RESET:	Reset
AVREF:	Analog reference voltage	RxD6:	Receive data
INTP0 to INTP3:	External interrupt input	TI000, TI010:	Timer input
P20 to P23:	Port 2	TO00, TOH1:	Timer output
P30, P31, P34:	Port 3	TxD6:	Transmit data
P40 to P45:	Port 4	VDD:	Power supply
P121 to P123:	Port 12	VSS:	Ground
P130:	Port 13	X1, X2:	Crystal oscillator (X1 input clock)

BLOCK DIAGRAM



**Note** In the μ PD78F9221CS, 78F9222CS, V<sub>SS</sub> functions alternately as the ground potential of the A/D converter. Be sure to connect V<sub>SS</sub> to a stabilized GND (= 0 V).

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1. PIN FUNCTIONS

1.1 Port Functions

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20 to P23	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	ANI0 to ANI3
P30	I/O	Port 3	Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.	Input	TI000/INTP0
P31					TI010/TO00/ INTP2
P34	Input		Input only	Input	RESET
P40	I/O	Port 4. 6-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–
P41					INTP3
P42					TOH1
P43					TxD6/INTP1
P44					RxD6
P45					–
P121	I/O	Port 12. 3-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected only to P123 by setting software.		Input	X1
P122					X2
P123					–
P130	Output	Port 13. 1-bit output-only port		Output	–

**Caution** The P121/X1 and P122/X2 pins are pulled down during reset.

1.2 Non-port Functions

Pin Name	I/O	Function	After Reset	Alternate-Function Pin
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI000
INTP1				P43/TxD6
INTP2				P31/TI010/TO00
INTP3				P41
RxD6	Input	Serial data input for asynchronous serial interface	Input	P44
TxD6	Output	Serial data output for asynchronous serial interface	Input	P43/INTP1
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture registers (CR000 and CR010) of 16-bit timer/event counter 00	Input	P30/INTP0
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P31/TO00/INTP2
TO00	Output	16-bit timer/event counter 00 output	Input	P31/TI010/INTP2
TOH1	Output	8-bit timer H1 output	Input	P42
ANI0 to ANI3	Input	Analog input of A/D converter	Input	P20 to P23
AV <sub>REF</sub>	–	Reference voltage of A/D converter	–	–
RESET	Input	System reset input	–	P34
X1	Input	Connection of crystal/ceramic resonator for system clock oscillation. External clock input	–	P121
X2	–	Connection of crystal/ceramic resonator for system clock oscillation.	–	P122
V <sub>DD</sub>	–	Positive power supply	–	–
V <sub>SS</sub>	–	Ground potential	–	–

**Caution** The P121/X1 and P122/X2 pins are pulled down during reset.

**1.3 Pin I/O Circuits and Connection of Unused Pins**

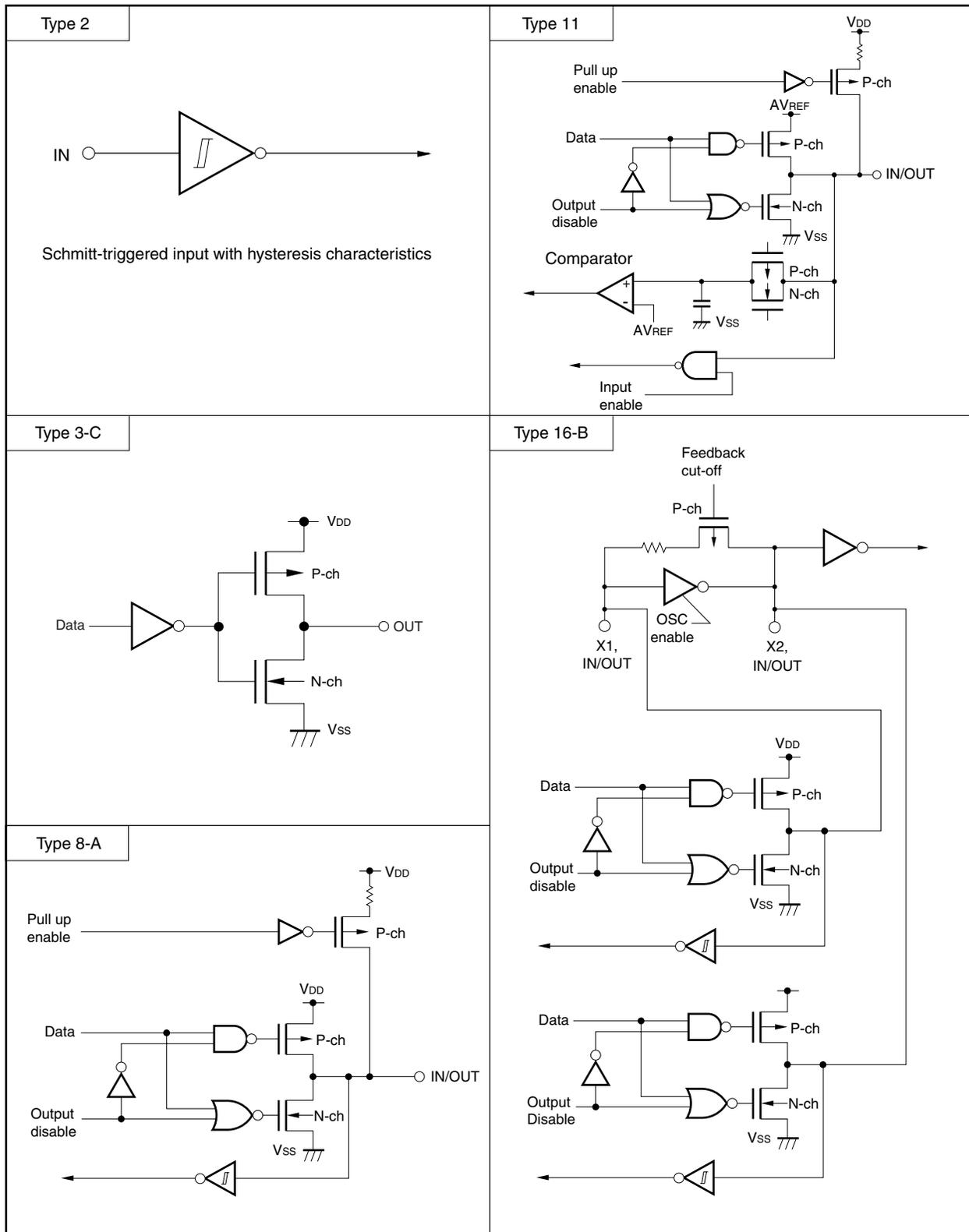
Table 1-1 shows I/O circuit type of each pin and the connections of unused pins.

For the configuration of the I/O circuit of each type, refer to **Figure 1-1**.

**Table 1-1. Types of Pin I/O Circuits and Connection of Unused Pins**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/ANI0 to P23/ANI3	11	I/O	Input: Independently connect to AV <sub>REF</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P30/TI000/INTP0	8-A		Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P31/TI010/TO00/INTP2			
P34/RESET	2	Input	Connect to V <sub>DD</sub> via a resistor.
P40	8-A	I/O	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P41/INTP3			
P42/TOH1			
P43/TxD6/INTP1			
P44/RxD6			
P45			
P121/X1	16-B		Input: Independently connect to V <sub>SS</sub> via a resistor. Output: Leave open.
P122/X2			
P123	8-A		Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P130	3-C	Output	Leave open.
AV <sub>REF</sub>	–	Input	Directly connect to V <sub>DD</sub> .

Figure 1-1. Pin I/O Circuits



**2. ELECTRICAL SPECIFICATIONS (TARGET)**

These specifications are only target values, and may not be satisfied by mass-produced products.

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C)**

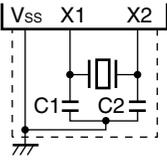
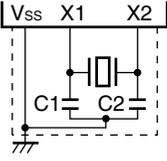
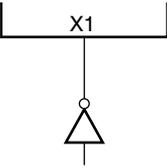
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.3 to +6.5	V
	V <sub>SS</sub>		-0.3 to +0.3	V
	AV <sub>REF</sub>		-0.3 to V <sub>DD</sub> + 0.3 <sup>Note</sup>	V
Input voltage	V <sub>I1</sub>	P30, P31, P34, P40 to P45, P121 to P123	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note</sup>	V
	V <sub>I2</sub>	P20 to P23	-0.3 to AV <sub>REF</sub> + 0.3 <sup>Note</sup> and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note</sup>	V
Output voltage	V <sub>O</sub>		-0.3 to V <sub>DD</sub> + 0.3 <sup>Note</sup>	V
Analog input voltage	V <sub>AN</sub>		-0.3 to AV <sub>REF</sub> + 0.3 <sup>Note</sup> and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note</sup>	V
Output current, high	I <sub>OH</sub>	Per pin	-10.0	mA
		Total of pins other than P20 to P23	-44.0	mA
		Total of P20 to P23	-44.0	mA
Output current, low	I <sub>OL</sub>	Per pin	20.0	mA
		Total of all pins	44.0	mA
Operating ambient temperature	T <sub>A</sub>	In normal operation mode	-40 to +85	°C
		During flash memory programming		
Storage temperature	T <sub>stg</sub>	Flash memory blank status	-65 to +150	°C
		Flash memory programming already performed	-40 to +125	°C

**Note** Must be 6.5 V or lower

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**X1 Oscillator Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note 1</sup>, V<sub>SS</sub> = 0 V)**

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 2</sup>		2.0		10.0	MHz
Crystal resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 2</sup>		2.0		10.0	MHz
External clock		X1 input frequency (f <sub>x</sub> ) <sup>Note 2</sup>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	2.0		10.0	MHz
			2.0 V ≤ V <sub>DD</sub> < 2.7 V	2.0		5.0	
		X1 input high-/low-level width (t <sub>xH</sub> , t <sub>xL</sub> )	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.045		0.25	μs
			2.0 V ≤ V <sub>DD</sub> < 2.7 V	0.09		0.25	

- Notes**
1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.
  2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**Caution** When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V<sub>SS</sub>.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

**Remark** For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

**High-Speed Internal Oscillator Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note 1</sup>, V<sub>SS</sub> = 0 V)**

Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
High-speed internal oscillator	Oscillation frequency (f <sub>x</sub> = 8 MHz <sup>Note 2</sup> ) deviation	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	T <sub>A</sub> = -10 to +80°C			±3	%
			T <sub>A</sub> = -40 to +85°C			±5	%
	Oscillation frequency (f <sub>x</sub> ) <sup>Note 2</sup>	2.0 V ≤ V <sub>DD</sub> < 2.7 V		5.5			MHz

- Notes**
1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.
  2. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**Low-Speed Internal Oscillator Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note</sup>, V<sub>SS</sub> = 0 V)**

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Low-speed internal oscillator	Oscillation frequency (f <sub>RL</sub> )		120	240	480	kHz

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note</sup>, V<sub>SS</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I <sub>OH1</sub>	Pins other than P20 to P23	Per pin	2.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		-5	mA
			Total	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		-25	mA
				2.0 V ≤ V <sub>DD</sub> < 4.0 V		-15	mA
	I <sub>OH2</sub>	P20 to P23	Per pin	2.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V		-5	mA
			Total	2.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V		-15	mA
	Output current, low	I <sub>OL</sub>	Per pin		2.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		10
Total of all pins			4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V		30	mA	
			2.0 V ≤ V <sub>DD</sub> < 4.0 V		15	mA	
Input voltage, high	V <sub>IH1</sub>	P30, P31, P34, P40 to P45, P123		0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	P20 to P23		0.7AV <sub>REF</sub>		AV <sub>REF</sub>	V
	V <sub>IH3</sub>	P121, P122		0.8V <sub>DD</sub>		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	P30, P31, P34, P40 to P45, P123		0		0.2V <sub>DD</sub>	V
	V <sub>IL2</sub>	P20 to P23		0		0.3AV <sub>REF</sub>	V
	V <sub>IL3</sub>	P121, P122		0		0.2V <sub>DD</sub>	V
Output voltage, high	V <sub>OH1</sub>	Total of pins other than P20 to P23	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	V <sub>DD</sub> - 1.0			V
		I <sub>OH1</sub> = -15 mA	I <sub>OH1</sub> = -5 mA				
		I <sub>OH1</sub> = -100 μA	2.0 V ≤ V <sub>DD</sub> < 4.0 V	V <sub>DD</sub> - 0.5			V
	V <sub>OH2</sub>	Total of pins P20 to P23	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V	AV <sub>REF</sub> - 1.0			V
		I <sub>OH2</sub> = -10 mA	I <sub>OH2</sub> = -5 mA				
		2.0 V ≤ AV <sub>REF</sub> < 4.0 V		AV <sub>REF</sub> - 0.5			V
		I <sub>OH2</sub> = -100 μA					
Output voltage, low	V <sub>OL</sub>	Total of pins	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V			1.3	V
		I <sub>OL</sub> = 30 mA	I <sub>OL</sub> = 10 mA				
		2.0 V ≤ V <sub>DD</sub> ≤ 4.0 V				0.4	V
		I <sub>OL</sub> = 400 μA					
Input leakage current, high	I <sub>LIH1</sub>	V <sub>i</sub> = V <sub>DD</sub>	Pins other than X1			1	μA
Input leakage current, low	I <sub>LIL1</sub>	V <sub>i</sub> = 0 V	Pins other than X1			-1	μA
Output leakage current, high	I <sub>LOH</sub>	V <sub>o</sub> = V <sub>DD</sub>	Pins other than X2			1	μA
Output leakage current, low	I <sub>LOL</sub>	V <sub>o</sub> = 0 V	Pins other than X2			-1	μA
Pull-up resistance	R <sub>PU</sub>	V <sub>i</sub> = 0 V		10	30	100	kΩ
Pull-down resistance	R <sub>PD</sub>	P121, P122, reset status		10	30	100	kΩ

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note 1</sup>, V<sub>SS</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 2</sup>	I <sub>DD1</sub> <sup>Note 3</sup>	Crystal/ceramic oscillation, external clock input oscillation operating mode <sup>Note 6</sup>	f <sub>x</sub> = 10 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When A/D converter is stopped		6.1	12.2	mA
				When A/D converter is operating <sup>Note 8</sup>		7.6	15.2	
			f <sub>x</sub> = 6 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When A/D converter is stopped		5.5	11.0	mA
				When A/D converter is operating <sup>Note 8</sup>			14.0	
			f <sub>x</sub> = 5 MHz V <sub>DD</sub> = 3.0 V ±10% <sup>Note 5</sup>	When A/D converter is stopped		3.0	6.0	mA
				When A/D converter is operating <sup>Note 8</sup>		4.5	9.0	
	I <sub>DD2</sub>	Crystal/ceramic oscillation, external clock input HALT mode <sup>Note 6</sup>	f <sub>x</sub> = 10 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When peripheral functions are stopped		1.7	3.8	mA
				When peripheral functions are operating			6.7	
			f <sub>x</sub> = 6 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When peripheral functions are stopped		1.3	3.0	mA
				When peripheral functions are operating			6.0	
			f <sub>x</sub> = 5 MHz V <sub>DD</sub> = 3.0 V ±10% <sup>Note 5</sup>	When peripheral functions are stopped		0.48	1	mA
				When peripheral functions are operating			2.1	
	I <sub>DD3</sub> <sup>Note 3</sup>	High-speed internal oscillation operating mode <sup>Note 7</sup>	f <sub>x</sub> = 8 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When A/D converter is stopped		5.0	10.0	mA
				When A/D converter is operating <sup>Note 8</sup>		6.5	13.0	
I <sub>DD4</sub>	High-speed internal oscillation HALT mode <sup>Note 7</sup>	f <sub>x</sub> = 8 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When peripheral functions are stopped		1.4	3.2	mA	
			When peripheral functions are operating			5.9		
I <sub>DD5</sub>	STOP mode	V <sub>DD</sub> = 5.0 V ±10%	When low-speed internal oscillation is stopped		3.5	20.0	μA	
			When low-speed internal oscillation is operating		17.5	32.0		
		V <sub>DD</sub> = 3.0 V ±10%	When low-speed internal oscillation is stopped		3.5	15.5	μA	
			When low-speed internal oscillation is operating		11.0	26.0		

- Notes**
1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.
  2. Total current flowing through the internal power supply (V<sub>DD</sub>). Peripheral operation current is included (however, the current that flows through the pull-up resistors of ports is not included).
  3. These currents include peripheral operation currents.
  4. When the processor clock control register (PCC) is set to 00H.
  5. When the processor clock control register (PCC) is set to 02H.
  6. When crystal/ceramic oscillation clock, external clock input is selected as the system clock source using the option byte.
  7. When the high-speed internal oscillation clock is selected as the system clock source using the option byte.
  8. The current that flows through the AV<sub>REF</sub> pin is included.

AC Characteristics

(1) Basic operation ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note 1}}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (minimum instruction execution time)	$t_{CY}$	Crystal/ceramic oscillation clock, external clock input	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.2		16	$\mu\text{S}$
			$3.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.33		16	$\mu\text{S}$
			$2.7\text{ V} \leq V_{DD} < 3.0\text{ V}$	0.4		16	$\mu\text{S}$
			$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1		16	$\mu\text{S}$
		High-speed internal oscillation clock	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.23		4.22	$\mu\text{S}$
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.47		4.22	$\mu\text{S}$
$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.95			4.22	$\mu\text{S}$		
TI000 input high-level width, low-level width	$t_{TIH}$ , $t_{TIL}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$2/f_{sam} + 0.1^{\text{Note 2}}$			$\mu\text{S}$	
		$2.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	$2/f_{sam} + 0.2^{\text{Note 2}}$			$\mu\text{S}$	
Interrupt input high-level width, low-level width	$t_{INTH}$ , $t_{INTL}$		1			$\mu\text{S}$	
RESET input low-level width	$t_{RSL}$		2			$\mu\text{S}$	

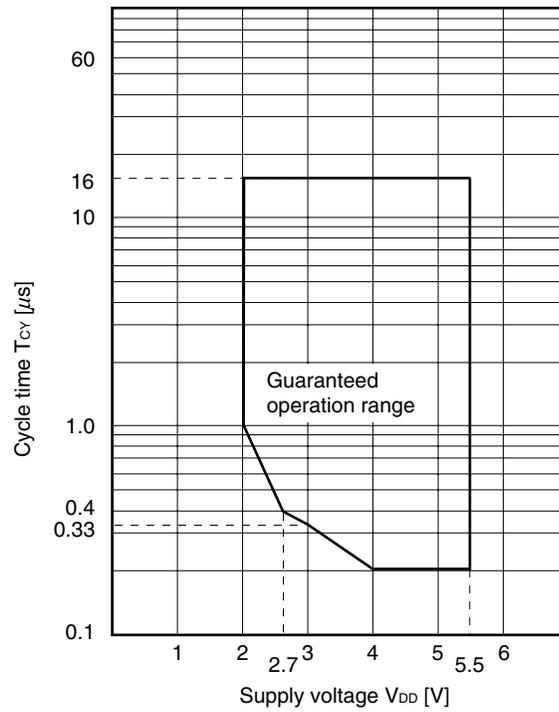
- Notes**
1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .
  2. Selection of  $f_{sam} = f_{XP}$ ,  $f_{XP}/4$ , or  $f_{XP}/256$  is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock,  $f_{sam} = f_{XP}$ .

CPU Clock Frequency, Peripheral Clock Frequency

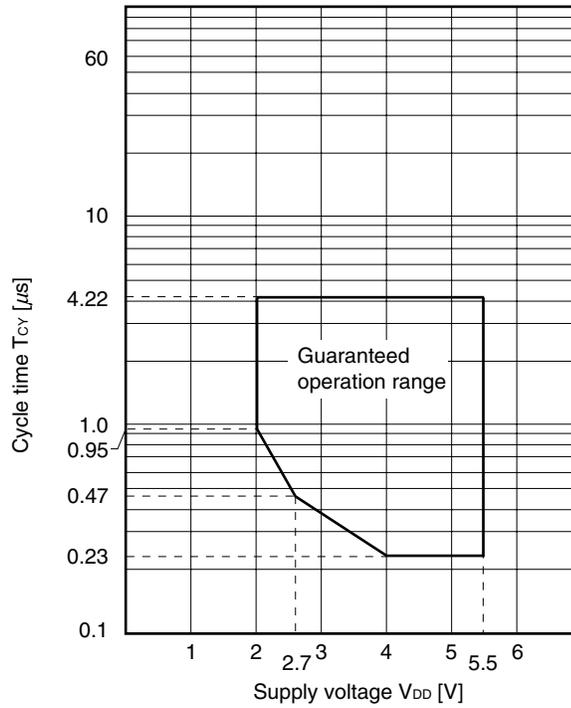
Parameter	Conditions	CPU Clock ( $f_{CPU}$ )	Peripheral Clock ( $f_{XP}$ )
Ceramic resonator, crystal resonator, external clock	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$125\text{ kHz} \leq f_{CPU} \leq 10\text{ MHz}$	$500\text{ kHz} \leq f_{XP} \leq 10\text{ MHz}$
	$3.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	$125\text{ kHz} \leq f_{CPU} \leq 6\text{ MHz}$	
	$2.7\text{ V} \leq V_{DD} < 3.0\text{ V}$	$125\text{ kHz} \leq f_{CPU} \leq 5\text{ MHz}$	
	$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}^{\text{Note}}$	$125\text{ kHz} \leq f_{CPU} \leq 2\text{ MHz}$	$500\text{ kHz} \leq f_{XP} \leq 5\text{ MHz}$
High-speed internal oscillator	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$500\text{ kHz (Typ.)} \leq f_{CPU} \leq 8\text{ MHz (Typ.)}$	$2\text{ MHz (Typ.)} \leq f_{XP} \leq 8\text{ MHz (Typ.)}$
	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	$500\text{ kHz (Typ.)} \leq f_{CPU} \leq 4\text{ MHz (Typ.)}$	
	$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}^{\text{Note}}$	$500\text{ kHz (Typ.)} \leq f_{CPU} \leq 2\text{ MHz (Typ.)}$	$2\text{ MHz (Typ.)} \leq f_{XP} \leq 4\text{ MHz (Typ.)}$

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

**T<sub>CY</sub> vs. V<sub>DD</sub> (Crystal/Ceramic Oscillation Clock, External Clock Input)**



**T<sub>CY</sub> vs. V<sub>DD</sub> (High-Speed Internal Oscillation Clock)**



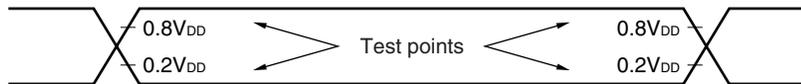
(2) Serial interface ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note}}$ ,  $V_{SS} = 0\text{ V}$ )

**UART mode (UART6, dedicated baud rate generator output)**

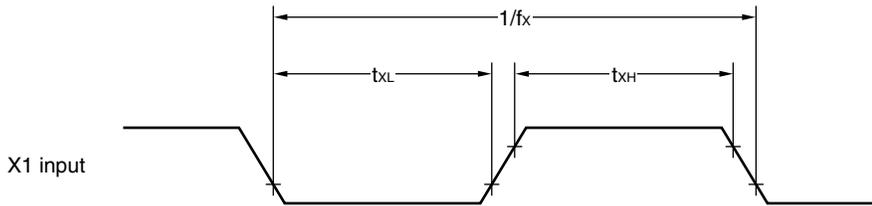
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

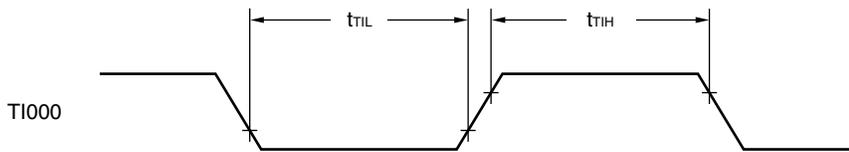
**AC Timing Test Points (Excluding X1 Input)**



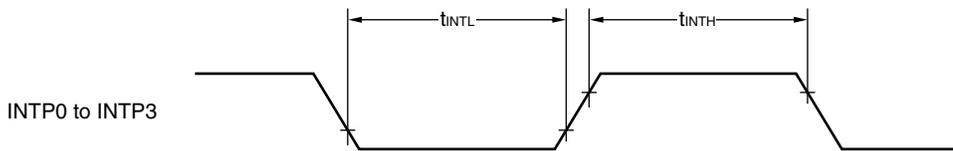
**Clock Timing**



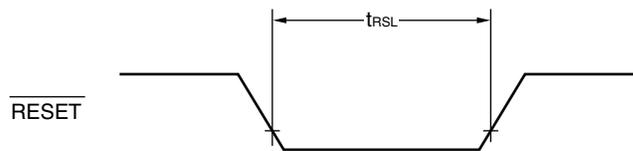
**TI000 Timing**



**Interrupt Input Timing**



**RESET Input Timing**



**A/D Converter Characteristics (T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ AV<sub>REF</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V<sup>Note 1</sup>)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error <sup>Notes 2, 3</sup>	AINL	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V		±0.3	±0.6	%FSR
Conversion time	t <sub>CONV</sub>	4.5 V ≤ AV <sub>REF</sub> ≤ 5.5 V	3.0		100	μs
		4.0 V ≤ AV <sub>REF</sub> < 4.5 V	4.8		100	μs
		2.85 V ≤ AV <sub>REF</sub> < 4.0 V	6.0		100	μs
		2.7 V ≤ AV <sub>REF</sub> < 2.85 V	14.0		100	μs
Zero-scale error <sup>Notes 2, 3</sup>	Ezs	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±0.6	%FSR
Full-scale error <sup>Notes 2, 3</sup>	Efs	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±0.6	%FSR
Integral non-linearity error <sup>Note 2</sup>	ILE	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±4.5	LSB
Differential non-linearity error <sup>Note 2</sup>	DLE	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±2.0	LSB
Analog input voltage	V <sub>AIN</sub>		V <sub>SS</sub> <sup>Note 1</sup>		AV <sub>REF</sub>	V

- Notes**
1. In the 78K0S/KA1+, V<sub>SS</sub> functions alternately as the ground potential of the A/D converter. Be sure to connect V<sub>SS</sub> to a stabilized GND (= 0 V).
  2. Excludes quantization error (±1/2 LSB).
  3. This value is indicated as a ratio (%FSR) to the full-scale value.

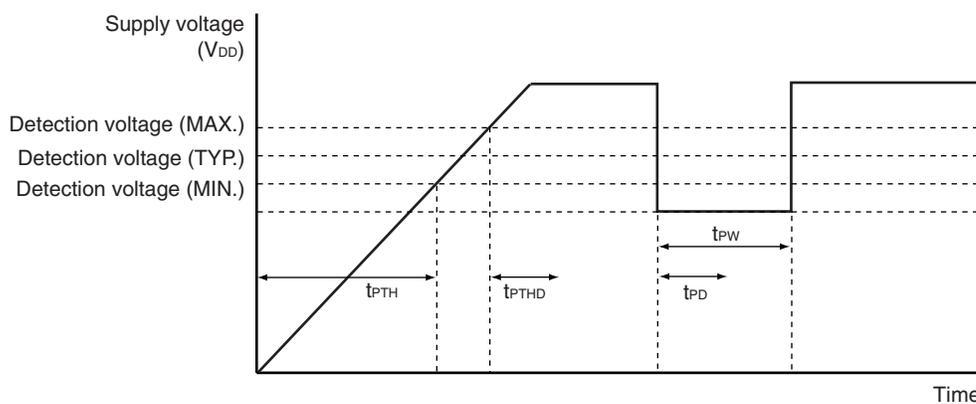
**Caution** The conversion accuracy may be degraded when the analog input pin is used as an alternate I/O port or if a port is changed during A/D conversion.

**POC Circuit Characteristics (T<sub>A</sub> = -40 to +85°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V <sub>POC</sub>		2.0	2.1	2.2	V
Power supply boot time	t <sub>PTH</sub>	V <sub>DD</sub> : 0 V → 2.1 V	1.5			μs
Response delay time 1 <sup>Note 1</sup>	t <sub>PTHD</sub>	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2 <sup>Note 2</sup>	t <sub>PD</sub>	When power supply falls			1.0	ms
Minimum pulse width	t <sub>PW</sub>		0.2			ms

- Notes**
1. Time required from voltage detection to internal reset release.
  2. Time required from voltage detection to internal reset signal generation.

**POC Circuit Timing**



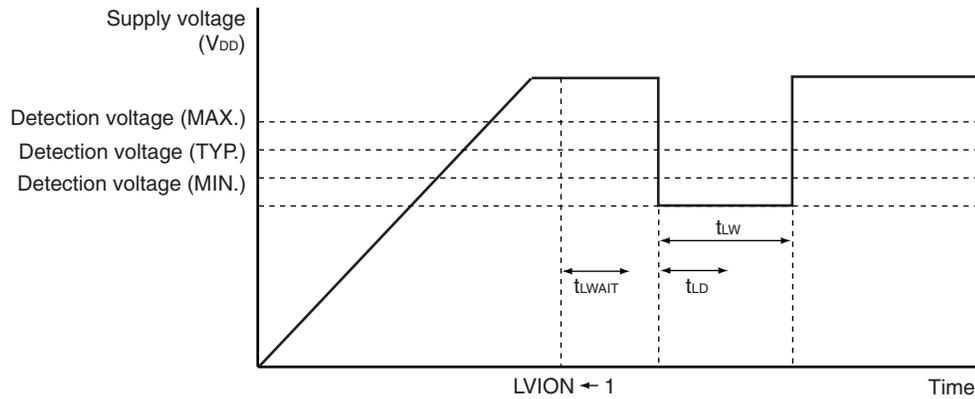
**LVI Circuit Characteristics (T<sub>A</sub> = -40 to +85°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V <sub>LV10</sub>		4.1	4.3	4.5	V
	V <sub>LV11</sub>		3.9	4.1	4.3	V
	V <sub>LV12</sub>		3.7	3.9	4.1	V
	V <sub>LV13</sub>		3.5	3.7	3.9	V
	V <sub>LV14</sub>		3.3	3.5	3.7	V
	V <sub>LV15</sub>		3.15	3.3	3.45	V
	V <sub>LV16</sub>		2.95	3.1	3.25	V
	V <sub>LV17</sub>		2.7	2.85	3.0	V
	V <sub>LV18</sub>		2.5	2.6	2.7	V
	V <sub>LV19</sub>		2.25	2.35	2.45	V
Response time <sup>Note 1</sup>	t <sub>LD</sub>			0.2	2.0	ms
Minimum pulse width	t <sub>LW</sub>		0.2			ms
Operation stabilization wait time <sup>Note 2</sup>	t <sub>LWAIT</sub>			0.1	0.2	ms

- Notes**
1. Time required from voltage detection to interrupt output or internal reset signal generation.
  2. Time required from setting LVION to 1 to operation stabilization.

- Remarks**
1. V<sub>LV10</sub> > V<sub>LV11</sub> > V<sub>LV12</sub> > V<sub>LV13</sub> > V<sub>LV14</sub> > V<sub>LV15</sub> > V<sub>LV16</sub> > V<sub>LV17</sub> > V<sub>LV18</sub> > V<sub>LV19</sub>
  2. V<sub>POC</sub> < V<sub>LV1m</sub> (m = 0 to 9)

**LVI Circuit Timing**



**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		2.0		5.5	V
Release signal set time	t <sub>SREL</sub>		0			μs

Flash Memory Programming Characteristics (T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I <sub>DD</sub>	V <sub>DD</sub> = 5.5 V			7.0	mA
Erase count <sup>Note 1</sup> (per 1 block)	N <sub>ERASE</sub>	T <sub>A</sub> = -40 to +85°C	1000			Times
Chip erase time	T <sub>CERASE</sub>	T <sub>A</sub> = -10 to +85°C, N <sub>ERASE</sub> ≤ 100	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		0.8	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		1.0	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		1.2	s
		T <sub>A</sub> = -10 to +85°C, N <sub>ERASE</sub> ≤ 1000	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		4.8	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		5.2	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		6.1	s
		T <sub>A</sub> = -40 to +85°C, N <sub>ERASE</sub> ≤ 100	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		1.6	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		1.8	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		2.0	s
		T <sub>A</sub> = -40 to +85°C, N <sub>ERASE</sub> ≤ 1000	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		9.1	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		10.1	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		12.3	s
Block erase time	T <sub>BERASE</sub>	T <sub>A</sub> = -10 to +85°C, N <sub>ERASE</sub> ≤ 100	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		0.4	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		0.5	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		0.6	s
		T <sub>A</sub> = -10 to +85°C, N <sub>ERASE</sub> ≤ 1000	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		2.6	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		2.8	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		3.3	s
		T <sub>A</sub> = -40 to +85°C, N <sub>ERASE</sub> ≤ 100	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		0.9	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		1.0	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		1.1	s
		T <sub>A</sub> = -40 to +85°C, N <sub>ERASE</sub> ≤ 1000	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		4.9	s
			3.5 V ≤ V <sub>DD</sub> < 4.5 V		5.4	s
			2.7 V ≤ V <sub>DD</sub> < 3.5 V		6.6	s
Byte write time	T <sub>WRITE</sub>	T <sub>A</sub> = -40 to +85°C, N <sub>ERASE</sub> ≤ 1000			150	μs
Internal verify	T <sub>VERIFY</sub>	Per 1 block			6.8	ms
		Per 1 byte			27	μs
Blank check	T <sub>BLKCHK</sub>	Per 1 block			480	μs
Retention years		T <sub>A</sub> = 85°C <sup>Note 2</sup> , N <sub>ERASE</sub> ≤ 1000	10			Years

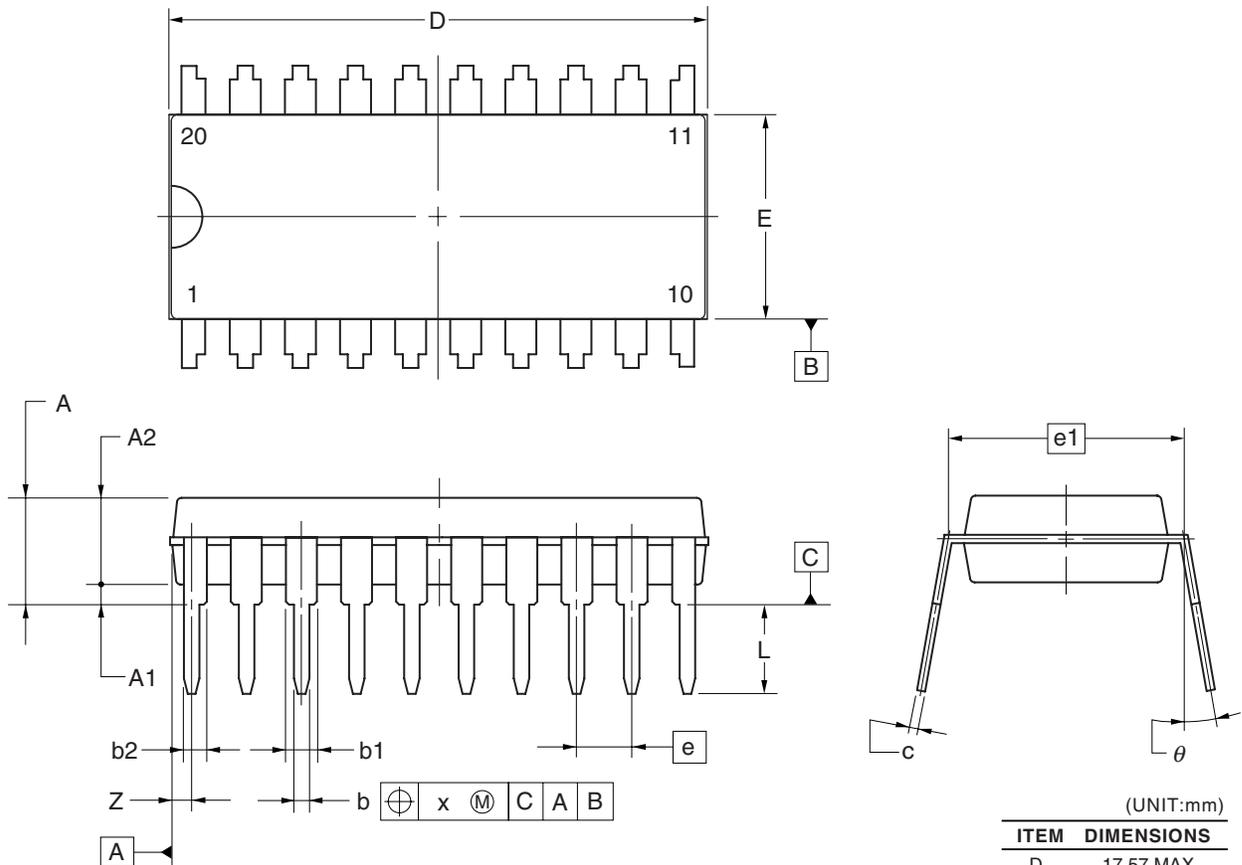
**Notes** 1. Depending on the erasure count (N<sub>ERASE</sub>), the erase time varies. Refer to the chip erase time and block erase time parameters.

2. When the average temperature when operating and not operating is 85°C.

**Remark** When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

3. PACKAGE DRAWING

20-PIN PLASTIC SDIP (7.62mm (300))



(UNIT:mm)

ITEM	DIMENSIONS
D	17.57 MAX.
E	6.60
A	3.70 MAX.
A1	0.65±0.10
A2	2.80
e	1.778
e1	7.62
b	0.52±0.10
b1	1.02±0.10
b2	0.77±0.10
c	0.27±0.07
L	2.86±0.20
x	0.25
θ	0° to 5°
Z	0.609

P20CS-70-CAC

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**APPENDIX A. RELATED DOCUMENTS**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents Related to Devices**

Document Name	Document No.
μPD78F9221CS, 78F9222CS Preliminary Product Information	This manual
78K0S/KA1+ User's Manual	U16898E
78K/0S Series Instructions User's Manual	U11047E

**Documents Related to Development Software Tools (User's Manuals)**

Document Name	Document No.	
RA78K0S Assembler Package	Operation	U16656E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U16654E
	Language	U14872E
ID78K0S-NS Ver. 2.52 Integrated Debugger	Operation	U16584E
ID78K0S-QB Ver. 2.81 Integrated Debugger	Operation	U17287E
PM plus Ver. 5.20		U16934E

**Documents Related to Development Hardware Tools (User's Manuals)**

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
QB-78K0SKX1MINI In-Circuit Emulator	U17272E
QB-78K0SKX1 In-Circuit Emulator	U18219E
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E

**Documents Related to Flash Memory Writing (User's Manuals)**

Document Name	Document No.
PG-FP4 Flash Memory Programmer	U15260E
PG-FPL2 Flash Memory Programmer	U17307E

**Caution** The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

**Other Related Documents**

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	<b>Note</b>
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

**Note** See the “Semiconductor Device Mount Manual” website (<http://www.necel.com/pkg/en/mount/index.html>).

**Caution** The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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