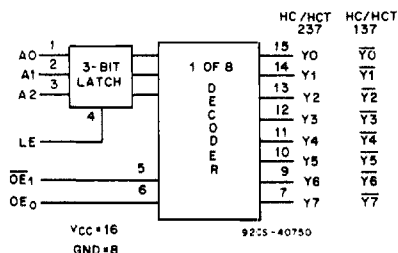


CD54/74HC137, CD54/74HCT137
CD54/74HC237, CD54/74HCT237

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

The RCA-CD54/74HC137, 237 and CD54/74HCT137, 237 are high speed silicon gate CMOS decoders, and are well suited to memory address decoding or data routing applications. Both devices feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

Both circuits have three binary select inputs (A0, A1, and A2) that can be latched by an active High Latch Enable (LE) signal to isolate the outputs from select-input changes. A "Low" LE makes the output transparent to the input and the circuit functions as a one-of-eight decoder. Two Output Enable inputs ($\overline{OE}_1$ and $\overline{OE}_0$) are provided to simplify cascading and to facilitate demultiplexing. The demultiplexing function is accomplished by using the A0, A1, A2 inputs to select the desired output and using one of the Output Enable inputs as the data input while holding the other Output Enable input in its active state. In the HC/HCT137 the selected output is a "Low"; in the HC/HCT237 the selected output is a "High".

The CD54HC137, 237 and CD54/74HCT137, 237 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC137, 237 and CD74HCT137, 237 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both types are also available in chip form (H suffix).

3-to-8 Line Decoder/Demultiplexer With Address Latches

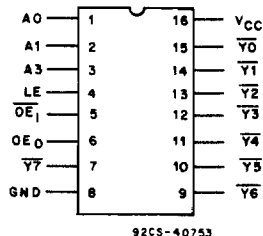
HC/HCT137 - Inverting
HC/HCT237 - Non-Inverting

Type Features:

- Select one of eight data outputs (active LOW for 137, active HIGH for 237)
- I/O port or memory selector
- 2 Enable inputs to simplify cascading
- Typical propagation delay of 13 ns @ $V_{CC} = 5\text{ V}$, 15 pF, $T_A = +25^\circ\text{C}$ (HC237)

Family Features:

- **Fanout (Over Temperature Range):**
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- **Wide Operating Temperature/Range:**
CD74HC/HCT: -40 to +85°C
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **Alternate Source is Phillips/Signetics**
- **CD54HC/CD74HC Types:**
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5$ V
- **CD54HCT/CD74HCT Types:**
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}



**TERMINAL ASSIGNMENT FOR HC/HCT137
FOR HC/HCT237 ALL Y's ARE Y's**



TRUTH TABLE
CD54/74HC137, CD54/74HCT137

H = High Level, L = Low Level, X = Don't Care.

CD54/74HC137, CD54/74HCT137
CD54/74HC237, CD54/74HCT237

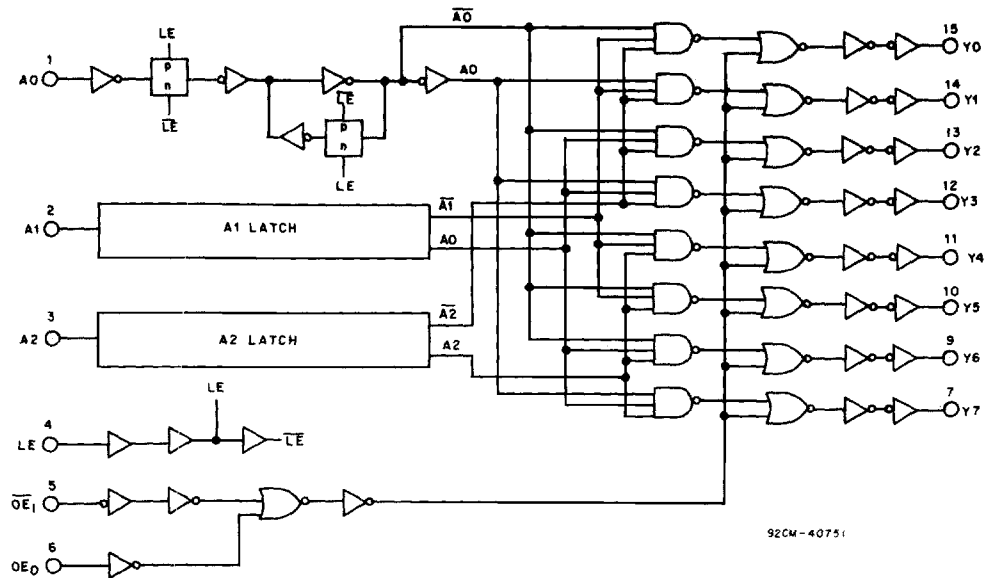


Fig. 2 - Logic diagram for HC/HCT237.

TRUTH TABLE
CD54/74HC237, CD54/74HCT237

INPUTS						OUTPUTS							
LE	OE ₀	OE ₁	A ₂	A ₁	A ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	H	L	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	*							

* Depends upon the address previously applied while LE was at a logic low.

H = High Level, L = Low Level, X = Don't Care.

CD54/74HC137, CD54/74HCT137

CD54/74HC237, CD54/74HCT237

MAXIMUM RATINGS, Absolute-Maximum Values:**DC SUPPLY-VOLTAGE, (V_{CC}):**

(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ± 20 mADC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ± 20 mADC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ± 25 mADC V_{CC} OR GROUND CURRENT (I_{CC}) ± 50 mA**POWER DISSIPATION PER PACKAGE (P_D):**For $T_A = -40$ to $+80^\circ\text{C}$ (PACKAGE TYPE E) 500 mWFor $T_A = +80$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mWFor $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H) 500 mWFor $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mWFor $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) 400 mWFor $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW**OPERATING-TEMPERATURE RANGE (T_A):**PACKAGE TYPE F, H -55 to $+125^\circ\text{C}$ PACKAGE TYPE E, M -40 to $+85^\circ\text{C}$ STORAGE TEMPERATURE (T_{STG}) -65 to $+150^\circ\text{C}$ **LEAD TEMPERATURE (DURING SOLDERING):**At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$ Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only $+300^\circ\text{C}$ **RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC} : *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_{in} , V_{out}	0	V_{CC}	V
Operating Temperature, T_A :			
CD74 Types	-40	$+85$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Times, t_r , t_f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC137, CD54/74HCT137

CD54/74HC237, CD54/74HCT237

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC137/237, CD54HC137/237										CD74HCT137/237, CD54HCT137/237										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V _I V	I _O mA	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V _I V	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	Min	
High-Level Input Voltage	V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—	—	to 5.5	—	—	—	—	—	—	—	
				6	4.2	—	—	4.2	—	4.2	—	—									
Low-Level Input Voltage	V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	—	—	0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35	—	to 5.5	—	—	—	—	—	—	—	
				6	—	—	1.8	—	1.8	—	1.8	—									
High-Level Output Voltage	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
CMOS Loads				4.5	4.4	—	—	4.4	—	4.4	—										
				6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V _{IL} or V _{IH}			2	—	—	—	—	—	—	—	V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
				-4	4.5	3.98	—	—	3.84	—	3.7	—									
				-5.2	6	5.48	—	—	5.34	—	5.2	—									
Low-Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
CMOS Loads				4.5	—	—	0.1	—	0.1	—	0.1										
				6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V _{IL} or V _{IH}			2	—	—	—	—	—	—	—	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
				4	4.5	—	—	0.26	—	0.33	—	0.4									
				5.2	6	—	—	0.26	—	0.33	—	0.4									
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load	ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All	1.5

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

CD54/74HC137, CD54/74HCT137

CD54/74HC237, CD54/74HCT237

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC		TYPICAL VALUES				UNITS
		137		237		
		HC	HCT	HC	HCT	
Propagation Delay, Address to Output Y (C _L = 15pF) (Fig. 3)	t _{PLH}	15	16	13	16	ns
	t _{PHL}					
Power Dissipation Capacitance *	* C _{PD}	19	19	23	23	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$PD = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	V _{CC}	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CD54/74HC137, CD54/74HCT137														
A _n to LE	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
Setup	4.5	10	—	10	—	13	—	13	—	15	—	15	—	
Time t _{su}	6	9	—	—	—	11	—	—	—	13	—	—	—	
A _n to LE	2	30	—	—	—	40	—	—	—	45	—	—	—	ns
Hold	4.5	6	—	7	—	8	—	9	—	9	—	11	—	
Time t _H	6	5	—	—	—	7	—	—	—	8	—	—	—	
LE Pulse	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
Width t _w	4.5	10	—	10	—	13	—	13	—	15	—	15	—	
	6	9	—	—	—	11	—	—	—	13	—	—	—	
CD54/74HC237, CD54/74HCT237														
A _n to LE	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
Setup	4.5	10	—	10	—	13	—	13	—	15	—	15	—	
Time t _{su}	6	9	—	—	—	11	—	—	—	13	—	—	—	
A _n to LE	2	30	—	—	—	40	—	—	—	45	—	—	—	ns
Hold	4.5	6	—	5	—	8	—	5	—	9	—	5	—	
Time t _H	6	5	—	—	—	7	—	—	—	8	—	—	—	
LE Pulse	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
Width t _w	4.5	10	—	10	—	13	—	13	—	15	—	15	—	
	6	9	—	—	—	11	—	—	—	13	—	—	—	

CD54/74HC137, CD54/74HCT137 **CD54/74HC237, CD54/74HCT237**

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

CHARACTERISTIC	V _{CC}	LIMITS												UNITS	
		25°C				-40°C to +85°C				-55°C to +125°C					
		HC		HCT		74HC		74HCT		54HC		54HCT			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Propagation Delay t _{PLH} , t _{PHL}															
CD54/74HC137, CD54/74HCT137	A _n to any $\overline{Y}$	2	—	180	—	—	—	225	—	—	—	270	—	—	ns
		4.5	—	36	—	38	—	45	—	48	—	54	—	57	
		6	—	31	—	—	—	38	—	—	—	46	—	—	
OE ₀ to any $\overline{Y}$	2	—	145	—	—	—	180	—	—	—	220	—	—	ns	
	4.5	—	29	—	35	—	36	—	44	—	44	—	53		
	6	—	25	—	—	—	31	—	—	—	38	—	—		
$\overline{OE}_1$ to any $\overline{Y}$	2	—	145	—	—	—	180	—	—	—	220	—	—	ns	
	4.5	—	29	—	37	—	36	—	46	—	44	—	56		
	6	—	25	—	—	—	31	—	—	—	38	—	—		
LE to any $\overline{Y}$	2	—	190	—	—	—	240	—	—	—	285	—	—	ns	
	4.5	—	38	—	44	—	48	—	55	—	57	—	66		
	6	—	32	—	—	—	41	—	—	—	48	—	—		
Propagation Delay t _{PLH} , t _{PHL}															
CD54/74HC237, CD54/74HCT237	A _n to any Y	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
		4.5	—	32	—	38	—	40	—	48	—	48	—	57	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
OE ₀ to any Y	2	—	145	—	—	—	180	—	—	—	220	—	—	ns	
	4.5	—	29	—	33	—	36	—	41	—	44	—	50		
	6	—	25	—	—	—	31	—	—	—	38	—	—		
$\overline{OE}_1$ to any Y	2	—	145	—	—	—	180	—	—	—	220	—	—	ns	
	4.5	—	29	—	35	—	36	—	44	—	44	—	53		
	6	—	25	—	—	—	31	—	—	—	38	—	—		
LE to any Y	2	—	190	—	—	—	240	—	—	—	285	—	—	ns	
	4.5	—	38	—	42	—	48	—	53	—	57	—	63		
	6	—	32	—	—	—	41	—	—	—	48	—	—		
Output Transition Times t _{THL} , t _{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns	
	4.5	—	15	—	15	—	19	—	19	—	22	—	22		
Input Capacitance C _i	6	—	13	—	—	—	16	—	—	—	19	—	—	pF	
	—	—	10	—	10	—	10	—	10	—	10	—	10		

CD54/74HC137, CD54/74HCT137 CD54/74HC237, CD54/74HCT237

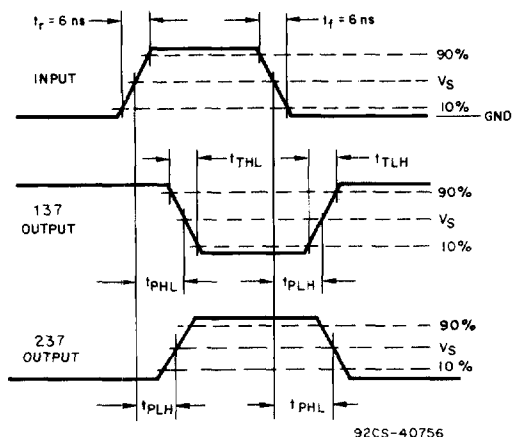


Fig. 3 - Transition times and propagation delay times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

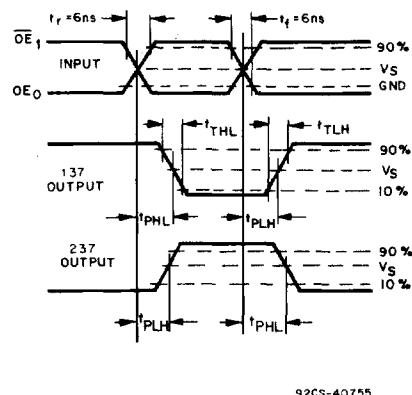


Fig. 4 - Transition times and propagation delay times.

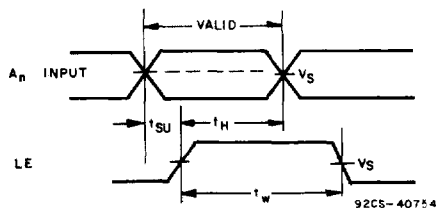


Fig. 5 - Latch enable setup and hold times.