BURR - BROWN®

OPA621

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 2.3nV/$\sqrt{Hz}$
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- HIGH OUTPUT CURRENT: 150mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 500MHz
- STABLE IN GAINS: ≥ 2V/V
- LOW OFFSET VOLTAGE: ±100µV
- SLEW RATE: 500V/µs
- 8-PIN DIP, SOIC PACKAGES

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LINE DRIVER
- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

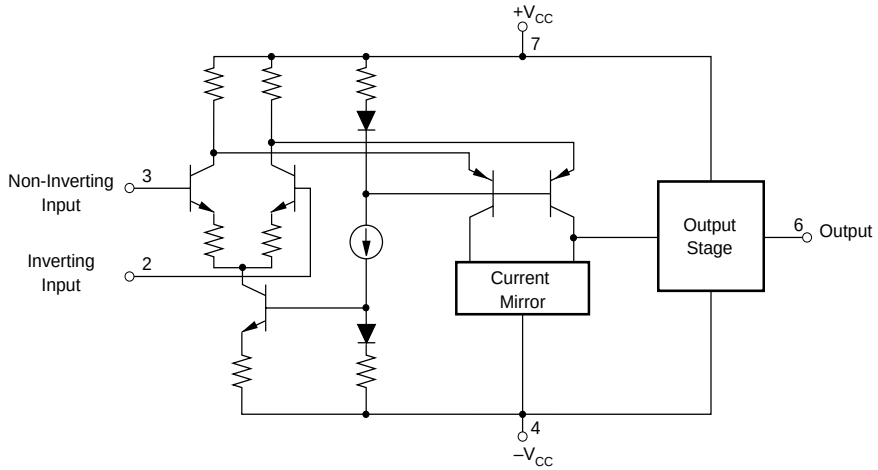
DESCRIPTION

The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of ±2V/V or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in DIP and SO-8 packages.



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SBOS164

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP, KU MIN	OPA621KP, KU TYP	OPA621KP, KU MAX	UNITS
INPUT NOISE					
Voltage: f_O = 100Hz	R_S = 0Ω		10		nV/√Hz
f_O = 1kHz			5.5		nV/√Hz
f_O = 10kHz			3.3		nV/√Hz
f_O = 100kHz			2.5		nV/√Hz
f_O = 1MHz to 100MHz			2.3		nV/√Hz
f_B = 100Hz to 10MHz			8.0		µV, rms
Current: f_O = 10kHz to 100MHz			2.3		pA/√Hz
OFFSET VOLTAGE[1]					
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±12		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	50	60		dB
BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC		18	30	µA
OFFSET CURRENT					
Input Offset Current	V_{CM} = 0VDC		0.2	2	µA
INPUT IMPEDANCE					
Differential	Open-Loop		15 || 1		kΩ || pF
Common-Mode			1 || 1		MΩ || pF
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±3.0	±3.5		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	R_L = 100Ω	50	60		dB
	R_L = 50Ω	48	58		dB
FREQUENCY RESPONSE					
Closed-Loop Bandwidth					
(–3dB)	Gain = +2V/V		500		MHz
	Gain = +5V/V		100		MHz
	Gain = +10V/V		50		MHz
Gain-Bandwidth Product	Gain ≥ +10V/V		500		MHz
Differential Gain	3.58MHz, G = +2V/V		0.05		%
Differential Phase	3.58MHz, G = +2V/V		0.05		Degrees
Harmonic Distortion	G = +2V/V, f = 10MHz, V_O = 2Vp-p				
	f = 10MHz, Second Harmonic		–62	–50	dBc[3]
	Third Harmonic		–80	–70	dBc
Full Power Bandwidth	V_O = 5Vp-p, Gain = +2V/V	22	32		MHz
	V_O = 2Vp-p, Gain = +2V/V	55	80		MHz
Slew Rate	2V Step, Gain = –2V/V	350	500		V/µs
Overshoot	2V Step, Gain = –2V/V		15		%
Settling Time: 0.1%	2V Step, Gain = –2V/V		15		ns
0.01%			25		ns
Phase Margin	Gain = +2V/V		50		Degrees
Rise Time	Gain = +2V/V, 10% to 90%				
	V_O = 100mVp-p; Small Signal		1.8		ns
	V_O = 6Vp-p; Large Signal		8		ns
RATED OUTPUT					
Voltage Output	R_L = 100Ω	±3.0	±3.5		V
	R_L = 50Ω	±2.5	±3.0		V
Output Resistance	1MHz, Gain = +2V/V		0.015		Ω
Load Capacitance Stability	Gain = +2V/V		15		pF
Short Circuit Current	Continuous		±150		mA
POWER SUPPLY					
Rated Voltage	±V_{CC}		5		VDC
Derated Performance	±V_{CC}	4.0		6.0	VDC
Current, Quiescent	I_O = 0mA		26	28	mA
TEMPERATURE RANGE					
Specification: KP, KU	Ambient Temperature	–40		+85	°C
Operating: KP, KU		–40		+85	°C
θ_{JA} KP			100		°C/W
KU			125		°C/W

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

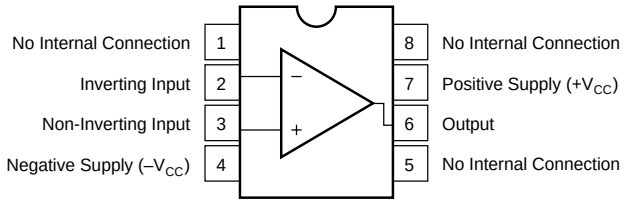
At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP, KU			UNITS
		MIN	TYP	MAX	
TEMPERATURE RANGE					
Specification: KP, KU	Ambient Temperature	–40		+85	°C
OFFSET VOLTAGE(1)					
Average Drift	Full Temperature Range		±12		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	45	60		dB
BIAS CURRENT					
Input Bias Current	Full Temperature, V_{CM} = 0VDC		18	40	µA
OFFSET CURRENT					
Input Offset Current	Full Temperature, V_{CM} = 0VDC		0.2	5	µA
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±2.5	±3.0		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		dB
OPEN LOOP GAIN, DC					
Open-Loop Voltage Gain	R_L = 100Ω	46	60		dB
	R_L = 50Ω	44	58		dB
RATED OUTPUT					
Voltage Output	R_L = 100Ω	±3.0	±3.5		V
	R_L = 50Ω	±2.5	±3.0		V
POWER SUPPLY					
Current, Quiescent	I_O = 0mA		26	30	mA

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is guaranteed by characterization. (3) dBc = dB referred to carrier-input signal.

PIN CONFIGURATION

Top View **DIP/SO-8**



ORDERING INFORMATION

OPA621 ( ) ( )

Basic Model Number

Performance Grade Code
K = –40°C to +85°C

Package Code
P = 8-pin Plastic DIP
U = 8-pin Plastic SO-8

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation(1)	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range KP, KU:	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO-8 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA621KP	8-Pin Plastic DIP	006
OPA621KU	8-Pin SO-8	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

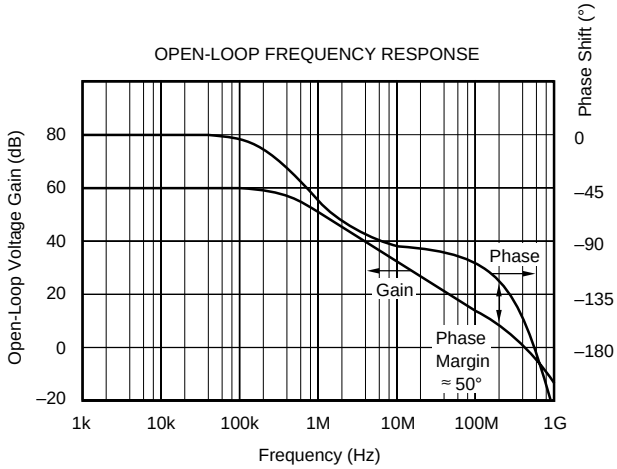
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

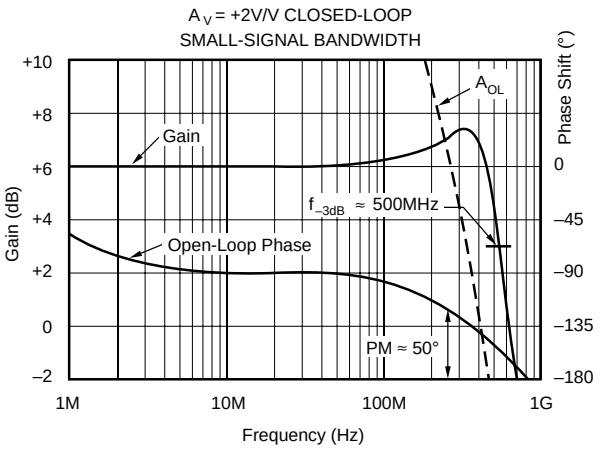
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C, unless otherwise noted.

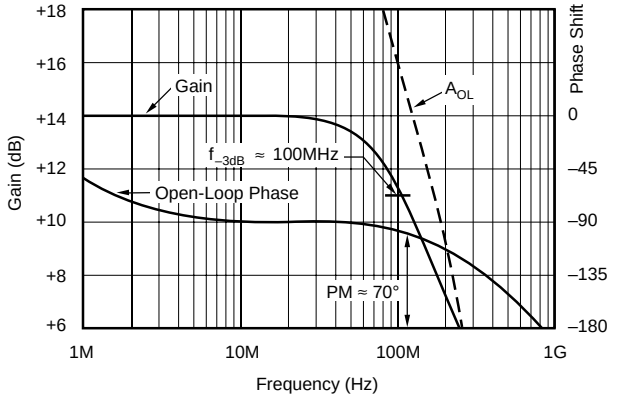
OPEN-LOOP FREQUENCY RESPONSE



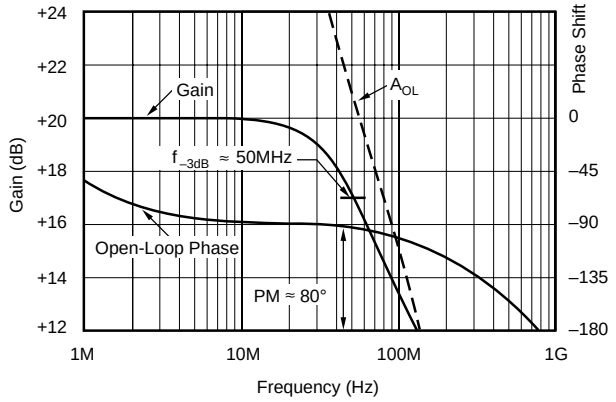
A_V = +2V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



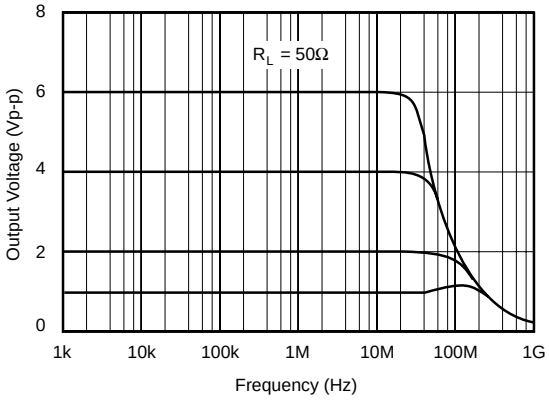
A_V = +5V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



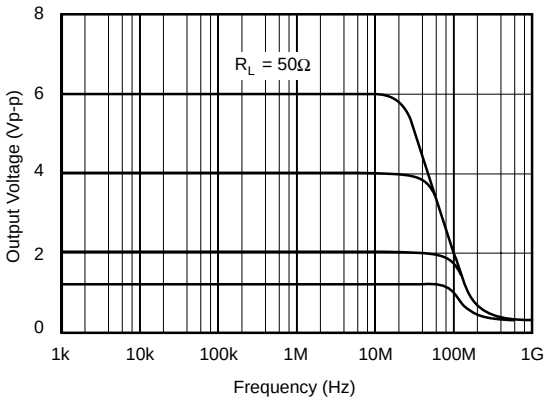
A_V = +10V/V CLOSED-LOOP SMALL-SIGNAL BANDWIDTH



A_V = +2V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



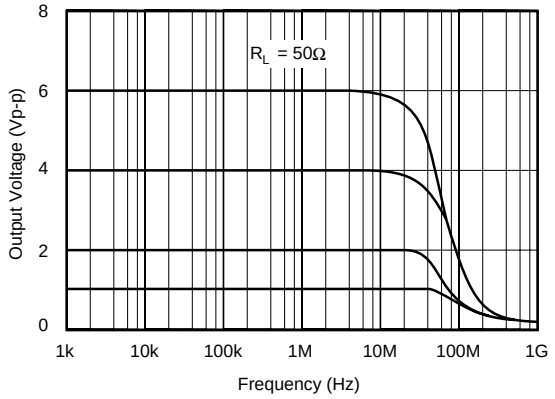
A_V = +5V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



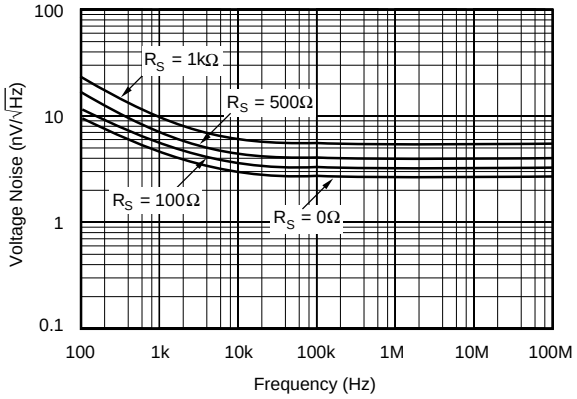
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C, unless otherwise noted.

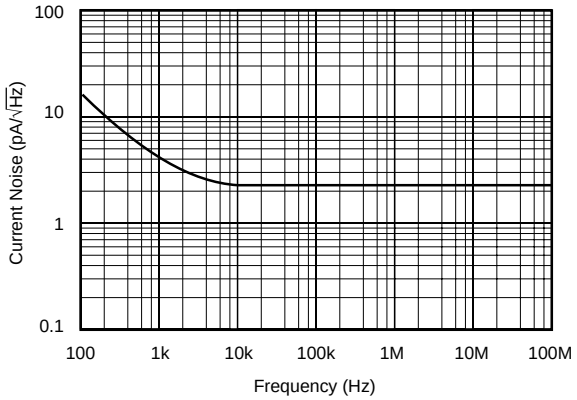
A_V = +10V/V CLOSED-LOOP BANDWIDTH vs OUTPUT VOLTAGE SWING



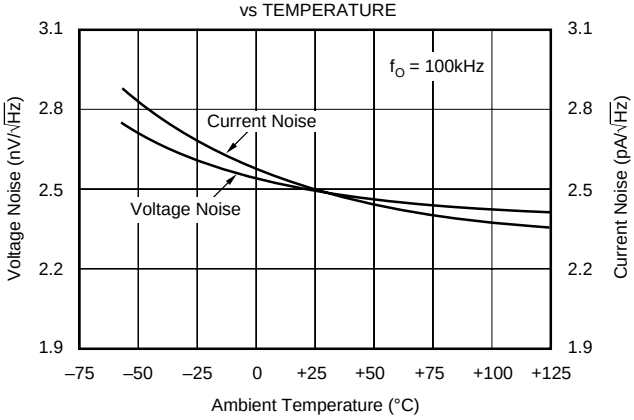
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



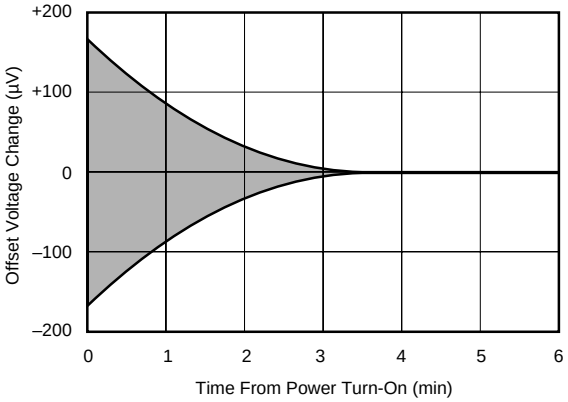
INPUT CURRENT NOISE SPECTRAL DENSITY



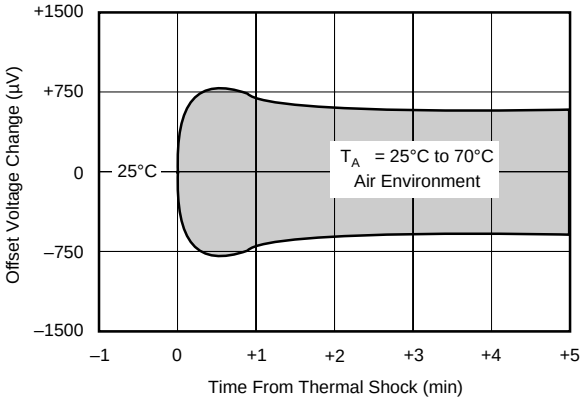
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



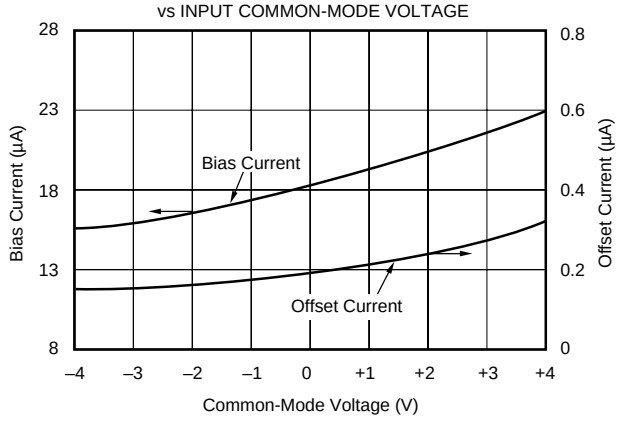
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



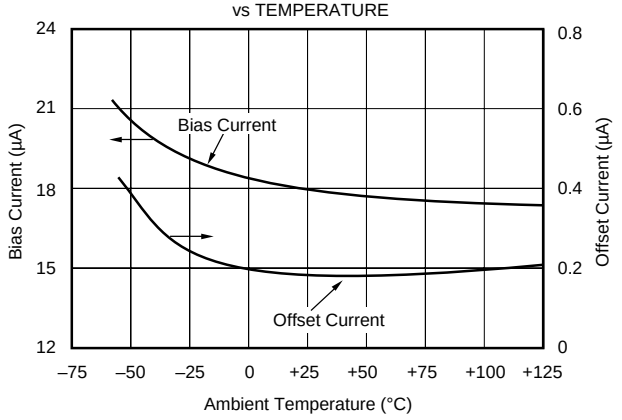
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C, unless otherwise noted.

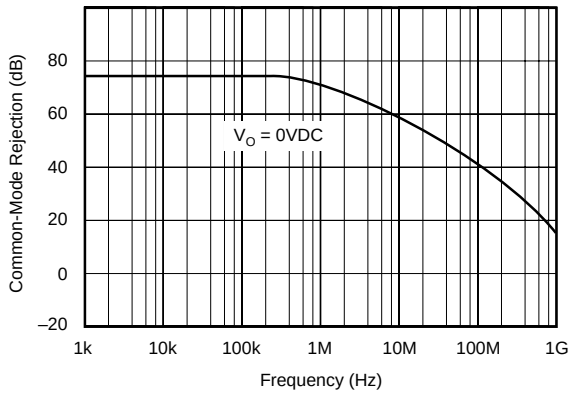
BIAS AND OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



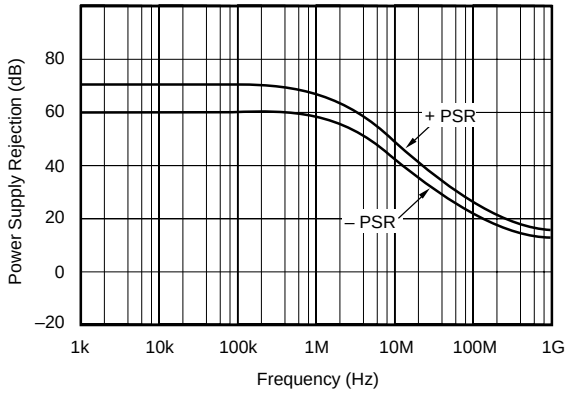
BIAS AND OFFSET CURRENT
vs TEMPERATURE



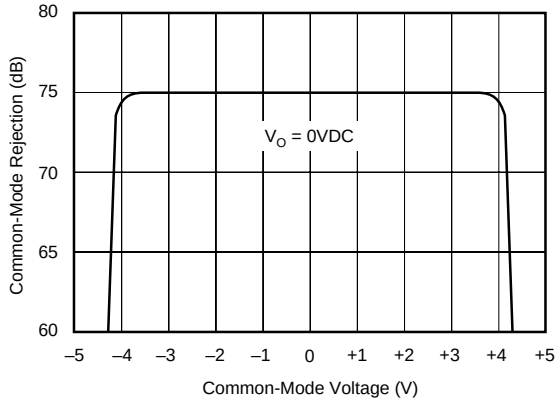
COMMON-MODE REJECTION vs FREQUENCY



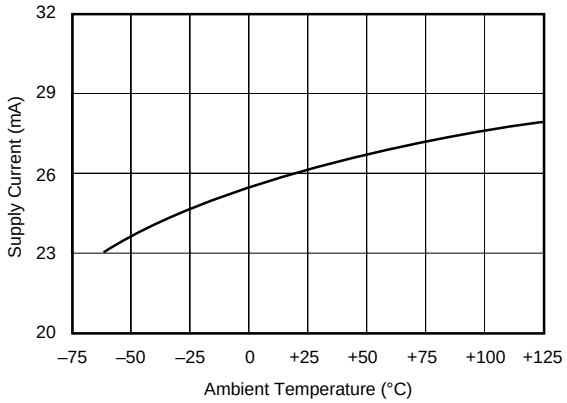
POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



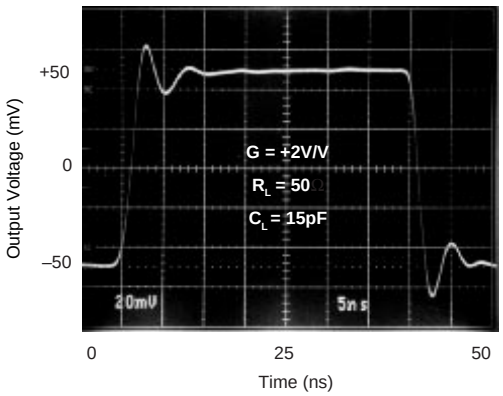
SUPPLY CURRENT vs TEMPERATURE



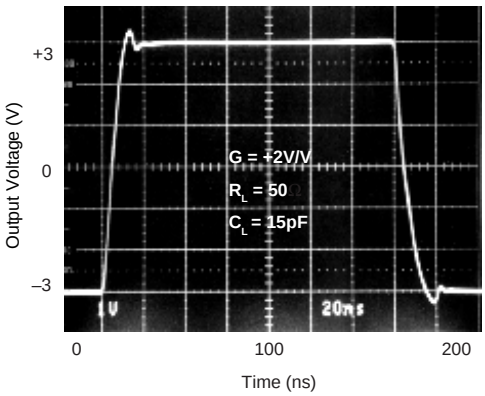
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C, unless otherwise noted.

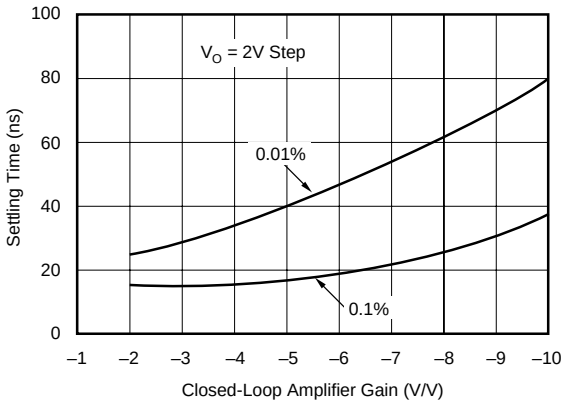
SMALL-SIGNAL TRANSIENT RESPONSE



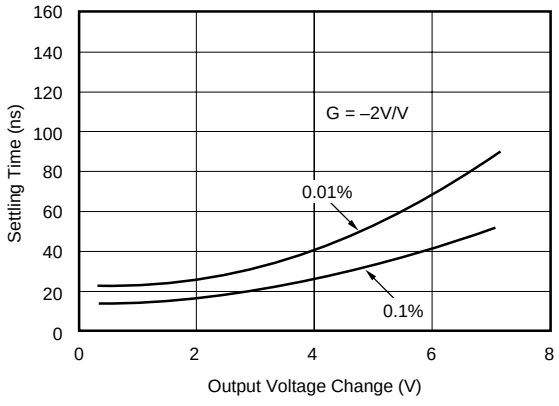
LARGE-SIGNAL TRANSIENT RESPONSE



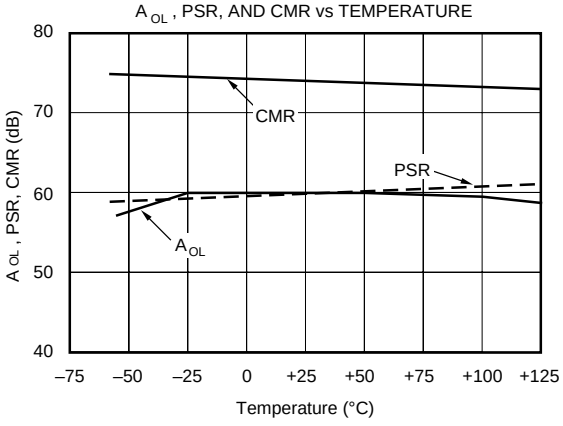
SETTLING TIME vs CLOSED-LOOP GAIN



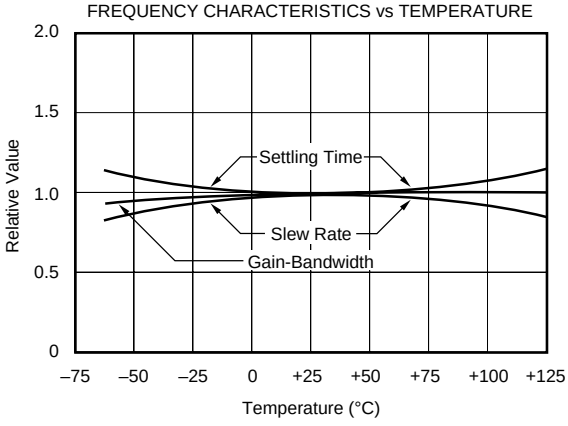
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



A $_{OL}$, PSR, AND CMR vs TEMPERATURE



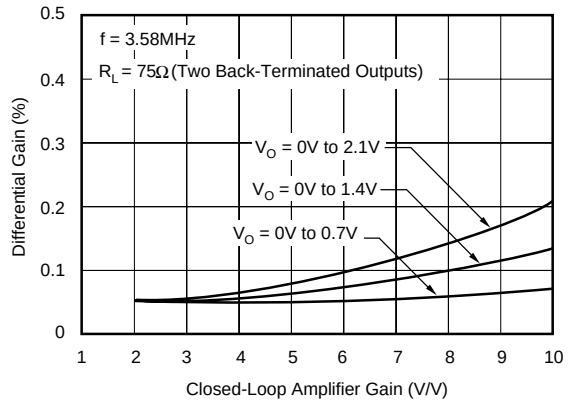
FREQUENCY CHARACTERISTICS vs TEMPERATURE



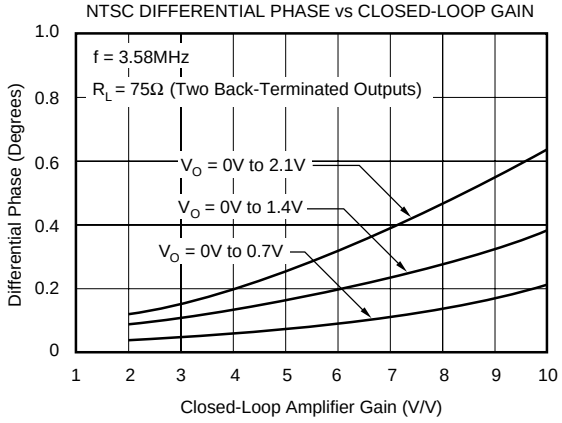
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C, unless otherwise noted.

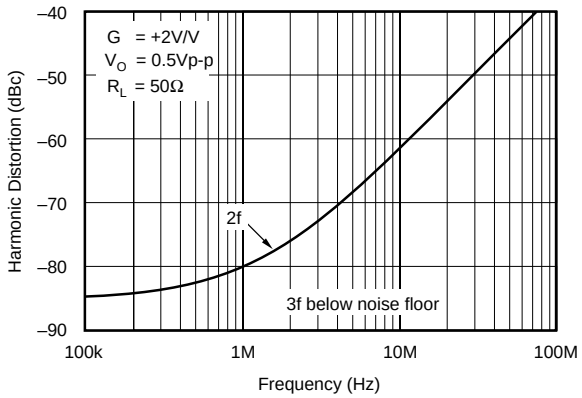
NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



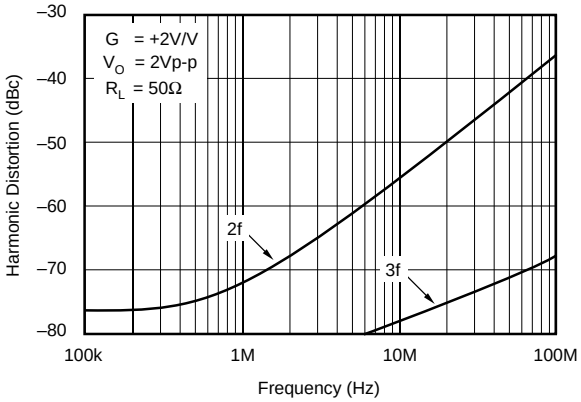
NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



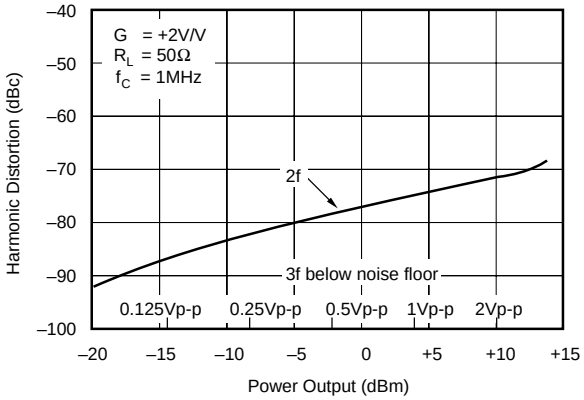
SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



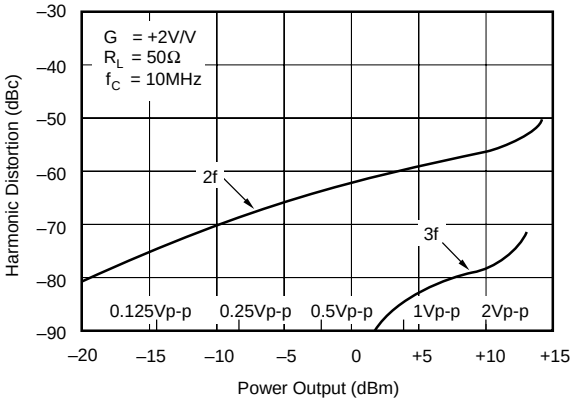
LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



1MHz HARMONIC DISTORTION
vs POWER OUTPUT



10MHz HARMONIC DISTORTION
vs POWER OUTPUT



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA621 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA621's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 microseconds even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA621's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA621. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 500MHz, a 0.01% settling time of 25ns, and an input offset voltage of 200µV.

WIRING PRECAUTIONS

Maximizing the OPA621's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA621, as it is with all high-frequency circuits. Oscillations at frequencies of 500MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must always be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. A parallel 0.1µF ceramic should be added at the supply pins. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA621 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits.

5) Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly

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recommended. Circuits using all surface mount components with the OPA621AU (SO-8 package) will offer the best AC performance. The parasitic package inductance and capacitance for the SO-8 is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA621's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA621's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R3. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

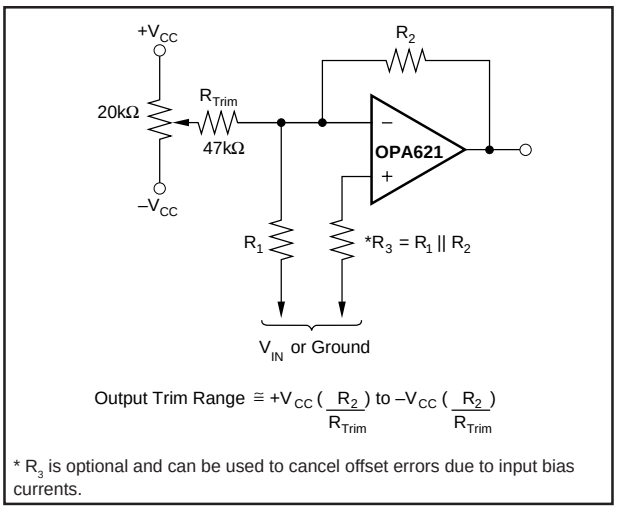

FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA621 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

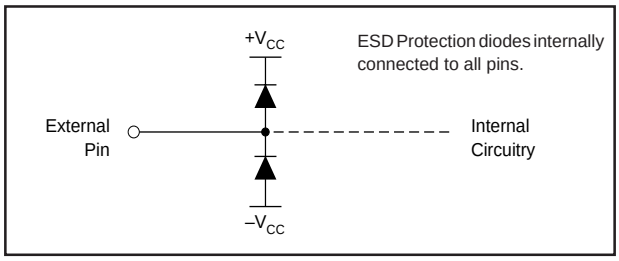

FIGURE 2. Internal ESD Protection.

All pins on the OPA621 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA621.

OUTPUT DRIVE CAPABILITY

The OPA621's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA621 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential

when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA621 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

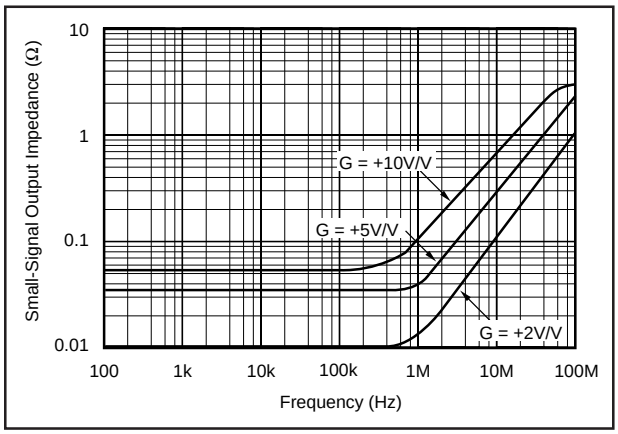

FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA621 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

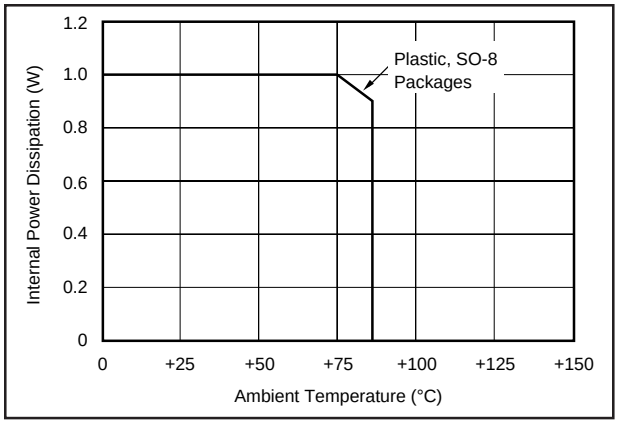

FIGURE 4. Maximum Power Dissipation.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 28mA = 280mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to ground $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 280mW + 750mW = 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

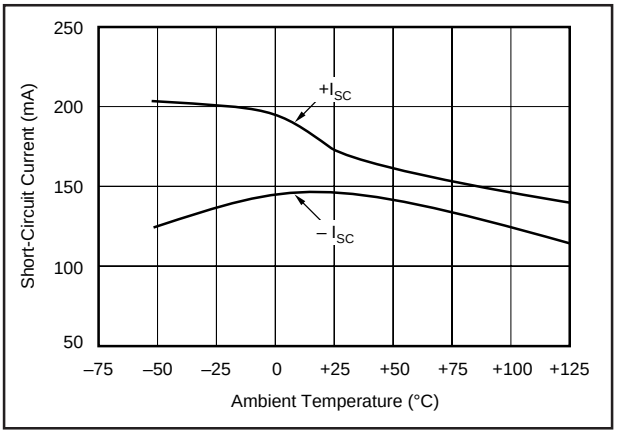

FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA621's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 15pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

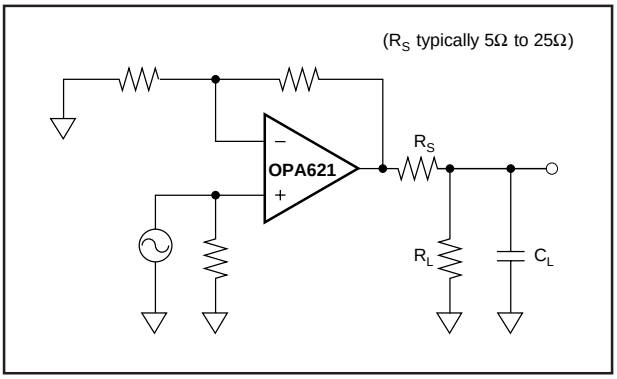

FIGURE 6. Driving Capacitive Loads.

COMPENSATION

The OPA621 is stable in inverting gains of ≥–2V/V and in non-inverting gains ≥+2V/V. Phase margin for both configurations is approximately 50°. Inverting and non-inverting gains of unity should be avoided. The minimum stable gains of +2V/V and –2V/V are the most demanding circuit configurations for loop stability and oscillations are most likely to occur in these gains. If possible, use the device in a noise gain greater than three to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –2V/V is equivalent to a noise gain of 3.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA621 in a good layout is flat with frequency for higher-gain circuits. However, low-gain circuits and configurations where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of two, occurs in only 25ns to 0.01% for a 2V step, making the OPA621 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under “Wiring Precautions.” The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA621 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA621. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional “false-summing junction,” which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope’s built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is

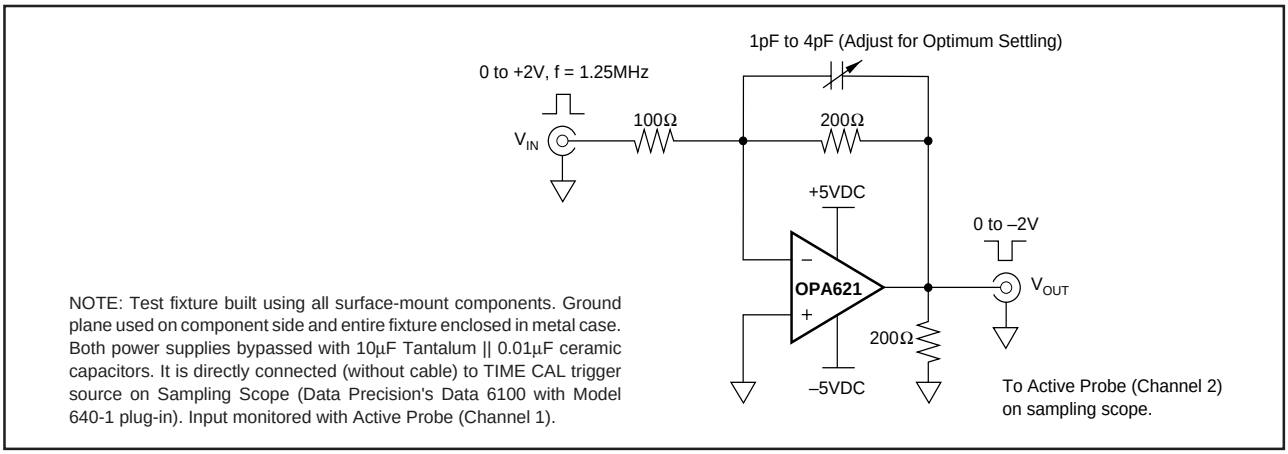

FIGURE 7. Settling Time Test Circuit.

defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA621's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

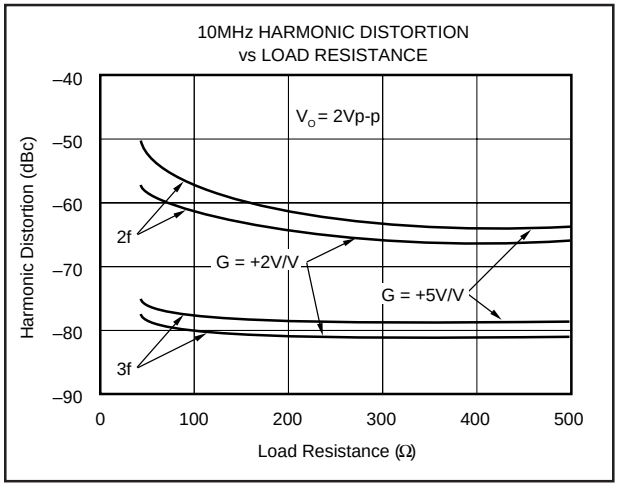

FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA621's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA621 to operate in a gain of +2V/V and drive 2Vp-p (4dBm for each tone) into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +47dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(OPI^3P - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

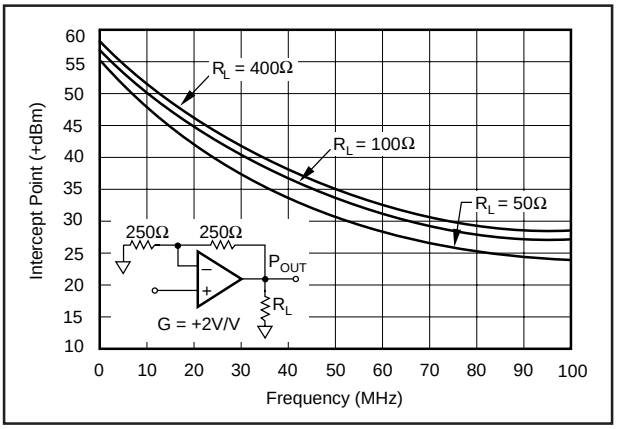

FIGURE 9. Two-Tone Third-Order Intermodulation Intercept vs Frequency.

For this case OPI^3P = 47dBm, P_O = 4dBm, and the third-order IMD = 2(47 – 4) = 86dB below either 4dBm tone. The OPA621's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

NOISE FIGURE

The OPA621's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA621's Noise Figure vs Source Resistance is shown in Figure 10.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model using MicroSim Corporation's PSpice is available for the OPA621. This simulation model is available through the Burr-Brown web site at www.burr-brown.com or by calling the Burr-Brown Applications Department.

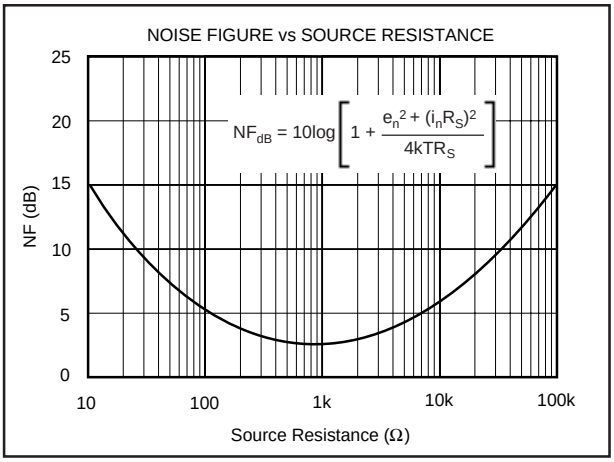

FIGURE 10. Noise Figure vs Source Resistance.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA621. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: DIP = 5.02E+7 Hours, and SO-8 = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24 hrs
Temperature Cycling	Temperature = –55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Hermetic Seal	Fine: He leak rate < 1 X 10 atm cc/s Gross: per Fluorocarbon bubble test
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on SG package only.

DEMONSTRATION BOARDS

Demonstration boards are available to speed protyping. The 8-pin DIP packaged parts may be evaluated using the DEM-OPA65XP board while the SO-8 packaged part may be evaluated using the DEM-OPA65XU board. Both of these boards come partially assembled from your local distributor (the external resistors or the amplifier is not included).

APPLICATIONS

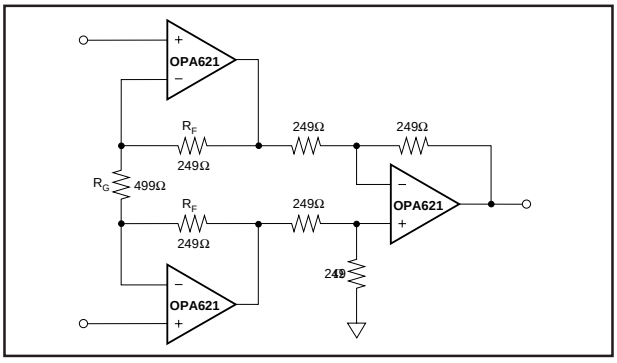

FIGURE 11. Unity Gain Difference Amplifier.

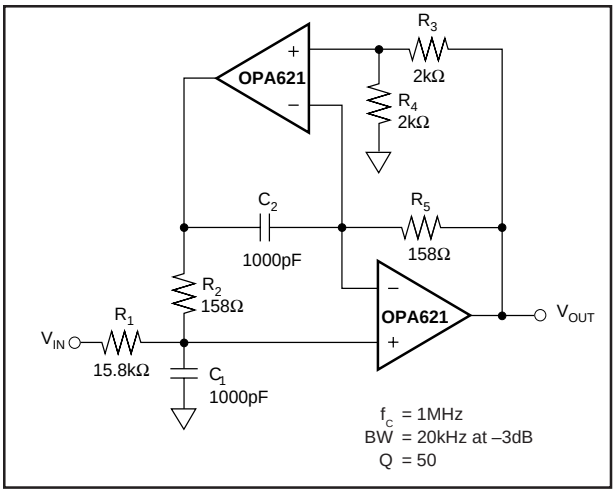

FIGURE 12. High-Q 1MHz Bandpass Filter

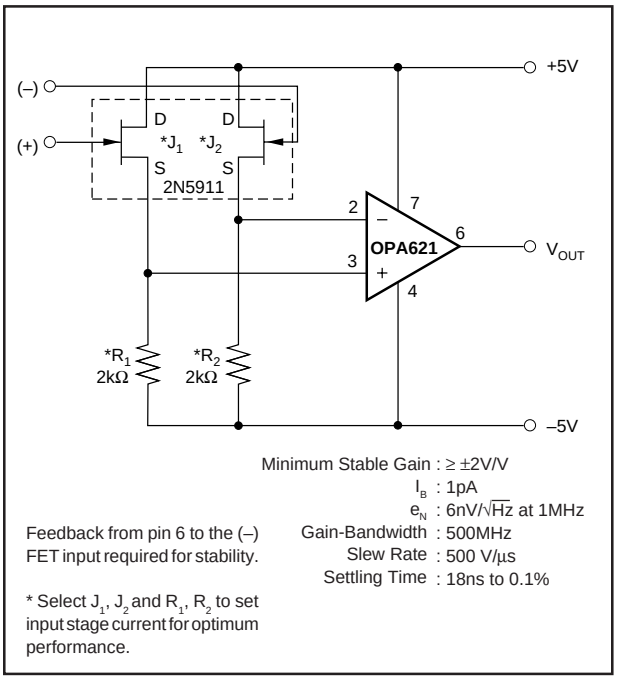

FIGURE 13. Low Noise, Wideband FET Input Op Amp.

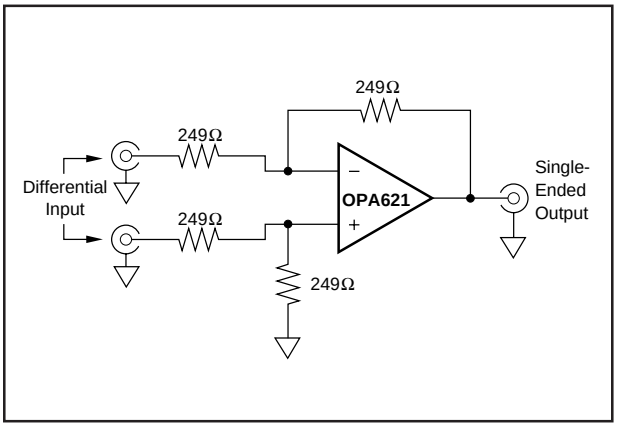

FIGURE 14. Differential Input Buffer Amplifier (G = –2V/V).

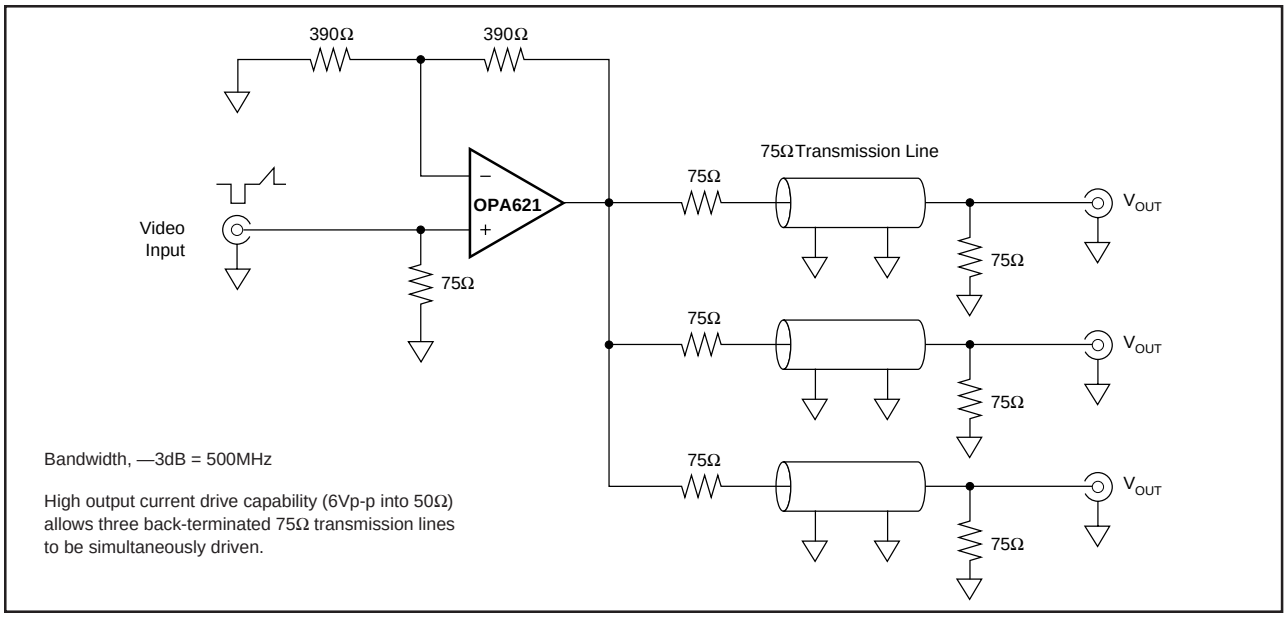

FIGURE 15. Video Distribution Amplifier.

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