T-46-13-47

PAL20R8 Family

20L8, 20R8 20R6, 20R4

Features/Benefits

- **Standard 24-pin architectures**
- **TTL and CMOS versions**
- **High speed, as fast as 15 ns tPD for PAL20R8B Series**
- **Low power, as low as zero standby for PALC20R8Z Series**
- **Security fuse/cell on all devices**

Description

The PAL20R8 Series consists of four devices, each with twenty array inputs and eight outputs. The devices have either 0, 4, 6, or 8 registered outputs, with the remaining being combinatorial.

The PAL device transfer function is the familiar Boolean sum of products. The PAL device consists of a programmable AND array driving a fixed OR array. Product terms with all bits programmed (disconnected) assume the logical high state, and product terms with both true and complement of any signal connected assume the logical low state.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The combinatorial device has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied directly to VCC or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with programmable three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any combination of device inputs or output feedback. The output provides a bidirectional I/O pin in the combinatorial configuration, and may be configured as a dedicated input if the buffer is always disabled.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops which are loaded on the low-to-high transition of the clock input.

Polarity

All outputs are active low.

Performance

Several speed/power versions are available.

SUFFIX	t_{PD} (ns)	I_{CC} (mA)
B	15	210
B-2	25	105
A	25	210
A-2	35	105
Z-35	35	0.1
Z-45	45	0.1

Preload and Power-Up Reset

The B-2 and CMOS Series offer register preload for device testability. The registers can be preloaded from the outputs by using super-voltages (see waveforms at end of section) in order to simplify functional testing. The B-2 Series also offers Power-Up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

Packages

The commercial PAL20R8 Series is available in the plastic SKINNYDIP (NS) and ceramic SKINNYDIP (JS) packages. The PAL20R8B/A/A-2 Series is available in the plastic leaded chip carrier with no-connects on 4, 8, 11, and 19 (NL), while the PAL20R8B-2/Z-35/Z-45 Series is available in the plastic leaded chip carrier with no-connects on 1, 8, 15, and 22 (FN). The PALC20R8Z-35/45 Series is also available in the ceramic windowed SKINNYDIP (QS) package.

Package Drawings

(refer to PAL Device Package Outlines, page 3-179)

PAL20R8 Series

DEVICE	DEDICATED INPUTS	OUTPUTS	
		COMBINATORIAL	REGISTERED
PAL20L8	12	8 (6 I/O)	0
PAL20R8	10	0	8
PAL20R6	10	2 I/O	6
PAL20R4	10	4 I/O	4

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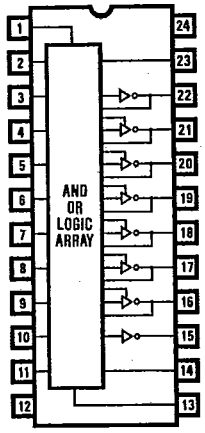
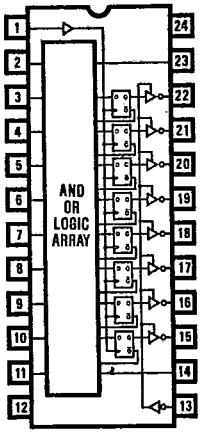
DIP Pinouts

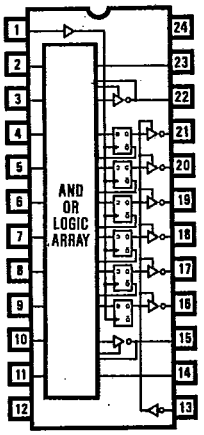
20L8A/A-2/B/B-2/Z-35/Z-45



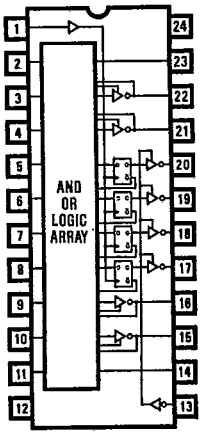
20R8A/A-2/B/B-2/Z-35/Z-45



20R6A/A-2/B/B-2/Z-35/Z-45

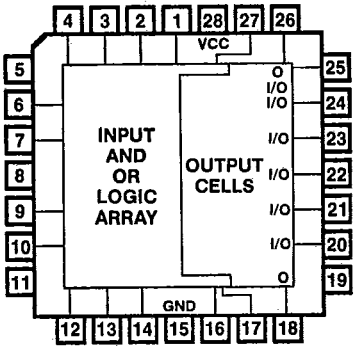


20R4A/A-2/B/B-2/Z-35/Z-45

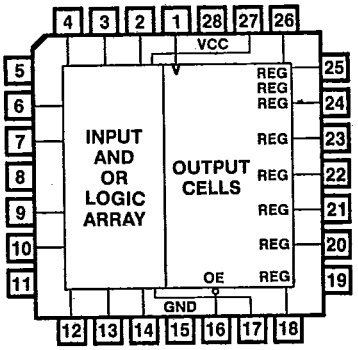


PLCC Pinouts (NL)

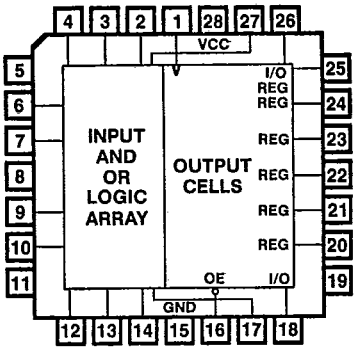
20L8A/A-2/B



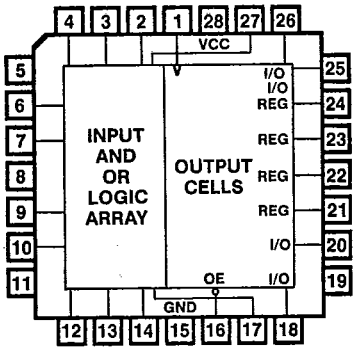
20R8A/A-2/B



20R6A/A-2/B



20R4A/A-2/B



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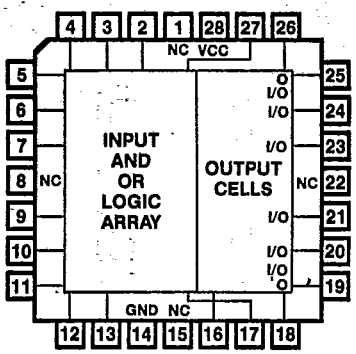
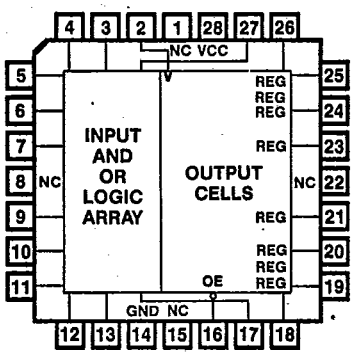
PLCC Pinouts (FN)

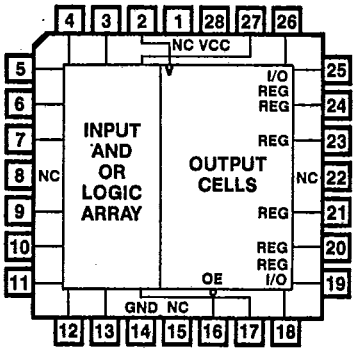
PAL20L8B-2/Z-35/Z-45



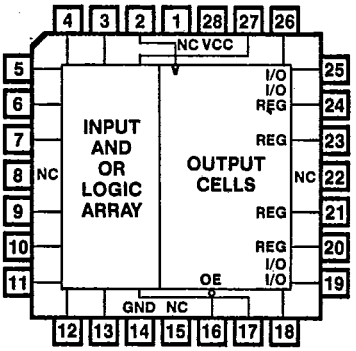
PAL20R8B-2/Z-35/Z-45



PAL20R6B-2/Z-35/Z-45



PAL20R4B-2/Z-35/Z-45



Ordering Information — Newer Products

PALC20R8Z-35 C QS STD

- PROGRAMMABLE ARRAY LOGIC
- TECHNOLOGY: None = Bipolar; C = CMOS
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE: R = Registered; L = Active Low Combinatorial
- NUMBER OF OUTPUTS
- POWER: None = Standard; Z = Zero Standby Power
- SPEED (tPD)
- OPERATING CONDITIONS: C = Commercial; I = Industrial (CMOS Only)
- PACKAGE: NS = Plastic SKINNYDIP; JS = Ceramic SKINNYDIP; QS = Windowed SKINNYDIP (CMOS Only); FN = Plastic Leaded Chip Carrier; SG = Small-Outline Gull-wing
- PROCESSING: STD = Standard; XXXX = Other

Ordering Information — Older Products

PAL20R8B-2 C NS STD

- PROGRAMMABLE ARRAY LOGIC
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE: R = Registered; L = Active Low Combinatorial
- NUMBER OF OUTPUTS
- SPEED: A = High Speed; B = Very High Speed
- POWER: None = Standard; -2 = Half Power
- OPERATING CONDITIONS: C = Commercial
- PACKAGE: NS = Plastic DIP; JS = Ceramic DIP; NL = Plastic Leaded Chip Carrier; FN = Plastic Leaded Chip Carrier (with Center No-connects) (PAL20R8B-2 Series Only); SG = Small-Outline Gull-wing
- PROCESSING: STD = Standard; XXXX = Other

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature		-65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	10	6		ns
		High	12	8		
t_{su}	Set up time from input or feedback to clock	20R8B, 20R6B, 20R4B	15	10		ns
t_h	Hold time		0	-10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -3.2 mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}[3]			V_O = 2.4 V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX			140	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output		20L8B, 20R6B, 20R4B	R_1 = 200 Ω, R_2 = 390 Ω		12	15	ns
t_{CLK}	Clock to output or feedback except 20L8B					8	12	ns
t_{PZX}	Pin 13 to output enable except 20L8B					10	15	ns
t_{PXZ}	Pin 13 to output disable except 20L8B					8	12	ns
t_{EA}	Input to output enable		20L8B, 20R6B, 20R4B			12	18	ns
t_{ER}	Input to output disable		20L8B, 20R6B, 20R4B			12	15	ns
f_{MAX}	Maximum frequency	External	20R8B, 20R6B, 20R4B		37	40		MHz
		No feedback			45	50		

1. The PAL20R8B Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 V to 7.0 V	−0.5 V to 12.0 V
Input voltage	−1.5 V to 5.5 V	−1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature		−65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low	*20R8B-2, 20R6B-2, 20R4B-2	15	10		ns
		High		15	10		
t_{su}	Setup time from input or feedback to clock			25	15		ns
t_h	Hold time			0	−10		ns
T_A	Operating free-air temperature			0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2 mA	2.4	3.4		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			−100	μA
I_{OZH}[3]			V_O = 2.4 V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			80	105	mA
C_{IN}	Input capacitance	V_{IN} = 2.0 V at f = 1 MHz			6		pF
C_{OUT}	Output capacitance	V_{OUT} = 2.0 V at f = 1 MHz			9		pF

Notes: 1. The PAL20R8B-2 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL[1] MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 20L8B-2, 20R6B-2, 20R4B-2		$R_1 = 200\,\Omega$ $R_2 = 390\,\Omega$		15	25	ns
t_{CLK}	Clock to output or feedback	20R8B-2, 20R6B-2, 20R4B-2			10	15	ns
t_{PZX}	Pin 13 to output enable				10	20	ns
t_{PXZ}	Pin 13 to output disable				11	20	ns
t_{EA}	Input to output enable	20L8B-2, 20R6B-2, 20R4B-2			10	25	ns
t_{ER}	Input to output disable				13	25	ns
f_{MAX}	Maximum frequency 20R8B-2, 20R6B-2, 20R4B-2	External		25	30		MHz
		Internal		28.5	35		
		No feedback		33.3	40		

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	15	7		ns
		High	15	7		
t_{su}	Set up time from input or feedback to clock	20R8A, 20R6A, 20R4A	25	15		ns
t_h	Hold time		0	-10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage					0.8	V
V_{IH}[1]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -3.2 mA	2.4	2.8		V
I_{OZL}[2]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}[2]			V_O = 2.4 V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-30	-90	-130	mA
I_{CC}	Supply current	V_{CC} = MAX			160	210	mA

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output		20L8A, 20R6A, 20R4A	$R_1 = 200\ \Omega$ $R_2 = 390\ \Omega$		15	25	ns
t_{CLK}	Clock to output or feedback					10	15	ns
t_{CF}	Clock to feedback					8	10	ns
t_{PZX}	Pin 13 to output enable except 20L8A					10	20	ns
t_{PXZ}	Pin 13 to output disable except 20L8A					11	20	ns
t_{EA}	Input to output enable		20L8A, 20R6A, 20R4A			10	25	ns
t_{ER}	Input to output disable		20L8A, 20R6A, 20R4A			13	25	ns
f_{MAX}	Maximum frequency	External	20R8A, 20R6A, 20R4A		25	40		MHz
		Internal			28.5	43		
		No feedback			33	71		

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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12.0 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 22.0 V
Off-state output voltage	5.5 V	12.0 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	10		ns
		High	25	10		
t_{su}	Set up time from input or feedback to clock	20R8A-2, 20R6A-2, 20R4A-2	35	25		ns
t_h	Hold time		0	-15		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

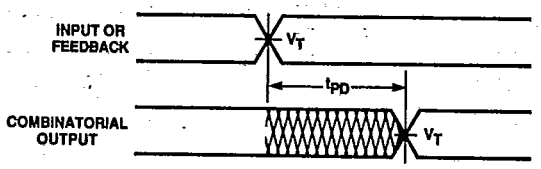
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA		-0.8	-1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4 V		-0.02	-0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24 mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -3.2 mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4 V			-100	μA
I_{OZH}[3]			V_O = 2.4 V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX			80	105	mA

1. The PAL20R8A-2 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

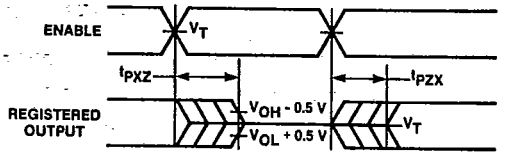
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output		20L8A-2, 20R6A-2, 20R4A-2	Commercial $R_1 = 200\,\Omega$ $R_2 = 390\,\Omega$		25	35	ns
t_{CLK}	Clock to output or feedback except 20L8A-2					15	25	ns
t_{PZX}	Pin 13 to output enable except 20L8A-2					15	25	ns
t_{PXZ}	Pin 13 to output disable except 20L8A-2					15	25	ns
t_{EA}	Input to output enable		20L8A-2, 20R6A-2, 20R4A-2			25	35	ns
t_{ER}	Input to output disable		20L8A-2, 20R6A-2, 20R4A-2			25	35	ns
f_{MAX}	Maximum frequency	External	20R8A-2, 20R6A-2, 20R4A-2		16	25		MHz
		No feedback			20	50		

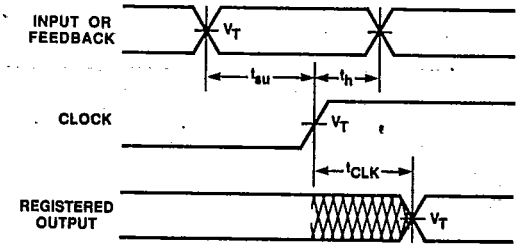
Switching Waveforms



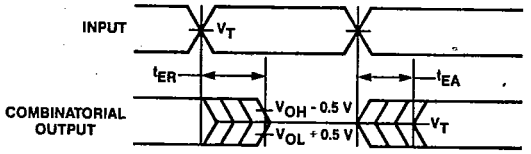
Combinatorial Output



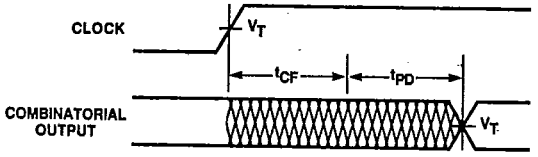
Pin 13 to Output Disable/Enable



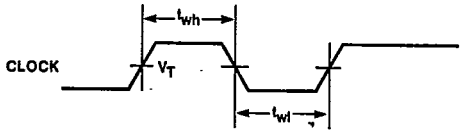
Registered Output



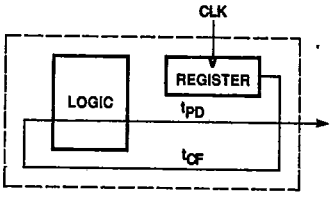
Input to Output Disable/Enable



Clock to Feedback to Combinatorial Output (See Path Below)

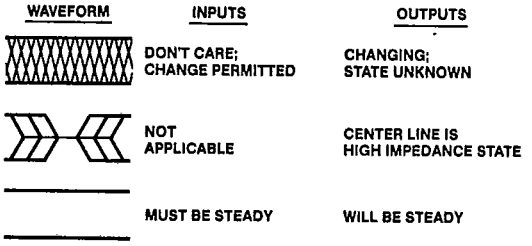


Clock Width



Notes:
1. VT = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2-5 ns typical

Key to Timing Diagrams



Switching Test Load
(refer to page 5-164)

Programmers/Development Systems
(refer to Programmer Reference Guide, page 3-81)

Register Preload Waveform
(refer to page 5-164)

Power-Up Reset Waveform
(refer to page 5-164)

Schematic of Inputs and Outputs
(refer to page 5-164)

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
DC input voltage, V_I ..... -0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... -0.5 V to V_{CC} +0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I<0 ..... -20 mA
V_I>V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O<0 ..... -20 mA
V_O>V_{CC} ..... +20 mA
Storage temperature ..... -65°C to 150°C
Static discharge voltage ..... >2001 V
Latchup current ..... >100 mA

Operating Conditions

SYMBOL	PARAMETER		INDUSTRIAL[1] -50 MIN	TYP	MAX	INDUSTRIAL[1] -40 MIN	TYP	MAX	COMMERCIAL -45 MIN	TYP	MAX	COMMERCIAL -35 MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
t_w	Width of clock	20R8 20R6 20R4	15	10		15	10		15	10		15	10		ns
t_{su}	Setup time from input or feedback to clock		45	30		35	25		40	30		30	25		ns
t_h	Hold time		0	-15		0	-15		0	-15		0	-15		ns
T_A	Operating free-air temperature		-40	25	85	-40	25	85	0	25	75	0	25	75	°C

Electrical Characteristics Over Operating Conditions

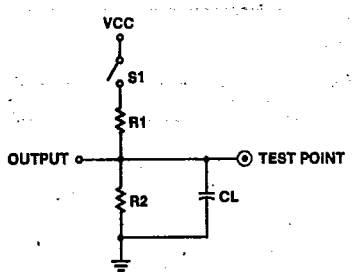
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage			0		0.8	V
V_{IH}[2]	High-level input voltage			2		V_{CC}	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = GND			-1	µA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			1	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.25	0.45	V
		V_{CC} = 5 V	I_{OL} = 1 µA			0.05	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -6 mA[3]	3.76	4.1		V
		V_{CC} = 5 V	I_{OH} = -1 µA	4.95			
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = GND		0	-10	µA
I_{OZH}			V_O = V_{CC}		0	10	µA
I_{CC}	Standby supply current[4]	I_O = 0 mA, V_I = GND or V_{CC}			0	100	µA
	Operating supply current[5]	f = 1 MHz	I_O = 0 mA, V_I = GND or V_{CC}		7	10	mA
C_{IN}	Input capacitance[6]	V_{IN} = 2.0 V at f = 1 MHz			6		pF
C_{OUT}	Output capacitance[6]	V_{OUT} = 2.0 V at f = 1 MHz			9		pF

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER[7]			INDUSTRIAL						COMMERCIAL						UNIT
				-50			-40			-45			-35			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	20L8, 20R6, 20R4			45	50		35	40		40	45		30	35	ns
t_{CLK}	Clock to output or feedback		20R8 20R6 20R4		20	25		15	20		20	25		15	20	ns
t_{PZX}	Pin 13 (DIP) to output enable		20L8 20R6 20R4		20	25		15	20		20	25		15	20	ns
t_{PXZ}	Pin 13 (DIP) to output disable															
t_{EA}[6]	Input to output enable		20R8 20R6 20R4		45	50		35	40		40	45		30	35	ns
t_{ER}[6]	Input to output disable															
f_{MAX}	Maximum frequency	External feedback ($1/t_{SU}+t_{CLK}$)		14.2	20		18.1	25		15.3	20		20	25		MHz

1. The PALC20R8Z Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. JEDEC standard no. 7 for high-speed CMOS devices.
4. Disabled output pins = V_{CC} or GND.
5. Frequency of any input or clock. See graph page 5.
6. Equivalent function to t_{PZX}/t_{PXZ} but using product term control.
7. Test conditions (see Test Load) R_1 = 440 Ω, R_2 = 190 Ω.
8. Sampled but not 100% tested.

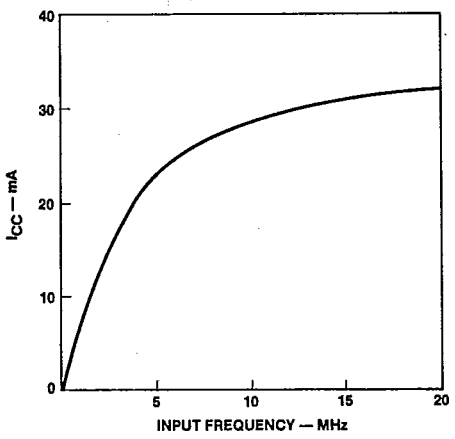
Switching Test Load -PALC20R8Z Series



SPECIFICATION	SWITCH S1	C_L	MEASURED OUTPUT VALUE
t_{PD}, t_{CLK}	Closed	50 pF	1.5 V
t_{PZX}, t_{EA}	Z->H: closed Z->L: closed	50 pF	2.0 V 0.8 V
t_{PXZ}, t_{ER}	H->Z: closed L->Z: closed	5 pF	H->Z: V_{OH}-0.5 V L->Z: V_{OL}+0.5 V

I_{CC} vs. Frequency-PALC20R8Z Series

Typical: V_{CC} = 5 V, T_A = 25°C



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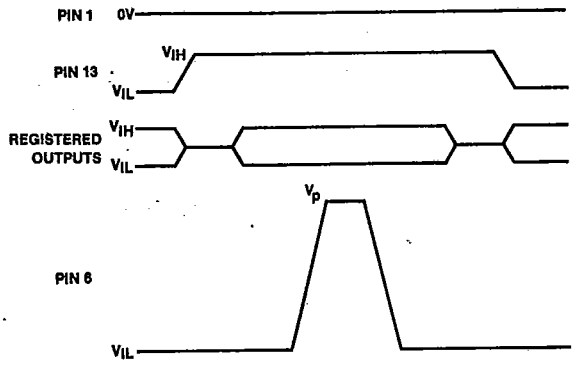
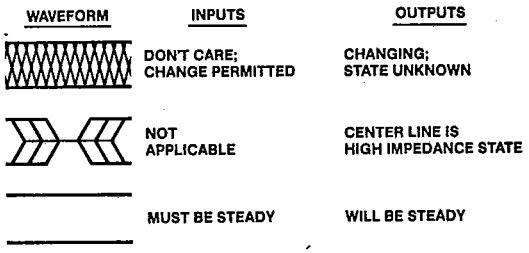
Output Register PRELOAD -PALC20R8Z Series

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of state sequencer designs by allowing direct setting of output states for improved test coverage. The PRELOAD procedure (using DIP pin numbers) is as follows:

1. Raise V_{CC} to 5 V.
2. Disable output registers by setting pin 13 to V_{IH}. Set pin 1 to 0 V.
3. Apply V_{IL}/V_{IH} (as desired) to all registered outputs.
4. Pulse pin 6 to V_P (12 V), then back to 0 V.
5. Remove V_{IL}/V_{IH} from all registered outputs.
6. Lower pin 13 to V_{IL} to enable the registered outputs.
7. Verify for V_{OL}/V_{OH} at all registered outputs.



Key to Timing Diagrams



Programming and Erasing -PALC20R8Z Series

The PALC20R8Z Series can be programmed on standard logic programmers. The PALC20R8Z Series may be erased by ultraviolet light when contained in the windowed package.

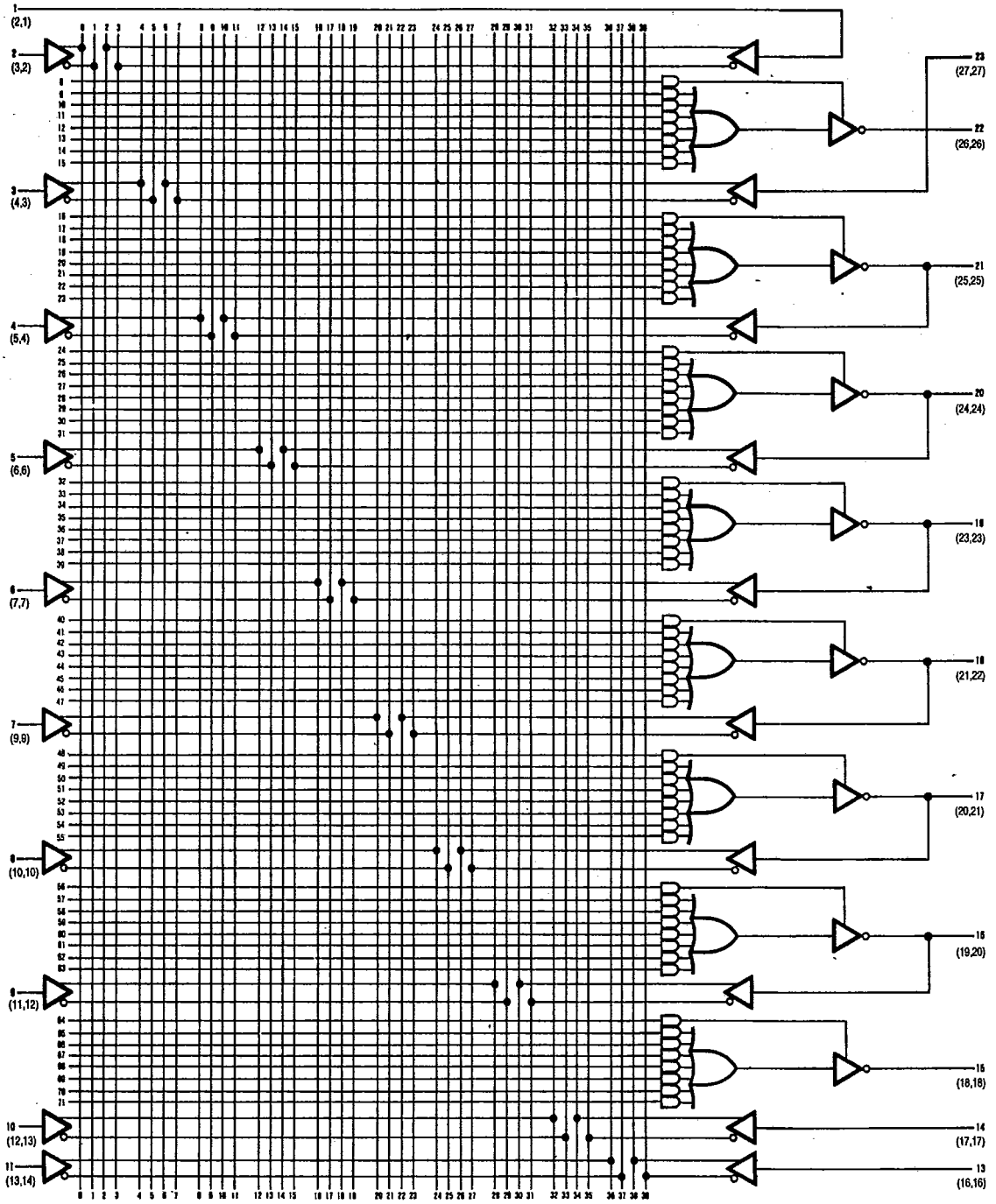
For erasure, the recommended ultraviolet light wavelength is 2537 Angstroms. The minimum dose required is 72,000 mW-sec/cm^2 (UV intensity x exposure time). For an ultraviolet lamp with a 20 mW/cm^2 power rating, the minimum exposure time would be 72,000/20 seconds = 60 minutes. The device needs to be within one inch of the lamp during erasure.

Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. The recommended maximum dosage is 7258 W-sec/cm^2.

Wavelengths of light less than 4000 Angstroms can partially erase the device in the windowed package. For this reason, an opaque label should be placed over the window, especially if the device will be exposed to sunlight or fluorescent lighting for extended periods of time.

Logic Diagram
DIP (FN, NL) Pinouts

20L8



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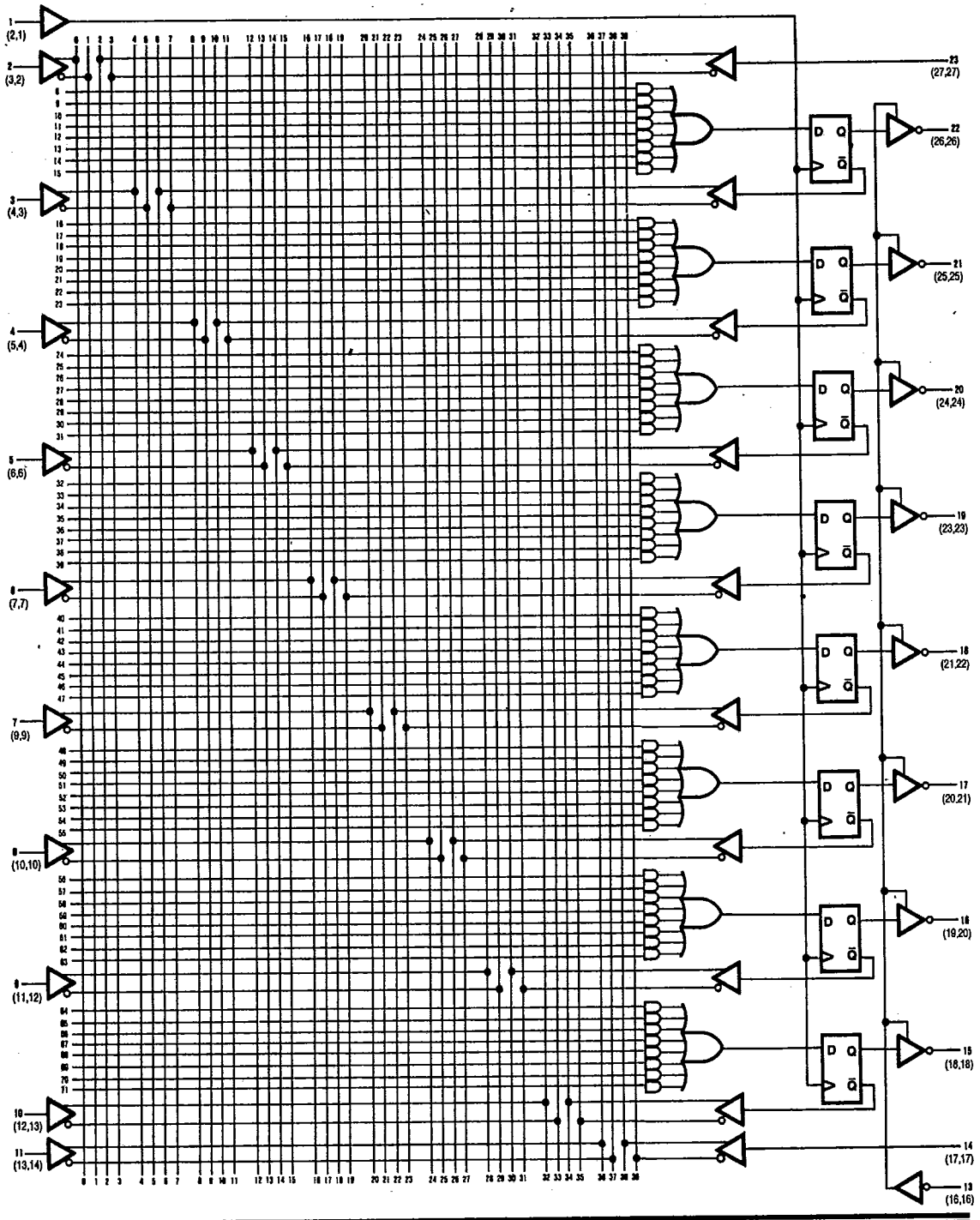
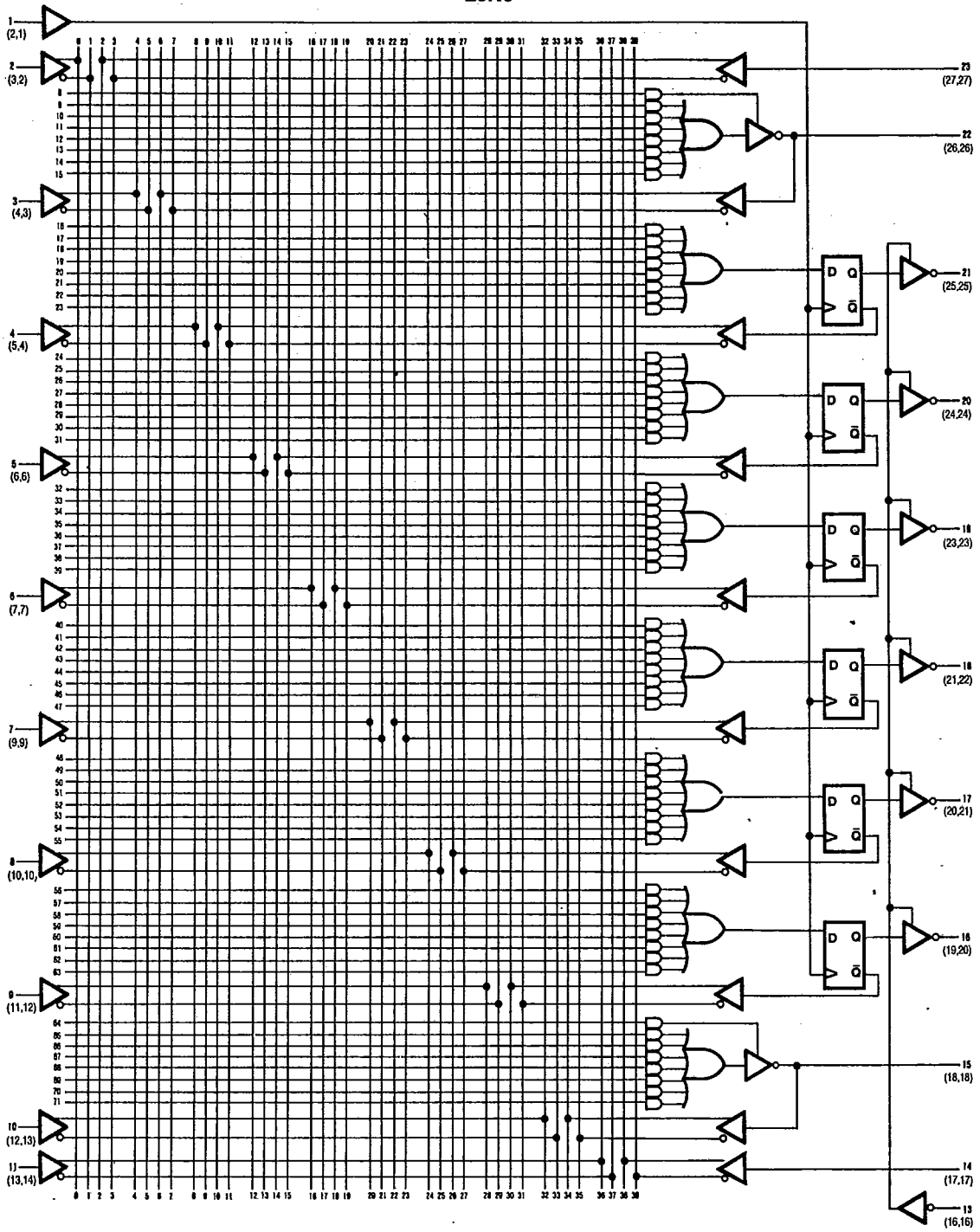
Logic Diagram DIP (FN, NL) Pinouts 20R8



Logic Diagram DIP (FN, NL) Pinouts 20R6



Logic Diagram DIP (FN, NL) Pinouts 20R4