Quad 8-Bit, 65 MSPS, Serial LVDS 3 V A/D Converter

AD9289

FEATURES

Four ADCs in one package
Serial LVDS digital output data rates to 520 Mbps (ANSI-644)
Data and frame clock outputs
SNR = 48 dBc (to Nyquist)
Excellent linearity
DNL = ±0.2 LSB (typical)
INL = ±0.25 LSB (typical)
300 MHz full power analog bandwidth
Power dissipation = 112 mW/channel at 65 MSPS
1 Vp-p to 2 Vp-p input voltage range
3.0 V supply operation
Power-down mode
Digital test pattern enable for timing alignments

APPLICATIONS

Tape drives
Medical imaging

FUNCTIONAL BLOCK DIAGRAM

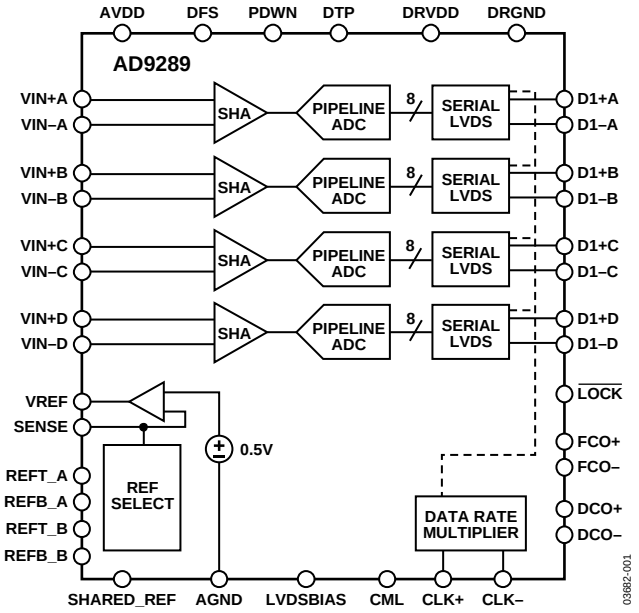


Figure 1.

PRODUCT DESCRIPTION

The AD9289 is a quad 8-bit, 65 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The product operates at up to a 65 MSPS conversion rate and is optimized for outstanding dynamic performance where a small package size is critical.

The ADC requires a single, 3 V power supply and an LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) trigger for signaling a new output byte are provided. Power-down is supported. The ADC typically consumes 7 mW when enabled.

Fabricated on an advanced CMOS process, the AD9289 is available in a 64-ball mini-BGA package (64-BGA). It is specified over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Four ADCs are contained in a small, space-saving package.
2. A data clock out (DCO) is provided, which operates up to 260 MHz and supports double-data rate operation (DDR).
3. The outputs of each ADC are serialized LVDS with data rates up to 520 Mbps (8 bits × 65 MSPS).
4. The AD9289 operates from a single 3.0 V power supply.
5. The internal clock duty cycle stabilizer maintains performance over a wide range of input clock duty cycles.

Rev. 0
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703 **© 2004 Analog Devices, Inc. All rights reserved.**

TABLE OF CONTENTS

Specifications 3
AC Specifications 4
Digital Specifications 4
Switching Specifications 5
Timing Diagrams 5
Absolute Maximum Ratings 6
Explanation of Test Levels 6
ESD Caution 6
Pin Configuration and Function Descriptions 7
Equivalent Circuits 8
Typical Performance Characteristics 9
Terminology 12
Theory of Operation 14
Analog Input and Reference Overview 14
Clock Input and Considerations 15
Evaluation Board 20
Outline Dimensions 30
Ordering Guide 30

REVISION HISTORY

10/04—Initial Version: Revision 0

SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, conversion rate = 65 MSPS, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 1.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
RESOLUTION			8			Bits
ACCURACY						
No Missing Codes	Full	VI		Guaranteed		
Offset Error	Full	VI		±5	±57	mV
Offset Matching	Full	VI		±12	±68	mV
Gain Error [1]	Full	VI		±0.5	±2.5	% FS
Gain Matching[1]	Full	VI		±0.2	±0.9	% FS
Differential Nonlinearity (DNL)	25°C	V		±0.2		LSB
	Full	VI		±0.2	±0.6	LSB
Integral Nonlinearity (INL)	25°C	V		±0.25		LSB
	Full	VI		±0.25	±0.6	LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		±16		ppm/°C
Gain Error	Full	V		±40		ppm/°C
Reference Voltage (VREF = 1 V)	Full	V		±10		ppm/°C
REFERENCE						
Output Voltage Error (VREF = 1 V)	Full	VI		±10	±35	mV
Load Regulation @ 1.0 mA (VREF = 1 V)	Full	V		0.7		mV
Output Voltage Error (VREF = 0.5 V)	Full	VI		±8	±26	mV
Load Regulation @ 0.5 mA (VREF = 0.5 V)	Full	V		0.2		mV
Input Resistance	Full	V		7		kΩ
COMMON MODE						
Common-Mode Level Output	Full	VI		±1.5	±50	mV
ANALOG INPUTS						
Differential Input Voltage Range (VREF = 1 V)	Full	VI		2		V p-p
Differential Input Voltage Range (VREF = 0.5 V)	Full	VI		1		V p-p
Common-Mode Voltage	Full	V		1.5		V
Input Capacitance	Full	V		5		pF
Analog Bandwidth, Full Power	Full	V		300		MHz
POWER SUPPLY						
AVDD	Full	IV	2.7	3.0	3.3	V
DRVDD	Full	IV	2.7	3.0	3.3	V
IAVDD	Full	VI		150	168	mA
DRVDD	Full	VI		33	40	mA
Power Dissipation[2]	Full	VI		550	625	mW
Power-Down Dissipation	Full	VI		7	12	mW
CROSSTALK	Full	V		–75		dB

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.0 V external reference and a 2 V p-p differential analog input).
[2] Power dissipation measured with rated encode and 2.4 MHz analog input at –0.5 dBFS.

AC SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, conversion rate = 65 MSPS, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 2.

Parameter		Temperature	Test Level	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)	f_{IN} = 2.4 MHz	Full	IV	47.7	49.0		dB
	f_{IN} = 10.3 MHz	25°C	V		48.5		dB
	f_{IN} = 35 MHz	Full	VI	46.7	48.0		dB
SIGNAL-TO-NOISE RATIO (SINAD)	f_{IN} = 2.4 MHz	Full	IV	47.6	48.9		dB
	f_{IN} = 10.3 MHz	25°C	V		48.4		dB
	f_{IN} = 35 MHz	Full	VI	46.2	47.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)	f_{IN} = 2.4 MHz	Full	IV	7.6	7.8		Bits
	f_{IN} = 10.3 MHz	25°C	V		7.7		Bits
	f_{IN} = 35 MHz	Full	VI	7.4	7.6		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	f_{IN} = 2.4 MHz	Full	IV	61.0	70.0		dBc
	f_{IN} = 10.3 MHz	25°C	V		68.0		dBc
	f_{IN} = 35 MHz	Full	VI	54.0	65.0		dBc
WORST HARMONIC (Second or Third)	f_{IN} = 2.4 MHz	Full	IV		–75.0	–61.0	dBc
	f_{IN} = 10.3 MHz	25°C	V		–70.0		dBc
	f_{IN} = 35 MHz	Full	VI		–65.0	–54.0	dBc
WORST OTHER (Excluding Second or Third)	f_{IN} = 2.4 MHz	Full	IV		–70.0	–61.0	dBc
	f_{IN} = 10.3 MHz	25°C	V		–68.0		dBc
	f_{IN} = 35 MHz	Full	VI		–65.0	–57.5	dBc
TWO TONE INTERMOD DISTORTION (IMD) AIN1 and AIN2 = –7.0 dBFS	f_{IN1} = 15 MHz f_{IN2} = 16 MHz	25°C	V		–72.0		dBc

DIGITAL SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, conversion rate = 65 MSPS, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 3.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
CLOCK INPUTS[1] (CLK+, CLK–)						
Logic Compliance			LVDS			
Differential Input Voltage	Full	IV	250	350	450	mV p-p
High Level Input Current	Full	VI		30	75	µA
Low Level Input Current	Full	VI		30	75	µA
Input Common-Mode Voltage	Full	IV	1.125	1.25	1.375	V
Input Resistance	25°C	V		100		kΩ
Input Capacitance	25°C	V		2		pF
LOGIC INPUTS (DFS, PDWN, SHARED_REF)						
Logic 1 Voltage	Full	IV	2.0			V
Logic 0 Voltage	Full	IV			0.8	V
Input Resistance	25°C	V		30		kΩ
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS ($\overline{\text{LOCK}}$)						
Logic 1 Voltage	Full	IV	2.45			V
Logic 0 Voltage	Full	IV			0.05	V
DIGITAL OUTPUTS (D1+, D1–)						
Logic Compliance			LVDS			
Differential Output Voltage	Full	VI	260	350	440	mV
Output Offset Voltage	Full	VI	1.15	1.25	1.35	V
Output Coding	Full	VI	Twos complement or binary			

[1] Clock inputs are LVDS-compatible. They require external dc bias and cannot be ac-coupled.

SWITCHING SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, conversion rate = 65 MSPS, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
CLOCK						
Maximum Clock Rate	Full	VI	65			MSPS
Minimum Clock Rate	Full	IV			12	MSPS
Clock Pulse Width High (t_{EH})	Full	VI	6.9	7.7		ns
Clock Pulse Width Low (t_{EL})	Full	VI	6.9	7.7		ns
OUTPUT PARAMETERS						
Valid Time (t_V)[1]	Full	IV	0.5		<1.5	CLK cycles
Propagation Delay (t_{PD})	Full	VI	6.9	9.0	11.6	ns
Rise Time (t_R) (20% to 80%)	Full	V		250		ps
Fall Time (t_F) (20% to 80%)	Full	V		250		ps
FCO Propagation Delay (t_{FCO})	Full	V		9.0		ns
DCO Propagation Delay (t_{CPD})	Full	V		9.0		ns
DCO-to-Data Delay (t_{DATA})	Full	VI		±100	±550	ps
DCO-to-FCO Delay (t_{FRAME})	Full	VI		±100	±500	ps
Data-to-Data Skew ($t_{DATA-MAX} – t_{DATA-MIN}$)	Full	IV		±100	±250	ps
PLL Lock Time (t_{LOCK})	25°C	V		1.8		µs
Wake-Up Time	25°C	V		7		ms
Pipeline Latency	Full	IV		6		CLK cycles
APERTURE						
Aperture Delay (t_A)	25°C	V		4.5		ns
Aperture Uncertainty (Jitter)	25°C	V		<1		ps rms
OUT-OF-RANGE RECOVERY TIME	25°C	V		1		CLK cycles

[1] Actual valid time is dependent on the moment when $\overline{LOCK}$ goes low.

TIMING DIAGRAMS

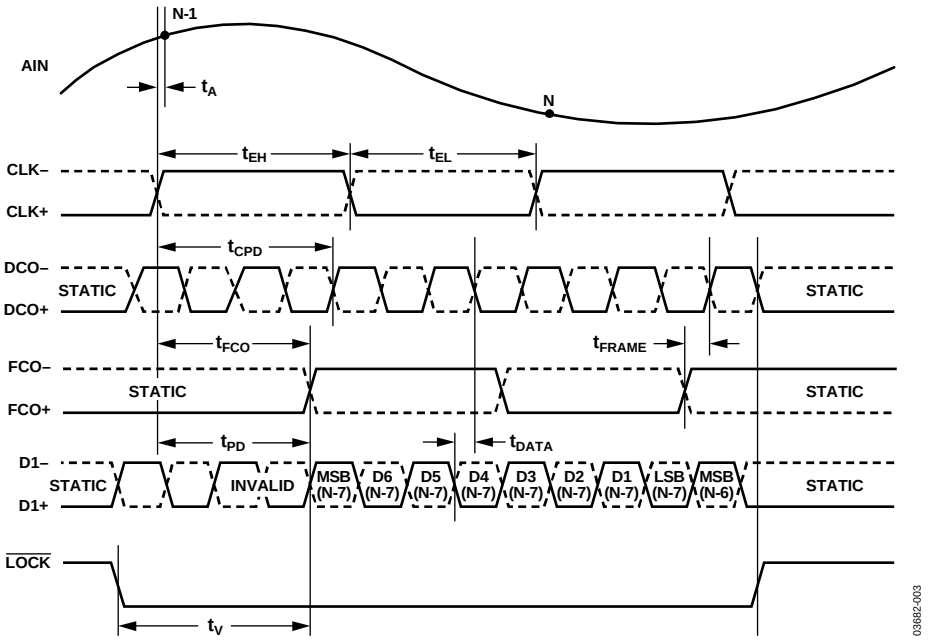


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+3.9	V
DRVDD	DRGND	–0.3	+3.9	V
AGND	DRGND	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
Digital Outputs (D1+, D1–, DCO+, DCO–, FCO+, FCO–)	DRGND	–0.3	DRVDD	V
$\overline{\text{LOCK}}$, LVDSBIAS	DRGND	–0.3	DRVDD	V
CLK+, CLK–	AGND	–0.3	AVDD	V
VIN+, VIN–	AGND	–0.3	AVDD	V
PDWN, DFS, DTP	AGND	–0.3	AVDD	V
REFT, REFB, SHARED_REF, CML	AGND	–0.3	AVDD	V
VREF, SENSE	AGND	–0.3	AVDD	V
ENVIRONMENTAL				
Operating Temperature Range (Ambient)		–40	+85	°C
Maximum Junction Temperature			150	°C
Lead Temperature (Soldering, 10 sec)			300	°C
Storage Temperature Range (Ambient)		–65	+150	°C
Thermal Impedance[1]			40	°C/W

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] θ_{JA} for a 4-layer PCB with solid ground plane in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

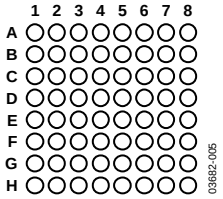


Figure 3. BGA Top View (Looking Through)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	D1–A	ADC A Complement Digital Output
B1	D1+A	ADC A True Digital Output
C1	FCO+	Frame Clock Output (MSB Indicator) True Output
D1	DNC	Do Not Connect
E1	AGND	Analog Ground
F1	VIN–A	ADC A Analog Input—Complement
G1	VIN+A	ADC A Analog Input—True
H1	LVDSBIAS[1]	LVDS Output Bias Pin
A2	DNC	Do Not Connect
B2	DNC	Do Not Connect
C2	FCO–	Frame Clock Output (MSB Indicator) Complement Output
D2	DNC	Do Not Connect
E2	AGND	Analog Ground
F2	AVDD	Analog Supply
G2	AGND	Analog Ground
H2	VIN+B	ADC B Analog Input—True
A3	D1–B	ADC B Complement Digital Output
B3	D1+B	ADC B True Digital Output
C3	DRVDD	Digital Supply
D3	DRGND	Digital Ground
E3	AGND	Analog Ground
F3	CML	Common Mode Level Output (= AVDD/2)
G3	SHARED_REF[3]	Shared Reference Control Bit
H3	VIN–B	ADC B Analog Input—Complement
A4	DNC	Do Not Connect
B4	DNC	Do Not Connect
C4	DCO+	Data Clock Output—True
D4	$\overline{\text{LOCK}}$	PLL Lock Output
E4	AVDD	Analog Supply
F4	REFT_A	Reference Buffer Decoupling (Positive)
G4	REFB_A	Reference Buffer Decoupling (Negative)
H4	SENSE	Reference Mode Selection
A5	D1–C	ADC C Complement Digital Output
B5	D1+C	ADC C True Digital Output
C5	DCO–	Data Clock Output—Complement
D5	AGND	Analog Ground
E5	AGND	Analog Ground
F5	REFT_B	Reference Buffer Decoupling (Positive)
G5	REFB_B	Reference Buffer Decoupling (Negative)
H5	VREF	Voltage Reference Input/Output
A6	DNC	Do Not Connect
B6	DNC	Do Not Connect
C6	DRVDD	Digital Supply
D6	DRGND	Digital Ground
E6	AVDD	Analog Supply
F6	AGND	Analog Ground
G6	AGND	Analog Ground
H6	VIN–C	ADC C Analog Input—Complement
A7	D1–D	ADC D Complement Digital Output
B7	D1+D	ADC D True Digital Output
C7	DFS[2]	Data Format Select
D7	AGND	Analog Ground
E7	AGND	Analog Ground
F7	AVDD	Analog Supply
G7	AGND	Analog Ground
H7	VIN+C	ADC C Analog Input—True
A8	DNC	Do Not Connect
B8	DNC	Do Not Connect
C8	CLK+	Input Clock—True
D8	CLK–	Input Clock—Complement
E8	PDWN[3]	Power Down Selection
F8	VIN–D	ADC D Analog Input—Complement
G8	VIN+D	ADC D Analog Input—True
H8	DTP[3, 4]	Digital Test Pattern

[1] LVDSBIAS use a 3.9 kΩ resistor-to-analog ground to set the LVDS output differential swing of 350 mV p-p.
[2] DFS has an internal on-chip pull-down resistor and defaults to offset binary output coding if untied. If twos complement output coding is desired then tie this pin to AVDD.
[3] To enable, tie this pin to AVDD. To disable, tie this pin to AGND.
[4] DTP has an internal on-chip pull-down resistor.

EQUIVALENT CIRCUITS

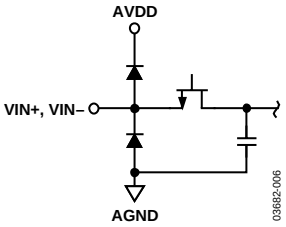


Figure 4. Equivalent Analog Input Circuit

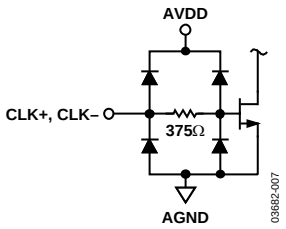


Figure 5. Equivalent Clock Input Circuit

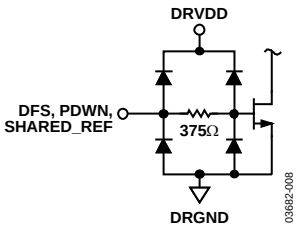


Figure 6. Equivalent Digital Input Circuit

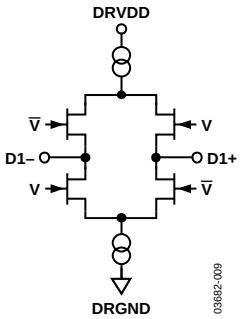


Figure 7. Equivalent Digital Output Circuit

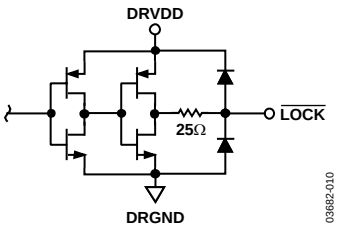


Figure 8. Equivalent $\overline{LOCK}$ Output Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

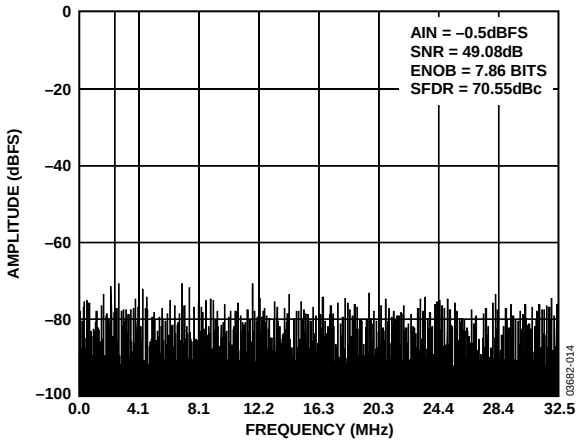


Figure 9. Single-Tone 32k FFT With f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

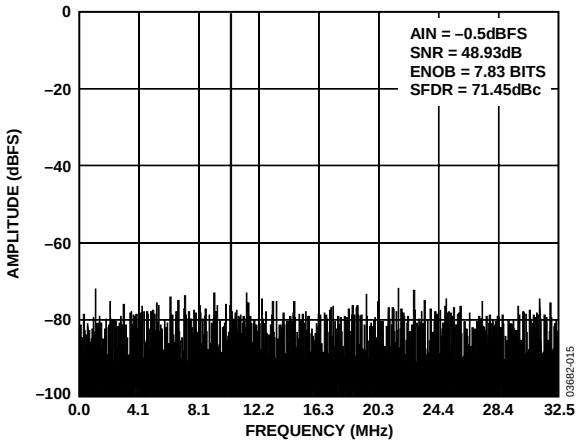


Figure 10. Single-Tone 32k FFT With f_{IN} = 10.3 MHz, f_{SAMPLE} = 65 MSPS

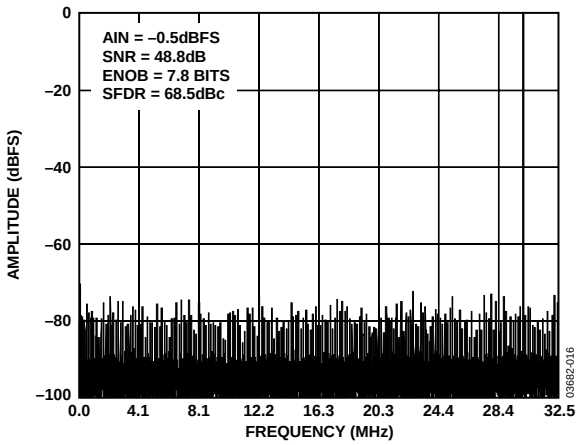


Figure 11. Single-Tone 32k FFT With f_{IN} = 35 MHz, f_{SAMPLE} = 65 MSP

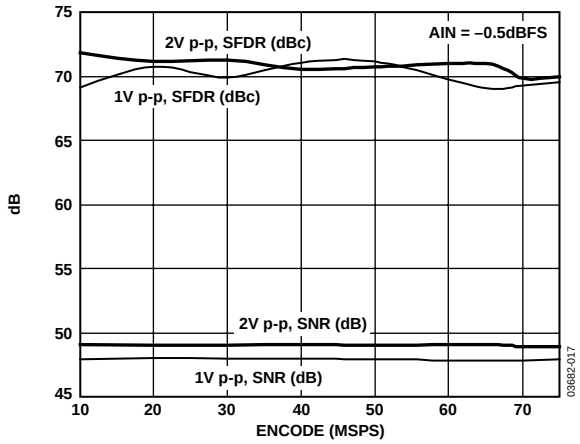


Figure 12. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 2.4 MHz

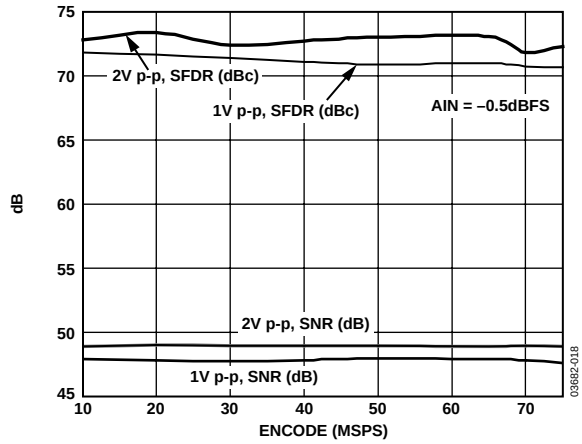


Figure 13. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

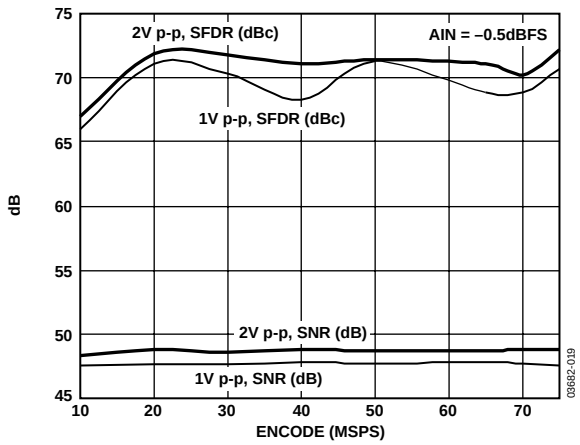


Figure 14. SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 35 MHz

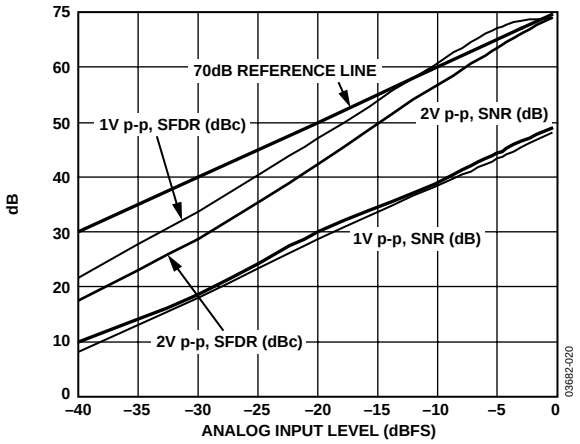


Figure 15. SNR/SFDR vs. Analog Input Level, f_{SAMPLE} = 65 MSPS, f_{IN} = 2.4 MHz

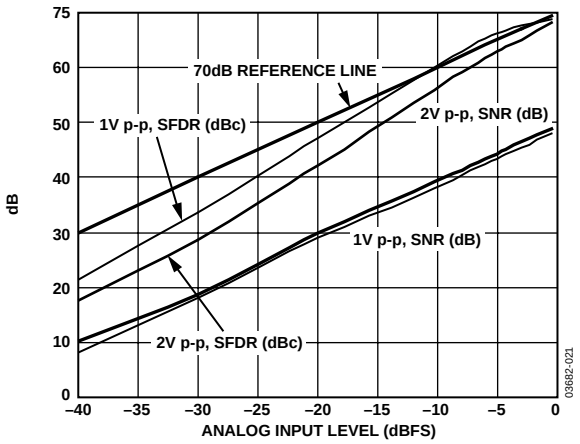


Figure 16. SNR/SFDR vs. Analog Input Level, f_{SAMPLE} = 65 MSPS, f_{IN} = 10.3 MHz

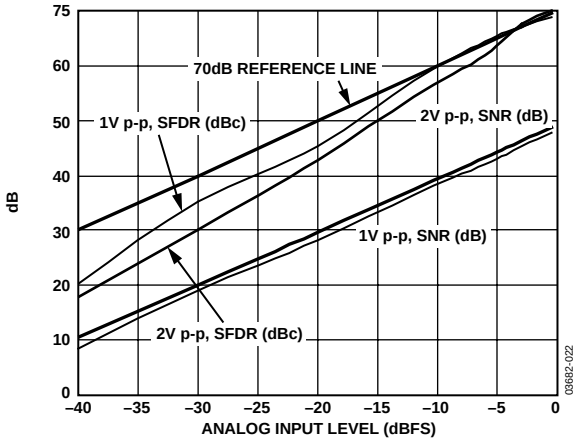


Figure 17. SNR/SFDR vs. Analog Input Level, f_{SAMPLE} = 65 MSPS, f_{IN} = 35 MHz

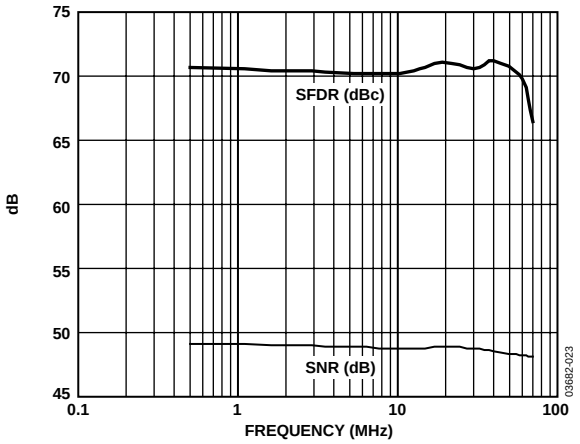


Figure 18. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 65 MHz

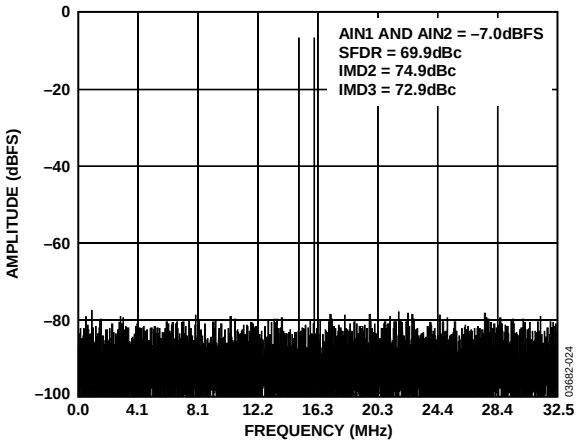


Figure 19. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

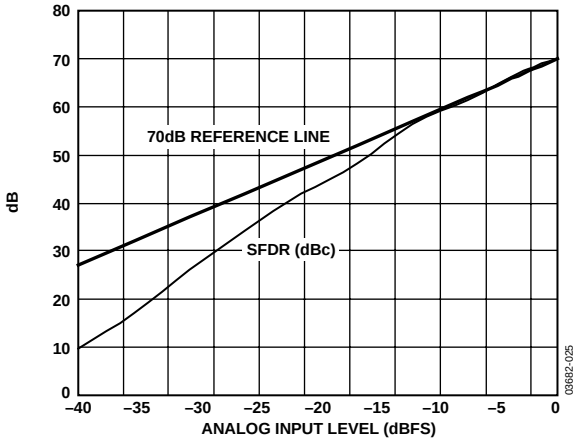


Figure 20. Two-Tone SFDR vs. Analog Input Level with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

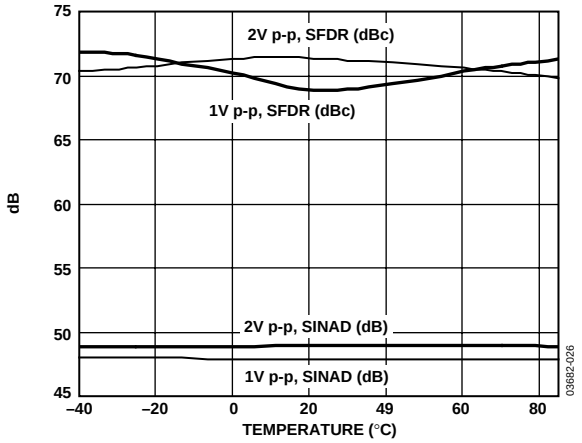


Figure 21. SINAD/SFDR vs. Temperature, f_{SAMPLE} = 65 MSPS, f_{IN} 10.3 MHz

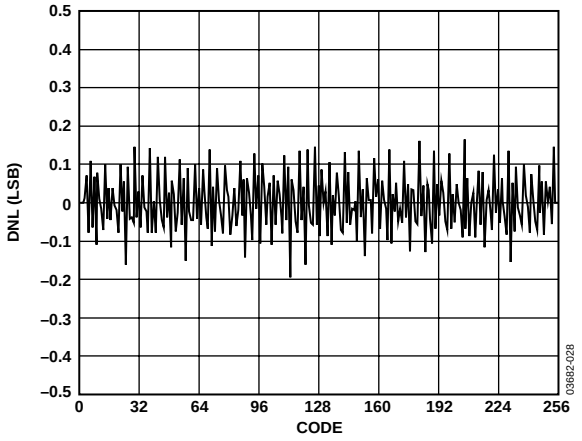


Figure 23. Typical DNL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

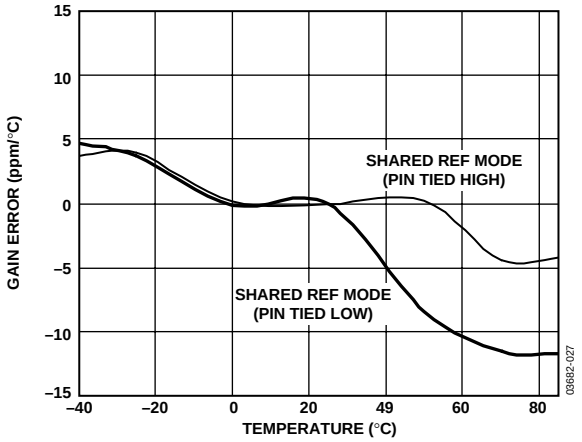


Figure 22. Gain vs. Temperature

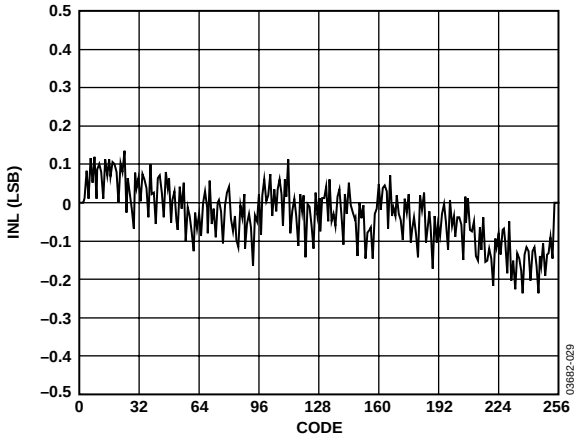


Figure 24. Typical INL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

TERMINOLOGY

Analog Bandwidth

Analog Bandwidth is the analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB from full scale.

Aperture Delay

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the 50% point rising edge of the clock input to the time at which the input signal is held for conversion.

Aperture Uncertainty (Jitter)

Aperture jitter is the variation in aperture delay for successive samples and can be manifested as frequency-dependent noise on the ADC input.

Clock Pulse Width and Duty Cycle

Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve a rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Crosstalk

Crosstalk is defined as the coupling of a channel when all channels are driven by a full-scale signal.

Differential Analog Input Capacitance

The complex impedance simulated at each analog input port.

Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a pin and subtracting the voltage from a second pin that is 180° out of phase. Peak-to-peak differential is computed by rotating the input phase 180° and taking the peak measurement again. The difference is computed between both peak measurements.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to an 8-bit resolution indicates that all 256 codes, respectively, must be present over all operating ranges.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, it is possible to obtain a measure of performance expressed as *N*, the effective number of bits:

$$N = (\text{SINAD} - 1.76)/6.02$$

Thus, the effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Gain Error

The largest gain error is specified and is considered the difference between the measured and ideal full-scale input voltage range.

Gain Matching

Expressed in %FSR. Computed using the following equation:

$$GainMatching = \frac{FSR_{\max} - FSR_{\min}}{\left(\frac{FSR_{\max} + FSR_{\min}}{2}\right)} \times 100\%$$

where FSR_{MAX} is the most positive gain error of the ADCs, and FSR_{MIN} is the most negative gain error of the ADCs.

Second and Third Harmonic Distortion

The ratio of the rms signal amplitude to the rms value of the second or third harmonic component, reported in dBc.

Integral Nonlinearity (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Offset Error

The largest offset error is specified and is considered the difference between the measured and ideal voltage at the analog input that produces the midscale code at the outputs.

Offset Matching

Expressed in mV. Computed using the following equation:

$$OffsetMatching = OFF_{MAX} - OFF_{MIN}$$

where OFF_{MAX} is the most positive offset error and OFF_{MIN} is the most negative offset error.

Out-of-Range Recovery Time

Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Output Propagation Delay

The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Signal-to Noise and Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It may be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

THEORY OF OPERATION

Each A/D converter in the AD9289 architecture consists of a front send sample-and-hold amplifier (SHA) followed by a pipe-lined, switched capacitor ADC. The pipelined ADC is divided into two sections, consisting of six 1.5-bit stages and a final 2-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 8-bit result in the digital correc-tion logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data and carries out the error correction. The data is serialized and aligned to the frame, output clock, and lock detection circuitry.

ANALOG INPUT AND REFERENCE OVERVIEW

The analog input to the AD9289 is a differential-switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range and maintain excellent performance, as shown in Figure 26 sand Figure 27. An input common-mode voltage of midsupply minimizes signal dependent errors and provides optimum performance.

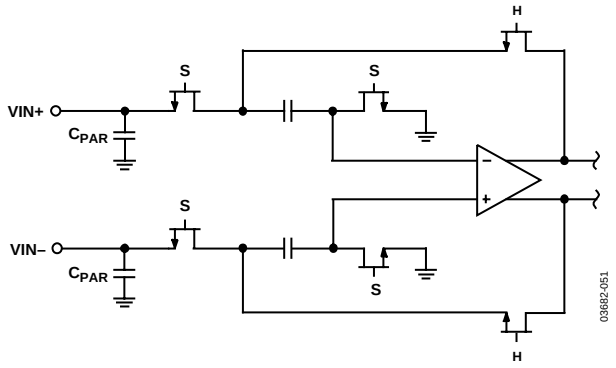


Figure 25. Switched-Capacitor SHA Input UPDATE

The clock signal alternately switches the SHA between sample mode and hold mode (see Figure 25). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent on the application.

The analog inputs of the AD9289 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure 26 and Figure 27).

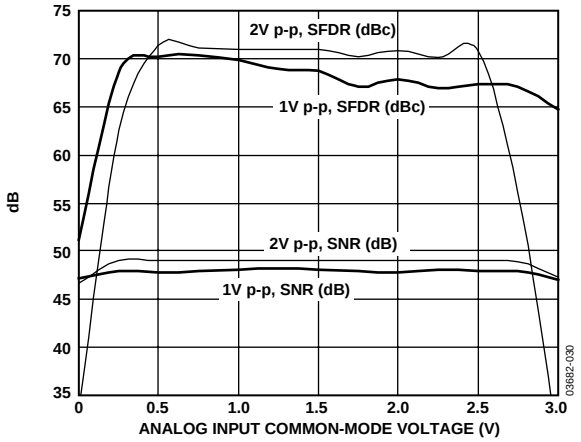


Figure 26. SNR, SFDR vs. Common-Mode Voltage, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

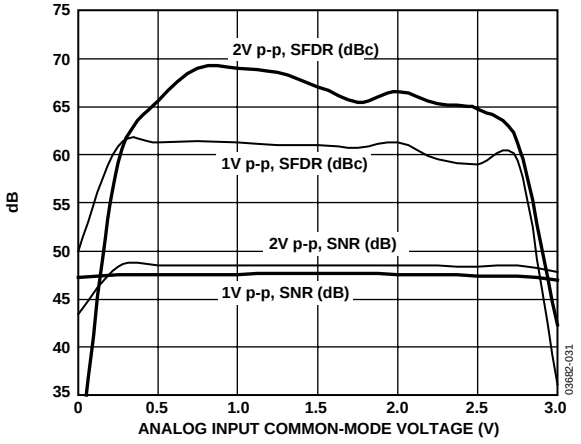


Figure 27. SNR, SFDR vs. Common-Mode Voltage, f_{IN} = 35 MHz, f_{SAMPLE} = 65 MSPS

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that defines the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the *REFT* and *REFB* voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V or adjusted within the same range, as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved by setting the AD9289 to the largest input span of 2 V p-p.

The SHA should be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined in Figure 26 and Figure 27.

Differential Input Configurations

Optimum performance is achieved by driving the AD9289 in a differential input configuration. For baseband applications, the AD8351 differential driver provides excellent performance and a flexible interface to the ADC (see Figure 28).

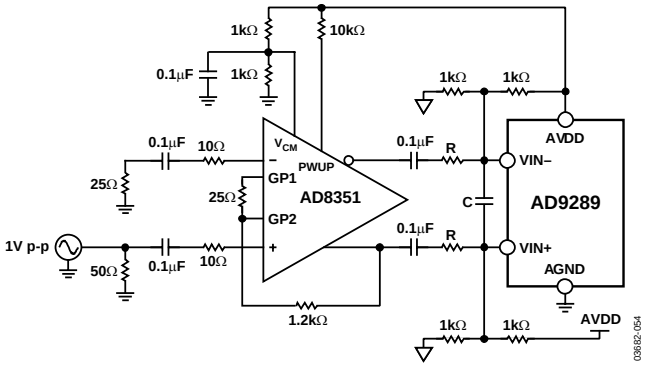


Figure 28. Differential Input Configuration Using the AD8351

However, the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9289. For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example of this is shown in Figure 29.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

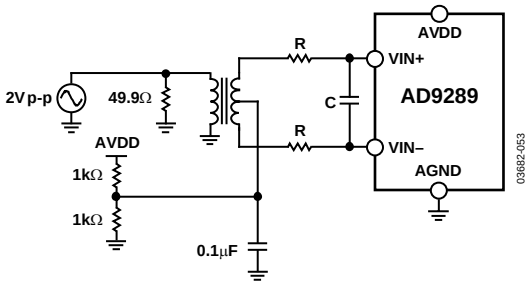


Figure 29. Differential Transformer-Coupled Configuration

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there is a degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 30 details a typical single-ended input configuration.

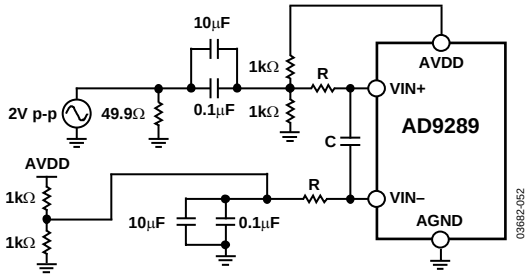


Figure 30. Single-Ended Input Configuration

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Typically, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9289 has a self-contained clock duty cycle stabilizer that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9289.

An on-board phase-locked loop (PLL) multiplies the input clock rate for the purpose of shifting the serial data out. As a result, any change to the sampling frequency requires a minimum of 100 clock periods to allow the PLL to reacquire and lock to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_A) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \times \log10\ [1/2 \times \pi \times f_A \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Applications that require undersampling are particularly sensitive to jitter.

The LVDS clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9289. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

The AD9289 can also support a single-ended CMOS clock. Refer to the evaluation board schematics to enable this feature.

Power Dissipation and Standby Mode

As shown in Figure 31, the power dissipated by the AD9289 is proportional to its sample rate. The digital power dissipation does not vary because it is determined primarily by the strength of the digital drivers and the load on each output bit.

Digital power consumption can be minimized by reducing the capacitive load presented to the output drivers. The data in Figure 31 was collected while a 5 pF load was placed on each output driver.

The analog circuitry of the AD9289 is optimally biased to achieve excellent performance while affording reduced power consumption.

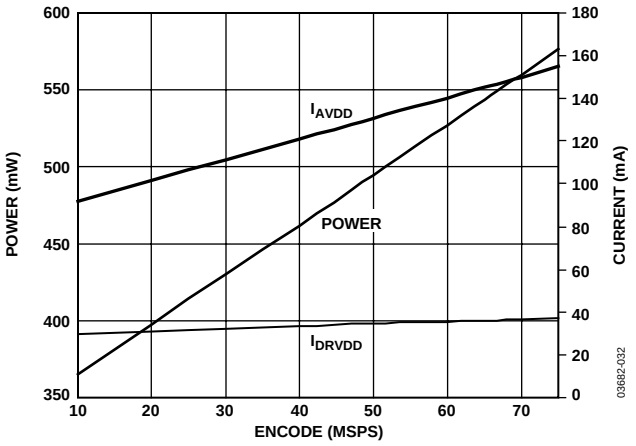


Figure 31. Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

By asserting the PDWN pin high, the AD9289 is placed in standby mode. In this state, the ADC typically dissipates 7 mW. During standby the LVDS output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9289 into its normal operational mode.

In standby mode, low power dissipation is achieved by shutting down the reference, reference buffer, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode, and shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately 1 s to fully discharge the reference buffer decoupling capacitors and 7 ms to restore full operation.

Digital Outputs

The AD9289's differential outputs conform to the ANSI-644 LVDS standard. To set the LVDS bias current place a resistor (RSET is nominally equal to 3.9 kΩ) to ground at the LVDSBIAS pin. The RSET resistor current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal ±350 mV swing at the receiver. To adjust the differential signal swing, simply change the resistor to a different value, as shown in Table 7.

Table 7. LVDSBIAS Pin Configuration

RSET	Differential Output Swing
3.6k	375 mV p-p
3.9k (Default)	350 mV p-p
4.3k	325mV p-p

The AD9289's LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. It is recommended to keep the trace length no longer than 12 inches and to keep differential output traces close together and at equal lengths.

The format of the output data can be selected as offset binary or twos complement. A quick example of each output coding format can be found in Table 8. The DFS pin is used to set the format (see Table 9).

Table 8. Digital Output Coding

Code	VIN+ – VIN– Input Span = 2 V p-p (V)	VIN+ – VIN– Input Span = 1 V p-p (V)	Digital Output Offset Binary (D7...D0)	Digital Output Twos Complement (D7...D0)
255	1.000	0.500	1111 1111	0111 1111
128	0	0	1000 0000	0000 0000
127	–0.00781	–0.00391	0111 1111	1111 1111
0	–1.00	–0.5000	0000 0000	1000 0000

Table 9. Data Format Configuration

DFS Mode	Data Format
AVDD	Twos complement
AGND	Offset binary

Timing

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to eight bits times the sample clock rate, with a maximum of 520 MHz (8 bits x 65 MSPS = 520 MHz). The lowest typical conversion rate is 12 MSPS.

Two output clocks are provided to assist in capturing data from the AD9289. The DCO is used to clock the output data and is equal to four times the sampling clock (CLK) rate. Data is clocked out of the AD9289 and can be captured on the rising and falling edges of the DCO that supports double-data rate operation (DDR). The frame clock out (FCO) signals the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

$\overline{\text{LOCK}}$ Pin

The AD9289 contains an internal PLL that is used to generate the DCO. When the PLL is locked, the $\overline{\text{LOCK}}$ signal will be low, indicating valid data on the outputs.

If for any reason the PLL loses lock, the $\overline{\text{LOCK}}$ signal goes high as soon as the lock circuitry detects an unlocked condition. While the PLL is unlocked, the data outputs and DCO remains in the last known state. If the $\overline{\text{LOCK}}$ signal goes high in the middle of a byte, no data or DCO signals will be available for the rest of the byte. It takes at least 1.8 µs at 65 MSPS to regain lock once it is lost. Note that regaining lock is sample rate-dependent and takes at least 100 input periods after the PLL acquires the input clock.

Once the PLL regains lock the DCO starts. The first valid data byte is indicated by the FCO signal. The FCO rising edge occurs 0.5 to <1.5 input clock periods after $\overline{\text{LOCK}}$ goes low.

CML Pin

A common-mode level output is available at Pin F3. This output self biases to AVDD/2. This is a relatively high impedance output (2.5k nominal), which may need to be considered when used as a reference.

DTP Pin

When the digital test pattern (DTP) pin is enabled (pulled to AVDD), all of the ADC channel outputs shift out the following pattern: 11000000. The FCO and DCO outputs still work as usual while all channels shift out the test pattern. This pattern allows the user to perform timing alignment adjustments between the DCO and the output data.

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9289. The input range can be adjusted by varying the reference voltage applied to the AD9289, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

The shared reference mode (see Figure 32) allows the user to externally connect the reference buffers from the quad ADC for better gain and offset matching performance. If the ADCs are to function independently, the reference decoupling can be treated independently and can provide better isolation between the four channels. To enable shared reference mode, the SHARED_REF pin must be tied high and external reference buffer decoupling pins must be externally shorted. (REFT_A must be externally shorted to REFT_B and REFB_A must be shorted to REFB_B.) Note that Channels A and B are referenced to REFT_A and REFB_A and Channels C and D are referenced to REFT_B and REFB_B.

Table 10. Reference Settings

Selected Mode	SENSE Voltage	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal, 1 V p-p FSR	VREF	0.5	1.0
Programmable	0.2 V to VREF	0.5 × (1 + R2/R1)	2 × VREF
Internal, 2 V p-p FSR	AGND to 0.2 V	1.0	2.0

Internal Reference Connection

A comparator within the AD9289 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 10. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 33), setting VREF to 1 V. Connecting the SENSE pin to the VREF pin switches the amplifier output to the SENSE pin, configuring the internal op amp circuit as a voltage follower and providing a 0.5 V reference output. If an external resistor divider is connected as shown in Figure 34 the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

In all reference configurations, REFT_A and REFT_B and REFB_A and REFB_B establish their input span of the ADC core. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

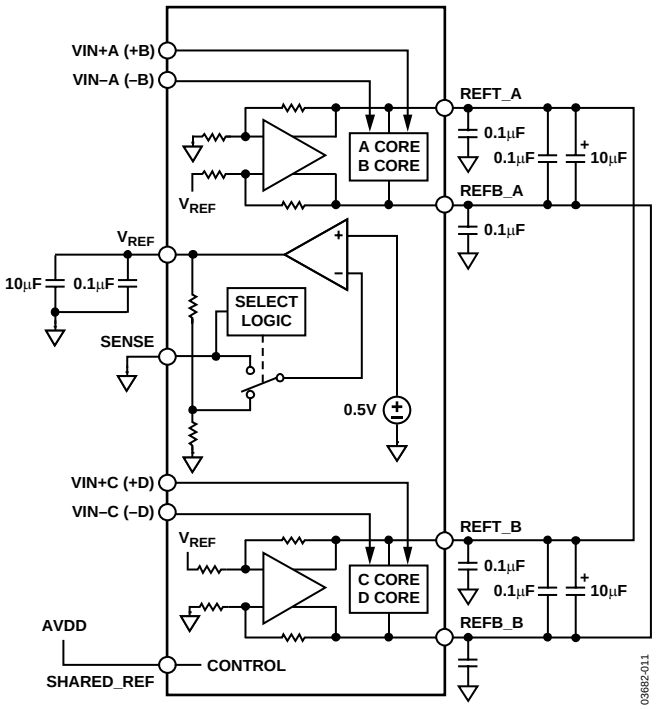


Figure 32. Shared Reference Mode Enabled

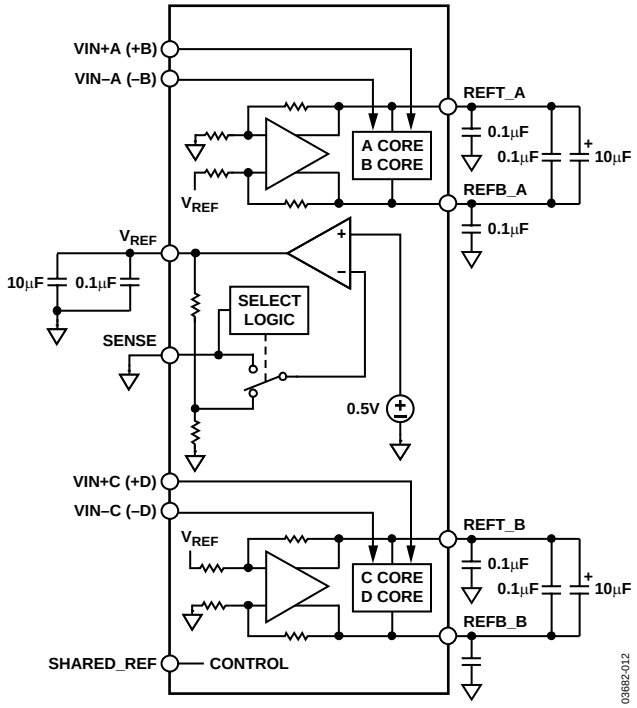


Figure 33. Internal Reference Configuration

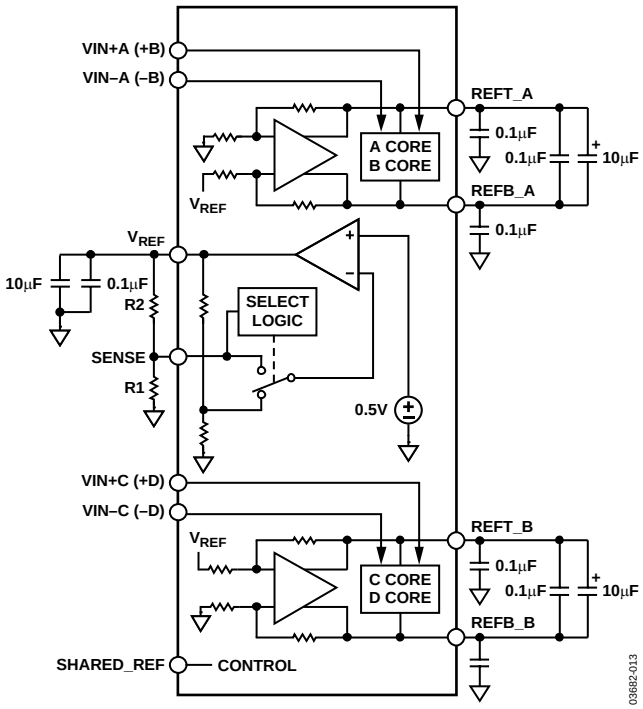


Figure 34. Programmable Reference Configuration

If the internal reference of the AD9289 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 35 depicts how the internal reference voltage is affected by loading.

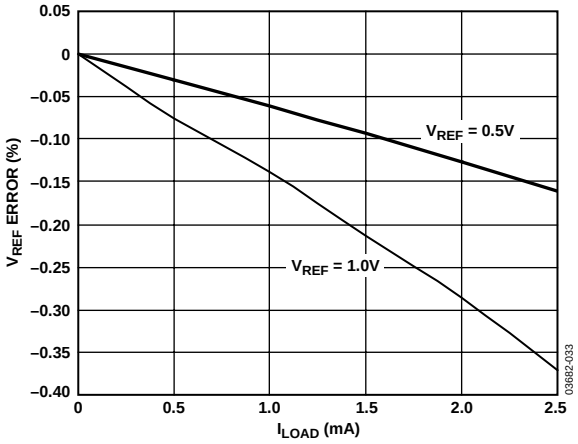


Figure 35. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 36 shows the typical drift characteristics of the internal shared reference in both 1 V and 0.5 V modes.

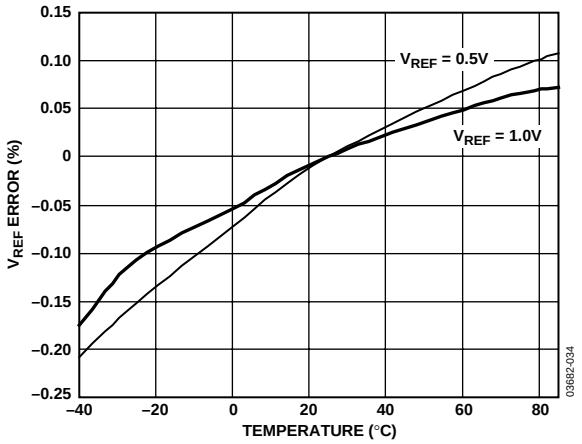


Figure 36. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT_A and REFT_B and REFB_A and REFB_B , for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

Power and Ground Recommendations

When connecting power to the AD9289, it is recommended that two separate 3.0 V supplies be used. One for analog (AVDD) and one for digital (DRVDD). If only one supply is available then it should be routed to the AVDD first and tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors proceeding. One may want to use several different decoupling capacitors to cover both high and low frequencies. These should be located close the point of entry at the pc board level as well as close to the parts with minimal trace length.

A single pc board ground plane should be sufficient when using the AD9289. With proper decoupling and smart partitioning of the pc board's analog, digital, and clock sections, optimum performance is easily achieved.

EVALUATION BOARD

The AD9289 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially through a transformer (default) or the AD8351 driver. Provisions have also been made to drive the ADC single-ended. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (refer to the schematics). Figure 37 shows the typical bench characterization setup used to evaluate the ac performance of the AD9289. It is critical that the signal sources that are used have very low phase noise (< 1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 37 to Figure 47 for complete schematics and layout plots, which demonstrate the routing and grounding techniques that should be applied at the system level.

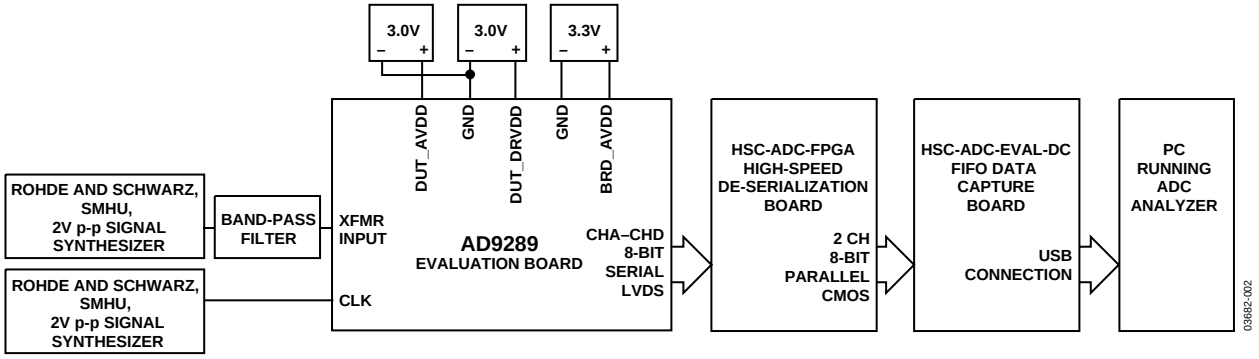


Figure 37. Evaluation Board Connections

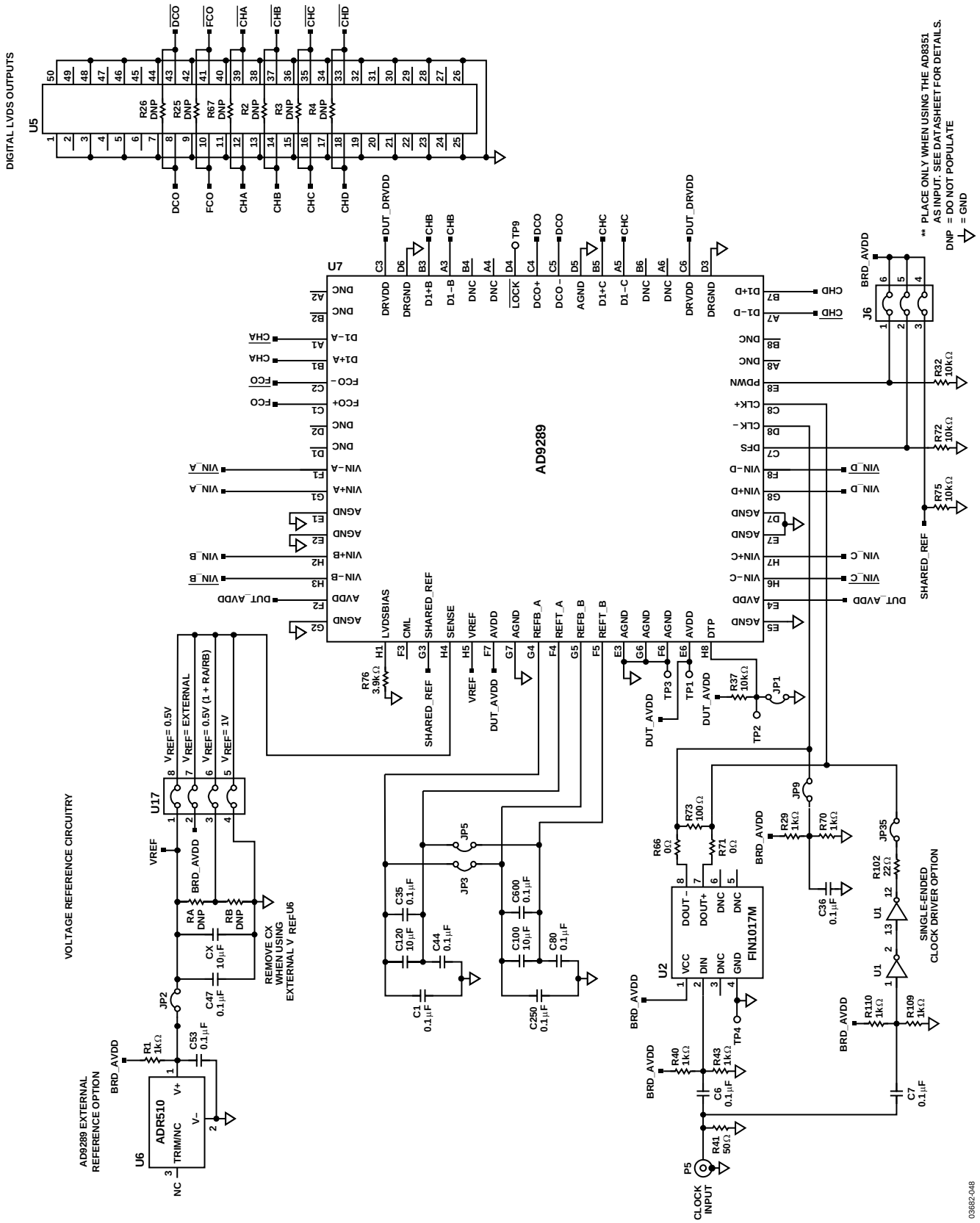


Figure 38. Evaluation Board Schematic, DUT, VREF, and Clock Inputs

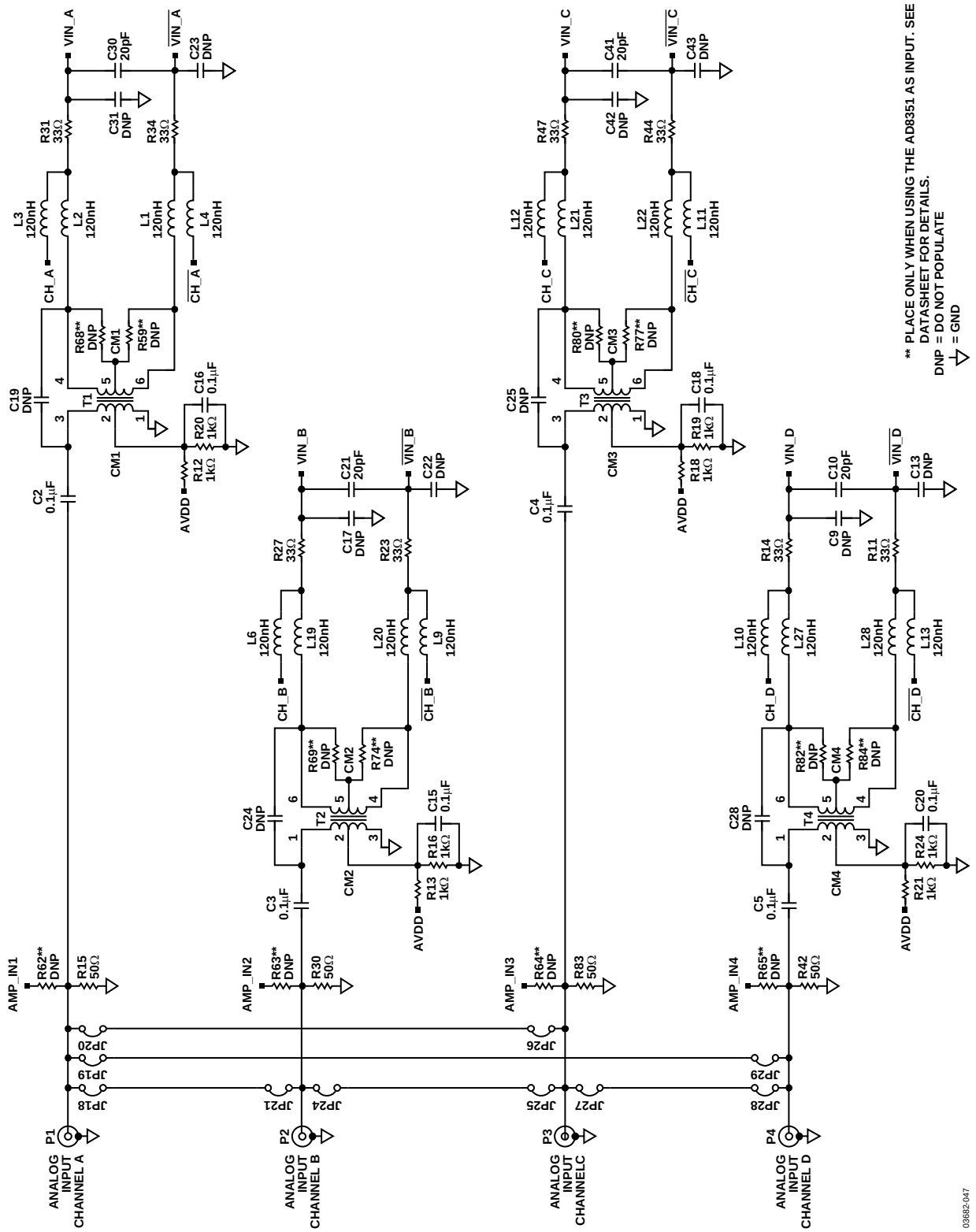


Figure 39. Evaluation Board Schematic, DUT Analog Input

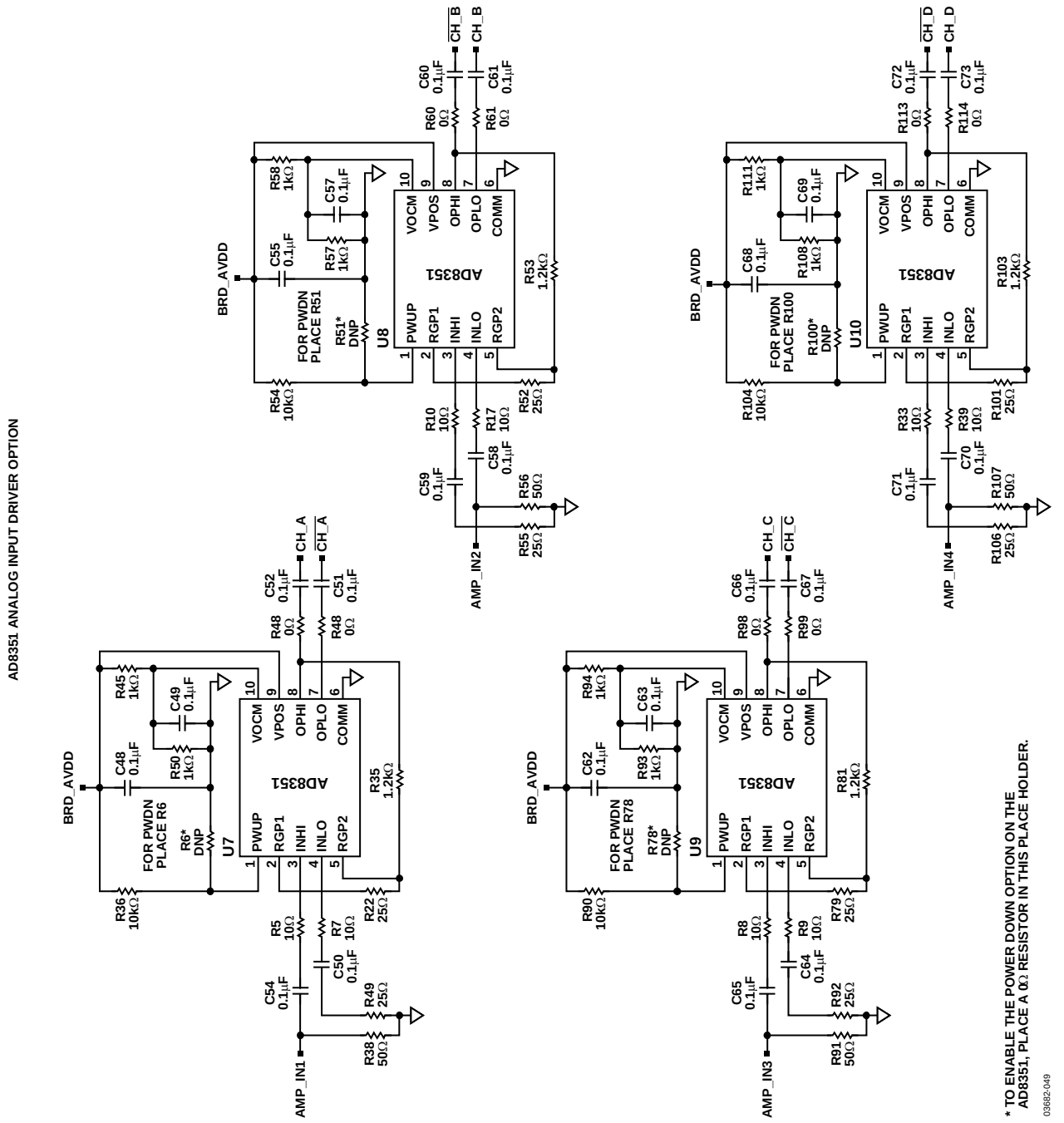


Figure 40. Evaluation Board Schematic, Optional DUT Analog Input Drive

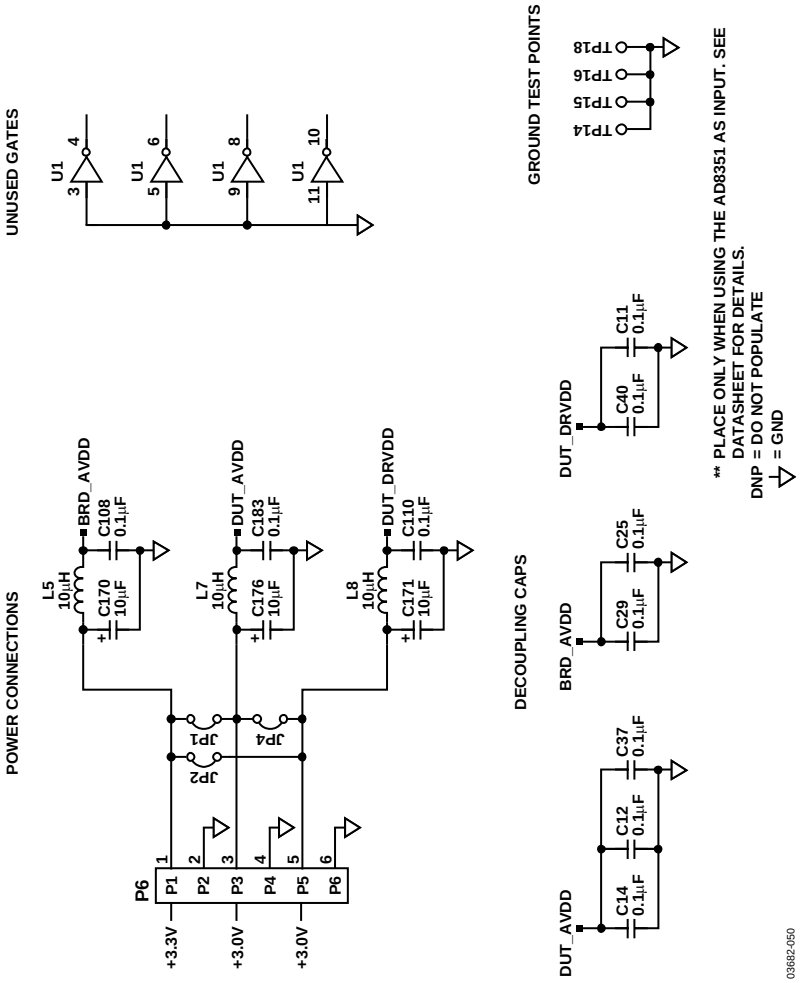


Figure 41. Evaluation Board Schematic, Power, and Decoupling

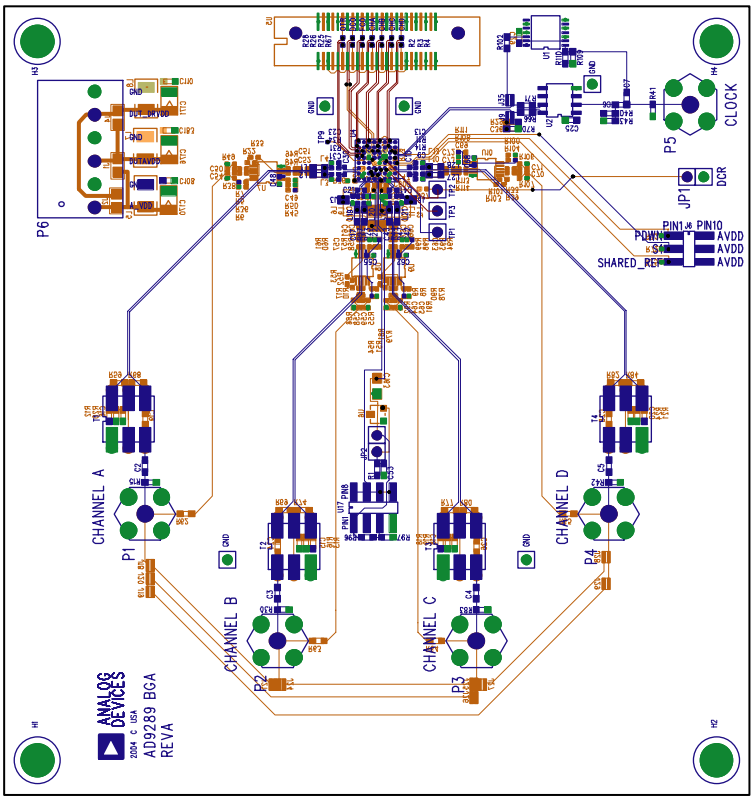


Figure 42. Evaluation Board Layout, Primary Side

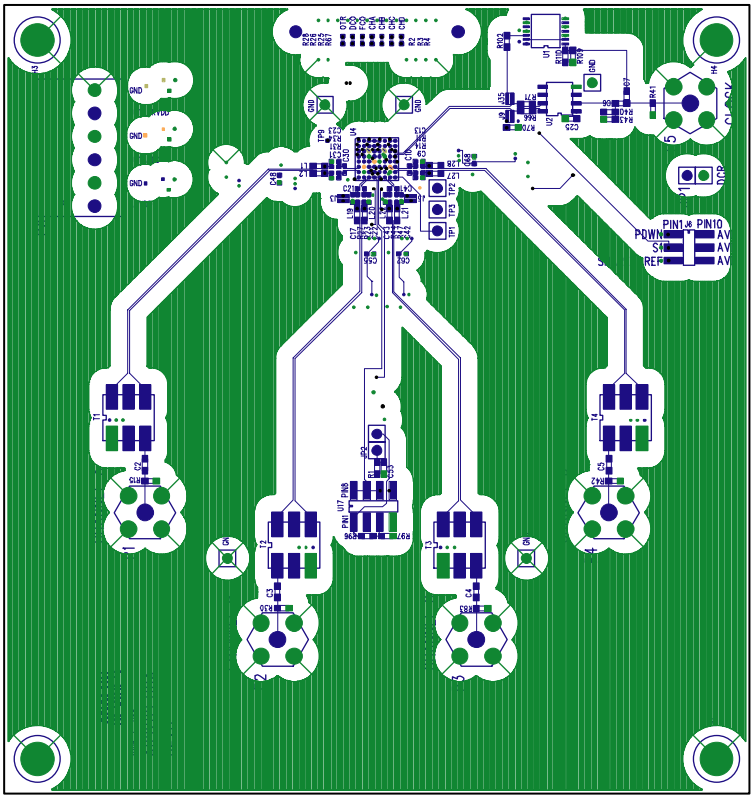


Figure 43. Evaluation Board Layout, Primary Side (With Ground Copper Pour)

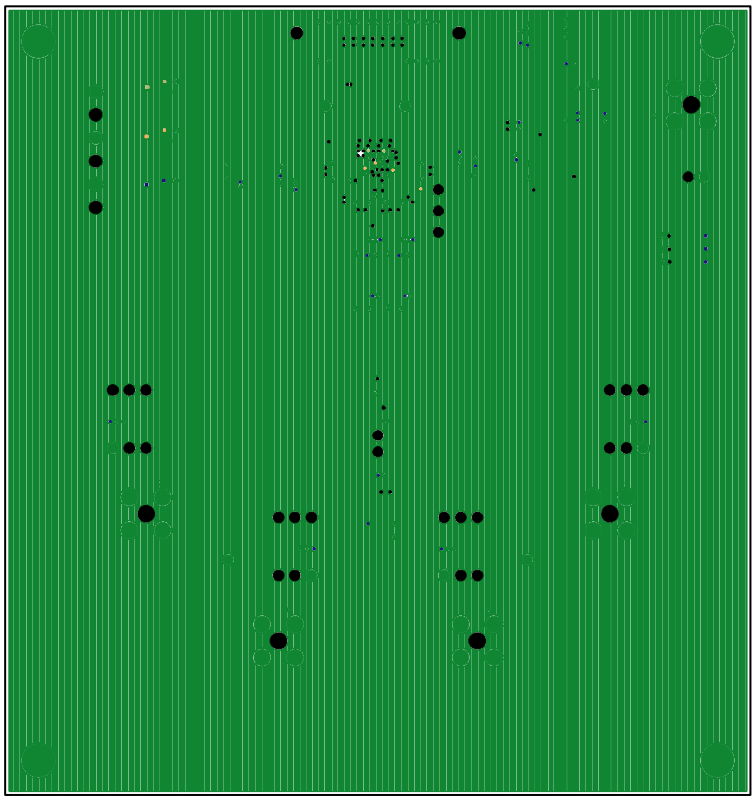


Figure 44. Evaluation Board Layout, Ground Plane

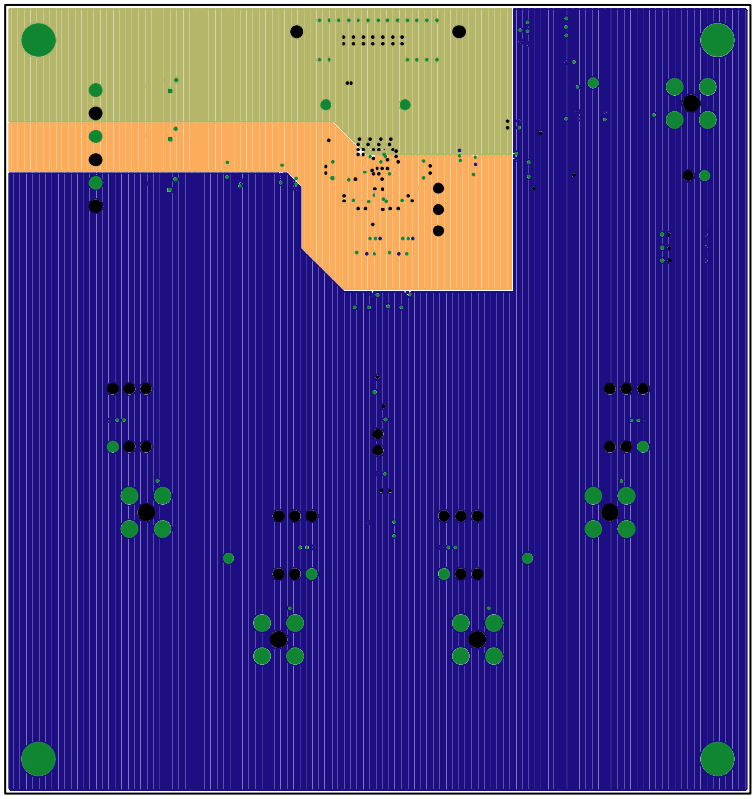


Figure 45. Evaluation Board Layout, Power Plane

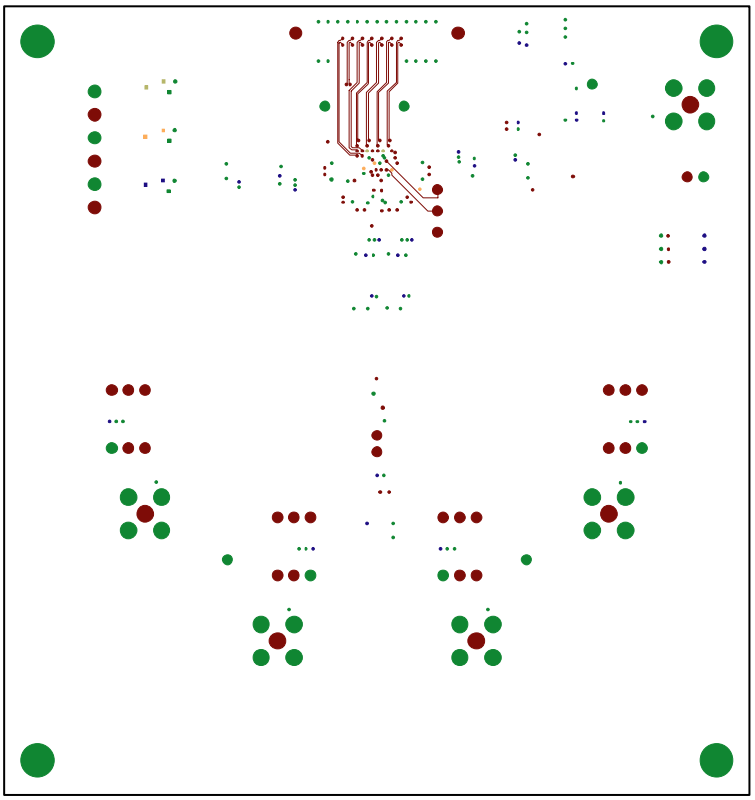


Figure 46. Evaluation Board Layout, Secondary Side

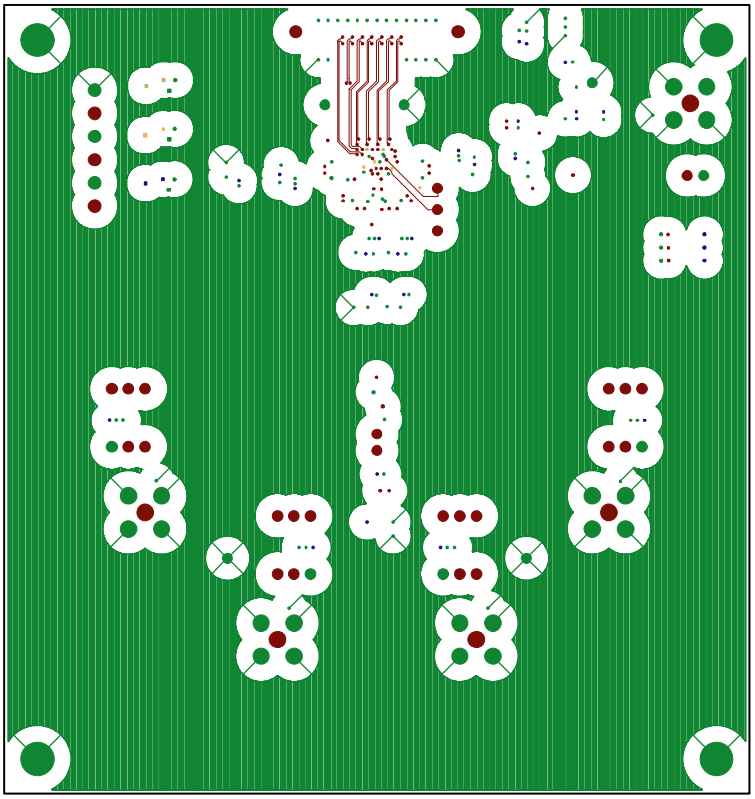


Figure 47. Evaluation Board Layout, Secondary Side (With Ground Copper Pour)

Table 11. Evaluation Board Bill of Materials (BOM)

Item	Qnty. per Board	REFDES	Device	Package	Value	Manufacturing	Mfg. Part Number
1	1	AD9289 BGA REVA/PCB	PCB	PCB	PCB	PCSM	PCSM
2	1	Assembly				Protronics	Protronics
3	8	R46, R48, R60, R61, R98, R99, R113, R114	RES_402	402	0	Yageo America	9C04021A0R00JLHF3
4	8	R5, R7, R8, R9, R10, R17, R33, R39	RES_402	402	10	Susumu Co Ltd	RR0510R-100-D
5	8	R22,R49, R52, R55, R79, R92, R101, R106	RES_402	402	25	Susumu Co Ltd	RR0510R-240-D
6	8	R11,R14, R23, R27, R31, R34, R44, R47	RES_402	402	33	Susumu Co Ltd	RR0510R-330-D
7	4	R38, R56, R91, R107	RES_402	402	50	Panasonic-ECG	ERJ-L14KF50MU
8	1	R73	RES_402	402	100	Yageo America	9C04021A1000FLHF3
9	8	R45, R50, R57, R58, R93, R94, R108, R111	RES_402	402	1K	Panasonic-ECG	ERJ-2GEJ102X
10	4	R35, R53, R81, R103	RES_402	402	1.2K	Panasonic-ECG	ERJ-2GEJ122X
11	13	R6, R32, R36, R51, R54, R72, R75, R78, R90, R100, R104, R37, R76	RES_402	402	10K	Susumu Co Ltd	RR0510P-103-D
12	6	R62, R63, R64, R65, R66, R71	BRES603	603	0	Panasonic-ECG	ERJ-3GEY0R00V
13	1	R102	BRES603	603	22	Susumu Co Ltd	RR0816Q-220-D
14	5	R15, R30, R41, R42, R83	BRES603	603	50	Susumu Co Ltd	RR0816Q-49R9-D-68R
15	23	R1, R12, R13, R16, R18, R19, R20, R21, R24, R29, R40, R43, R59, R68, R69, R70, R74, R77, R80, R82, R84, R109, R110	BRES603	603	1K	Susumu Co Ltd	RR0816P-102-D
16	2	R96, R97	BRES603	603	XXX		
17	4	C10, C21, C30, C41	CAP402	402	20PF	Kemet	C0402C220J5GACTU
18	36	C1, C35, C44, C47, C80, C250, C600, C11, C12, C14, C37, C40, C48, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73	CAP402	402	1UF	Panasonic-ECG	ECJ-0EF1C104Z
19	17	C2, C3, C4, C5, C6, C7, C15, C16, C18, C20, C25, C29, C36, C53, C108, C110, C183	BYPASSCAP	603	0.1UF	Kemet	C0603C104Z3VACTU
20	3	C100, C120, C163	TANTALUMB	805	10UF	Panasonic-ECG	ECJ-2FB0J106M
21	3	C170, C171, C176	TANTALUMB	T491B06K01	10UF	Kemet	T491B106K016AS
22	16	L1, L2 ,L3, L4, L6, L9, L10, L11, L12, L13, L19, L20, L21, L22, L27, L28	INDUCTOR_6	603	120NH	Murata	BLM18BB750SN1D
23	3	L5,L7,L8	IND1210	1210	10UH	Panasonic-ECG	ELJ-SA100KF
24	1	P6	PTMICRO6	PTMICRO6	6-Pole PCB Header	Wieland	Z5.531.3625.0

Item	Qnty. per Board	REFDES	Device	Package	Value	Manufacturing	Mfg. Part Number
	1				6-Pole PCB Connector	Wieland	25.600.5653.0
25	5	P1, P2, P3, P4, P5	SMBMST	SMB	SMBMST	Amphenol-RF Division	901-144-8RFX
26	4	T1, T2, T3, T4	ADT1-1WT	CD542_X65	ADT1-1WT	Minicircuits	ADT1-1WT
27	1	U17	HEADER	2MMSMT-872	WM18158-ND	Molex/Waldom Electronics Corp	87267-0850
28	1	U5	DIFF_CONN	FCN_268M01	DIFF_CONN	Fujitsu	FCN-268M012-G/1D
29	1	J6	MINIJMPR3	2MMSMT-872	MINIJMPR3	Molex/Waldom Electronics Corp	87267-0850
30	2	JP1, JP2	SGLJMPR	SGLJMPR	87267-0850	Samtec	TSW-120-07-G-S
31	2		11/4" STANDOFF	NYLON	1/4" 6-32	RAF	4040-632-N
32	2		6-32NUTS	NYLON	6-32	RAF	3058-N
33	1	U1	74VHC04MTC	TSSOP-14	74VHC04	Fairchild Semiconductor	74VHC04MTC
34	1	U2	FIN1017M	MO8A_(SOIC)	FIN1017M	Fairchild Semiconductor	FIN1017M
35	1	U4	AD9289BBC-65	9289BGA	9289BGA	ADI	AD9289BBC-65
36	1	U6	ADR510	SOT23	ADR510	ADI	ADR510
37	4	U7, U8, U9, U10	AD8351ARM	MSOP010	AD8351	ADI	AD8351ARM

OUTLINE DIMENSIONS

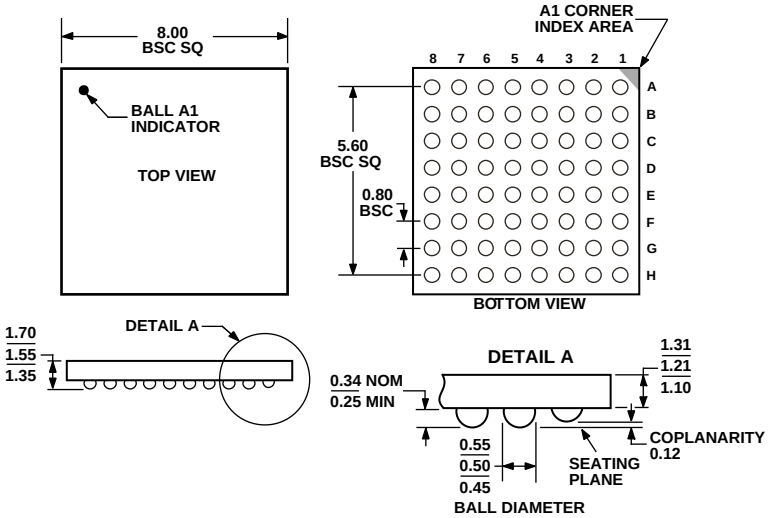


Figure 48. 64-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9289BBC	–40°C to +85°C	64-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-64-1
AD9289-65EB		Evaluation Board	

NOTES

NOTES

© 2004 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D03682-0-10/04(0)

ANALOG DEVICES

www.analog.com