

FEATURES

- **Error Detection and Handling (EDH) according to SMPTE RP-165**
- **drop-in replacement for the GS9021**
- **EDH insertion and extraction in one device**
- **auto-standard operation with override via host interface**
- **noise immune extraction of HVF timing signals**
- **TRS insertion/correction and ANC header correction for all standards**
- **ITU-R-601 output clipping for active picture area**
- **selectable I²C interface or 8-bit parallel port for access to EDH flags and device configuration bits**
- **all error flags available on dedicated output pins**
- **24-bit Errored Field counter**
- **BYPASS mode to bypass EDH insertion/updating**
- **dynamic blanking control input**
- **8-bit or 10-bit compatibility**
- **up to 54MHz operating frequency**
- **seamless flag-mapping with GS9020 serial digital video input processor**

APPLICATIONS

EDH processing for SMPTE 259M serial digital interfaces for composite and component standards including 4:4:4:4 at 540Mb/s; Noise immune digital sync and timing generation. Source, destination, distribution and test equipment; General purpose, TRS formatted, blank video stream generator with EDH.

DESCRIPTION

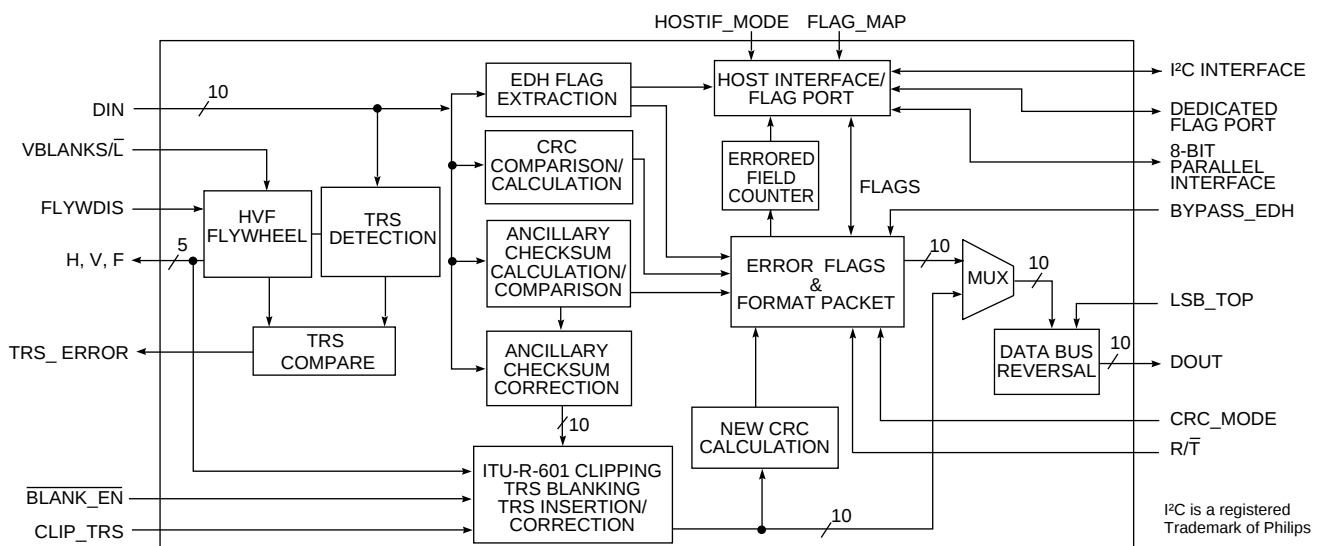
The GS9021A implements error detection and handling (EDH) according to SMPTE RP-165. Interfacing to the parallel inputs of either the GS9002, GS9022 or GS9032 serial digital encoders, the GS9021A is primarily used on the transmit end of the SDI interface. The GS9021A provides EDH insertion and extraction for 4fsc NTSC, 4fsc PAL and all component PAL and NTSC standards including 4:2:2 (13.5MHz and 18MHz luminance sampling), and 4:4:4:4.

The GS9021A generates noise immune timing signals such as horizontal sync, vertical blanking and field ID. In addition, TRS-ID correction/insertion and data blanking are implemented for all standards.

A host interface, configurable as an 8-bit parallel interface or an I²C (I²C is a registered trademark of Philips) serial interface allows for communication with a microcontroller. The interface can be used to read and/or write the complete set of error flags and override the flag status prior to re-transmission. A 5-bit flag port provides access to all error flags on dedicated pins for applications where the microcontroller is not used. The device automatically determines the operating standard, but this can be overridden through the programming interface.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS9021ACFU	64 pin LQFP Tray	0°C to 70°C



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.3V to 6.0V
Input Voltage Range (any input)	-0.3 to $V_{DD} + 0.3V$
Operating Temperature Range	0°C to 70°C
Storage Temperature	-55°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5.0V$, $T_A = 0$ to 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}		4.75	5.0	5.25	V	
Supply Current Unloaded	I_{DD}	27MHz	-	39	-	mA	
		54MHz	-	75	-	mA	
TTL Compatible CMOS Inputs	V_{ILMAX}		-	-	0.8	V	
	V_{IHMIN}		2.0	-	-	V	
	I_{IN}	$V_{IN} = V_{DD}$ or GND	-	-	150	μA	1
			-	-	1		2
	C_{IN}		-	10	-	pF	
TTL Compatible CMOS Outputs	V_{OLMAX}	at I_{OUT}	-	-	0.4	V	
	V_{OHMIN}	at I_{OUT}	2.4	-	-	V	
	I_{OUT}		-	4	-	mA	3
			-	2	-	mA	4

NOTES

1. The following inputs have internal pull-up resistors: R/T. The following inputs have internal pull-down resistors: FLYWIS, LSB_TOP, CRC_MODE, RESET, FLAG_MAP, HOSTIF_MODE and DIN[9:0]. To ensure reliable operation these pins should be externally connected to GND or V_{CC} .
2. All other inputs.
3. The following outputs have 4mA drivers (typical): S[1:0], FL[4:0], DOUT[9:0], H, V and F[2:0].
4. The following outputs have 2mA drivers (typical): P[7:0].

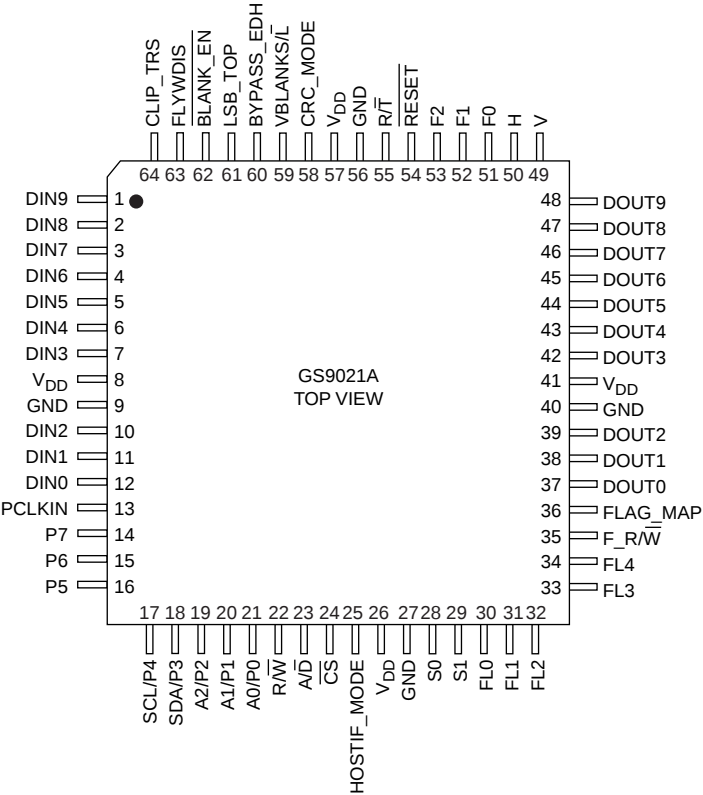
AC ELECTRICAL CHARACTERISTICSV_{DD} = 5.0V, T_A = 0 to 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Clock Frequency			-	-	54	MHz	
Clock Pulse Width Low	t _{PWL}		7.4	-	-	ns	
Clock Pulse Width High	t _{PWH}		7.4	-	-	ns	
Input Setup Time	t _S		3	-	-	ns	1, 2
Input Hold Time	t _H		3	-	-	ns	1, 2
Output Delay Time	t _{OD}	with 10pF loading	-	-	15	ns	2
Output Hold Time	t _{OH}	with 10pF loading	5	-	-	ns	2
Output Setup Time	t _{OS}	with 10pF loading	3.5	-	-	ns	2,4
Flag Port Disable Time	t _{FDIS}	with 25pF loading	-	-	15	ns	
Flag Port Enable Time	t _{FEN}	with 25pF loading	-	-	16	ns	
I ² C Clock Frequency	f _{SCL}		-	-	400	kHz	
Host Interface Setup Time	t _{HS}		6	-	-	ns	
Host Interface Hold Time	t _{HH}		6	-	-	ns	
Host Interface Output Enable Time	t _{HEN}	with 25pF loading	-	-	21	ns	
Host Interface Output Disable Time	t _{HDIS}	with 25pF loading	-	-	10	ns	
Reset Time Pulse Width	t _{RESET}		100	-	-	ns	
Device Latency	t _{LAT}		8	8	8	clks	3

NOTES

1. See section 1.2 for a list of signals synchronous and asynchronous to PCLKIN.
2. See Figures 1 and 2.
3. Latency is defined as the number of clock cycles between the time when the data is latched into the device and when the corresponding output data is clocked into the next device as shown in Figure 3.
4. Based upon 54MHz clock (18.5ns). Output Setup Time = Clock Period - Output Delay Time

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1-7, 10-12	DIN[9:0]	I	Parallel digital video data inputs.
13	PCLKIN	I	Parallel clock input.
14-16	P[7:5]	I/O	In parallel port mode, these are bits 7:5 of the host interface address/data bus. In I ² C mode, these pins must be set LOW.
17	SCL/P4	I/O	In parallel port mode, this is bit 4 of the host interface address/data bus. In I ² C mode, this is the serial clock input for the I ² C port.
18	SDA/P3	I/O	In parallel port mode, this is bit 3 of the host interface address/data bus. In I ² C mode, this is the serial data pin for the I ² C port.
19-21	A[2:0]/P[2:0]	I/O	In parallel port mode, these are bits 2:0 of the host interface address/data bus. In I ² C mode, these are input bits which define the I ² C slave address for the device.
22	R/W	I	Parallel port read/write control. When HIGH, the parallel port is configured as an output (read mode). When LOW, the parallel port is configured as an input (write mode). In I ² C mode, this pin must be set HIGH.
23	A/D	I	Parallel port address/data bus control. When HIGH, the parallel port is used for address input. When LOW, the parallel port is used for data input or output. In I ² C mode, this pin must be set LOW.
24	CS	I	Parallel port chip select. When CS is LOW and R/W is HIGH, the GS9021A drives the address/data bus. When CS is LOW and R/W is LOW, the user should drive the address/data bus. When CS is HIGH, the address/data bus is in a high impedance state (Hi - Z). In I ² C mode, this pin must be set HIGH.
25	HOSTIF_MODE	I	Host Interface mode select. When HIGH, the host interface is configured for I ² C mode. When LOW, the host interface is configured for parallel port mode.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
28, 29	S[1:0]	I/O	Control bits which select whether FF, AP, or ANC EDH flags are active on the EDH flag data port (FL[4:0]). In FLAG_MAP mode, the S[1:0] pins become outputs (see device description).
30-34	FL[4:0]	I/O	EDH flag data port to allow access to the EDH flags.
35	F_R/ $\overline{W}$	I	Flag port read/write control. When HIGH, FL[4:0] are configured as outputs allowing EDH flags to be read from the device. When LOW, FL[4:0] are configured as inputs allowing EDH flags to be overwritten into the outgoing EDH packet. In FLAG_MAP mode this pin must be set HIGH.
36	FLAG_MAP	I	FLAG_MAP mode enable. When HIGH, FLAG_MAP mode is enabled. When LOW, FLAG_MAP mode is disabled.
37-39, 42-48	DOUT[9:0]	O	Parallel digital video data outputs.
49	V	O	Vertical sync indication.
50	H	O	Horizontal sync indication.
51-53	F[2:0]	O	Field indication. F2 is the MSB.
54	$\overline{\text{RESET}}$	I	Reset. When LOW, the internal control circuitry is reset.
55	R/ $\overline{T}$	I	Receive/Transmit mode select. When HIGH, the device operates in receive mode. When LOW, the device operates in transmit mode.
58	CRC_MODE	I	CRC_MODE enable. When HIGH, CRC_MODE is enabled. When LOW, CRC_MODE is disabled.
59	VBLANKS/ $\overline{L}$	I	Vertical blanking interval control. For NTSC signals, when VBLANKS/ $\overline{L}$ is set LOW the 19 line blanking interval is selected and when set HIGH the 9 line blanking interval is selected. For PAL D2 signals, when VBLANKS/ $\overline{L}$ is set LOW the 17 line blanking interval is selected and when set HIGH the 7 line blanking interval is selected. For PAL component signals VBLANKS/ $\overline{L}$ should be set LOW.
60	BYPASS_EDH	I	Bypass EDH control. When HIGH, the device allows the EDH packet to pass through unaltered.
61	LSB_TOP	I	Data output LSB position control. When HIGH, the video data output bus is reversed, placing the LSB at pin 48.
62	$\overline{\text{BLANK_EN}}$	I	Blanking enable. When LOW, incoming data words are set to appropriate blanking levels.
63	FLYWDIS	I	Flywheel disable. When HIGH, the internal flywheel is disabled. When LOW, the internal flywheel is enabled.
64	CLIP_TRS	I	Clip and TRS correction control. When HIGH, the TRS Blanking, ITU-R-601 clipping and TRS insertion features are enabled.
8, 26, 41, 57	V _{DD}		Power supply (nominally +5V).
9, 27, 40, 56	GND		Ground.

DETAILED DESCRIPTION

The GS9021A EDH coprocessor consists of five major blocks:

1. Data Input/Output Block (with automatic standard detect)
2. Flywheel Block
3. EDH Block
4. Data Processing Block
5. Host Interface (HOSTIF) Block

The following convention is used to differentiate device pins from HOST interface table bits.

PIN	LOGIC OPR	HOSTIF
XX		YY

LOGIC OPR (logic operator) gives the combinational relationship (if one exists), between pins which also have a corresponding HOST bit. This operator governs the signal the GS9021A receives. The following is the list of possible logic operators and their meaning.

LOGIC OPR	MEANING
AND	XX AND YY
OR	XX OR YY
>	XX takes precedence over YY
<	YY takes precedence over XX

1. DATA INPUT/OUTPUT BLOCK

1.1 Parallel Digital Video Data Inputs

PIN	LOGIC OPR	HOST BIT
DOUT[9:0]		

Parallel digital video data is supplied to the GS9021A chip via the DIN[9:0] input pins. The data is clocked into the GS9021A by the rising edge of PCLKIN.

Eight input signal standards are supported: Composite, 4:2:2 Component with 13.5MHz Y sampling, 4:2:2 16 x 9 wide screen with 18 MHz Y sampling, and 4:4:4:4 Component Single Link with 13.5MHz Y sampling, all in both NTSC and PAL formats (See Table 1). Both 8 and 10 bit inputs are supported. However, when using 8 bit data, the 2 LSBs of the input must be tied to GND.

1.2 Parallel Clock Inputs

PIN	LOGIC OPR	HOST BIT
PCLKIN		

The PCLKIN pin is the input used to clock the video data into the GS9021A, and serves as the reference to which all synchronous inputs and outputs are timed. The following table shows which pins are synchronous with PCLKIN and which are not. Timing for synchronous I/O is found in Figures 1 and 2.

SYNCHRONOUS	ASYNCHRONOUS
FL[4:0]	P[7:5]
S[1:0]	SCL/P4
$\overline{\text{FIFO_RESET}}$	$\overline{\text{INTERRUPT}}$
DOUT[9:0]	SDA/P3
F[2:0]	A[2:0]/P[2:0]
V	R/ $\overline{W}$
H	A/ $\overline{D}$
ANC_DATA	$\overline{\text{CS}}$
$\overline{\text{BLANK_EN}}$	FLAG_MAP
F_R/ $\overline{W}$	$\overline{\text{RESET}}$
NO_EDH	CRC_MODE
STD[3:0]	VBANKS/ $\overline{\text{L}}$
TRS_ERROR	HOSTIF_MODE
DIN[9:0]	FIFOE/ $\overline{\text{S}}$
	FLYWDIS
	BYPASS_EDH
	SDO_MODE
	ANC_CHKSM
	CLIP_TRS

1.3 Parallel Digital Video Data Outputs

PIN	LOGIC OPR	HOST BIT
DOUT[9:0]		
LSB_TOP		

The output of the device is 10-bit digital video data and is present on the DOUT[9:0] output pins. The latency through the device is 8 clock cycles and is illustrated in Figure 3.

The default position of the LSB is DOUT0. Asserting the LSB_TOP pin HIGH on the GS9021A reverses the order of the output bits, placing the LSB at DOUT9 and simplifying board layout in some applications. Figure 11 shows a simple application circuit illustrating the connections to the GS9032.

1.4 Automatic Standard Detection

PIN	LOGIC OPR	HOST BIT
		STD_SEL
		STD[3:0]
		S

The device automatically detects the incoming video standard. The detected standard is encoded on the STD[3:0] bits of the HOSTIF read table as shown in Tables 1 and 4.

TABLE 1

STANDARD NAME	STD[3:0]
NTSC 4:2:2 Component with 13.5MHz Y sampling	0000
NTSC Composite	0001
NTSC 4:2:2 16x9 Widescreen with 18MHz Y sampling	0010
NTSC 4:4:4:4 Single Link with 13.5MHz Y sampling	0011
PAL 4:2:2 Component with 13.5MHz Y sampling	0100
PAL Composite	0101
PAL 4:2:2 16x9 Widescreen with 18MHz Y sampling	0110
PAL 4:4:4:4 Single Link with 13.5MHz Y sampling	0111

Noise immunity is included to ensure that momentary signal corruption does not affect the automatic standards detection function. This built in noise immunity results in delayed detection time during power up and when switching between standards. Delays range from as little as eight lines when switching between component standards

to as much as four frames when switching between PAL and NTSC standards. If this delay is intolerable, the user can manually set the standard through the HOSTIF write table. To set the standard manually, the STD_SEL bit must be set HIGH and the S bit and STD[3:0] bits set accordingly. The default standard upon resetting the device is NTSC 4:2:2 component (13.5MHz Y sampling).

The S bit, used for single link data standards only, is encoded in the TRSID word and indicates if the data is in RGB or YC_RC_B format as per SMPTE RP174. In automatic standard detection mode, the S bit can be read from the HOSTIF read table. In manual mode, the S bit must be set in the HOSTIF write table.

2. FLYWHEEL BLOCK

2.1 FVH Flywheel

PIN	LOGIC OPR	HOST BIT
FLYWDIS	OR	FLYWDIS
		SWITCHFLYW

The flywheel's primary function is to provide accurate field, vertical, and horizontal output signals in the presence of noisy or error prone input data. Flywheel synchronization is based on the TRS words in the incoming data stream. The FVH flywheel synchronizes to the incoming data stream in less than two fields once the incoming standard has been detected. Once synchronized, the TRS words in the incoming data stream and those generated by the flywheel are constantly compared to ensure that the flywheel remains synchronized.

Noise insensitivity is accomplished by re-synchronizing the flywheel to the data stream only if it is not aligned for long periods of time. For component signals, four mismatches between the EAV signal in the incoming and flywheel generated signals over a window of eight lines will trigger the flywheel to begin re-synchronization.

For composite signals, re-synchronization is triggered by mismatches in the TRS encoded line numbers or field bits for seven consecutive lines.

The flywheel can be disabled by asserting the FLYWDIS control signal HIGH. Disabling the flywheel will remove the effective noise immunity. In this mode, FVH values will be decoded directly from the incoming data stream rather than being decoded from the flywheel. Note that when the flywheel is disabled, TRS_BLANK and TRS_INSERT will not function correctly if enabled. Therefore, if the flywheel is disabled, then so should TRS_BLANK and TRS_INSERT. FLYWDIS is available as an input pin and as a bit in the HOSTIF write table.

The SWITCHFLYW control signal is used in applications where the data input to the GS9021A is switched between two synchronous signals. In this case, the two signals may be slightly misaligned and would normally require the flywheel to completely re-synchronize. In this scenario, the re-synchronization time would be undesirable. Asserting the SWITCHFLYW bit of the HOSTIF write table HIGH allows the flywheel to re-synchronize to the new incoming signal at the end of the switching line. For this functionality to operate properly, the two signals must both be in the active picture portion of the switching line at the time of the switch.

2.2 Accurate FVH Timing Signals

PIN	LOGIC OPR	HOST BIT
F[2:0]		F[2:0]
V		
H		
VBANKS/ $\bar{L}$	AND	VBANKS/ $\bar{L}$

The F[2:0] signals indicate the current field of the video data. Three F bits are necessary to accommodate the composite PAL standard which has 8 fields. For component standards only F0 is used to represent F = 0 or F = 1. The F[2:0] bits are available on dedicated output pins and via the HOSTIF read table. Figure 4a and 4b illustrate the position of the F[2:0] transition within a line for component and composite signals, respectively. The lines on which the transitions occur conform to the SMPTE standards.

For component signals, the horizontal (H) signal is HIGH during the horizontal blanking region of the output signal, from EAV to SAV inclusive. For composite signals, the H signal remains HIGH only for the 3FF, 000, 000, 000, and TRSID words. Figure 4a and 4b illustrate the H output signal timing for component and composite signals, respectively.

The vertical (V) signal timing is dependent on the incoming video standard and the VBANKS/ $\bar{L}$ control signal. The VBANKS/ $\bar{L}$ signal is available as an input pin and via the HOSTIF write table and should be set to indicate the form of the incoming data stream. This allows the flywheel to correctly structure the V bit for flywheel synchronization, TRS insertion, and TRS error indication.

For component based standards, the transition of the V output signal within a line is shown in Figure 4a. The line on which the V output signal transitions from HIGH to LOW is summarized in the following table.

The lines on which the LOW to HIGH transition occurs conform to the SMPTE standards.

STANDARD	VBANKS/ $\bar{L}$ =1	VBANKS/ $\bar{L}$ =0
NTSC 4:2:2 Component (13.5MHz Y sampling)	9/272	19/282
NTSC 4:2:2 16x9 Widescreen (18MHz Y sampling)	9/272	19/282
NTSC 4:4:4:4 Single Link (13.5MHz Y sampling)	9/272	19/282
PAL 4:2:2 Component (13.5MHz Y sampling)	22/335	22/335
PAL 4:2:2 16x9 Widescreen (18MHz Y sampling)	22/335	22/335
PAL 4:4:4:4 Single Link (13.5MHz Y sampling)	22/335	22/335

For composite based standards, the V output signal is asserted HIGH as described in the table below:

	VBANKS/ $\bar{L}$ =1	VBANKS/ $\bar{L}$ =0
NTSC Composite	from Line 525/ Sample 768 to Line 9/ Sample 767 inclusive AND from Line 263/ Sample 313 to Line 272/ Sample 767 inclusive	from Line 525/ Sample 768 to Line 19/ Sample 767 inclusive AND from Line 263/ Sample 313 to Line 282/ Sample 767 inclusive
	VBANKS/ $\bar{L}$ =1	VBANKS/ $\bar{L}$ =0
PAL Composite	from Line 623/ Sample 382 to Line 5/ Sample 947 inclusive AND from Line 310/ Sample 948 to Line 317/ Sample 947 inclusive	from Line 623/ Sample 382 to Line 15/ Sample 947 inclusive AND from Line 310/ Sample 948 to Line 327/ Sample 947 inclusive

2.3 TRS Errors

PIN	LOGIC OPR	HOST BIT
		TRS_ERROR

The flywheel is also used to indicate TRS errors. These errors are detected by comparing the TRS in the incoming data stream with the expected TRS based on the internal flywheel.

If a mismatch occurs, the TRS_ERR signal is immediately set HIGH and maintained HIGH until a correct TRS occurs. The types of TRS errors detected are:

- TRS missing
- TRS in wrong location
- TRS-ID is different from the one generated by the flywheel

The TRS_ERR signal is available via the HOSTIF read table. TRS_ERR signal should only be considered valid if the flywheel is enabled.

3. EDH PROCESSING BLOCK

This section describes the GS9021A's EDH features and functionality.

3.1 Receive and Transmit Modes

PIN	LOGIC OPR	HOST BIT
$R/\bar{T}$		

In normal operation, the GS9021A is configured for one of two modes, Receive ($R/\bar{T}$ = HIGH) or Transmit ($R/\bar{T}$ = LOW) mode.

Transmit mode is appropriate for equipment which accepts video that has no EDH packets or source equipment which must generate a video stream with EDH. Receive mode is appropriate for equipment where the input data already contains EDH information. When the GS9021A is configured in receive mode, the device expects to find an EDH packet in the incoming data stream. The encoded CRC values in the incoming data stream are compared with the calculated CRC values as discussed in more detail below. Error flags are set based on the results of these comparisons. If no EDH packet is present, a new EDH packet is inserted (as in transmit mode) but the UES flags are set to 1. In transmit mode, no comparison is performed but a new EDH packet is inserted with the calculated CRC values. All flags are set to 0, unless set otherwise by the HOSTIF or flag port. See Table 2 for the effect of the different settings of $R/\bar{T}$ and CRC_MODE. Receive or Transmit mode is set via the $R/\bar{T}$ control pin.

3.2 Error Flags

All 15 EDH error flags can be read from the HOSTIF read table. The INCOMING ERROR FLAGS represent the EDH error flags present in the incoming EDH packet. The OUTGOING ERROR FLAGS represent the EDH error flags present in the outgoing EDH packet (after modification by the GS9021A).

PIN	LOGIC OPR	HOST BIT
		INCOMING ERROR FLAGS
		OUTGOING ERROR FLAGS
		STICKY IN
		STICKY OUT
		OVERWRITE VALUES
		OVERWRITE CONTROL
		RO_CTRL
		RESERVED WORDS (INCOMING)
		RESERVED WORDS (OUTGOING)

The INCOMING and OUTGOING ERROR FLAGS, the incoming Validity bits (FFV and APV), and the EDH_CHKSM bit can be made "sticky". Sticky error flags that detect an error for a field remain asserted until a HOSTIF read is performed on those error flags. Sticky mode allows the user to perform HOSTIF reads on the error flags to detect if any errors have occurred since the last read, and are particularly useful when a read cannot be performed after every field. When STICKY IN is asserted HIGH, the incoming flags and validity bits are in sticky mode. When STICKY OUT is asserted HIGH, the outgoing flags and the EDH_CHKSM bit are in sticky mode. STICKY IN and STICKY OUT are available in the HOSTIF write table. The ERROR FLAGS and the EDH_CHKSM bit are sticky HIGH. That is, once they are set HIGH, they remain HIGH until a read operation. The validity bits are sticky LOW. That is, once they are set LOW, they remain LOW until a read operation.

In some applications, the user may wish to insert user defined EDH error flags into the outgoing EDH packet. The desired outgoing error flags are written into the OVERWRITE VALUES words of the HOSTIF write table and are placed in the outgoing EDH packet when the corresponding OVERWRITE CONTROL bit is asserted HIGH. See Table 3 for Host Interface WRITE table.

The GS9021A also allows the user to overwrite the 7 reserved words of the OUTGOING EDH packet. When RO_CTRL (Reserved Word Overwrite Control) is asserted HIGH, the GS9021A overwrites the reserved words in the OUTGOING EDH packet with those specified in the HOSTIF write table. If RO_CTRL is LOW, the GS9021A does not alter the reserved words. RO_CTRL is a control bit in the HOSTIF write table. The reserved words of the INCOMING EDH packet are also available via the HOSTIF read table.

3.3 CRC Calculation And Updating

PIN	LOGIC OPR	HOST BIT
		INCOMING FF CRC
		OUTGOING FF CRC
		INCOMING AP CRC
		OUTGOING AP CRC

Since the device has the potential of modifying the full-field and active picture data with features like ITU-R-601 clipping and TRS insertion, the full field and active picture CRC values must be calculated for both the incoming and outgoing data streams. The calculated CRC values based on the incoming data stream are used for comparison with the embedded CRC values. However, the calculated CRC values based on the outgoing data stream are the ones inserted into the data stream. As a result, the CRC values in the outgoing data stream correctly reflect the contents of the outgoing data stream.

The INCOMING FF and AP CRC values for the Full Field (FF) and Active Picture (AP) regions can be read from the HOSTIF read table. Similarly, the OUTGOING (calculated) FF and AP CRC values for the Full Field and Active Picture regions can be read from the HOSTIF read table.

3.4 Validity Bit

PIN	LOGIC OPR	HOST BIT
		FFV
		APV

The VALIDITY (V) bits (as per SMPTE 165) present in the incoming EDH packet are used to indicate whether the CRC values are valid or invalid. If the V bit is HIGH, the CRC value is considered valid. In this case, the incoming CRC value is compared with the calculated CRC value to identify errors. If the V bit is LOW, the incoming CRC is invalid and a CRC comparison is not performed. If the device receives an EDH packet with the V bit set LOW it behaves as follows:

1. EDH = 0 (Not asserted for an invalid CRC)
2. EDA = EDAin "OR" EDH_{in} (EDA calculated as usual)
3. A new calculated CRC value replaces the invalid one in the output EDH packet
4. The V bit will be set HIGH in the output EDH packet

5. Depending on whether one or both of FFV or APV is low, the Unknown Error Status (UES) flag corresponding to either FF or AP or both, is set HIGH in the output data. (No CRC check could be performed, so the data may or may not contain errors).

The incoming V bits for the Full Field and Active Picture regions are available in the HOSTIF read table as FFV and APV, respectively. Outgoing full field (FFV) and active picture (APV) validity bits are set HIGH unless explicitly over-written through the HOSTIF write table or the flag port.

3.5 Ancillary Checksum Verification

PIN	LOGIC OPR	HOST BIT
		ANC_CHKSM
		EDH_CHKSM

For each received ANC packet in the incoming data, the device compares the calculated checksum value to the embedded checksum for that ANC packet. If the checksum values do not match for any ANC packets within a field, an error is reported via the ANC EDH flag in the EDH packet. In addition, if the ANC_CHKSM input pin or HOSTIF write table bit is asserted HIGH, the ancillary checksum correction block is enabled and the checksum in the ANC packet is replaced with the calculated one. This update is required to prevent the ANC data error from being flagged at every downstream EDH chip.

When implementing applications which use the EDH core (ie. BYPASS_EDH set LOW), the ANC_CHKSM function will indicate a downstream FF/AP EDH error when an illegal/non-allowed (3FC_H-3FF_H) ANC_CHKSM input value is detected. As such, these values should not be present in the incoming data and the corresponding FF/AP EDH errors should not occur. However, if the user wishes to disable the ANC_CHKSM function, it can be deactivated by setting both the ANC_CHKSM pin and the ANC_CHKSM host interface bit LOW.

If the chip is receiving ANC EDH flag information through the flag port or the HOSTIF, then the ANC EDH flag generated by the ancillary checksum verification block will be overwritten. However, the additional FF/AP EDH flag will still appear at the next downstream chip if an illegal checksum of 3FC_H-3FF_H was detected and the ANC_CHKSM function was enabled.

If a checksum error is detected in the EDH packet itself, an additional separate error flag, EDH_CHKSM is set HIGH in the HOSTIF read table.

3.6 UES Error Flag Updating

In receive mode, a UES flag is set HIGH in the outgoing EDH packet if the corresponding UES flag was HIGH in the incoming packet or if the corresponding V bit was LOW. (For example, if the incoming Active Picture V bit is LOW, the outgoing Active Picture UES bit will be HIGH). If there is no EDH packet in the incoming data, all three UES flags (ANC, AP, FF) are set HIGH.

3.7 No EDH

PIN	LOGIC OPR	HOST BIT
		NO_EDH

Some input data streams may lack the EDH packet. In such cases, the NO_EDH bit in the HOSTIF read table is asserted HIGH. If only a few fields lack the EDH packet, the NO_EDH bit will be asserted only for those fields.

In determining if the input data stream contains an EDH packet, the GS9021A looks for two things. First, the presence of an ANC packet with the header 000 3FF 3FF 1F4 and second, that the ANC header is in the right spot for the video standard detected. The NO_EDH signal is a logical NAND of these two cases. If either one is false, the NO_EDH flag is set.

3.8 Errored Field Counter

PIN	LOGIC OPR	HOST BIT
		ERRORED FIELD COUNTER CLR[1:0] ERROR SENSITIVITY BITS

The device has a 24 bit ERRORED FIELD COUNTER. The counter increments by one on the occurrence of one or more error flags in an OUTGOING EDH packet. The error flags that can increment the counter are user-selectable through the 16 ERROR SENSITIVITY bits in the HOSTIF write table.

The error flag SENSITIVITY bits are active LOW, so that if a particular sensitivity bit is set LOW, the counter is sensitive to errors of that type in the OUTGOING EDH packet. The EDH_CHKSM SENSITIVITY bit is active HIGH.

There are four methods of counter operation. The mode is set through 2 bits in the HOSTIF write table, denoted CLR1 and CLR0.

In "Normal" mode the counter operates as previously discussed, such that the counter increments on detection of any error for which the sensitivity flags are set HIGH. If "Reset Counter to Zero" mode is selected, the counter is

CLR1	CLR0	MODE OF OPERATION
0	0	Normal
0	1	Reset Counter to Zero
1	0	Auto Reset
1	1	Hold Counter at Zero

reset to zero and begins counting again. The mode of operation will immediately return to 00 (normal mode) once the counter resets. In "Auto Reset" mode, the counter behaves in the normal fashion, except that it resets to zero every time a HOSTIF read of the lowest 8 bits of the error counter (address 17) is performed. This functionality allows the chip to count the number of errors since the last read. The "Hold Counter at Zero" mode instantly freezes the counter at zero until it is moved into one of the other modes.

3.9 Flag Port

PIN	LOGIC OPR	HOST BIT
F_R $\overline{W}$ S[1:0] FL[4:0]	>	OVERWRITE VALUES

In addition to the HOSTIF tables, the EDH error flags can also be read and written via the synchronous flag port. The five flag port pins, FL[4:0], allow access to all 15 error flags. The select pins S[1:0] control which flags are read/written as outlined below. If the flag port is not going to be used, it is best to set F_R $\overline{W}$ HIGH, leave FL[4:0] unconnected and set S[1:0] to any value desired but not floating.

3.9.1 Write Mode

When the F_R $\overline{W}$ pin is LOW, the flag port is in write mode and the FL[4:0] pins are configured as inputs. After writing to the flag port, the GS9021A inserts the written flags into the next outgoing EDH packet. Note that external flag overwriting via the flag port takes precedence over HOSTIF overwriting but the flag port write only affects the next outgoing EDH packet. Following this, if the flag port is not written to again, flag operation is returned to normal EDH functionality (unless it is being overwritten through the HOSTIF).

The data present on the FL[4:0] output pins, as controlled by the S[1:0] pins, is summarized below.

In addition to overwriting the 15 error flags, the outgoing validity bits for the active picture (APV) and full field (FFV) can be overwritten via the flag port.

Write Mode, $F_R/\overline{W} = 0$

S[1:0]	FL4	FL3	FL2	FL1	FL0
00	FF UES	FF IDA	FF IDH	FF EDA	FF EDH
01	AP UES	AP IDA	AP IDH	AP EDA	AP EDH
10	ANC UES	ANC IDA	ANC IDH	ANC EDA	ANC EDH
11	IN/ $\overline{OUT}$	APV	FFV	0	0

The IN/ $\overline{OUT}$ bit has no effect on writes to the error flags. IN/ $\overline{OUT}$ is a control bit used to determine if the flags read from the flag port during flag port read cycles represent incoming or outgoing EDH flags. If this bit is set HIGH, all subsequent reads are from the incoming EDH packet. If this bit is set LOW, then all subsequent reads are from the updated outgoing packet. When the IN/ $\overline{OUT}$ bit is written to, the value remains latched until it is reprogrammed. The IN/ $\overline{OUT}$ bit is set LOW upon reset of the chip.

3.9.2 Read Mode

When the $F_R/\overline{W}$ pin is HIGH, the flag port is in read mode and the FL[4:0] pins are configured as outputs. The data present on the FL[4:0] output pins, as controlled by the S[1:0] pins, is summarized below.

Read Mode, $F_R/\overline{W} = 1$

S[1:0]	FL4	FL3	FL2	FL1	FL0
00	FF UES	FF IDA	FF IDH	FF EDA	FF EDH
01	AP UES	AP IDA	AP IDH	AP EDA	AP EDH
10	ANC UES	ANC IDA	ANC IDH	ANC EDA	ANC EDH
11	EDH_CHKSUM	APV	FFV	S	

Note that the 15 error flags can be read from the incoming or outgoing EDH packet (see IN/ $\overline{OUT}$ control bit above). However, the EDH_CHKSM flag available on pin FL4 when S[1:0] = 11 is only valid if IN/ $\overline{OUT}$ is LOW. Also, the APV and FFV bits available on pins FL[3:2] when S[1:0] = 11 are only valid when IN/ $\overline{OUT}$ is HIGH (that is, the validity bits are always read from the incoming EDH packet). The S bit is available regardless of the state of the IN/ $\overline{OUT}$ bit.

3.9.3 Flag Port READ/WRITE Timing

Figure 5a shows a FLAG PORT write cycle followed by a FLAG PORT read cycle and illustrates the read/write timing requirements.

A write cycle is initiated by changing the $F_R/\overline{W}$ signal from HIGH to LOW.

The first time the device samples the $F_R/\overline{W}$ LOW (at t_0) it is instructed to stop driving the FL[4:0] pins. On each subsequent rising clock edge (and $F_R/\overline{W}$ LOW) the device latches in the data present on S[1:0] and FL[4:0] (at t_1 , t_2 , t_3 and t_4). In this example, the S[1:0] pins begin at "00" and are incremented each clock cycle to update all the error flags, validity bits, and the IN/ $\overline{OUT}$ control bit. Note that if a write cycle is performed to update, say the FF error flags (S[1:0] = 00), only the FF flags are updated, and the others are unaffected.

A delay time, t_{FDS} , is necessary to change the FL[4:0] pins from output mode to input mode as defined in the AC timing table (See Fig.5b). The external controller can begin to drive the FL[4:0] bus after this delay time. A simple way to allow for this is to wait one clock cycle before starting to drive the FL[4:0] port and thus prevent bus contention (but set the S[1:0] inputs when $F_R/\overline{W}$ goes LOW so the flags are not unintentionally affected).

At t_5 , the $F_R/\overline{W}$ pin is sampled HIGH, indicating a read operation. Also at this time, the device reads in the information on the S[1:0] pins. Upon sampling a read operation, the device will begin driving the FLAG PORT after a delay, t_{FEN} , (see Fig. 5c), with invalid data. The requested information is output on the FL[4:0] pins on the subsequent clock, t_6 , plus an output delay time, (see AC timing table and Fig. 2). That is, there is a one clock latency between sampling of the S[1:0] pins and when the corresponding output information is presented on the FL[4:0] pins. In this example, the S[1:0] pins begin at "00" and are incremented each clock cycle to read all the error flags, EDH_CHKSM, validity, and S bits.

The FLAG PORT is synchronous to the clock pin (PCLKIN) and hence adequate setup and hold times must be provided as indicated in the AC timing information and Fig. 1. FLAG PORT read/write cycles, relative to the data stream, should take place as outlined in section 5.3 (HOST INTERFACE READ/WRITE TIMING)

3.10 CRC_MODE and FLAG_MAP Mode

PIN	LOGIC OPR	HOST BIT
CRC_MODE	OR	FLAG_MAP
FLAG_MAP		

A common configuration is to have an input EDH chip that checks for errors at the input of a piece of equipment, followed by a processing block that manipulates the data, followed by an output EDH chip that updates the CRC values in the EDH packet before the data exits the equipment. Because the processing block changes the data values, the CRC values in the EDH packet no longer represent the data stream. The output EDH chip updates

the CRC values to correctly reflect the newly modified data. To prevent the output EDH chip from indicating erroneous CRC errors on each field, the GS9021A has two special modes of operation, CRC_MODE and FLAG_MAP MODE.

3.10.1 CRC_MODE

In CRC_MODE, the CRC values in the EDH packet are updated by the chip but the error flags are preserved and unaltered, unless they are overwritten via the HOSTIF or the FLAG PORT. This mode should be used by the output EDH chip to prevent the newly processed data from creating misleading EDH errors due to CRC mismatches. The CRC_MODE pin takes precedence over the $R/\bar{T}$ pin in the GS9021A with respect to the handling of the EDH flags. Thus when CRC_MODE is HIGH, no flags are set or altered (unless overwritten by the flags or HOSTIF port) regardless of the state of the $R/\bar{T}$ pin. See Table 2 for the effect of the different settings of $R/\bar{T}$ and CRC_MODE. The device is placed in CRC_MODE by asserting the CRC_MODE pin HIGH.

CRC_MODE is applicable when the processing circuitry does not corrupt the EDH packet, as illustrated in Figure 6a. In this configuration, the input EDH chip operates in normal mode while the output EDH chip is in CRC_MODE. In this scenario, the input IC receives the EDH packet and does normal EDH processing. The output IC updates the EDH packet with new CRC values but passes the EDH flags through unaltered. Because of this, erroneous EDH flag handling by the second GS9021A is not performed.

3.10.2 FLAG_MAP Mode

In FLAG_MAP mode, the FLAG PORT is used to read EDH flags from the GS9021A and write them to another EDH chip. To enable FLAG_MAP mode, the FLAG_MAP mode pin and the $F_R/\bar{W}$ pin must be asserted HIGH (set $F_R/\bar{W}$ at least one cycle ahead of FLAG_MAP). After a delay of t_{FEN} , the FL[4:0] and S[1:0] pins of the FLAG PORT become outputs and can be connected to the chip which you wish the GS9021A to write the FLAG data to. In this mode the GS9021A automatically increments the value of S[1:0] and subsequently displays the appropriate flags on the FL[4:0] port, synchronous to the rising edge of PCLKOUT. This is illustrated in Figure 5d.

Figure 5d displays three properties of the FLAG PORT in FLAG_MAP mode.

First, each data is present on the FLAG PORT for two clock cycles to eliminate any setup time violations that might occur due to clock data skew between chips placed far apart. However, the designer must still ensure that the hold time is satisfied. Second, the S[1:0] pins never cycle to the value of "11" in FLAG_MAP mode since the values contained in the FL[4:0] register when S[1:0] = "11" are not considered EDH flags. Also, the chip cycles S[1:0] in the sequence "01", "00", "10" since this is the order in which the flags are stored and subsequently decoded from the EDH

packet. Finally the S[1:0] pins only change value after receipt of an EDH packet and are thus static between packets. During this inter-packet time, the S[1:0] pins display a value of "01" and the FL[4:0] pins display the ANC EDH flags from the preceding EDH packet.

For reliable data output on the FLAG PORT, switching the FLAG_MAP pin when an EDH packet is exiting the device is not advised. Also, if the EDH core is bypassed by asserting the BYPASS_EDH pin HIGH, the flag port will always display zeros. This is because the incoming flags (which will be decoded and written to the HOSTIF table) will not be updated to reflect the condition of the input data, and as a result no outgoing flags will be generated (the FLAG PORT only displays the outgoing EDH flags).

FLAG_MAP mode can be used to write EDH flags to any chip, the most common use being applicable when the processing circuitry following the EDH chip corrupts the EDH packet. In this case, the FLAG_MAP mode can be used to route the EDH flags from an input EDH chip around the processing core and write them to an output EDH chip. In this configuration, the input IC is in FLAG_MAP mode. It receives the EDH packet, does normal EDH processing and transfers the new EDH flags to the output IC. The output IC, which is not in FLAG_MAP mode but is in write mode (FLAG_MAP and $F_R/\bar{W}$ stay LOW) receives these flags as they are written to it by the EDH chip. The output EDH chip then updates the EDH packet with the new CRC values and inserts the preserved EDH flags that have been transferred from the input IC. A diagram of this can be found in Figure 6b.

Because the flags are output as soon as they are decoded, the maximum processing latency supported between the two EDH chips is the number of clock cycles in the shortest field of the standard minus 15 clock cycles.

For example, D1 has one field of $262 \times 1716 = 449592$ clock cycles, and one field of $263 \times 1716 = 451308$ clock cycles. Thus the maximum latency for D1 is $449592 - 15 = 449577$ clock cycles.

Any additional latency requires that the flags be delayed before they can be piped to the output chip. Since writing to the flag port takes precedence over the HOSTIF writing, if any of the flags need to be forced at the output EDH chip, external logic in the routing path must be added. Alternately, the HOSTIF of the EDH chip can be used to perform any additional flag masking.

3.11 Bypass EDH Processing

PIN	LOGIC OPR	HOST BIT
BYPASS_EDH	OR	BYPASS_EDH

EDH processing can be bypassed by asserting the BYPASS_EDH pin or HOSTIF write table bit HIGH. When bypassed, EDH packets pass through the chip unaltered. Overwriting information in the EDH packet via the HOSTIF write table or the FLAG PORT has no effect. Data processing in the chip (as described below) can still occur even if BYPASS_EDH is asserted. In this case, valid incoming error flags can be read via the I²C or parallel port interface. However, reading outgoing error flags via the host port or the flag port returns values of 0.

4. DATA PROCESSING BLOCK

The GS9021A contains advanced data processing features that can simplify system design requirements. These include:

- TRS Blanking,
- ITU-R-601 Clipping
- Data Blanking,
- TRS Insertion, and
- ANC Header updating

It is important to note that these processing functions occur in the GS9021A in the order listed above.

When implementing applications which use the EDH core (ie. BYPASS_EDH set LOW), TRS blanking, data blanking, and TRS insertion will indicate a downstream FF/AP EDH error when a 3FC_H-3FF_H input data value is blanked out or overwritten to a value less than 3FB_H. As such, users may wish to disable data blanking, TRS blanking and TRS insertion by setting the BLANK_EN pin HIGH, the CLIP_TRS pin LOW, and leaving the corresponding host interface bits at their power-on default values.

4.1 TRS Blanking

PIN	LOGIC OPR	HOST BIT
		TRS_BLANK

When asserted HIGH, TRS_BLANK (HOSTIF write table) will blank out any incorrectly positioned TRS words with respect to the flywheel. The blanking values used will be appropriate for the detected video standard as described below in the Data Blanking section. When TRS_INSERT is enabled and TRS_BLANK is not, there may be 4 TRSs per line in the outgoing data stream during a standard switch.

Similarly, if TRS_BLANK is enabled and TRS_INSERT is not, then there may be 0 TRS per line during a switch. In most applications, these features should be either both enabled or both disabled to maintain only two TRSs per line. TRS blanking will function incorrectly if the flywheel is disabled. Thus if the flywheel is disabled the TRS_BLANK function should be disabled as well.

4.2 ITU-R-601 Clipping

PIN	LOGIC OPR	HOST BIT
		601_CLIP

This feature operates on the active picture portion (as defined in RP165) of the data stream only. When the 601_CLIP bit of the HOSTIF write table is asserted HIGH, the device remaps all reserved data words in the active picture to values compliant with ITU-R-601. That is, 000-003 is clipped to 004 and 3FC_H-3FF_H is clipped to 3FB_H.

4.3 Data Blanking

PIN	LOGIC OPR	HOST BIT
<u>BLANK_EN</u>	AND	<u>BLANK_EN</u>

Asserting the BLANK_EN pin or the corresponding HOSTIF write table bit LOW causes the corresponding input data to be forced to blanking levels. This is a dynamic control allowing the user to individually select which data words are to be blanked as shown in Figure 7. TRS and EDH insertion occurs after data blanking so if all these features are being used, the output data stream continues to have TRS words and EDH packets present, even if the BLANK_EN is constantly held LOW.

The outgoing EDH packet will contain the correct CRC values for the blanked fields since the CRC values are calculated and inserted just prior to the data exiting the device.

The blanking values in hexi-decimal notation for each standard are as follows:

NTSC/PAL 4:2:2	200 040 200 040 (CB:Y:CR:Y)
NTSC 4fsc	0F0
PAL 4fsc	100
NTSC/PAL 4:4:4:4	040 040 040 040 (B:G:R:A) 200 040 200 040 (CB:Y:CR:A)

Note that normally the device must first detect the incoming standard in order for the proper blanking values to be inserted. However, by setting $\overline{\text{BLANK_EN}}$ low, CLIP_TRS high and forcing the standard in the HOST write table, the GS9021A can be used to generate a blank, TRS formatted video stream (with or without EDH), just by supplying a clock to the device. The frequency of the clock being supplied should be less than or equal to the standard selected. The outgoing stream will just be a frequency scaled version of that standard.

4.4 TRS Insertion

PIN	LOGIC OPR	HOST BIT
		TRS_INSERT

TRS words, based on the internal flywheel, can be inserted into the outgoing data stream by asserting HIGH the TRS_INSERT bit of the HOSTIF write table. Note that for proper TRS insertion, the incoming standard must be detected and the flywheel synchronized. That is, the GS9021A does NOT provide proper TRS insertion for unformatted video data (video without TRS words).

In the case where the input signal disappears, TRSs will continue to be inserted based on the last detected standard. Further, if a TRS is already in the correct location, it will be overwritten which may have the effect of correcting the TRSID word.

TRS insertion will function incorrectly if the flywheel is disabled. Thus if the flywheel is disabled the TRS_INSERT function should be disabled as well.

4.5 Clipping And TRS Blanking/Insertion

PIN	LOGIC OPR	HOST BIT
CLIP_TRS	OR	601_CLIP TRS_BLANK TRS_INSERT

Asserting the CLIP_TRS pin HIGH turns on three features described previously:

1. ITU-R-601 Clipping,
2. TRS Blanking, and
3. TRS Insertion

These three functions can also be turned on individually through the HOSTIF as described above. The CLIP_TRS pin is logically ORed with each of the three bits from the HOSTIF table. As a result, as long as the CLIP_TRS pin is asserted, these functions cannot be turned off via the HOSTIF.

4.6 Ancillary Header

PIN	LOGIC OPR	HOST BIT
		ANC_HEADER

Updating of the ANC headers can occur to facilitate 8-bit to 10-bit conversion. If the ANC_HEADER bit of the HOSTIF write table is set HIGH, all 3FC-3FF data values corresponding to component ANC headers are remapped to 3FF in the output data stream. For example, if 8 bit data is input to the device, the ANC header of 00, FF, FF will appear as 000, 3FC, 3FC and will be remapped to 000, 3FF, 3FF by the GS9021A.

5. HOST INTERFACE TABLES

PIN	LOGIC OPR	HOST BIT
HOSTIF_MODE		

The HOST INTERFACE TABLES (HOSTIF) refer to memory locations within the GS9021A which store functional information about the device. There are two tables, a write table and read table.

The write table is organized into 15 word locations (each 8 bits wide) as shown in Table 3 and is used to set various configuration/flag bits. The read table is organized into 23 word locations (each 8 bits wide) as shown in Table 4 and is used to read status information from the device.

The HOSTIF tables can be accessed via an I²C (Inter-Integrated Circuit) serial interface or an 8-bit parallel interface. The HOSTIF_MODE pin selects which interface is used. If the HOSTIF_MODE pin is HIGH, the HOSTIF operates in I²C mode. If the HOSTIF_MODE pin is LOW, the HOSTIF operates in parallel mode.

Note that many bits stored in the tables are also available as device pins. Bits in the write table that have a default value of 0, are logically ORed with the corresponding pin. Write table control bits $\overline{\text{VBLANKS/L}}$ and $\overline{\text{BLANK_EN}}$, which have a default value of 1, are logically ANDed with the corresponding pin.

If the HOST interface is not going to be used, the best way to set the related pins is as follows:

HOSTIF_MODE = LOW

$\overline{CS}$ = HIGH

$R/\overline{W}$ = HIGH

$A/\overline{D}$ = DON'T CARE (BUT NOT FLOATING)

P[7:0] = N/C

5.1 I²C Serial Interface

PIN	LOGIC OPR	HOST BIT
SCL		
SDA		
A[2:0]		

The I²C interface consists of a bi-directional serial data pin (SDA) and a serial clock input pin (SCL). In addition, 3 input pins, A[2:0] are provided to assign the chip one of eight possible I²C addresses (0001A₂A₁A₀).

During an I²C write operation, the first byte written to the chip (after the device has been addressed) is interpreted as the starting HOSTIF write table address for the communication. The next byte is interpreted as data to be written to the specified address. The address then automatically increments so that the following bytes are written to subsequent addresses.

When executing a read operation, a write must be performed first to load the desired starting address. After this, bytes read from the chip will begin at this address and will auto-increment. If the read operation is halted and communication with the chip is later established for another read, the chip will resume reading at the next HOSTIF memory address.

In I²C mode, P[7:5] and $A/\overline{D}$ must be set LOW while $R/\overline{W}$ and $\overline{CS}$ must be set HIGH.

5.2 Parallel Interface

PIN	LOGIC OPR	HOST BIT
P[7:0]		
$A/\overline{D}$		
$R/\overline{W}$		
$\overline{CS}$		

The asynchronous parallel interface consists of an 8-bit multiplexed address/data bus (P[7:0]), a chip select pin ($\overline{CS}$), a read/write pin ($R/\overline{W}$), and an address/data pin ($A/\overline{D}$).

The following should be noted when interfacing to the parallel port:

- Read/Write cycles via the parallel interface are completely independent and asynchronous to the parallel clock PCLKIN.
- Signals are "strobed" into/out of the parallel port on the falling edge of the $\overline{CS}$ signal. Setup and hold times, as defined in the AC timing tables, are relative to this edge and must be met (see Figure 8a)
- The GS9021A drives the P[7:0] bus when the $R/\overline{W}$ pin is HIGH and the $\overline{CS}$ pin is LOW. At all other times, the P[7:0] port is in a high impedance state. The host interface enable and disable times are shown in Figure 8b and are specified in the AC timing information. In this figure, the rising/falling edges of $R/\overline{W}$ and $\overline{CS}$ are not aligned to illustrate that the state of the P[7:0] I/Os is only a combinatorial function of the $R/\overline{W}$ and $\overline{CS}$ pins.

A write cycle to the parallel interface is shown in Figure 8c. The starting address of the operation is written to the chip by putting the $R/\overline{W}$ pin LOW (indicating write) and the $A/\overline{D}$ pin high (indicating ADDRESS). At t_0 , the falling edge of $\overline{CS}$ strobes in the information. Following this, the $A/\overline{D}$ line should be asserted LOW indicating data. The $R/\overline{W}$ line remains LOW indicating a write operation and at t_1 the data is strobed into the device.

A read example follows the write cycle. Note that the read cycle begins with a write operation to indicate the starting address. At t_2 , $R/\overline{W}$ is LOW (indicating write), $A/\overline{D}$ is HIGH (indicating address) and P[7:0] represent the starting address for the read cycle. After sufficient hold time, the microcontroller releases the P[7:0] bus and the $R/\overline{W}$ is asserted HIGH to indicate a read operation. At t_3 , the $\overline{CS}$ is asserted low causing the GS9021A to present the required data on the P[7:0] bus.

If two consecutive data read/write operations are performed, the device will automatically increment the address. However, for a completely random-access operation, the address can be specified prior to every data read/write operation.

5.3 Host Interface Read/Write Timing

Figure 9 illustrates valid times for reading/writing information from the HOSTIF tables. Figure 9 represents two fields of video data entering and exiting the GS9021A. The relative position of the EDH packet in the data stream is also shown. (Note that the EDH packet entering the device at t_0 , EDH F0, represents the EDH information from the previous field, FIELD 0).

It is safe to read or write EDH information at least two lines after an EDH packet exits the chip but before the subsequent EDH packet enters the chip. Reading during the time interval shown will show values from EDH F0. Writing during the time interval shown will affect EDH F1.

Note that the above read/write timing should also be observed when reading/writing flag information via the FLAG PORT.

6.0 RESET

PIN	LOGIC OPR	HOST BIT
$\overline{\text{RESET}}$		

Setting the $\overline{\text{RESET}}$ input pin LOW re-initializes the internal control circuitry including returning all HOST interface programming values to their original default values. The data pipe is not affected by the reset, so data continues to

flow through the chip unprocessed during resetting. An internal power-on-reset cell is also present in the device so that device initialization occurs on power-up. Figure 10a illustrates the reset circuitry. The internal power-on reset circuit of the GS9021A is sensitive to the rise time of the power supply, hence an external power on reset chip or board level reset line is strongly recommended. When using this technique, the user must ensure that a minimum pulse width of 100ns is present on the reset line.

In applications where a board-level reset is not available, a circuit similar to figure 10b can be used to ensure correct reset on power-up. The $\overline{\text{RESET}}$ pin will typically take 1.4ms to reach 2.5V on power up, but can take longer for power supplies with slower rise times. A bleed resistor such as the one shown (20k) will assist the capacitor to discharge once power is removed. The user should allow the capacitor to discharge to at least 0.5V before power is reapplied, to permit a full internal reset. The time taken by the $\overline{\text{RESET}}$ pin to reach 0.5V on power down, is dependent upon the fall time of the power supply.

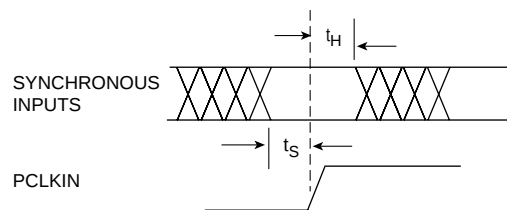


Fig. 1 Input Setup & Hold Times (Synchronous Inputs)

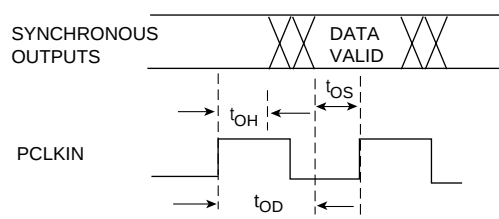


Fig. 2 Output Delay & Hold Times (Synchronous Outputs)

TABLE 2: GS9021A Case Table

	CASE NUMBER	MODE		EDH PACKET	RESULTS	COMMENTS / SUGGESTIONS
		R/ $\bar{T}$	CRC_MODE			
TX MODE	1	0	0	NO	No EDH comparison is performed. A new EDH packet is inserted into the data stream with all the EDH flags cleared unless overwritten by the dedicated flag port or the host interface. The EDH packet will include CRC values calculated from the data stream.	Use this MODE if you wish to insert EDH if it is not present. If EDH is present, clear all flags and update CRC.
	2	0	0	YES		
CRC MODE	3	X	1	NO	Same results as Case #1	Use this MODE on the output EDH chip when mapping flags from an input EDH chip around a processing core (which would alter the picture data) to an output EDH chip so that EDH errors are not generated. You can also use this mode when you simply want to update the CRC values after processing, if the processing does not corrupt the EDH packet. In both cases, the EDH flags are preserved.
	4	X	1	YES	No EDH comparison is performed (i.e. no attempt is made to detect errors). The CRC is updated and all flags preserved or unaltered unless overwritten by the dedicated flag port or host interface.	
RX MODE	5	1	0	NO	New EDH packet inserted into data stream with all error flags cleared and all UES flags set high unless overwritten by the dedicated flag port or the host interface.	Use this MODE when you wish to detect errors in the data stream, or on an input EDH chip when mapping flags around a processing core (that would alter the picture data) to an output EDH chip so that EDH errors are not generated due to the data processing.
	6	1	0	YES	EDH comparison performed and error flags set and mapped appropriately unless overwritten by the dedicated flag port or the host interface. The CRC is updated and the EDH packet is re-inserted.	Use this MODE when you want to insert EDH if it is not present or update CRC values and preserve the flags in an existing EDH packet.

NOTE

1. "X" in the table above means 'don't care' (but not left floating).

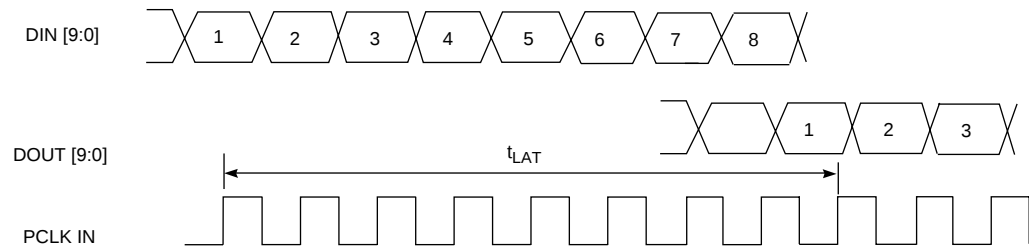


Fig. 3 Data Latency through the GS9021A

TABLE 3: GS9021A Host Interface Write Table

WRITE Table	ADDRESS	7	6	5	4	3	2	1	0
CONFIGURATION	1	⁰ STICKY IN	⁰ STICKY OUT	⁰ CLR1	⁰ CLR0	⁰ SWITCH FLYW	⁰ FLYWDIS	0	0
	2	0	¹ BLANKS/L	⁰ STD SEL	⁰ S	⁰ STD3	⁰ STD2	⁰ STD1	⁰ STD0
	3	⁰ 601_CLIP	¹ BLANK_EN	⁰ ANC_HEADER	⁰ BYPASS_EDH	⁰ FLAG_MAP	¹ ANC_CHKSM	⁰ TRS_INSERT	⁰ TRS_BLANK
OVERWRITE VALUES	4	⁰ FF UES	⁰ FF IDA	1	⁰ FF EDA	⁰ FF EDH	⁰ ANC UES	⁰ ANC IDA	1
	5	⁰ AP UES	⁰ AP IDA	1	⁰ AP EDA	⁰ AP EDH	⁰ AND EDA	⁰ ANC EDH	0
OVERWRITE CONTROL	6	⁰ FF UES	⁰ FF IDA	⁰ FF IDH	⁰ FF EDA	⁰ FF EDH	⁰ ANC UES	⁰ ANC IDA	⁰ ANC IDH
	7	⁰ AP UES	⁰ AP IDA	⁰ AP IDH	⁰ AP EDA	⁰ AP EDH	⁰ ANC EDA	⁰ ANC EDH	0
ERROR SENSITIVITY BITS	8	⁰ FF UES	⁰ FF IDA	⁰ FF IDH	⁰ FF EDA	⁰ FF EDH	⁰ ANC UES	⁰ ANC IDA	⁰ ANC IDH
	9	⁰ AP UES	⁰ AP IDA	⁰ AP IDH	⁰ AP EDA	⁰ AP EDH	⁰ ANC EDA	⁰ ANC EDH	¹ EDH_CHKSM
RESERVED (OUTGOING)	10	⁰ RW1 B7	⁰ RW1 B6	⁰ RW1 B5	⁰ RW1 B4	⁰ RW1 B3	⁰ RW1 B2	⁰ RW2 B7	⁰ RW2 B6
	11	⁰ RW2 B5	⁰ RW2 B4	⁰ RW2 B3	⁰ RW2 B2	⁰ RW3 B7	⁰ RW3 B6	⁰ RW3 B5	⁰ RW3 B4
	12	⁰ RW3 B3	⁰ RW3 B2	⁰ RW4 B7	⁰ RW4 B6	⁰ RW4 B5	⁰ RW4 B4	⁰ RW4 B3	⁰ RW4 B2
	13	⁰ RW5 B7	⁰ RW5 B6	⁰ RW5 B5	⁰ RW5 B4	⁰ RW5 B3	⁰ RW5 B2	⁰ RW6 B7	⁰ RW6 B6
	14	⁰ RW6 B5	⁰ RW6 B4	⁰ RW6 B3	⁰ RW6 B2	⁰ RW7 B7	⁰ RW7 B6	⁰ RW7 B5	⁰ RW7 B4
	15	⁰ RW7 B3	⁰ RW7 B2	⁰ RO_CTRL	¹ FFV	¹ APV	0	0	0

NOTE: 1. Superscripts denote default settings upon reset.

TABLE 4: GS9021A Host Interface Read Table

READ Table	ADDRESS	7	6	5	4	3	2	1	0
CONFIGURATION	1	F2	F1	F0	S	STD3	STD2	STD1	STD0
	2	NO_EDH	EDH_CHKSM	TRS_ERR	FFV	APV	0	0	0
INCOMING ERROR FLAGS	3	FF UES	FF IDA	FF IDH	FF EDA	FF EDH	ANC UES	ANC IDA	ANC IDH
	4	AP UES	AP IDA	AP IDH	AP EDA	AP EDH	ANC EDA	ANC EDH	0
OUTGOING ERROR FLAGS	5	FF UES	FF IDA	FF IDH	FF EDA	FF EDH	ANC UES	ANC IDA	ANC IDH
	6	AP UES	AP IDA	AP IDH	AP EDA	AP EDH	ANC EDA	ANC EDH	0
INCOMING FF CRC	7	b15	b14	b13	b12	b11	b10	b9	b8
	8	b7	b6	b5	b4	b3	b2	b1	b0
OUTGOING FF CRC	9	b15	b14	b13	b12	b11	b10	b9	b8
	10	b7	b6	b5	b4	b3	b2	b1	b0
INCOMING AP CRC	11	b15	b14	b13	b12	b11	b10	b9	b8
	12	b7	b6	b5	b4	b3	b2	b1	b0
OUTGOING AP CRC	13	b15	b14	b13	b12	b11	b10	b9	b8
	14	b7	b6	b5	b4	b3	b2	b1	b0
ERRORRED FIELD COUNTER	15	b23	b22	b21	b20	b19	b18	b17	b16
	16	b15	b14	b13	b12	b11	b10	b9	b8
	17	b7	b6	b5	b4	b3	b2	b1	b0
RESERVED WORDS (INCOMING)	18	RW1 B7	RW1 B6	RW1 B5	RW1 B4	RW1 B3	RW1 B2	RW2 B7	RW2 B6
	19	RW2 B5	RW2 B4	RW2 B3	RW2 B2	RW3 B7	RW3 B6	RW3 B5	RW3 B4
	20	RW3 B3	RW3 B2	RW4 B7	RW4 B6	RW4 B5	RW4 B4	RW4 B3	RW4 B2
	21	RW5 B7	RW5 B6	RW5 B5	RW5 B4	RW5 B3	RW5 B2	RW6 B7	RW6 B6
	22	RW6 B5	RW6 B4	RW6 B3	RW6 B2	RW7 B7	RW7 B6	RW7 B5	RW7 B4
	23	RW7 B3	RW7 B2	0	0	0	0	0	0

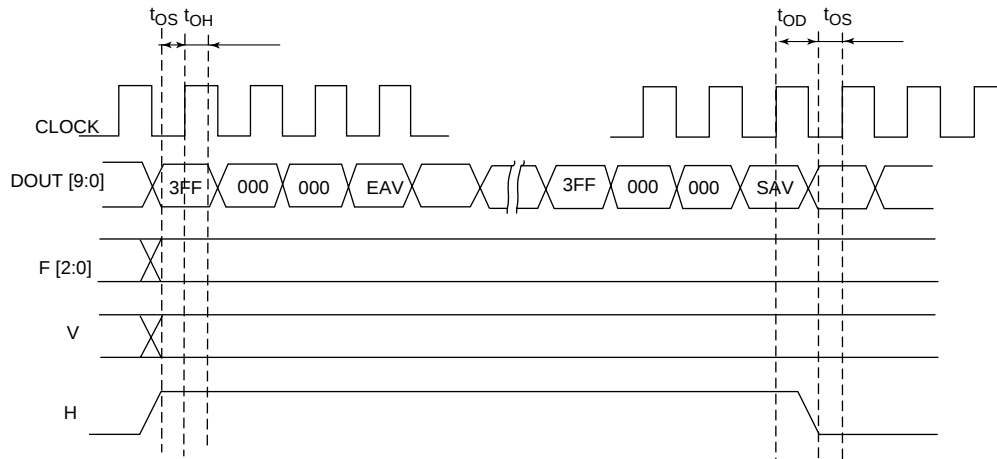


Fig. 4a FVH Timing for Component Video

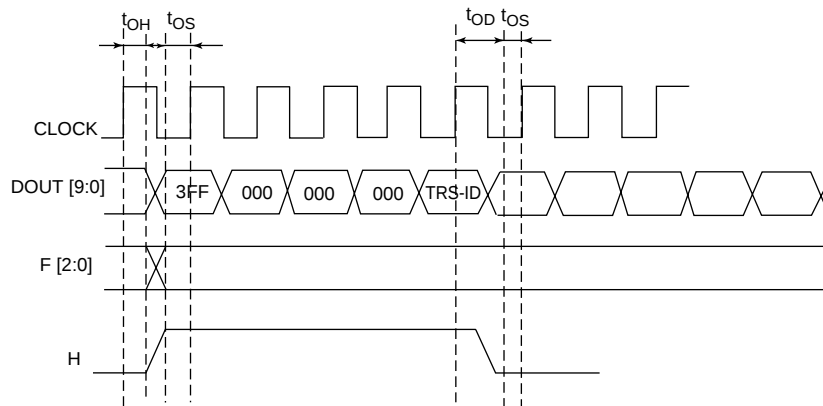


Fig. 4b F and H Timing for Composite Video

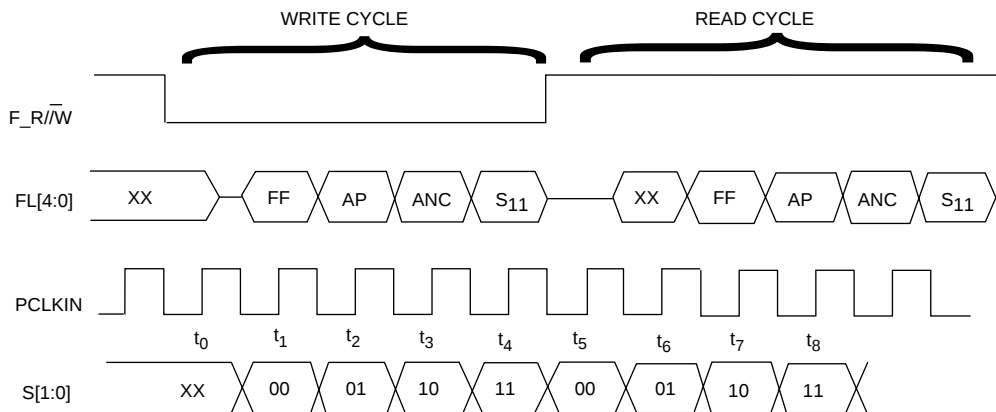


Fig. 5a Flag Port Read/Write Timing

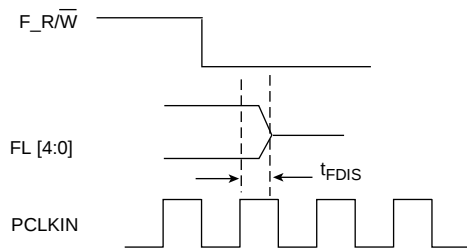


Fig. 5b Flag Port Disable Time

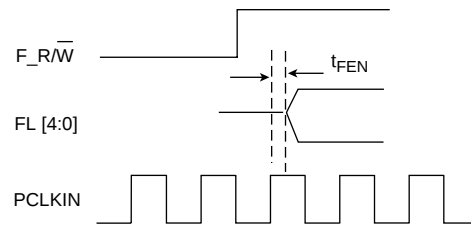


Fig. 5c Flag Port Enable Time

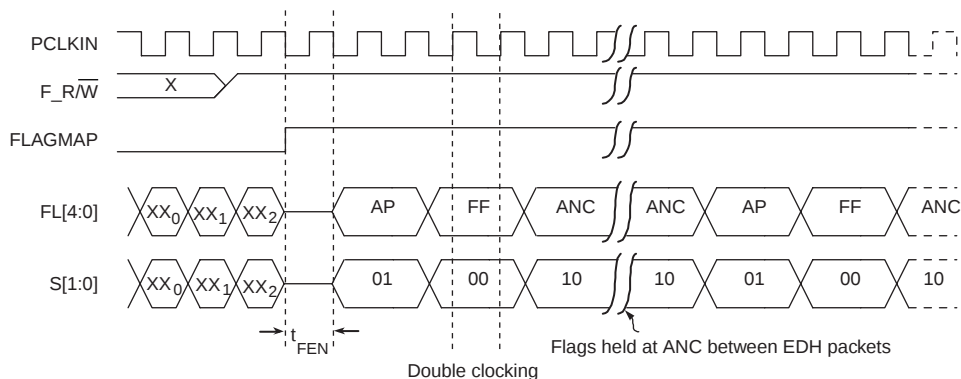


Fig. 5d Flag Port Timing in FLAG_MAP Mode

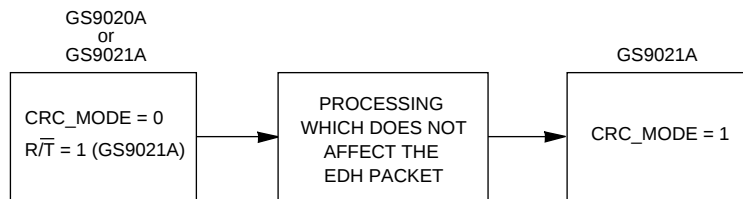


Fig. 6a Example of CRC_MODE Implementation

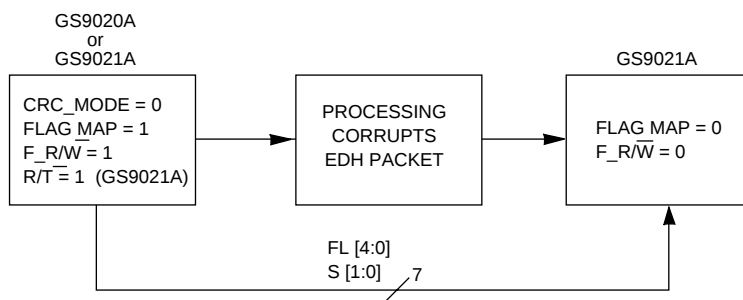


Fig. 6b Example of FLAG_MAP Mode Implementation

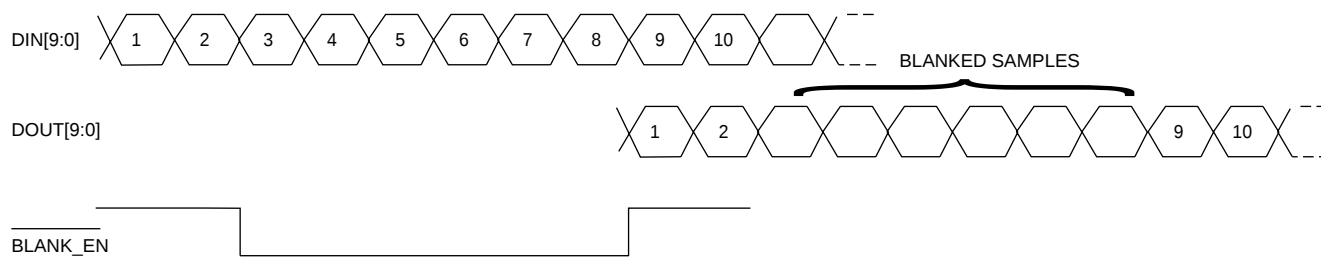


Fig. 7 Illustration of Data Blanking

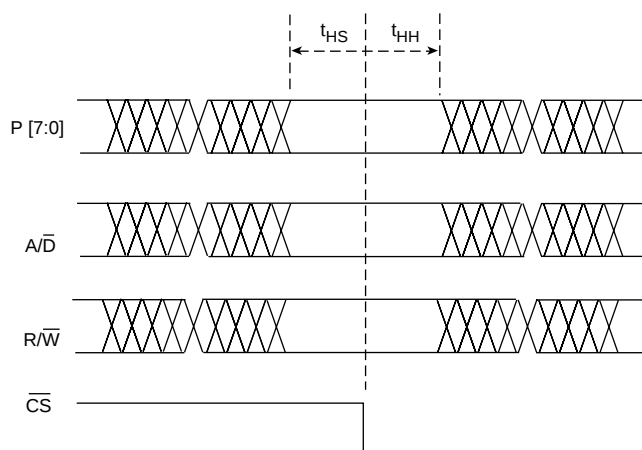


Fig. 8a HOSTIF Parallel Port Input Setup & Hold Times

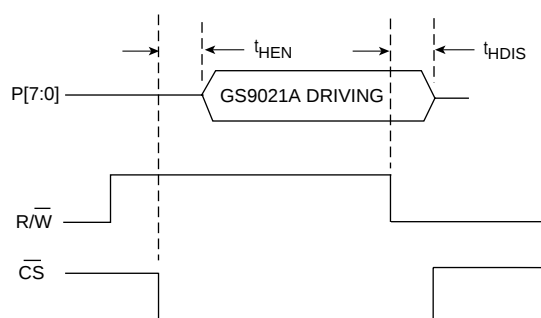


Fig. 8b HOSTIF Parallel Port Output Enable and Disable Times

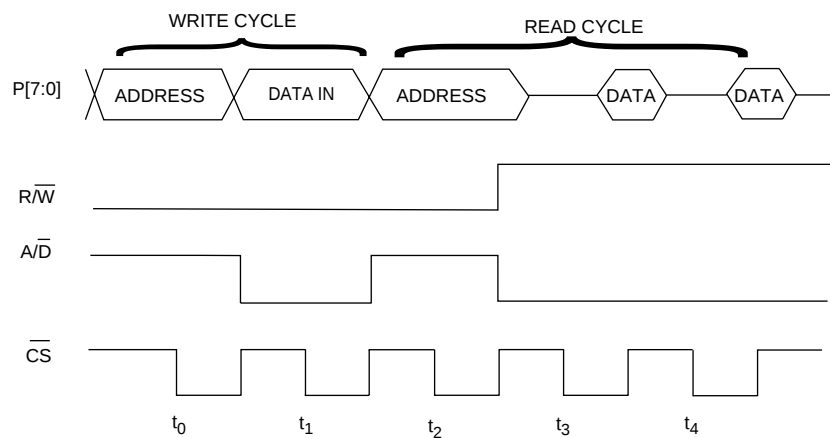


Fig. 8c HOSTIF Parallel Port Read/Write Cycles

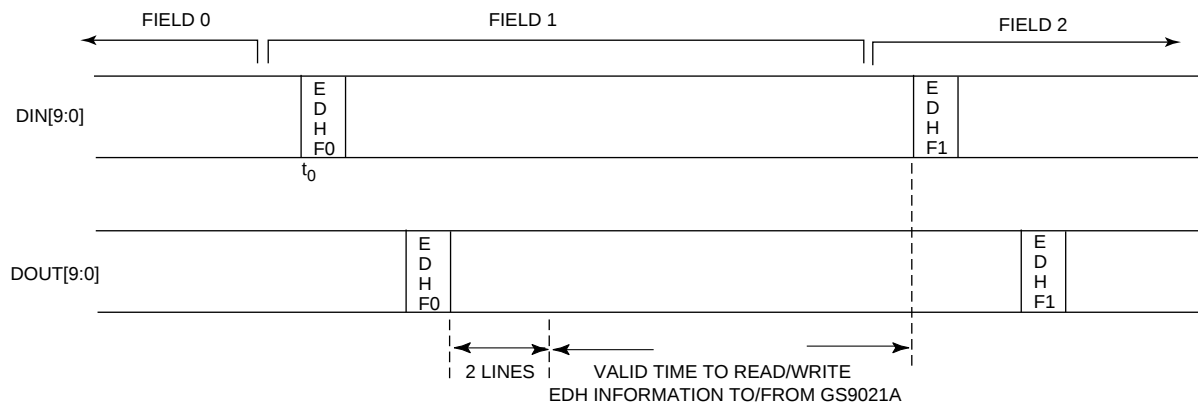


Fig. 9 Host Interface Read/Write Timing

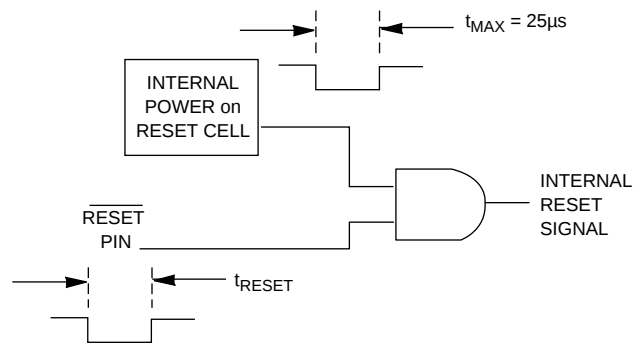


Fig. 10a Reset Circuitry

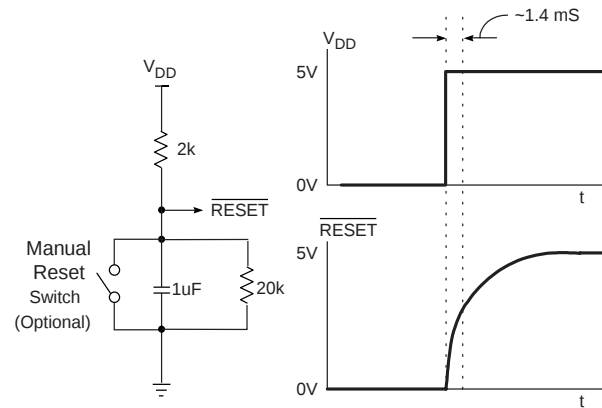


Fig. 10b Acceptable external reset circuit when a master reset is not available

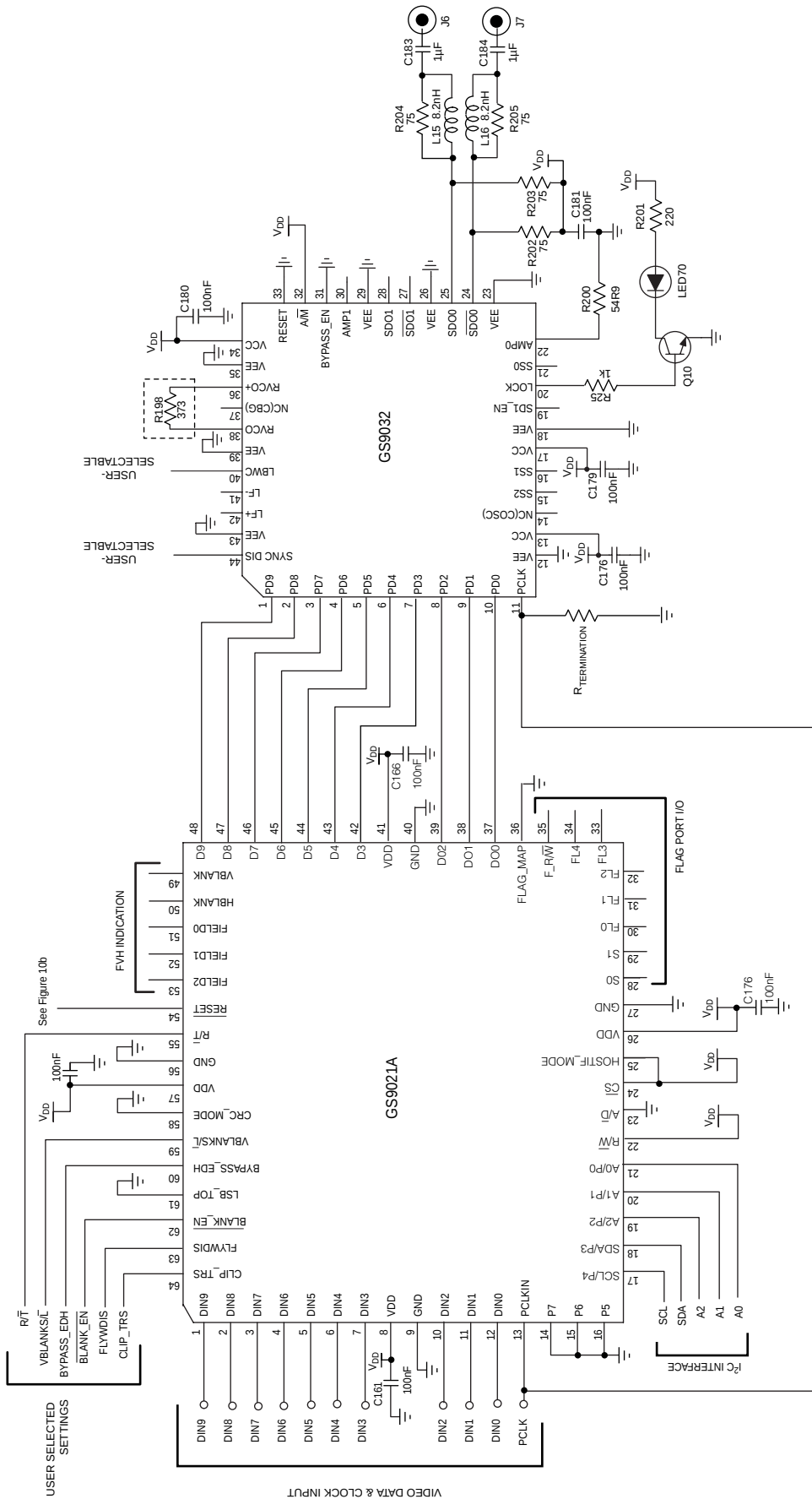
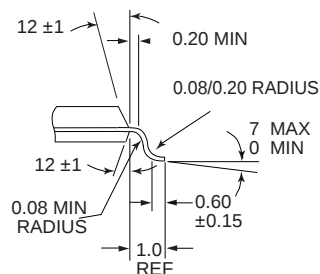
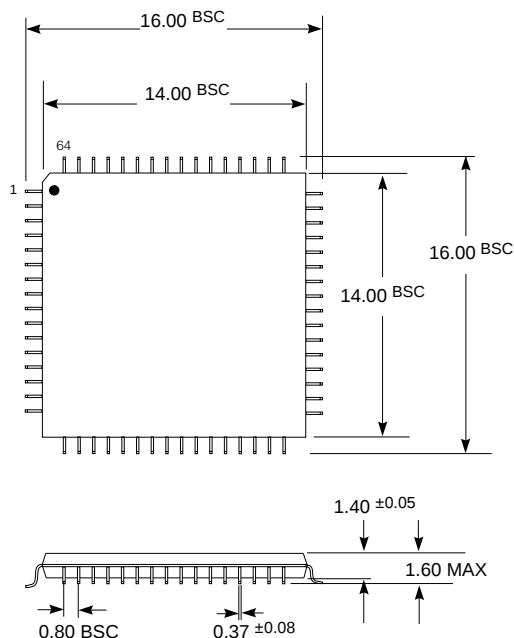


Fig. 11 GS9021A - GS9032 Application Circuit

PACKAGE DIMENSIONS



All dimensions in millimetres

64 pin LQFP

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



DOCUMENT IDENTIFICATION

DATA SHEET

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